

**PowerMOS transistor  
Logic level TOPFET**

**BUK127-50DL**

**DESCRIPTION**

Monolithic temperature and overload protected logic level power MOSFET in **TOPFET2** technology assembled in a 3 pin surface mount plastic package.

**APPLICATIONS**

General purpose switch for driving

- lamps
- motors
- solenoids
- heaters

in automotive systems and other applications.

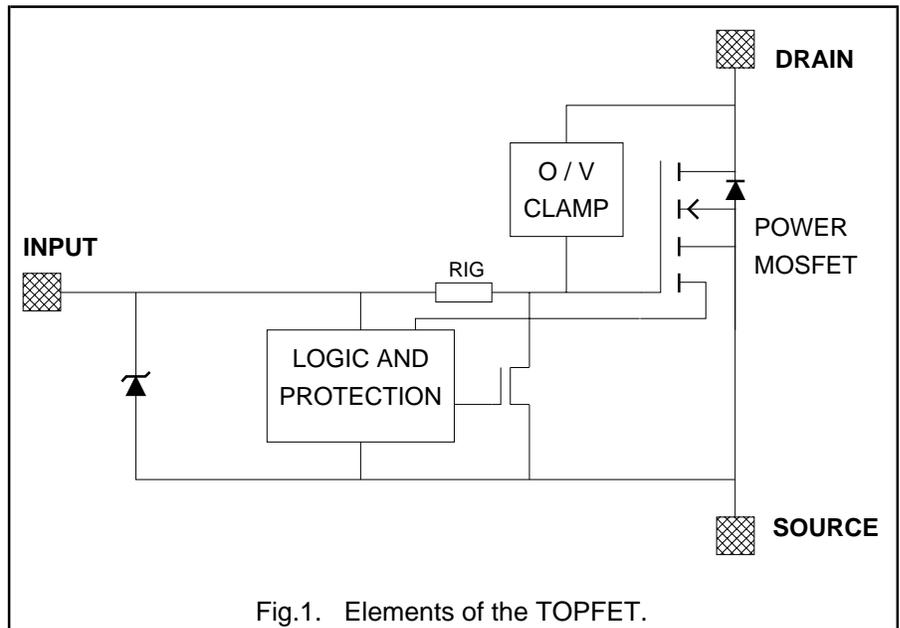
**FEATURES**

- TrenchMOS output stage
- Current limiting
- Overload protection
- Overtemperature protection
- Protection latched reset by input
- 5 V logic compatible input level
- Control of output stage and supply of overload protection circuits derived from input
- Low operating input current permits direct drive by micro-controller
- ESD protection on all pins
- Overvoltage clamping for turn off of inductive loads

**QUICK REFERENCE DATA**

SYMBOL	PARAMETER	MAX.	UNIT
$V_{DS}$	Continuous drain source voltage	50	V
$I_D$	Continuous drain current	0.7	A
$P_D$	Total power dissipation	1.8	W
$T_j$	Continuous junction temperature	150	°C
$R_{DS(ON)}$	Drain-source on-state resistance	200	mΩ

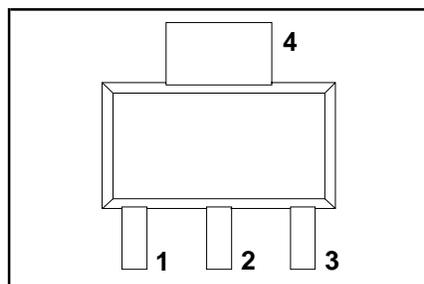
**FUNCTIONAL BLOCK DIAGRAM**



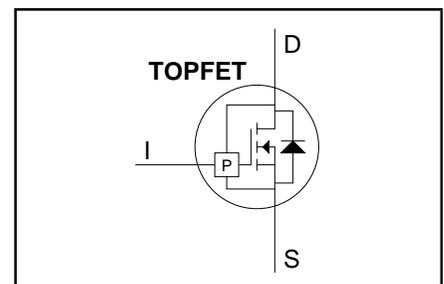
**PINNING - SOT223**

PIN	DESCRIPTION
1	input
2	drain
3	source
4	drain (tab)

**PIN CONFIGURATION**



**SYMBOL**



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### LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$V_{DS}$	Continuous drain source voltage <sup>1</sup>	-	-	50	V
$I_D$	Continuous drain current <sup>2</sup>	-	-	self limiting	A
$I_I$	Continuous input current	clamping	-	3	mA
$I_{IRM}$	Non-repetitive peak input current	$t_p \leq 1$ ms	-	10	mA
$P_D$	Total power dissipation	$T_a = 25^\circ\text{C}$	-	1.8	W
$T_{stg}$	Storage temperature	-	-55	150	$^\circ\text{C}$
$T_j$	Continuous junction temperature	normal operation <sup>3</sup>	-	150	$^\circ\text{C}$

### ESD LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$V_C$	Electrostatic discharge capacitor voltage	Human body model; $C = 250$ pF; $R = 1.5$ k $\Omega$	-	2	kV

### OVERVOLTAGE CLAMPING LIMITING VALUES

At a drain source voltage above 50 V the power MOSFET is actively turned on to clamp overvoltage transients.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$E_{DSM}$	Non-repetitive clamping energy	$T_a \leq 25^\circ\text{C}$ ; $I_{DM} < I_{D(lim)}$ ; inductive load	-	100	mJ
$E_{DRM}$	Repetitive clamping energy	$T_{sp} \leq 125^\circ\text{C}$ ; $I_{DM} = 50$ mA; $f = 250$ Hz	-	5	mJ

### OVERLOAD PROTECTION LIMITING VALUES

With the protection supply provided via the input pin, TOPFET can protect itself from short circuit loads.

Overload protection operates by means of drain current limiting and activating the overtemperature protection.

SYMBOL	PARAMETER	REQUIRED CONDITION	MIN.	MAX.	UNIT
$V_{DDP}$	Protected drain source supply voltage	$V_{IS} \geq 4$ V	-	35	V

### THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$R_{th\ j-sp}$	<b>Thermal resistance</b> Junction to solder point		-	12	18	K/W
$R_{th\ j-b}$	Junction to board <sup>4</sup>	Mounted on any PCB	-	40	-	K/W
$R_{th\ j-a}$	Junction to ambient	Mounted on PCB of fig. 22	-	-	70	K/W

<sup>1</sup> Prior to the onset of overvoltage clamping. For voltages above this value, safe operation is limited by the overvoltage clamping energy.

<sup>2</sup> Refer to OVERLOAD PROTECTION CHARACTERISTICS.

<sup>3</sup> Not in an overload condition with drain current limiting.

<sup>4</sup> Temperature measured 1.3 mm from tab.

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### OUTPUT CHARACTERISTICS

Limits are for  $-40^{\circ}\text{C} \leq T_{\text{mb}} \leq 150^{\circ}\text{C}$ ; typicals are for  $T_{\text{mb}} = 25^{\circ}\text{C}$  unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(\text{CL})\text{DSS}}$	Off-state Drain-source clamping voltage	$V_{\text{IS}} = 0\text{ V}$	50	-	-	V
		$I_{\text{D}} = 10\text{ mA}$ $I_{\text{D}} = 200\text{ mA}; t_{\text{p}} \leq 300\text{ }\mu\text{s}; \delta \leq 0.01$	50	60	70	V
$I_{\text{DSS}}$	Drain source leakage current	$V_{\text{DS}} = 40\text{ V}$	-	-	100	$\mu\text{A}$
		$T_{\text{mb}} = 25^{\circ}\text{C}$	-	0.1	10	$\mu\text{A}$
$R_{\text{DS(ON)}}$	On-state Drain-source resistance	$V_{\text{IS}} \geq 4\text{ V}; t_{\text{p}} \leq 300\text{ }\mu\text{s}; \delta \leq 0.01$	-	-	380	$\text{m}\Omega$
		$I_{\text{D}} = 100\text{ mA}$ $T_{\text{mb}} = 25^{\circ}\text{C}$	-	150	200	$\text{m}\Omega$

### INPUT CHARACTERISTICS

The supply for the logic and overload protection is taken from the input.

Limits are for  $-40^{\circ}\text{C} \leq T_{\text{mb}} \leq 150^{\circ}\text{C}$ ; typicals are for  $T_{\text{mb}} = 25^{\circ}\text{C}$  unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT	
$V_{\text{IS(TO)}}$	Input threshold voltage	$V_{\text{DS}} = 5\text{ V}; I_{\text{D}} = 1\text{ mA}$	0.6	-	2.4	V	
		$T_{\text{mb}} = 25^{\circ}\text{C}$	1.1	1.6	2.1	V	
$I_{\text{IS}}$	Input supply current	normal operation;	$V_{\text{IS}} = 5\text{ V}$	100	220	400	$\mu\text{A}$
			$V_{\text{IS}} = 4\text{ V}$	80	195	330	$\mu\text{A}$
$I_{\text{ISL}}$	Input supply current	protection latched;	$V_{\text{IS}} = 5\text{ V}$	200	400	650	$\mu\text{A}$
			$V_{\text{IS}} = 3\text{ V}$	130	250	430	$\mu\text{A}$
$V_{\text{ISR}}$	Protection reset voltage <sup>1</sup>	reset time $t_{\text{r}} \geq 100\text{ }\mu\text{s}$	1.5	2	2.9	V	
$t_{\text{r}}$	Latch reset time	$V_{\text{IS1}} = 5\text{ V}, V_{\text{IS2}} < 1\text{ V}$	10	40	100	$\mu\text{s}$	
$V_{(\text{CL})\text{IS}}$	Input clamping voltage	$I_{\text{I}} = 1.5\text{ mA}$	5.5	-	8.5	V	
$R_{\text{IG}}$	Input series resistance <sup>2</sup> to gate of power MOSFET	$T_{\text{mb}} = 25^{\circ}\text{C}$	-	33	-	$\text{k}\Omega$	

<sup>1</sup> The input voltage below which the overload protection circuits will be reset.

<sup>2</sup> Not directly measurable from device terminals.

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### OVERLOAD PROTECTION CHARACTERISTICS

TOPFET switches off to protect itself when one of the overload thresholds is exceeded. It remains latched off until reset by the input.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$I_D$	<b>Overload protection</b> Drain current limiting	$-40^\circ\text{C} \leq T_j \leq 150^\circ\text{C}$				
		$V_{IS} = 5\text{ V}$	0.8	1.3	1.7	A
		$V_{IS} = 4.5\text{ V}$	0.7	-	-	A
		$V_{IS} = 4\text{ V to } 5.5\text{ V}$	0.6	-	1.8	A
$P_{D(TO)}$	<b>Short circuit load protection</b> Overload power threshold	$V_{IS} = 5\text{ V}$				
		for protection to operate	-	17	-	W
$T_{DSC}$	Characteristic time	which determines trip time <sup>1</sup>	-	1.6	-	ms
$T_{j(TO)}$	<b>Overtemperature protection</b> Threshold junction temperature	from $I_D \geq 280\text{ mA}$ or $V_{DS} \geq 100\text{ mV}$				
		$V_{IS} = 4\text{ V to } 5.5\text{ V}$	150	165	-	$^\circ\text{C}$

### SWITCHING CHARACTERISTICS

$T_a = 25^\circ\text{C}$ ; resistive load  $R_L = 50\ \Omega$ ; adjust  $V_{DD}$  to obtain  $I_D = 250\text{ mA}$ ; refer to test circuit and waveforms

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$t_{d\ on}$	Turn-on delay time	$V_{IS}: 0\text{ V} \Rightarrow 5\text{ V}$	-	5	12	$\mu\text{s}$
$t_r$	Rise time		-	11	30	$\mu\text{s}$
$t_{d\ off}$	Turn-off delay time	$V_{IS}: 5\text{ V} \Rightarrow 0\text{ V}$	-	25	65	$\mu\text{s}$
$t_f$	Fall time		-	14	35	$\mu\text{s}$

### REVERSE DIODE LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$I_S$	Continuous forward current	$T_{mb} \leq 25^\circ\text{C}$ ; $V_{IS} = 0\text{ V}$	-	2	A

### REVERSE DIODE CHARACTERISTICS

Limits are for  $-40^\circ\text{C} \leq T_{mb} \leq 150^\circ\text{C}$ ; typicals are for  $T_{mb} = 25^\circ\text{C}$  unless otherwise specified

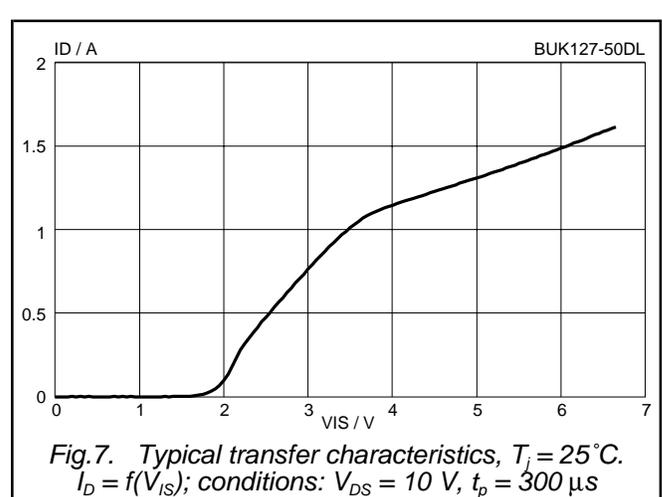
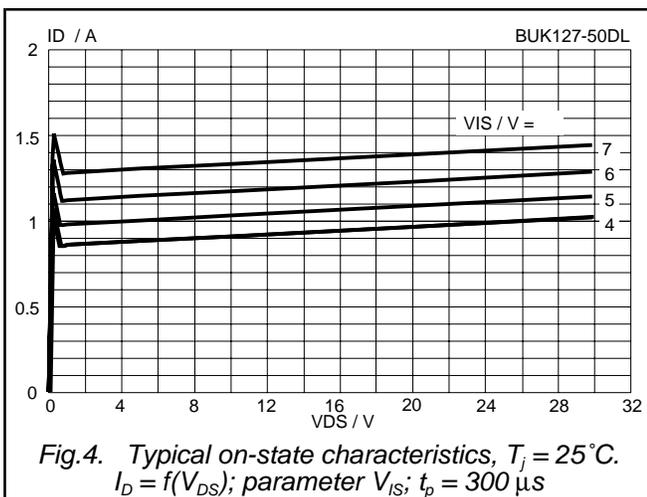
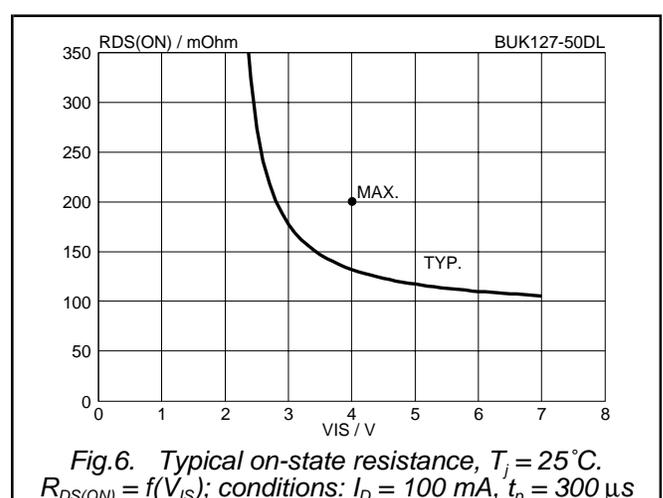
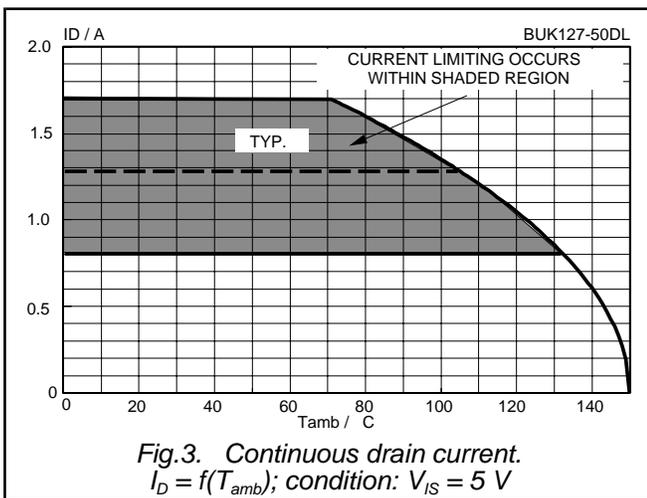
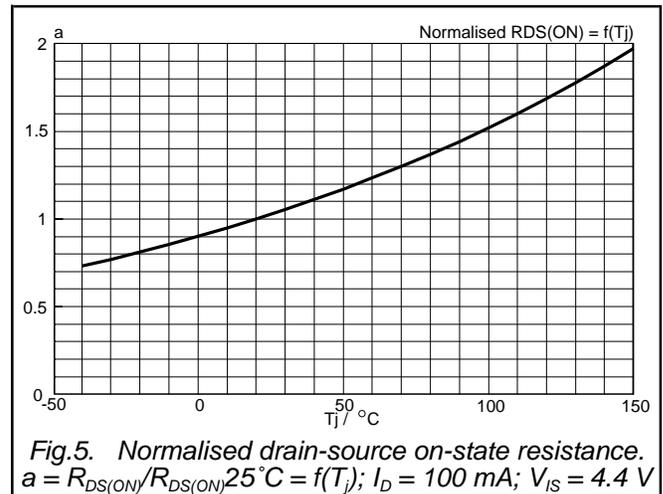
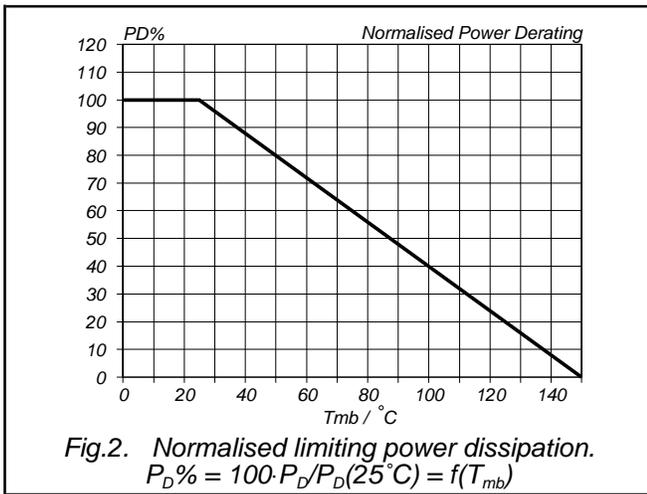
SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{SDO}$	Forward voltage	$I_S = 2\text{ A}$ ; $V_{IS} = 0\text{ V}$ ; $t_p = 300\ \mu\text{s}$	-	0.83	1.1	V
$t_{rr}$	Reverse recovery time	not applicable <sup>2</sup>	-	-	-	-

<sup>1</sup> Trip time  $t_{d\ sc}$  varies with overload dissipation  $P_D$  according to the formula  $t_{d\ sc} \approx T_{DSC} / [P_D / P_{D(TO)} - 1]$ .

<sup>2</sup> The reverse diode of this type is not intended for applications requiring fast reverse recovery.

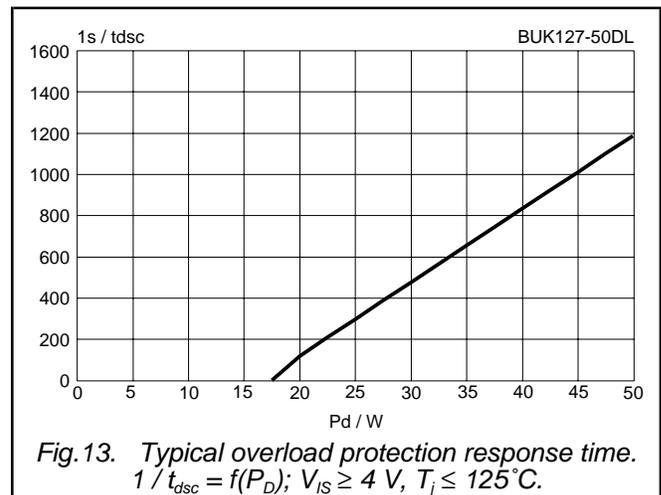
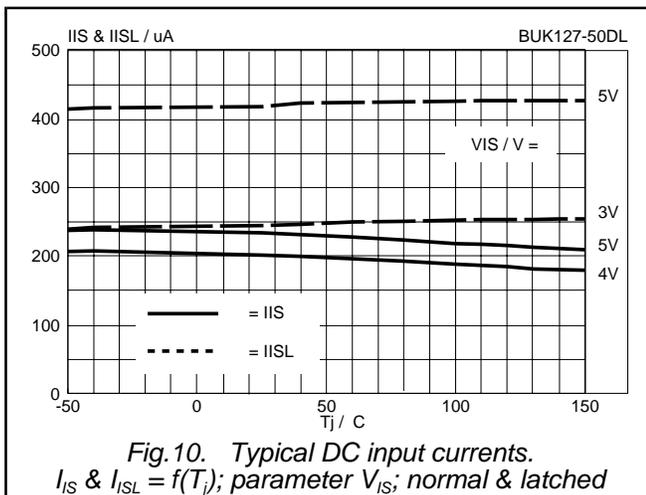
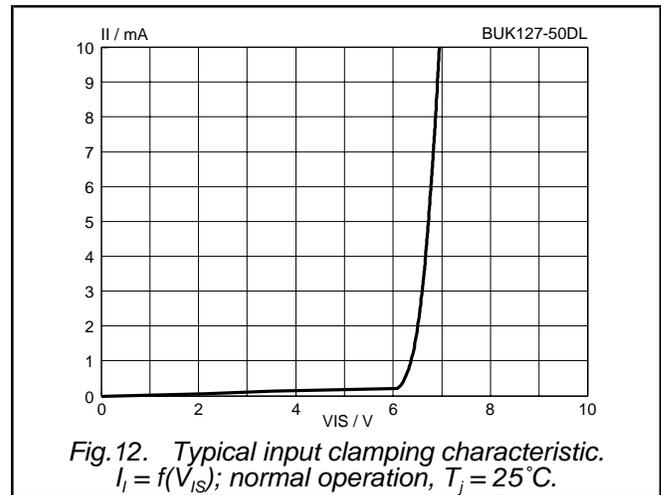
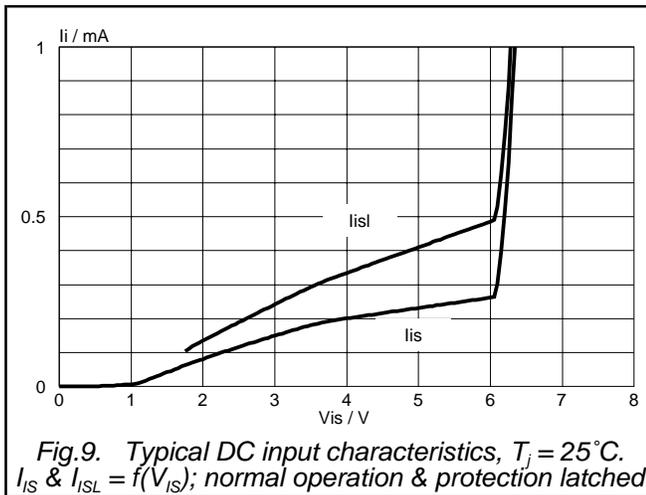
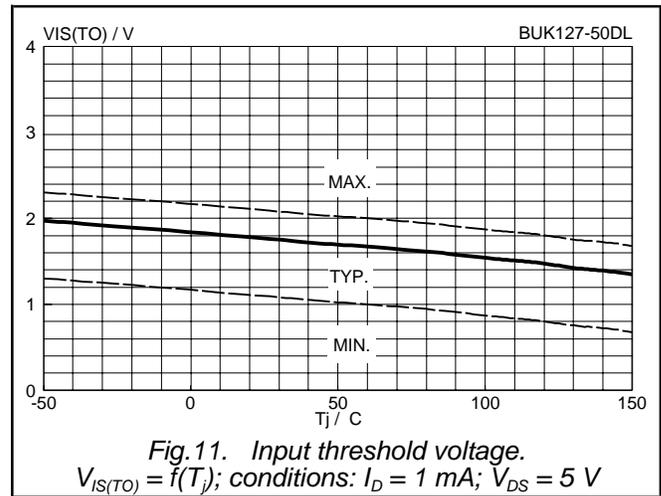
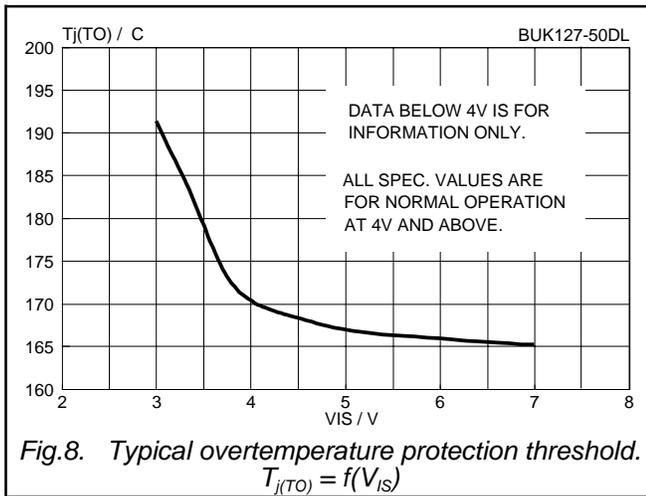
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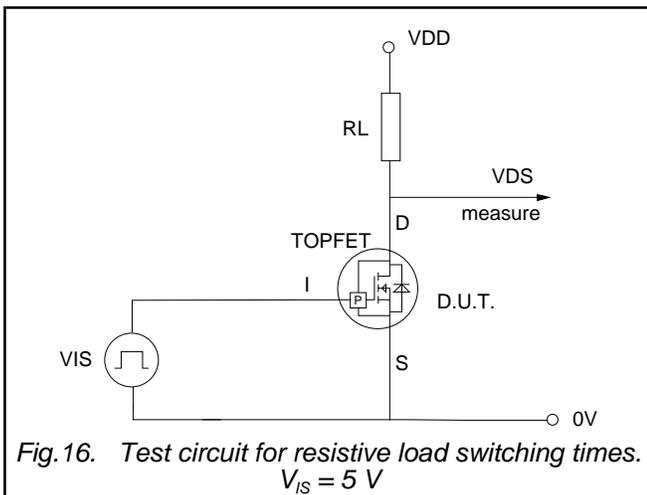
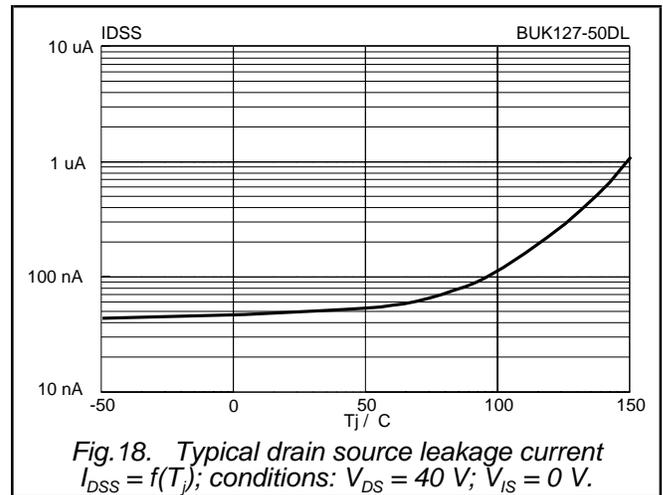
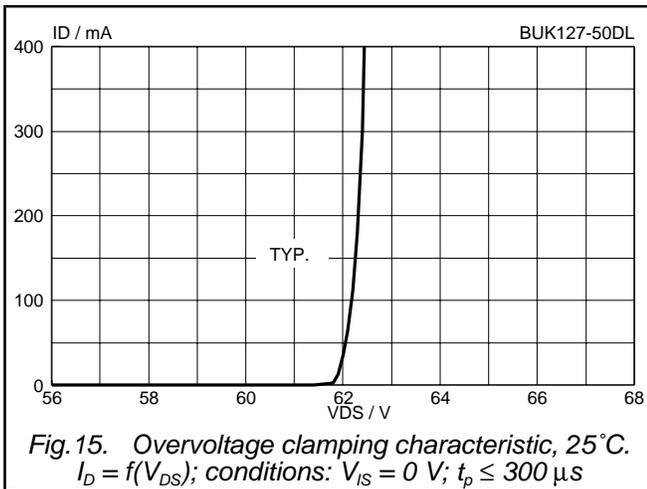
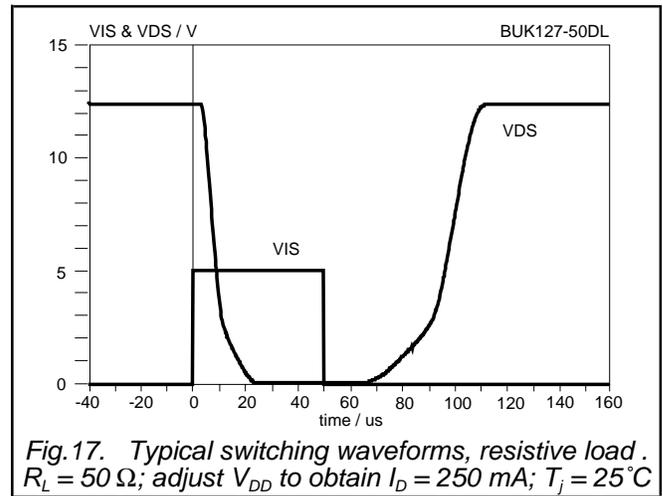
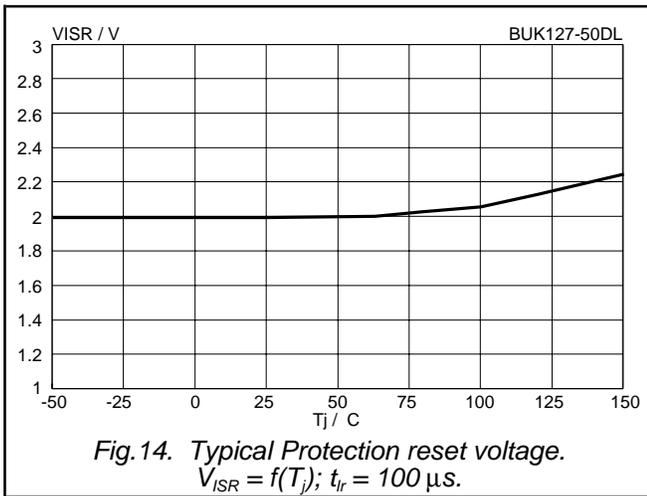
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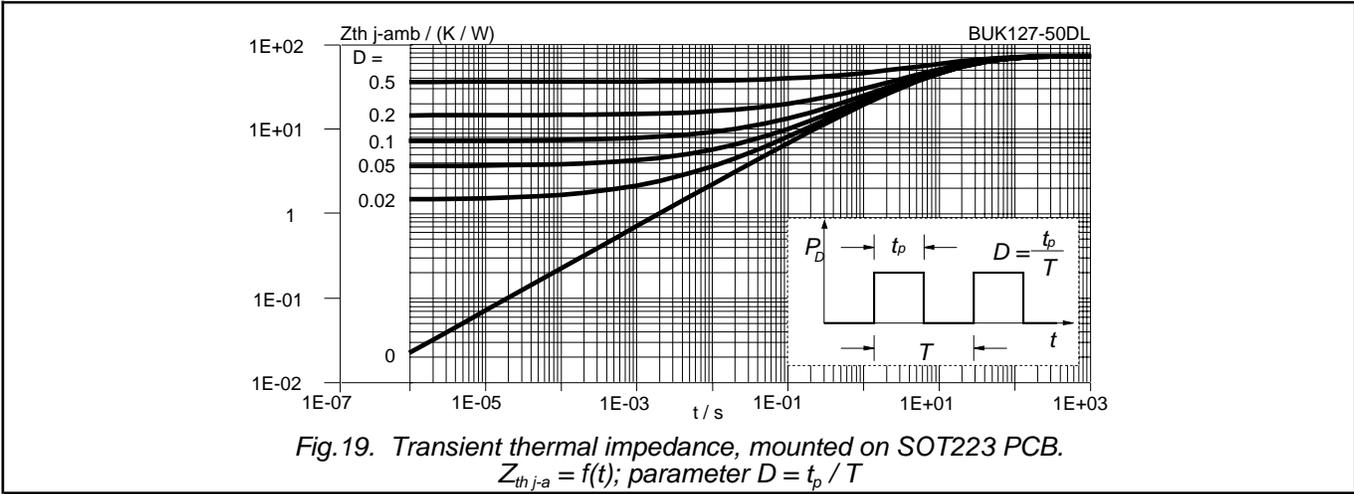
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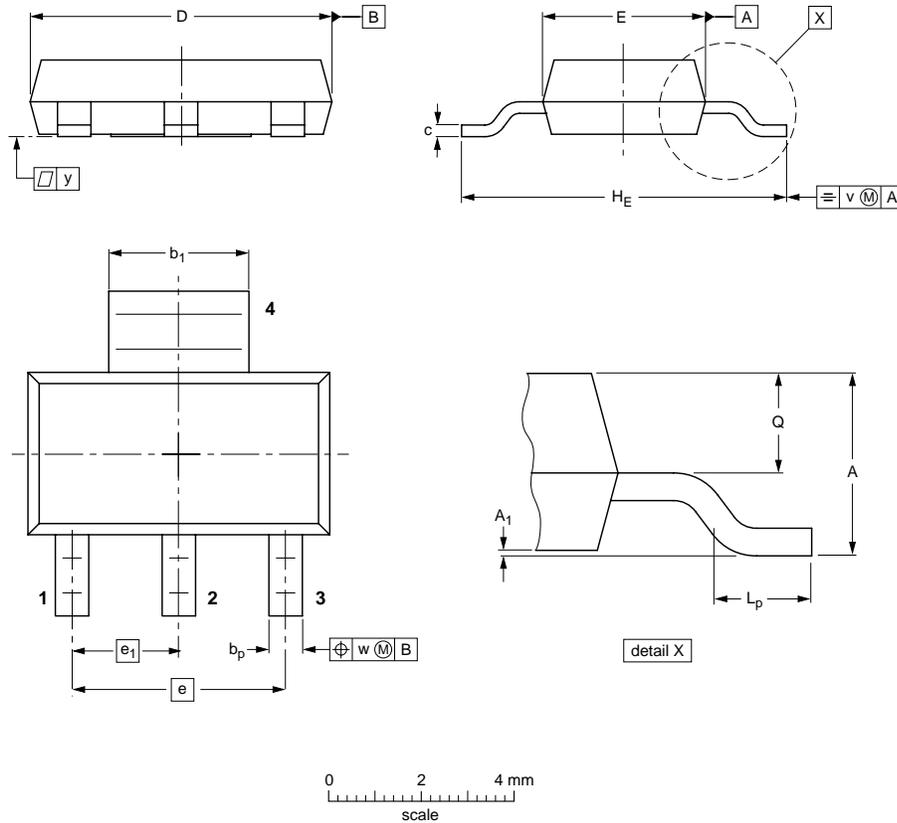
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MECHANICAL DATA

Plastic surface mounted package; collector pad for good heat transfer; 4 leads

SOT223



DIMENSIONS (mm are the original dimensions)

UNIT	A	A <sub>1</sub>	b <sub>p</sub>	b <sub>1</sub>	c	D	E	e	e <sub>1</sub>	H <sub>E</sub>	L <sub>p</sub>	Q	v	w	y
mm	1.8 1.5	0.10 0.01	0.80 0.60	3.1 2.9	0.32 0.22	6.7 6.3	3.7 3.3	4.6	2.3	7.3 6.7	1.1 0.7	0.95 0.85	0.2	0.1	0.1

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT223			SC-73			97-02-28 99-09-13

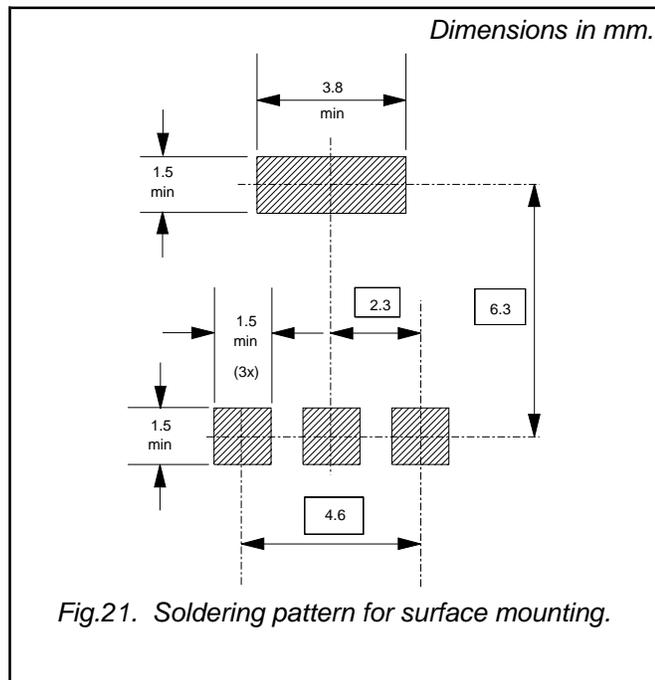
Fig.20. SOT223 surface mounting package<sup>3</sup>.

<sup>3</sup> For further information, refer to surface mounting instructions for SOT223 envelope. Epoxy meets UL94 V0 at 1/8". Net Mass: 0.11 g

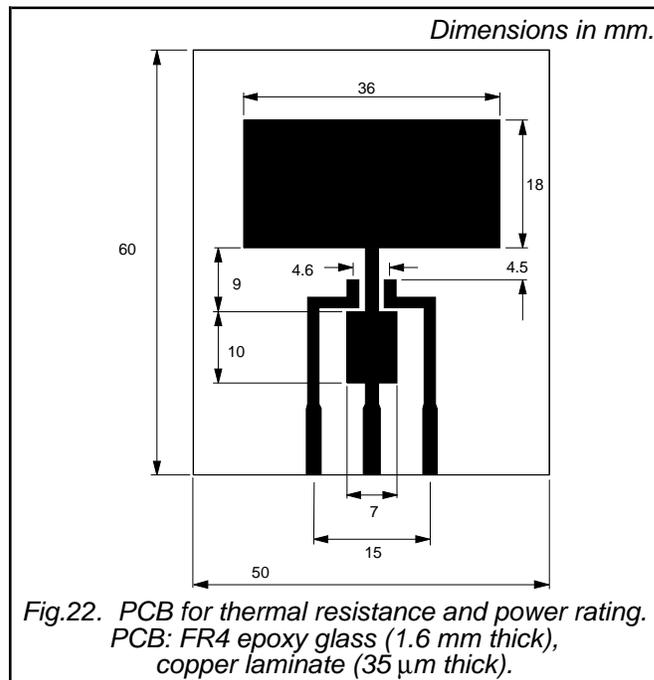
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**MOUNTING INSTRUCTIONS**



**PRINTED CIRCUIT BOARD**



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### DEFINITIONS

DATA SHEET STATUS		
DATA SHEET STATUS <sup>4</sup>	PRODUCT STATUS <sup>5</sup>	DEFINITIONS
Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice
Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product
Product data	Production	This data sheet contains data from the product specification. Philips Semiconductors reserves the right to make changes at any time in order to improve the design, manufacturing and supply. Changes will be communicated according to the Customer Product/Process Change Notification (CPCN) procedure SNW-SQ-650A
<b>Limiting values</b>		
Limiting values are given in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of this specification is not implied. Exposure to limiting values for extended periods may affect device reliability.		
<b>Application information</b>		
Where application information is given, it is advisory and does not form part of the specification.		
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<sup>5</sup> The product status of the device(s) described in this datasheet may have changed since this datasheet was published. The latest information is available on the Internet at URL <http://www.semiconductors.philips.com>.