EVALUATION KIT AVAILABLE

MAX98356

PDM Input Class D Audio Power Amplifier

General Description

The MAX98356 is a digital pulse-density modulated (PDM) input Class D power amplifier that provides Class AB audio performance with Class D efficiency. This IC offers five selectable gain settings (3dB, 6dB, 9dB, 12dB, and 15dB) set by a single gain-select input (GAIN).

The MAX98356 takes a stereo pulse density modulated (SPDM) input signal directly into the DAC. Data on the rising edge of PDM_CLK is considered left-channel data while data on the falling PDM_CLK edge is right channel. The IC can be configured to produce a left channel, right channel, or left/2 + right/2 output from the stereo input data. The IC also features an extremely robust digital audio interface with very high wideband jitter tolerance (12ns typ) on PDM_CLK.

Active emissions-limiting, edge-rate limiting, and overshoot control circuitry greatly reduce EMI. A filterless spread-spectrum modulation scheme eliminates the need for output filtering found in traditional Class D devices and reduces the component count of the solution.

The IC is available in a 9-pin WLP package (1.345mm x 1.435mm x 0.64mm) and is specified over the -40°C to +85°C temperature range.

Applications

Cellular Phones

Tablets

Portable Media Players

Notebook Computers

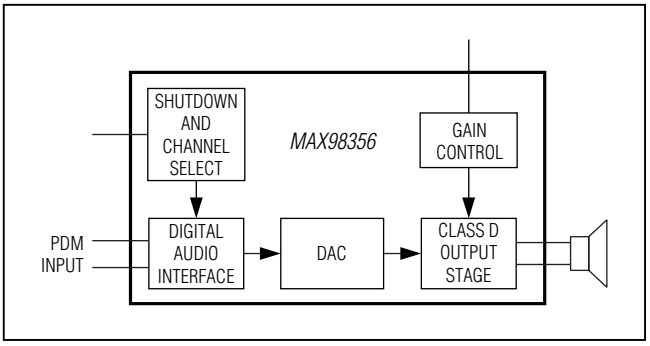
Ultrasonic Devices

***Ordering Information* and *Functional Diagram* appears at end of data sheet.**

Features

- **Single-Supply Operation (2.5V to 5.5V)**
- **3.2W Output Power into 4Ω at 5V**
- **1.8mA Quiescent Current**
- **92% Efficiency (R_L = 8Ω, P_{OUT} = 900mW, V_{DD} = 3.7V)**
- **29μV_{RMS} Output Noise (A_V = 6dB)**
- **Low 0.013% THD+N at 1kHz**
- **Exceptionally High Jitter Tolerance**
- **Supported PDM_CLK Rates of 1.84MHz–4.32MHz and 5.28MHz–8.64MHz**
- **Supports Left, Right, or Left/2 + Right/2 Outputs**
- **Sophisticated Edge Rate Control Enables Filterless Class D Outputs**
- **77dB PSRR at 217Hz**
- **Low RF Susceptibility Rejects TDMA Noise from GSM Radios**
- **Extensive Click-and-Pop Reduction Circuitry**
- **Robust Short-Circuit and Thermal Protection**
- **Available in Space-Saving Package: 1.345mm x 1.435mm WLP (0.4mm Pitch)**

Simplified Block Diagram



For related parts and recommended products to use with this part, refer to: www.maximintegrated.com/MAX98356.related

For pricing, delivery, and ordering information, please contact Maxim Direct at 1-888-629-4642, or visit Maxim's website at www.maximintegrated.com.

19-6311; Rev 1; 7/13

ABSOLUTE MAXIMUM RATINGS

V_{DD}, PDM_CLK and PDM_DATA to GND .....-0.3V to +6V
All Other Pins to GND ..... -0.3V to (V_{DD} + 0.3V)
Continuous Current In/Out of V_{DD}/GND/OUT_ ..... ±1.6A
Continuous Input Current (all other pins)..... ±20mA
Duration of OUT_ Short Circuit to GND or V_{DD}.....Continuous
Duration of OUTP Short to OUTN .....Continuous

Continuous Power Dissipation (T_A = +70°C)
WLP (derate 13.7mW/°C above +70°C).....1096mW
Junction Temperature .....+150°C
Operating Temperature Range ..... -40°C to +85°C
Storage Temperature Range..... -65°C to +150°C
Soldering Temperature (reflow) .....+230°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

PACKAGE THERMAL CHARACTERISTICS (Note 1)

WLP
Junction-to-Ambient Thermal Resistance (θ_{JA}) .....73°C/W
Junction-to-Case Thermal Resistance (θ_{JC}).....50°C/W

Note 1: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maximintegrated.com/thermal-tutorial**.

ELECTRICAL CHARACTERISTICS

(V_{DD} = 5V, V_{GND} = 0V, GAIN = V_{DD} (+6dB). PDM_CLK = 3.072MHz, speaker loads (Z_{SPK}) connected between OUTP and OUTN, Z_{SPK} = ∞, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Supply Voltage Range	V_{DD}	Guaranteed by PSSR test		2.5		5.5	V
Undervoltage Lockout	UVLO			1.4	1.8	2.3	V
Quiescent Current	I_{DD}	T_A = +25°C			2.2	2.7	mA
		T_A = +25°C, V_{DD} = 3.7V			1.8	2.2	
Shutdown Current	$I_{\overline{SHDN}}$	$\overline{SD\_MODE}$ = 0V, T_A = +25°C			0.6	2	µA
Standby Current	$I_{\overline{STNDBY}}$	$\overline{SD\_MODE}$ = 1.8V, no PDM_CLK, T_A = +25°C			300	400	µA
Turn-On Time	t_{ON}	Time from receipt of first clock cycle to full operation			0.6	0.7	ms
Output Offset Voltage	V_{OS}	T_A = +25°C, gain = 15dB			±0.3	±1.5	mV
Click-and-Pop Level	K_{CP}	Peak voltage, T_A = +25°C, A-weighted, 32 samples per second (Note 3)	Into shutdown		-66		dBV
			Out of shutdown		-72		
Power-Supply Rejection Ratio	PSRR	V_{DD} = 2.5V to 5.5V, T_A = +25°C		60	75		dB
		T_A = +25°C (Notes 3, 4)	f = 217Hz, 200mV_{P-P} ripple		77		
			f = 10kHz, 200mV_{P-P} ripple		60		

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = 5V, V_{GND} = 0V, GAIN = V_{DD} (+6dB). PDM_CLK = 3.072MHz, speaker loads (Z_{SPK}) connected between OUTP and OUTN, Z_{SPK} = ∞, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Output Power (Note 3)	P_{OUT}	THD+N 10%, gain = 12dB	Z_{SPK} = 4Ω + 33µH		3.2		W
			Z_{SPK} = 8Ω + 68µH		1.8		
			Z_{SPK} = 8Ω + 68µH, V_{DD} = 3.7V		0.93		
		THD+N = 1%, gain = 12dB	Z_{SPK} = 4Ω + 33µH		2.5		
			Z_{SPK} = 8Ω + 68µH		1.4		
			Z_{SPK} = 8Ω + 68µH, V_{DD} = 3.7V		0.77		
Total Harmonic Distortion + Noise	THD+N	f = 1kHz, P_{OUT} = 1W, T_A = +25°C, Z_{SPK} = 4Ω + 33µH			0.02	0.06	%
		f = 1kHz, P_{OUT} = 0.5W, T_A = +25°C, Z_{SPK} = 8Ω + 68µH			0.013		
Dynamic Range	DR	A-weighted, PDM_CLK = 6.144MHz, V_{RMS} = 2.54V			99		dB
Output Noise	V_N	A-weighted (Note 4)			29		μV_{RMS}
Gain (Relative to a 2.1dBV Reference Level)	A_V	GAIN = GND through 100kΩ		14.4	15	15.6	dB
		GAIN = GND		11.4	12	12.6	
		GAIN = unconnected		8.4	9	9.6	
		GAIN = V_{DD}		5.4	6	6.6	
		GAIN = V_{DD} through 100kΩ		2.4	3	3.6	
Current Limit	I_{LIM}				2.8		A
Efficiency	h	Z_{SPK} = 8Ω + 68µH, THD+N = 10%, f = 1kHz, gain = 12dB			92		%
DAC Gain Error					1		%
Frequency Response					±0.05		dB
DIGITAL AUDIO INTERFACE							
PDM_CLK High Frequency Range	f_{CLKH}			5.28		8.64	MHz
PDM_CLK Low Frequency Range	f_{CLKL}			1.84		4.32	MHz
PDM_CLK High Time	t_{PDM_CLKH}			40			ns
PDM_CLK Low Time	t_{PDM_CLKL}			40			ns
Maximum Low Frequency PDM_CLK Jitter		RMS jitter below 40kHz			0.5		ns
Maximum High Frequency PDM_CLK Jitter		RMS jitter above 40kHz			12		

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = 5V, V_{GND} = 0V, GAIN = V_{DD} (+6dB). PDM_CLK = 3.072MHz, speaker loads (Z_{SPK}) connected between OUTP and OUTN, Z_{SPK} = ∞, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input High Voltage	V_{IH}	Digital audio inputs	1.3			V
Input Low Voltage	V_{IL}	Digital audio inputs			0.6	V
Input Leakage Current	I_{IH}, I_{IL}	V_{IN} = 0V, V_{DD} = 5.5V, T_A = +25°C	-1		+1	µA
Input Capacitance	C_{IN}			3		pF
PDM Ones Density		Maximum		75		%
		Minimum		25		
PDM_DATA to PDM_CLK Setup Time	t_{SETUP}		10			ns
PDM_DATA to PDM_CLK Hold Time	t_{HOLD}		10			
$\overline{\text{SD\_MODE}}$ COMPARATOR TRIP POINTS						
B0		See $\overline{\text{SD\_MODE}}$ and shutdown operation for details	0.08	0.16	0.355	V
B1			0.65	0.77	0.825	
B2			1.245	1.4	1.5	
$\overline{\text{SD\_MODE}}$ Pulldown Resistor	R_{PD}		92	100	108	kΩ
GAIN COMPARATOR TRIP POINTS						
	V_{GAIN}	A_V = 3dB gain	0.65 x V_{DD}		0.85 x V_{DD}	V
		A_V = 6dB gain	0.9 x V_{DD}		V_{DD}	
		A_V = 9dB gain	0.4 x V_{DD}		0.6 x V_{DD}	
		A_V = 12dB gain	0		0.1 x V_{DD}	
		A_V = 15dB gain	0.15 x V_{DD}		0.35 x V_{DD}	

Note 2: 100% production tested at T_A = +25°C. Specifications over temperature limits are guaranteed by design.

Note 3: Class D amplifier testing performed with a resistive load in series with an inductor to simulate an actual speaker load. For R_L = 8Ω, L_L = 68µH. For R_L = 4Ω, L_L = 33µH.

Note 4: Digital silence used for input signal.

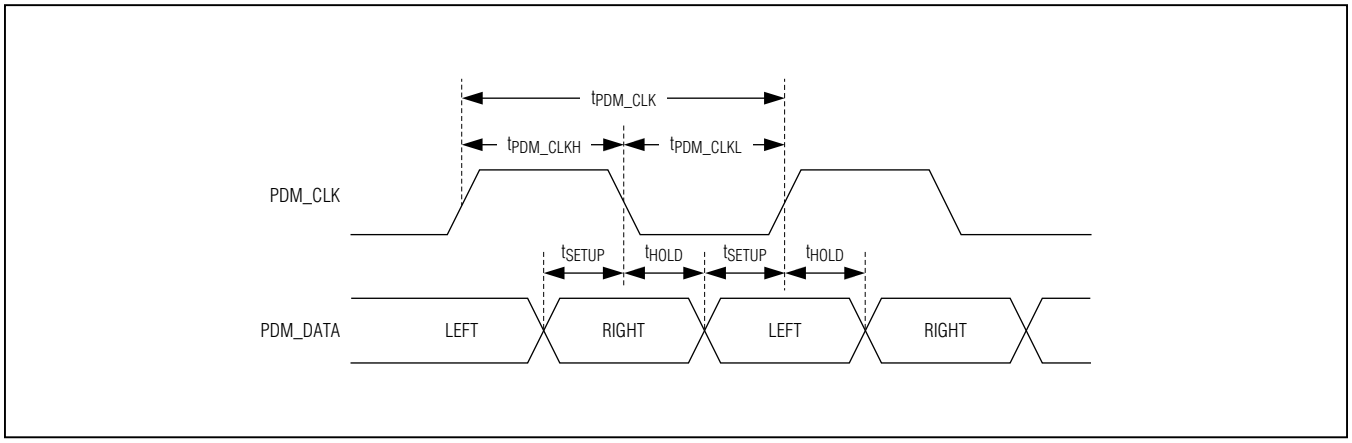


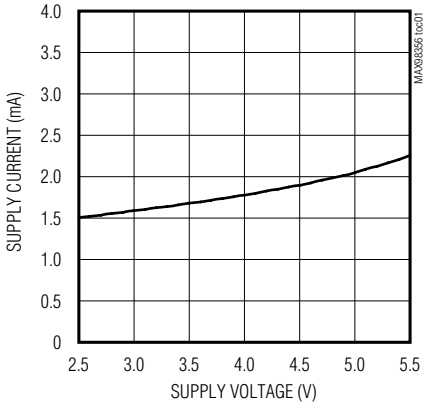
Figure 1. PDM Audio Interface Timing Diagram

Typical Operating Characteristics

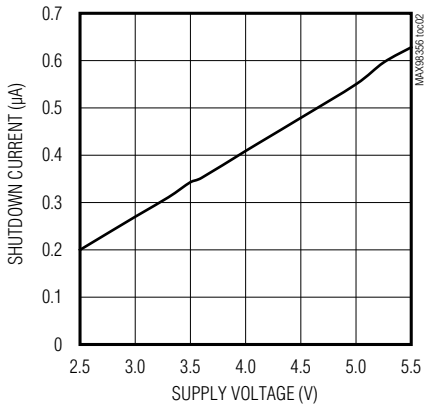
(V_{DD} = 5V, V_{GND} = 0V, GAIN = V_{DD} (+6dB). PDM_CLK = 3.072MHz, speaker loads (Z_{SPK}) connected between OUTP and OUTN, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

General

SUPPLY CURRENT vs. SUPPLY VOLTAGE



SHUTDOWN CURRENT vs. SUPPLY VOLTAGE

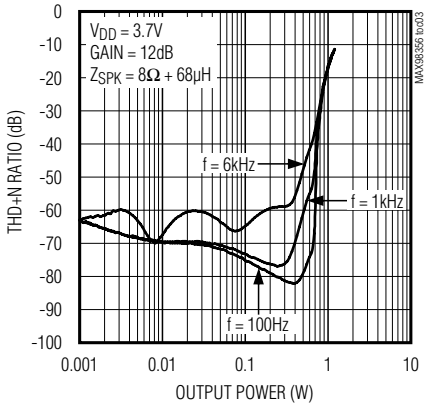


Typical Operating Characteristics (continued)

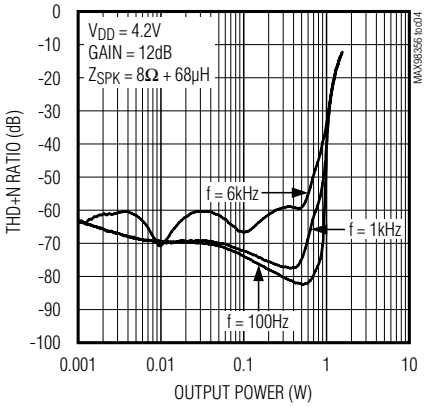
(V_{DD} = 5V, V_{GND} = 0V, GAIN = V_{DD} (+6dB). PDM_CLK = 3.072MHz, speaker loads (Z_{SPK}) connected between OUTP and OUTN, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

Speaker Amplifier

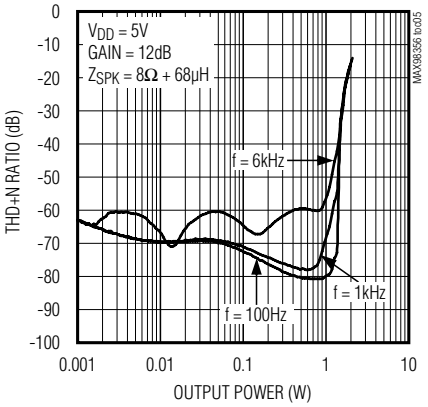
TOTAL HARMONIC DISTORTION PLUS NOISE vs. OUTPUT POWER



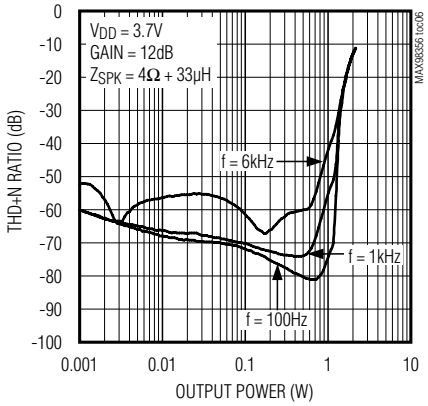
TOTAL HARMONIC DISTORTION PLUS NOISE vs. OUTPUT POWER



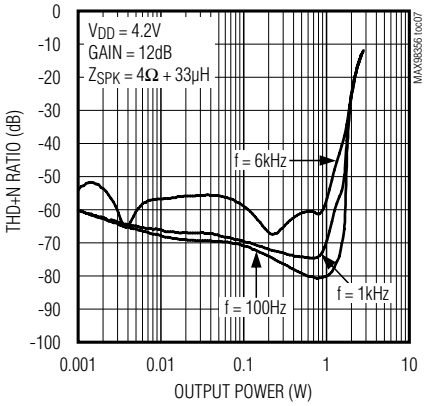
TOTAL HARMONIC DISTORTION PLUS NOISE vs. OUTPUT POWER



TOTAL HARMONIC DISTORTION PLUS NOISE vs. OUTPUT POWER



TOTAL HARMONIC DISTORTION PLUS NOISE vs. OUTPUT POWER



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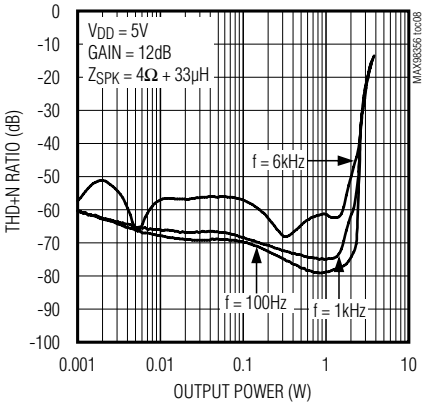
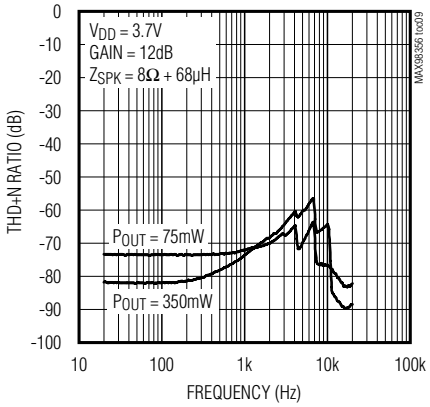


Typical Operating Characteristics (continued)

(V_{DD} = 5V, V_{GND} = 0V, GAIN = V_{DD} (+6dB). PDM_CLK = 3.072MHz, speaker loads (Z_{SPK}) connected between OUTP and OUTN, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

TOTAL HARMONIC DISTORTION PLUS NOISE vs. FREQUENCY



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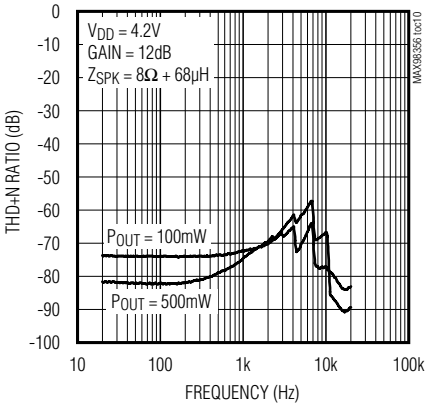

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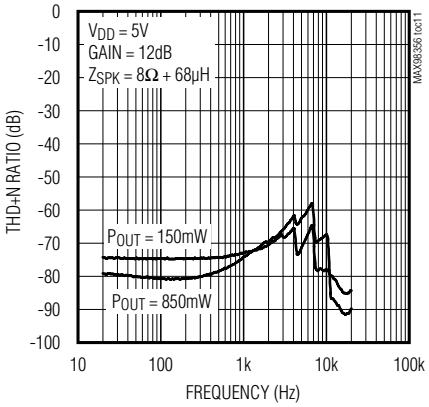

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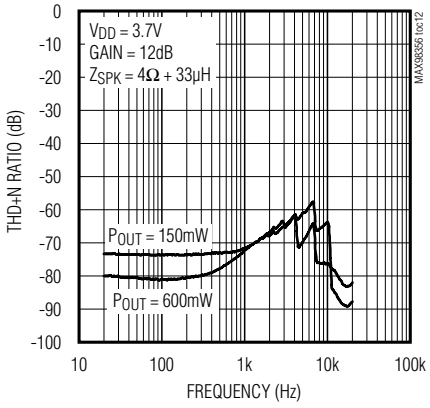

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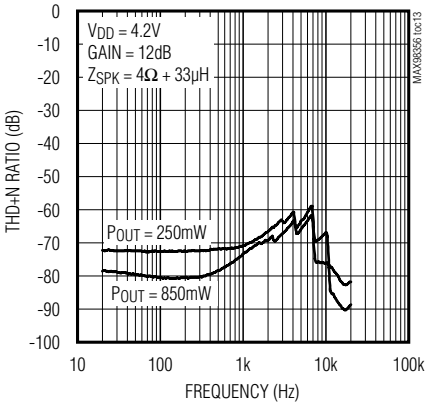

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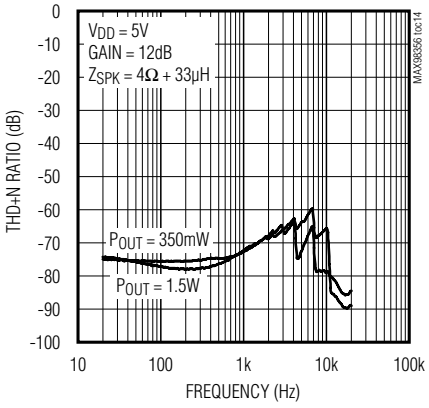
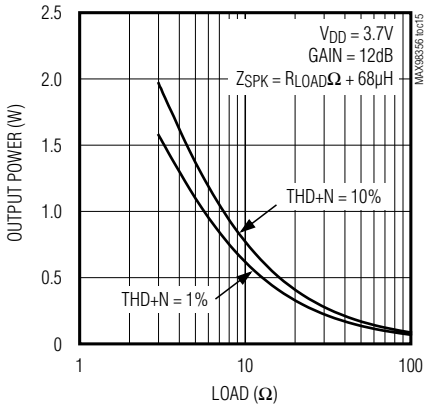


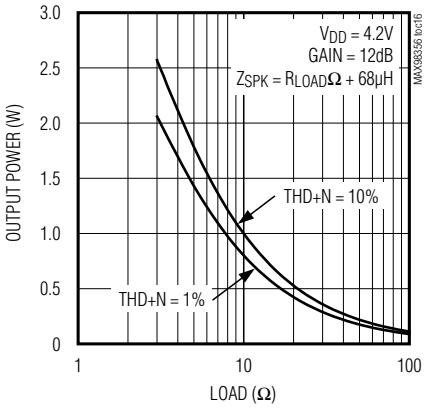
Typical Operating Characteristics (continued)

(V_{DD} = 5V, V_{GND} = 0V, GAIN = V_{DD} (+6dB). PDM_CLK = 3.072MHz, speaker loads (Z_{SPK}) connected between OUTP and OUTN, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

OUTPUT POWER vs. LOAD RESISTANCE



OUTPUT POWER vs. LOAD RESISTANCE



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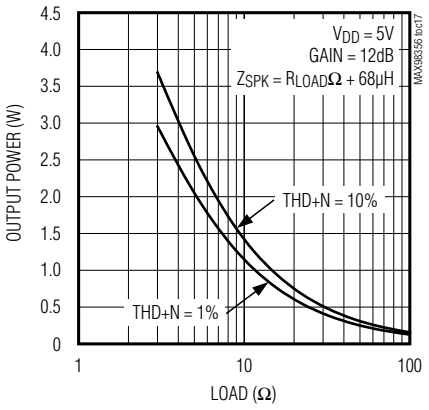
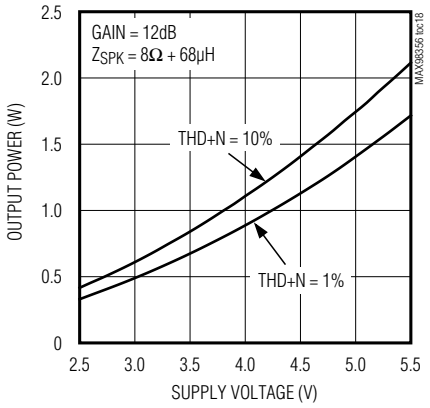
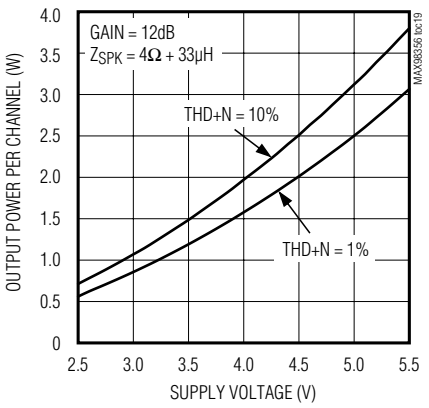


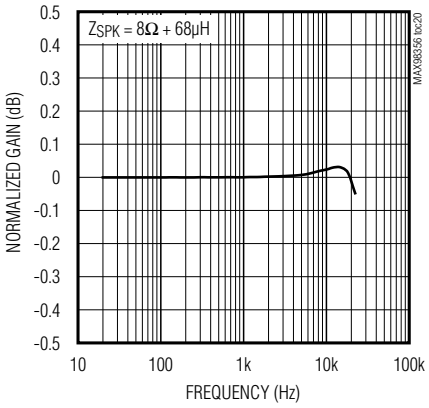
OUTPUT POWER vs. SUPPLY VOLTAGE



OUTPUT POWER vs. SUPPLY VOLTAGE



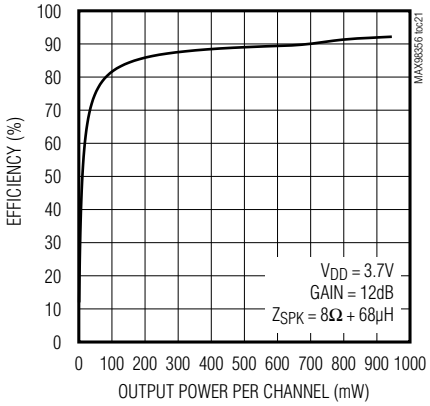
NORMALIZED GAIN vs. FREQUENCY



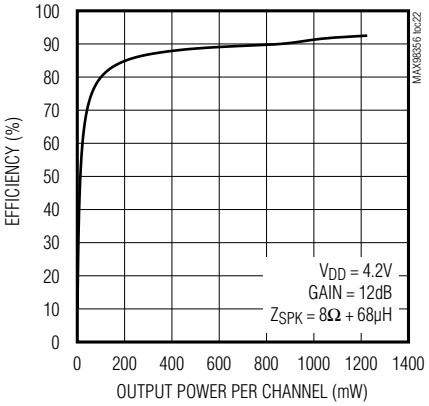
Typical Operating Characteristics (continued)

(V_{DD} = 5V, V_{GND} = 0V, GAIN = V_{DD} (+6dB). PDM_CLK = 3.072MHz, speaker loads (Z_{SPK}) connected between OUTP and OUTN, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

EFFICIENCY vs. OUTPUT POWER



EFFICIENCY vs. OUTPUT POWER



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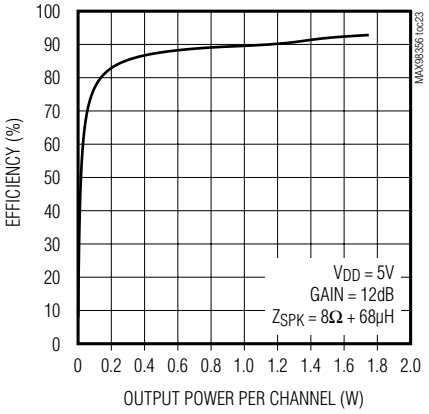

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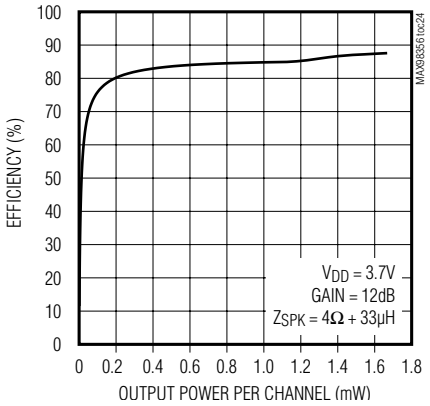

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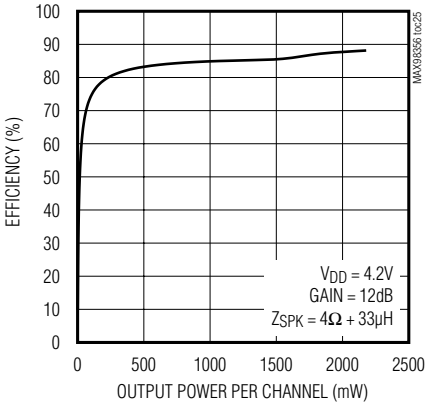

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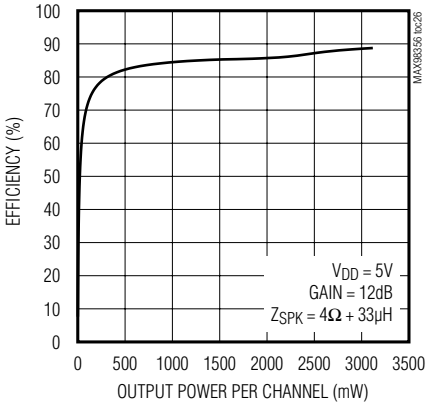
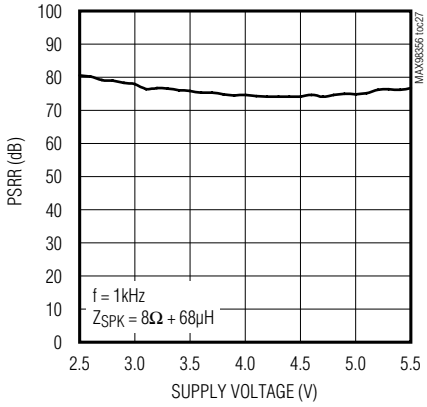


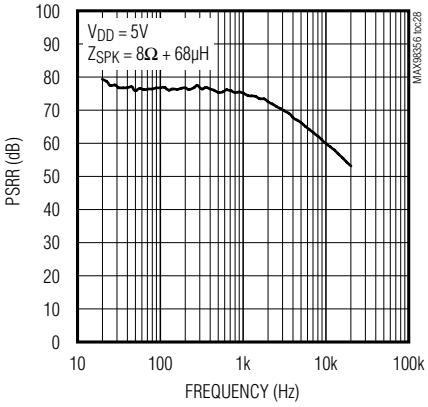
Typical Operating Characteristics (continued)

(V_{DD} = 5V, V_{GND} = 0V, GAIN = V_{DD} (+6dB). PDM_CLK = 3.072MHz, speaker loads (Z_{SPK}) connected between OUTP and OUTN, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

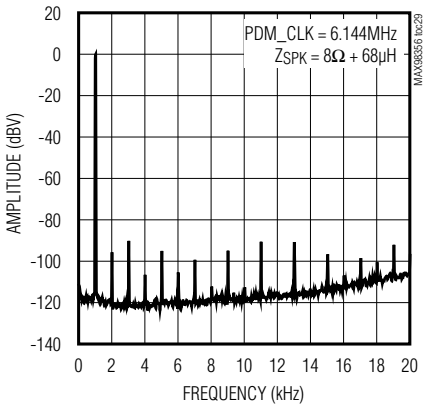
POWER-SUPPLY REJECTION RATIO vs. SUPPLY VOLTAGE



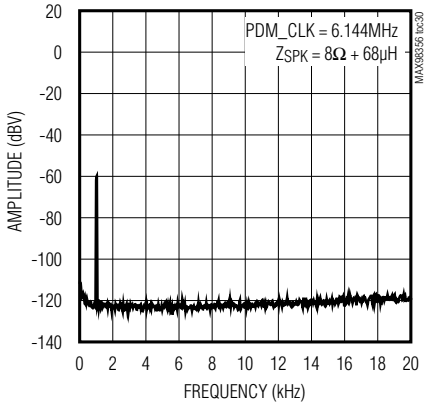
POWER-SUPPLY REJECTION RATIO vs. FREQUENCY



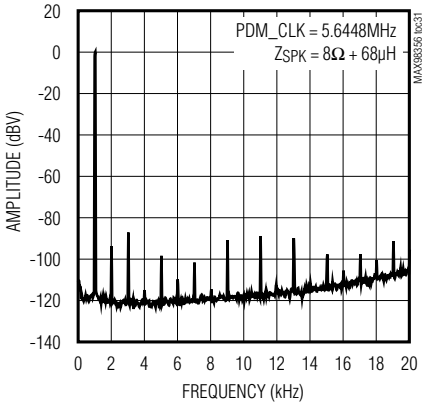
INBAND OUTPUT SPECTRUM



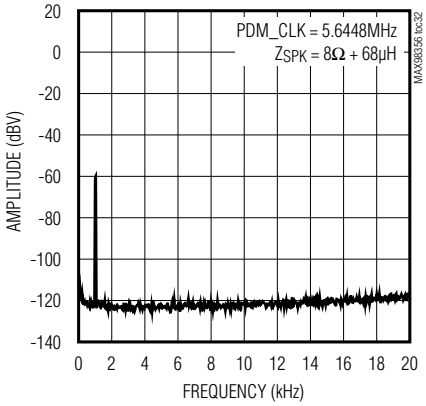
INBAND OUTPUT SPECTRUM



INBAND OUTPUT SPECTRUM



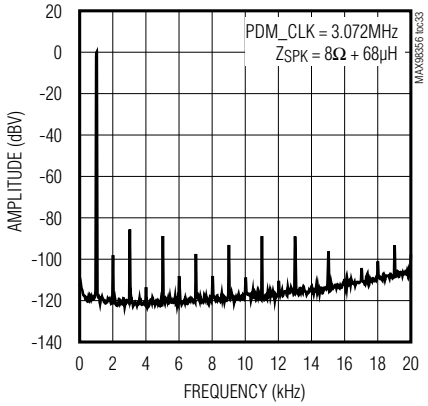
INBAND OUTPUT SPECTRUM



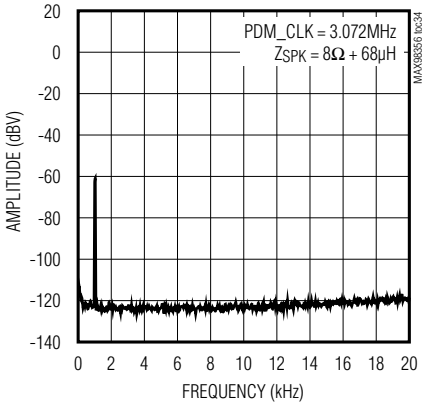
Typical Operating Characteristics (continued)

(V_{DD} = 5V, V_{GND} = 0V, GAIN = V_{DD} (+6dB). PDM_CLK = 3.072MHz, speaker loads (Z_{SPK}) connected between OUTP and OUTN, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

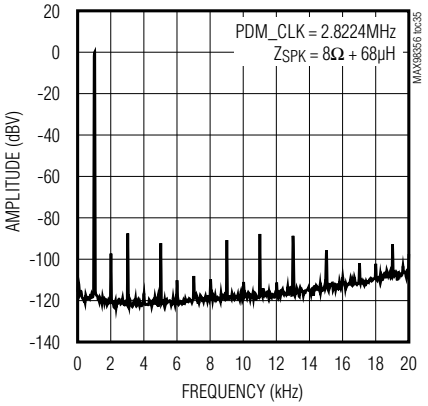
INBAND OUTPUT SPECTRUM



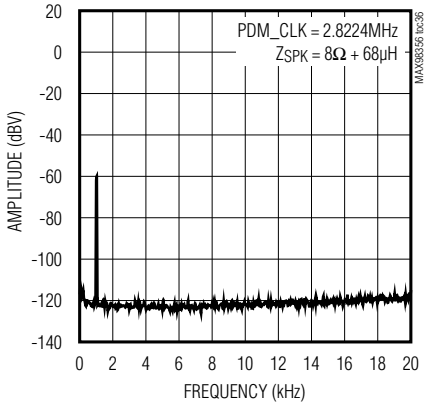
INBAND OUTPUT SPECTRUM



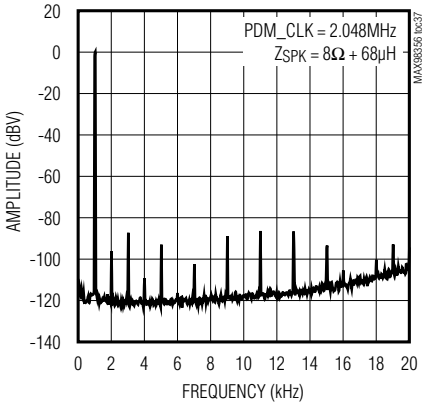
INBAND OUTPUT SPECTRUM



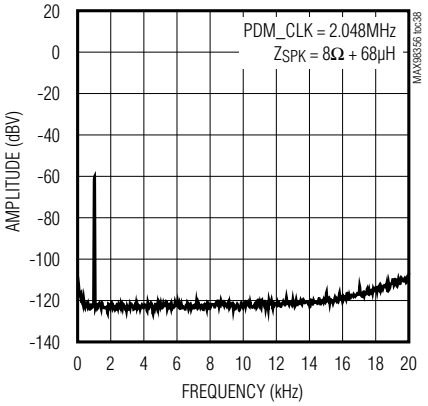
INBAND OUTPUT SPECTRUM



INBAND OUTPUT SPECTRUM

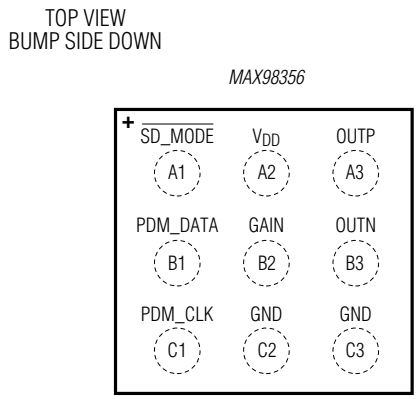


INBAND OUTPUT SPECTRUM



PDM Input Class D Audio Power Amplifier

Pin Configuration



WLP

Pin Description

PIN	NAME	FUNCTION	
A1	$\overline{SD\_MODE}$	Shutdown and Channel Select. Determines left, right, or left/2 + right/2 mix and also used for shutdown. See Table 5.	
A2	V_{DD}	Power-Supply Input	
A3	OUTP	Positive Speaker Amplifier Output	
B1	PDM_DATA	PDM Digital Input Signal	
B2	GAIN	**Amplifier Gain**	
		Gain Connections	**Gain (dB)**
		GND through 100kΩ resistor	15
		GND	12
		Unconnected	9
		V_{DD}	6
		V_{DD} through 100kΩ resistor	3
B3	OUTN	Negative Speaker Amplifier Output	
C1	PDM_CLK	PDM Bit Clock Input Signal. Supports frequency ranges: 1.84MHz–4.32MHz and 5.28 MHz–8.64MHz.	
C2, C3	GND	Ground	

Detailed Description

The MAX98356 is a digital PDM input Class D power amplifier. The PDM modulation scheme uses the relative density of digital pulses to represent the amplitude of an analog signal. The IC accepts stereo PDM data through PDM_DATA and PDM_CLK.

$\overline{SD\_MODE}$ selects which audio channel is output by the amplifier and is used to put the IC into shutdown. The GAIN pin offers five gain settings and allows the output of the amplifier to be tuned to the appropriate level.

Table 1. PDM_CLK Polarity

PDM_CLK EDGE DIRECTION	CHANNEL
Rising edge	Left
Falling edge	Right

Table 2. PDM_CLK Rates

SUPPORTED CLOCK RATES (MHz)
1.84–4.32
5.28–8.64

The output stage features low-quiescent current, comprehensive click-and-pop suppression, and excellent RF immunity. The IC offers Class AB audio performance with Class D efficiency in a minimal board-space solution. The Class D amplifier features spread-spectrum modulation with edge-rate and overshoot control circuitry that offers significant improvements in switch-mode amplifier radiated emissions. The amplifier features click-and-pop suppression that reduces audible transients on startup and shutdown. The amplifier includes thermal-overload and short-circuit protection.

Digital Audio Interface

The IC takes a stereo PDM input signal directly into the DAC. Data read on the rising edge of PDM_CLK is left-channel data while data read on the falling PDM_CLK edge is right channel (Table 1).

Supported PDM_CLK Rates

Table 2 indicates the range of PDM_CLK rates that are supported by the IC. Table 3 indicates the specific clock rates to use based on the baseband rate and the oversample rate of the incoming PDM signal.

PDM_CLK Jitter Tolerance

The IC features a very high PDM_CLK jitter tolerance of 0.5ns for RMS jitter below 40kHz and 12ns for wideband RMS jitter while maintaining a dynamic range greater than 98dB (Table 4).

Table 3. Calculated PDM_CLK Rates

BASEBAND SAMPLE RATE (kHz)	INPUT CLOCK RATES (MHz)			
	32x OVERSAMPLED PDM	64x OVERSAMPLED PDM	128x OVERSAMPLED PDM	256x OVERSAMPLED PDM
8	—	—	—	2.048
16	—	—	2.048	4.096
32	—	2.048	4.096	—
44.1	—	2.8224	5.6448*	—
48	—	3.072	6.144*	—
88.2	2.8224	5.6448*	—	—
96	3.072	6.144*	—	—

**The mono left/2 + right/2 feature is not supported at PDM_CLK rates of 5.28MHz and above.*

Table 4. RMS Jitter Tolerance

FREQUENCY	RMS JITTER TOLERANCE (ns)
< 40kHz	0.5
40kHz–BCLK	12

PDM Timing Characteristics

Figure 2 shows the PDM operation of the IC. The bit-depth is one bit and each bit alternates between left-channel and right-channel data.

If the PDM generator produces data that is stuck at logic-high or logic-low, then the output of the IC is railed, forcing DC at the load. Therefore, it is recommended that the PDM generator includes protection to detect this invalid condition. If such a condition is detected, then the IC should either be put into shutdown or PDM_CLK should be stopped.

Standby Mode

If PDM_CLK stops toggling, the IC automatically enters standby mode. In standby mode, the Class D speaker amplifier is turned off and the outputs go into a high-impedance state, ensuring that the unwanted current is not transferred to the load during this condition. Standby mode should not be used in place of the shutdown mode because the shutdown mode provides the lowest power consumption and the best power-on/off click-and-pop performance.

$\overline{\text{SD\_MODE}}$ Pin and Shutdown Operation

The IC features a low-power shutdown mode, drawing less than 0.6µA (typ) of supply current. During shutdown, all internal blocks are turned off, including setting the output stage to a high-impedance state. Drive $\overline{\text{SD\_MODE}}$ low to put the IC into shutdown.

The state of $\overline{\text{SD\_MODE}}$ determines the audio channel that is sent to the amplifier output (Table 5).

Drive $\overline{\text{SD\_MODE}}$ high to select the left channel of the stereo input data. Drive $\overline{\text{SD\_MODE}}$ high through a sufficiently small resistor to select the right channel of the stereo input data. Drive $\overline{\text{SD\_MODE}}$ high through a sufficiently large resistor to select both the left and right channels of the stereo input data (left/2 + right/2). The left/2 + right/2 mode is not supported for PDM_CLK rates above 5.28MHz. R_{LARGE} and R_{SMALL} are determined by the

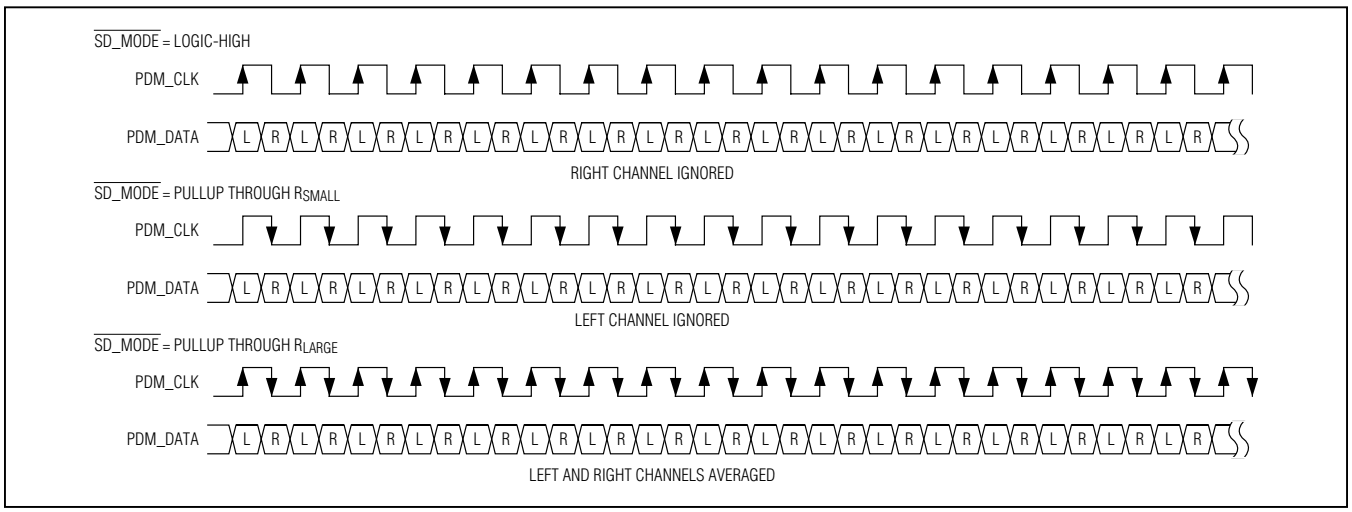


Figure 2. PDM Digital Audio Interface Timing

Table 5. $\overline{\text{SD\_MODE}}$ Control

$\overline{\text{SD\_MODE}}$ STATUS		SELECTED CHANNEL
High	$V_{\overline{SD\_MODE}}$ > B2 trip point (1.4V typ)	Left
Pullup through R_{SMALL}	B2 trip point (1.4V typ) > $V_{\overline{SD\_MODE}}$ > B1 trip point (0.77V typ)	Right
Pullup through R_{LARGE}	B1 trip point (0.77V typ) > $V_{\overline{SD\_MODE}}$ > B0 trip point (0.16V typ)	Left/2 + right/2
Low	B0 trip point (0.16V typ) > $V_{\overline{SD\_MODE}}$	Shutdown

V_{DDIO} voltage (logic voltage from control interface) that is driving $\overline{SD\_MODE}$ according to the following two equations:

$$R_{SMALL}\ (k\Omega) = 98.5 \times V_{DDIO} - 100$$

$$R_{LARGE}\ (k\Omega) = 222.2 \times V_{DDIO} - 100$$

Figure 3 and Figure 4 show how to connect an external resistor to $\overline{SD\_MODE}$ when using an open-drain driver or a pullup/down driver.

When the device is configured in left channel mode ($\overline{SD\_MODE}$ is directly driven to logic-high by the control interface) care must be taken to avoid violating the Absolute Maximum Ratings limits for $\overline{SD\_MODE}$. Ensuring that V_{DD} is always greater than V_{DDIO} is one way to prevent $\overline{SD\_MODE}$ from violating the Absolute Maximum Ratings limits. If this is not possible in the application (e.g., if V_{DD} < 3.0V and V_{DDIO} = 3.3V), then it is necessary to add a small resistance (~2kΩ) in series with $\overline{SD\_MODE}$ to limit the current into the $\overline{SD\_MODE}$ pin. This is not a concern when using the right channel or (left + right)/2 modes.

Class D Speaker Amplifier

The filterless Class D amplifier offers much higher efficiency than Class AB amplifiers. The high efficiency of a Class D amplifier is due to the switching operation of the output stage transistors. Any power loss associated with the Class D output stage is mostly due to the I^2R loss of the MOSFET on-resistance and quiescent current overhead.

Ultra-Low EMI Filterless Output Stage

Traditional Class D amplifiers require the use of external LC filters, or shielding, to meet EN55022B electromagnetic-interference (EMI) regulation standards. Maxim's active emissions-limiting edge-rate control circuitry and spread-spectrum modulation reduces EMI emissions while maintaining up to 92% efficiency.

Maxim's spread-spectrum modulation mode flattens wideband spectral components while proprietary techniques ensure that the cycle-to-cycle variation of the switching period does not degrade audio reproduction or efficiency. The ICs' spread-spectrum modulator randomly varies the switching frequency by ±10kHz around the center frequency (300kHz). Above 10MHz, the wideband spectrum looks like noise for EMI purposes (Figure 5).

Speaker Current Limit

If the output current of the speaker amplifier exceeds the current limit (2.8A typ), the IC disables the outputs for approximately 100µs. At the end of the 100µs, the outputs are re-enabled. If the fault condition still exists, the IC continues to disable and re-enable the outputs until the fault condition is removed.

Gain Selection

The IC offers five programmable gain selections through a singel gain input (GAIN). Gain is referenced to the full-scale output of the DAC, which is 2.1dBV (Table 7). Assuming that the desired output swing is not limited by the supply voltage rail, the IC's output level can be calculated based on the PDM input ones's density and selected amplifier gain according to the following equation:

Output signal level (dBV) = 20 x log[abs(PDM one's density(%) - 50) /25] (dBFS) + 2.1dB + selected speaker amplifier gain (dB)

where the one's density of the PDM input ranges from 75% (maximum positive magnitude) to 25% (maximum negative magnitude). 0dFBS is referenced to 0dBV.

Click-and-Pop Suppression

The IC speaker amplifier features Maxim's comprehensive click-and-pop suppression. During startup, the click-and-pop suppression circuitry reduces audible transient sources internal to the device. To achieve optimal click-and-pop reduction at startup, it is recommended that idle data be sent to the digital audio interface for the first 0.5ms of turn-on time. When entering shutdown, the differential speaker outputs immediately go to a high-impedance state without creating an audible click-and-pop noise.

Table 6. Examples of $\overline{SD\_MODE}$ Pullup Resistor Values

LOGIC VOLTAGE LEVEL (V_{DDIO}) (V)	R_{SMALL} (kΩ, 1% tolerance)	R_{LARGE} (kΩ, 1% tolerance)
1.8	76.8	300
3.3	226	634

Table 7. Gain Selection

GAIN	GAIN (dB)
Connect to GND through 100kΩ ±5% resistor	15
Connect to GND	12
Unconnected	9
Connect to V_{DD}	6
Connect to V_{DD} through 100kΩ ±5% resistor	3

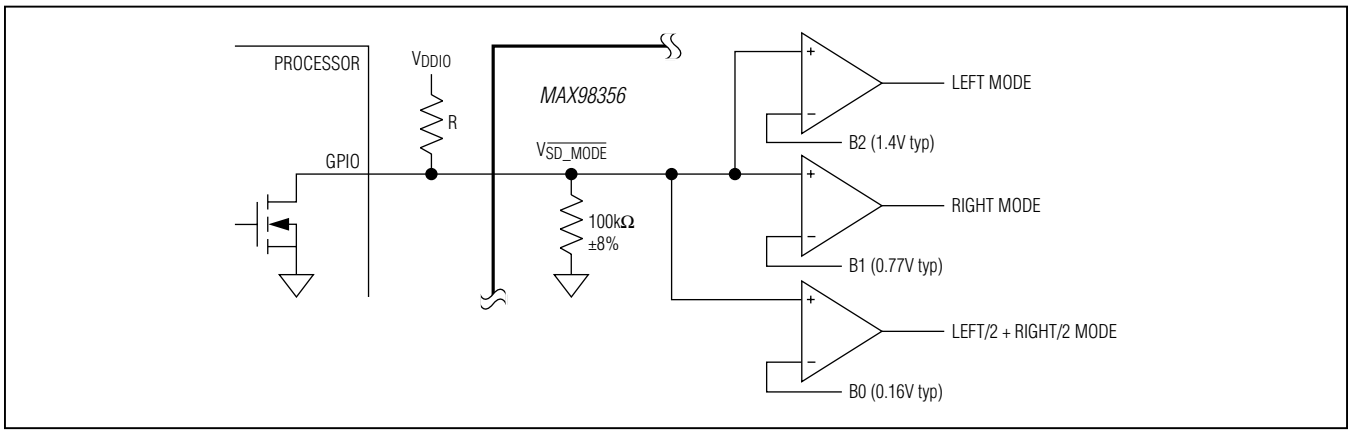


Figure 3. $\overline{SD\_MODE}$ Resistor Connection Using Open-Drain Driver

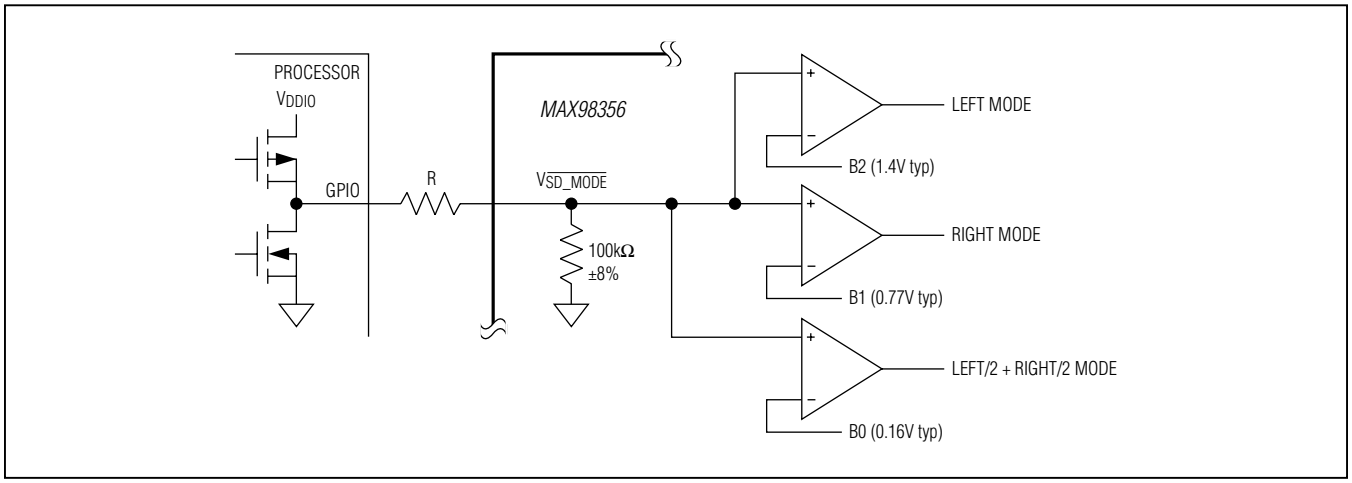


Figure 4. $\overline{SD\_MODE}$ Resistor Connection Using Pullup/Down Driver

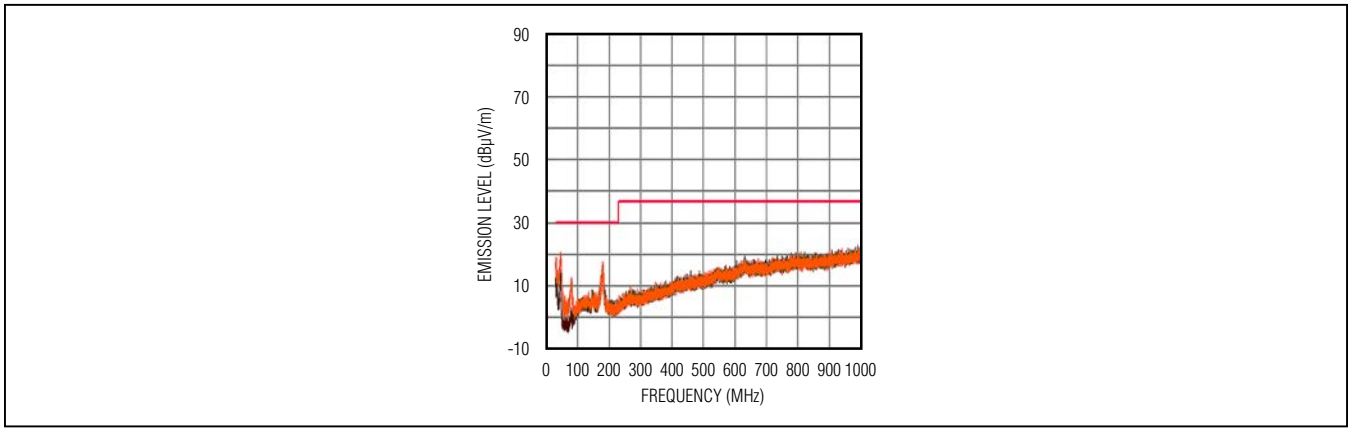


Figure 5. EMI with 12in of Speaker Cable and No Output Filtering

Applications Information

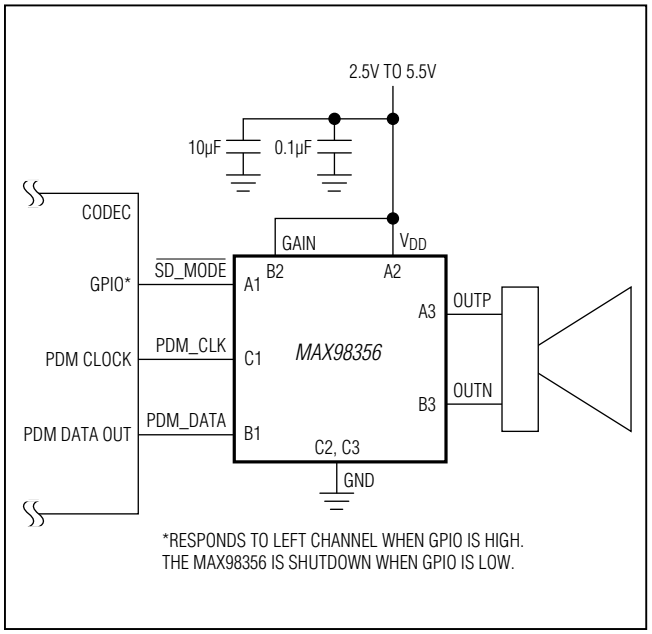


Figure 6. Left-Channel Operation with 6dB Gain

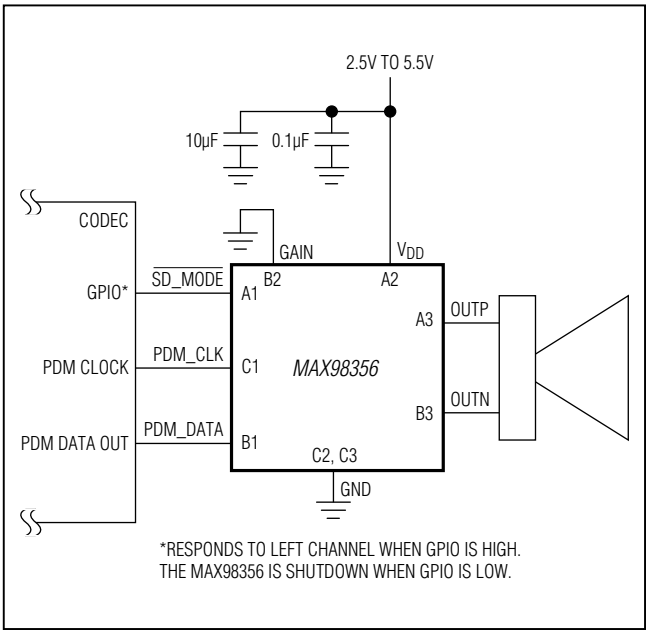


Figure 7. Left-Channel Operation with 12dB Gain

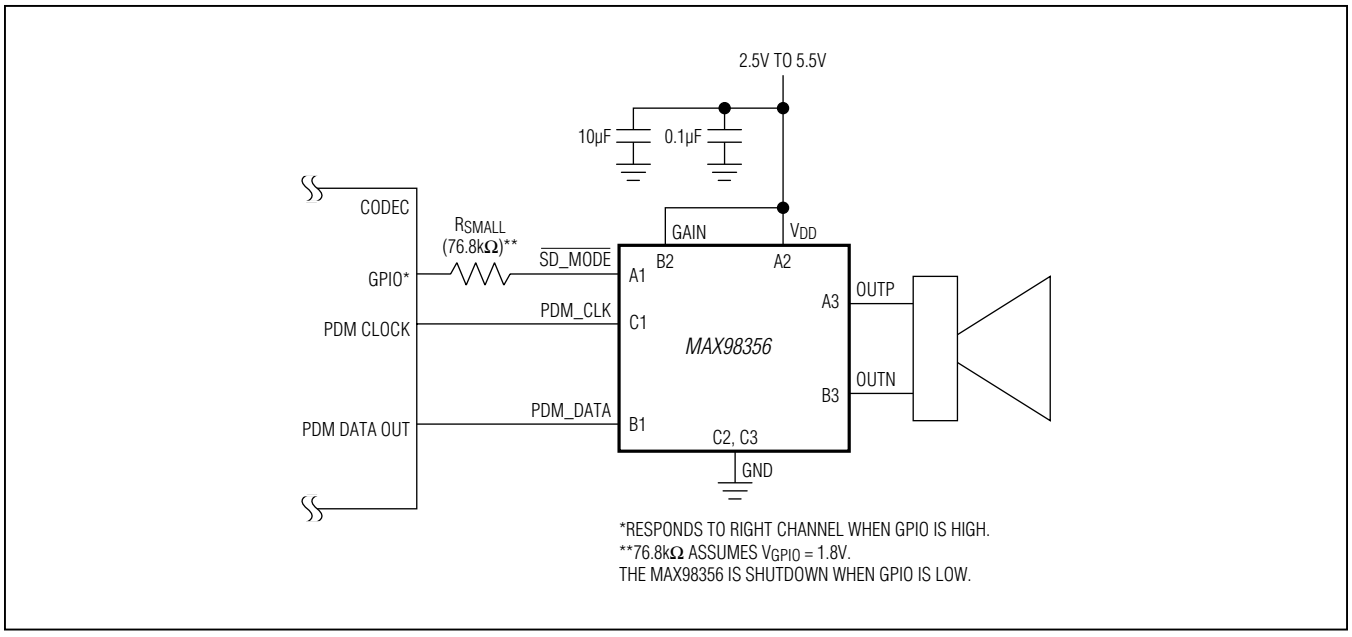


Figure 8. Right-Channel Operation with 6dB Gain

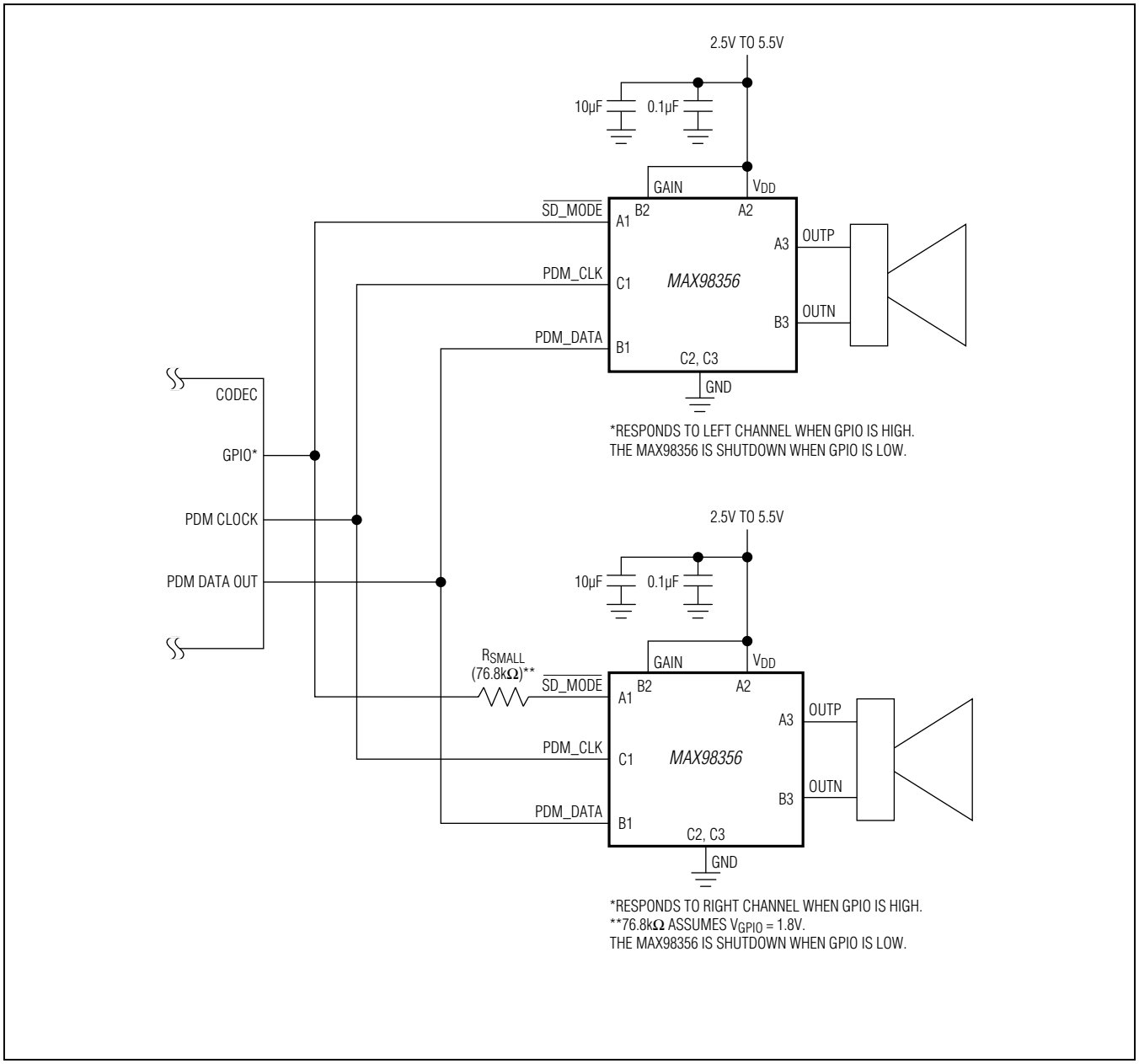


Figure 9. Stereo Operation Using Two ICs

Filterless Class D Operation

Traditional Class D amplifiers require an output filter to recover the audio signal from the amplifier's output. The filter adds cost, size, and decreases efficiency and THD+N performance. The IC's filterless modulation scheme does not require an output filter. The device relies on the inherent inductance of the speaker coil and the natural filtering of both the speaker and the human ear to recover the audio component of the square-wave output.

Because the switching frequency of the IC is well beyond the bandwidth of most speakers, voice coil movement due to the switching frequency is very small. Use a speaker with a series inductance > 10µH. Typical 8Ω speakers exhibit series inductances in the 20µH to 100µH range.

Power-Supply Input

V_{DD}, which ranges from 2.5V to 5.5V, powers the IC, including the speaker amplifier. Bypass V_{DD} with a 0.1µF and 10µF capacitor to GND. Some applications might require only the 10µF bypass capacitor, making it possible to operate with a single external component. Apply additional bulk capacitance at the IC if long input traces between V_{DD} and the power source are used.

Layout and Grounding

Proper layout and grounding are essential for optimum performance. Good grounding improves audio performance and prevents switching noise from coupling into the audio signal.

Use wide, low-resistance output traces. As load impedance decreases, the current drawn from the device outputs increases. At higher current, the resistance of the output traces decreases the power delivered to the load. For example, if 2W is delivered from the speaker output to a 4Ω load through 100mΩ of total speaker trace, 1.904W is being delivered to the speaker. If power is delivered through 10mΩ of total speaker trace, 1.951W is being delivered to the speaker. Wide output, supply, and ground traces also improve the power dissipation of the IC.

The IC is inherently designed for excellent RF immunity. For best performance, add ground fills around all signal traces on top or bottom PCB planes.

WLP Applications Information

For the latest application details on WLP construction, dimensions, tape carrier information, PCB techniques, bump-pad layout, and recommended reflow temperature profile, as well as the latest information on reliability testing results, refer to the Application Note 1891: *Wafer-Level Packaging (WLP) and Its Applications*. Figure 11 shows the dimensions of the WLP balls used on the IC.

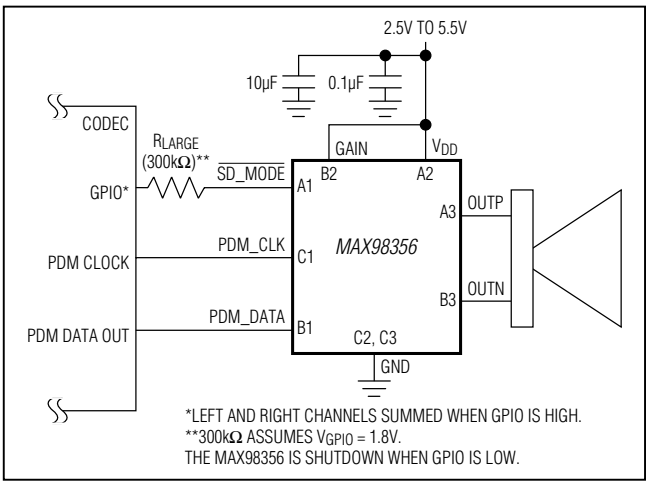


Figure 10. Left/2 + Right/2 Operation with 6dB Gain

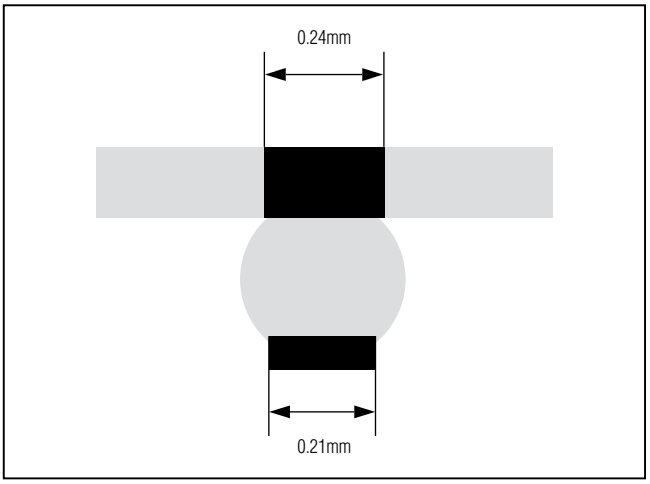
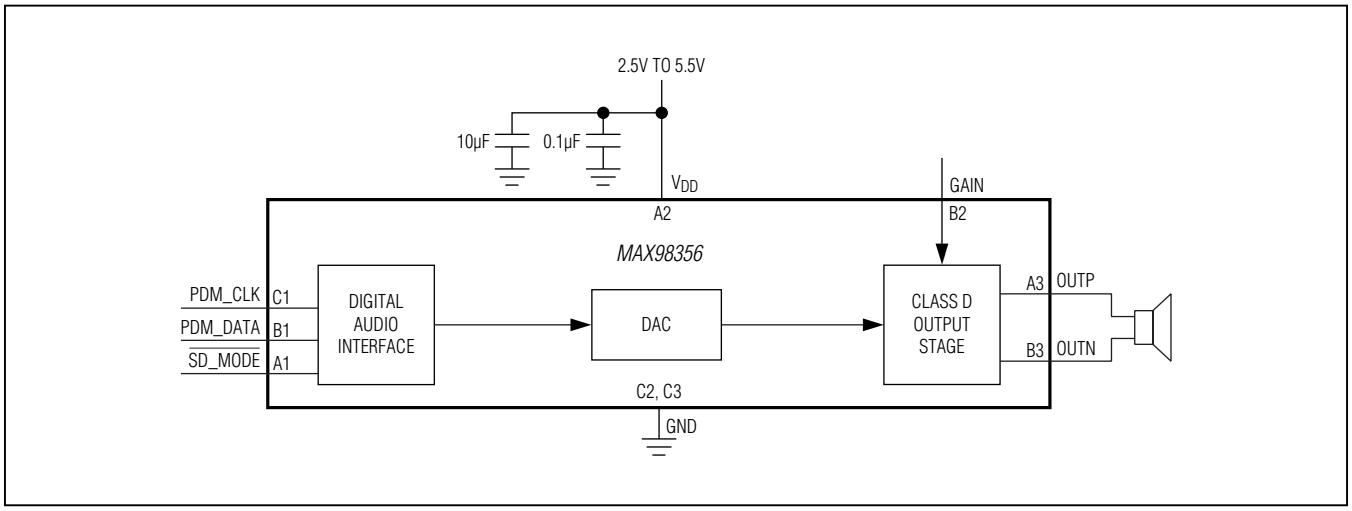


Figure 11. MAX98356 WLP Ball Dimensions

PDM Input Class D Audio Power Amplifier

Functional Diagram



Ordering Information

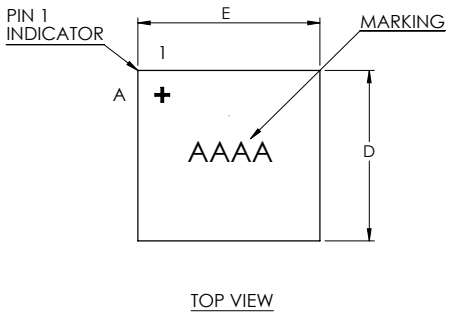
PART	TEMP RANGE	PIN-PACKAGE
MAX98356EWL+	-40°C to +85°C	9 WLP

+Denotes a lead(Pb)-free/RoHS-compliant package.

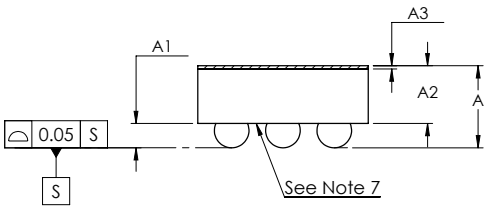
Package Information

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
9 WLP	W91F1+1	21-0459	Refer to Application Note 1891

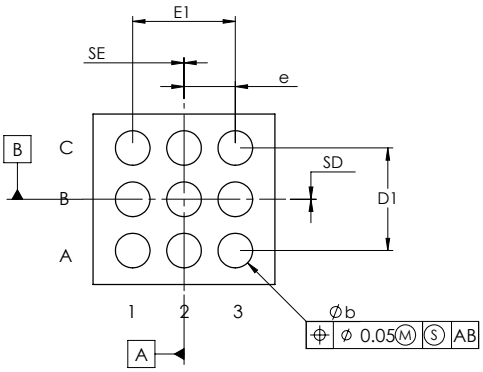


TOP VIEW



SIDE VIEW

COMMON DIMENSIONS		
A	0.64	±0.05
A1	0.19	±0.03
A2	0.45	REF
A3	0.025	BASIC
b	Ø0.27	±0.03
D1	0.80	BASIC
E1	0.80	BASIC
e	0.40	BASIC
SD	0.00	BASIC
SE	0.00	BASIC



BOTTOM VIEW

PKG. CODE	E	D	DEPOPULATED BUMPS
W91B1+7	1.260±0.040	1.260±0.040	NONE
W91C1+1	1.595±0.035	1.415±0.035	NONE
W91F1+1	1.435±0.015	1.345±0.015	NONE
W91G1+1	1.465±0.015	1.455±0.015	NONE
W91J1+1	1.238±0.015	1.238±0.015	NONE

NOTES:
1. Terminal pitch is defined by terminal center to center value.
2. Outer dimension is defined by center lines between scribe lines.
3. All dimensions in millimeter.
4. Marking shown is for package orientation reference only.
5. Tolerance is ± 0.02 unless specified otherwise.
6. All dimensions apply to PbFree (+) package codes only.
7. Front - side finish can be either Black or Clear.

- DRAWING NOT TO SCALE -

maxim integrated™

TITLE		
PACKAGE OUTLINE 9 BUMPS, WLP PKG. 0.4mm PITCH		
APPROVAL	DOCUMENT CONTROL NO. 21-0459	REV. G

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	5/12	Initial release	—
1	7/13	New lower tolerances in the *Electrical Characteristics* table and throughout; updates to the *Typical Operating Characteristics* global conditions	1–11

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