

DATA SHEET

CBT6800

10-bit bus switch with precharged outputs
for live insertion

Product data
Supersedes data of 1999 Oct 28

2003 Sep 12

10-bit bus switch with precharged outputs for live insertion

CBT6800

FEATURES

- 5 Ω switch connection between two ports
- TTL compatible input and output levels
- Outputs are precharged by bias voltage to minimize signal distortion during live insertion
- Latch-up protection exceeds 100 mA per JESD78
- ESD protection exceeds 2000 V HBM per JESD22-A114, 200 V MM per JESD22-A115 and 1000 V CDM per JESD22-C101

DESCRIPTION

The CBT6800 provides ten bits of high-speed TTL-compatible bus switching. The low on-state resistance of the switch allows bi-directional connections to be made while adding near-zero propagation delay. The device also precharges the B port to a user-selectable bias voltage (BIASV) to minimize live-insertion noise.

The CBT6800 is organized as one 10-bit switch with a single enable ($\overline{OE}$) input. When $\overline{OE}$ is low, the switch is on and port A is connected to port B. When $\overline{OE}$ is high, the switch between port A and port B is open and the B port is precharged to BIASV through the equivalent of a 10 k Ω resistor.

The CBT6800 is characterized for operation from -40 to 85 $^{\circ}\text{C}$.

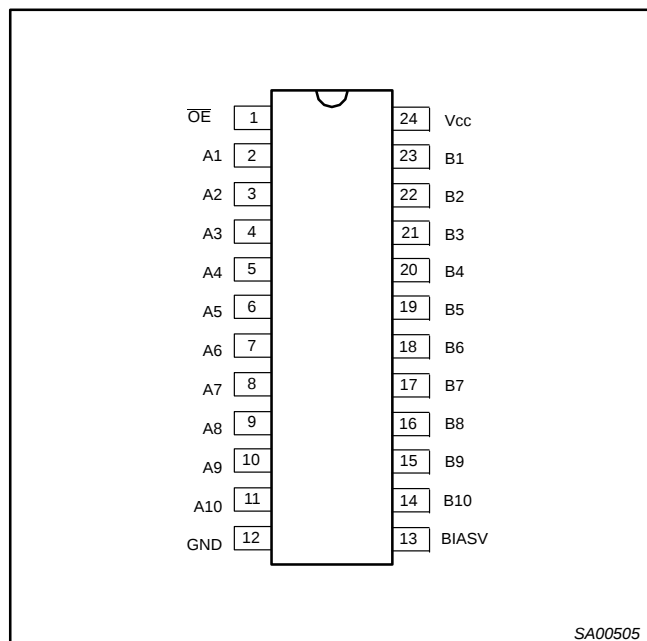
QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS $T_{\text{amb}} = 25^{\circ}\text{C}$; $\text{GND} = 0\text{ V}$	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay An to Bn or Bn to An	$C_L = 50\text{ pF}$; $V_{\text{CC}} = 5\text{ V}$	250	ps
C_{IN}	Input capacitance - control pin	$V_I = 0\text{ V}$ or V_{CC}	3.5	pF
C_{OUT}	Output capacitance - I/O pins	Outputs disabled; $V_O = 0\text{ V}$ or V_{CC}	8.2	pF
I_{CCZ}	Total supply current	Outputs disabled; $V_{\text{CC}} = 5.5\text{ V}$	1	μA

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	ORDER CODE	DWG NUMBER
24-Pin Plastic TSSOP	-40 to +85 $^{\circ}\text{C}$	CBT6800PW	SOT355-1

PIN CONFIGURATION



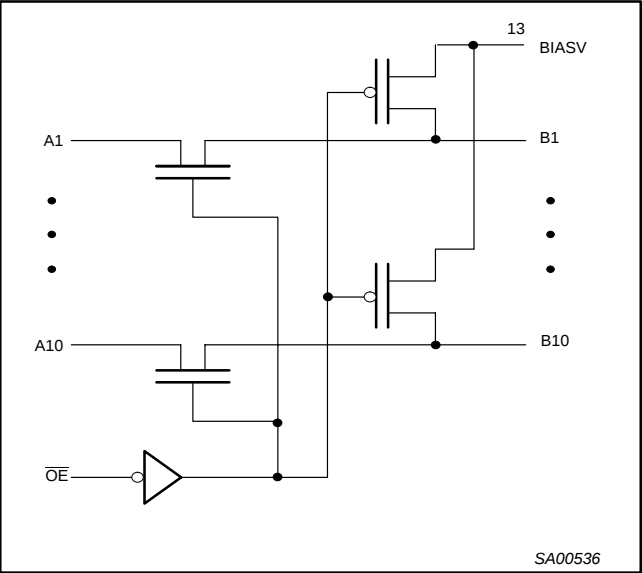
PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
1	$\overline{OE}$	Output enable
13	BIASV	Precharge bias voltage input
2, 3, 4, 5, 6, 7, 8, 9, 10, 11	A1-A10	A-port I/O pins
23, 22, 21, 20, 19, 18, 17, 16, 15, 14	B1-B10	B-port I/O pins - with active pullup
12	GND	Ground (V)
24	V_{CC}	Positive supply voltage

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LOGIC SYMBOL



FUNCTION TABLE

$\overline{OE}$	B1 - B10	FUNCTION
L	A1 - A10	Connect
H	BIASV	Precharge

H = HIGH voltage level
L = LOW voltage level
Z = HIGH impedance "off" state

ABSOLUTE MAXIMUM RATINGS^{1, 2}

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		-0.5 to +7.0	V
I_{IK}	DC input diode current		-50	mA
V_I	DC input voltage ³		-1.2 to +7.0	V
I_{SW}	DC clamp diode current	$V_O < 0$	-50	mA
T_{stg}	Storage temperature range		-65 to 150	°C
BiasV	DC voltage range		-0.5 to 6.0	V

NOTES:

- Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150 °C.
- The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS		UNIT
		Min	Max	
V_{CC}	DC supply voltage	4.5	5.5	V
BIASV	DC supply voltage	1.3	V_{CC}	V
V_{IH}	HIGH-level input voltage	2.0	—	V
V_{IL}	LOW-level Input voltage	—	0.8	V
T_{amb}	Operating free-air temperature range	-40	+85	°C

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DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			T _{amb} = -40 to +85 °C			
			Min	Typ ¹	Max	
V _{IK}	Input clamp voltage	V _{CC} = 4.5 V; I _I = -18 mA	—	—	-1.2	V
I _I	Input leakage current - $\overline{\text{OE}}$	V _{CC} = 5.5 V; V _I = GND or 5.5 V	—	—	±5	μA
I _O	Output bias current	V _{CC} = 4.5 V; BiasV = 2.4 V; V _O = 0	0.25	—	—	mA
I _{CC}	Quiescent supply current	V _{CC} = 5.5 V; I _O = 0, V _I = V _{CC} or GND	—	—	50	μA
ΔI _{CC}	Control pins ²	V _{CC} = 5.5 V, one input at 3.4 V, other inputs at V _{CC} or GND	—	—	2.5	mA
C _I	Control pins	V _I = 3 V or 0	—	3.5	—	pF
C _{O(OFF)}	Off-state capacitance - I/O pins	V _O = 3 V or 0; switch off	—	8.2	—	pF
r _{on} ³	On-resistance	V _{CC} = 4.5 V; V _I = 0 V; I _I = 64 mA	—	5	7	Ω
		V _{CC} = 4.5 V; V _I = 0 V; I _I = 30 mA	—	5	7	
		V _{CC} = 4.5 V; V _I = 2.4 V; I _I = 15 mA	—	10	15	
VP	Pass gate voltage	V _{IN} = V _{CC} = 5.0 V, I _{OUT} = -100 μA	3.4	3.6	3.9	V

NOTES:

1. All typical values are at $V_{\text{CC}} = 5 \text{ V}$, $T_{\text{amb}} = 25 \text{ }^{\circ}\text{C}$
2. This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND
3. Measured by the voltage drop between the A and the B terminals at the indicated current through the switch. On-state resistance is determined by the lowest voltage of the two (A or B) terminals.

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AC CHARACTERISTICS

GND = 0 V; $C_L = 50\text{ pF}$; $t_r = t_f \leq 2.5\text{ ns}$

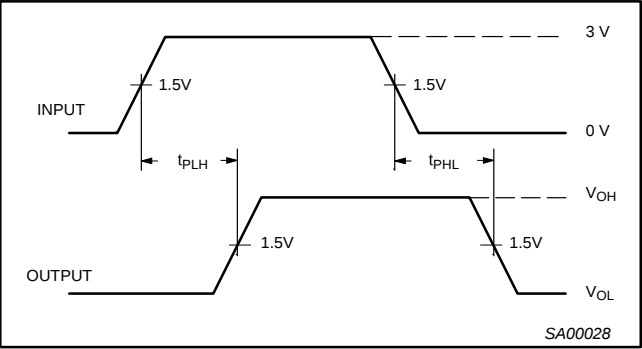
SYMBOL	PARAMETER	FROM (INPUT)	TO (OUTPUT)	LIMITS		UNIT
				V _{CC} = +5.0 V ±0.5 V		
				Min	Max	
t _{pd}	Propagation delay ¹	A or B	B or A	—	.25	ns
t _{pZH} T _{pZL}	BIASV = GND BIASV = 3 V	ON	A or B	2.4 3.0	7.7 8.3	ns
t _{pHZ} T _{PLZ}	BIASV = GND BIASV = 3 V	ON	A or B	1.0 3.1	5.3 7.8	ns

NOTE:

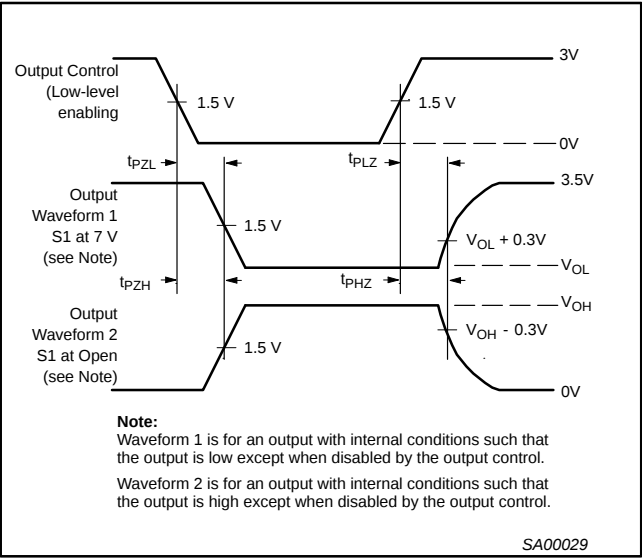
1. This parameter is warranted but not production tested. The propagation delay is based on the RC time constant of the typical on-state resistance of the switch and a load capacitance of 50 pF, when driven by an ideal voltage source (zero output impedance).

AC WAVEFORMS

$V_M = 1.5\text{ V}$, $V_{IN} = \text{GND to } 3.0\text{ V}$



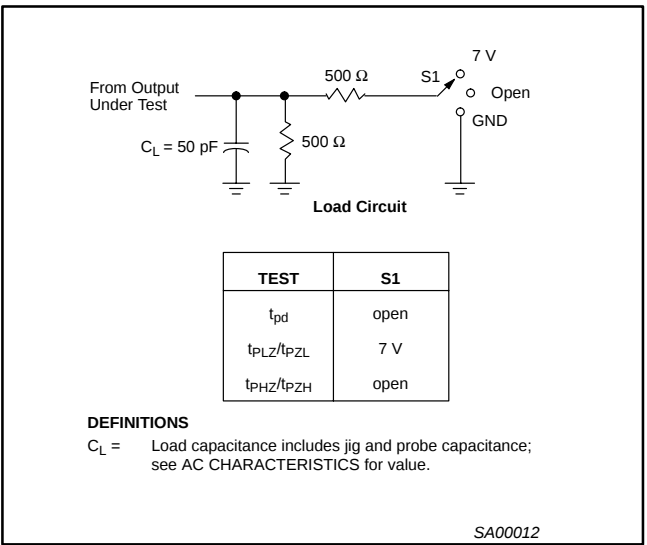
Waveform 1. Waveforms Showing the Input (An) to Output (Yn) Propagation Delays



Note:
Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.
Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

Waveform 2. Waveforms Showing the 3-State Output Enable and Disable Times

TEST CIRCUIT AND WAVEFORMS



NOTES:

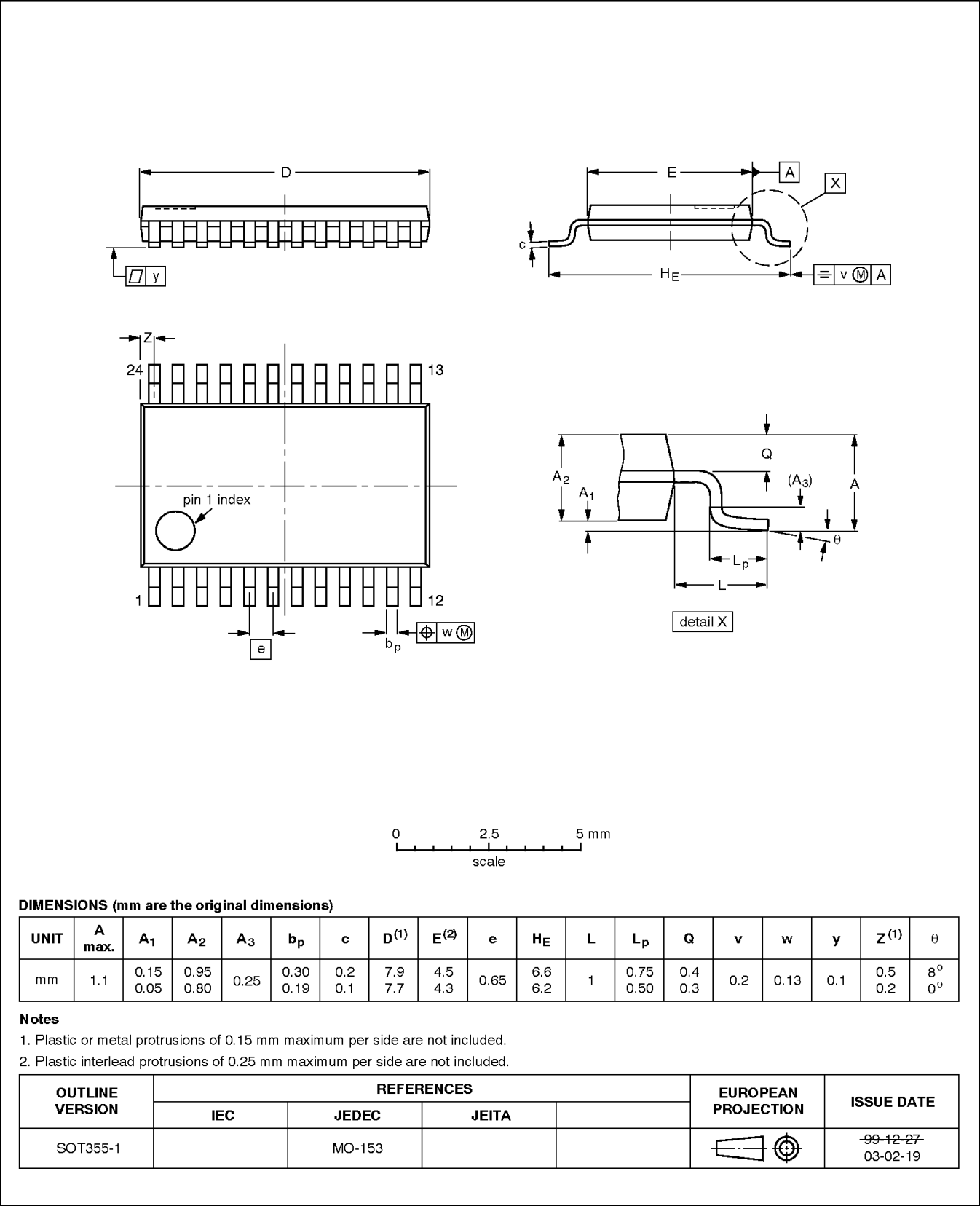
1. All input pulses are supplied by generators having the following characteristics: $\text{PRR} \leq 10\text{ MHz}$, $Z_O = 50\text{ }\Omega$, $t_r \leq 2.5\text{ ns}$, $t_f \leq 2.5\text{ ns}$.
2. The outputs are measured one at a time with one transition per measurement.

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TSSOP24: plastic thin shrink small outline package; 24 leads; body width 4.4 mm

SOT355-1



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CBT6800**REVISION HISTORY**

Rev	Date	Description
_2	20030912	Product data (9397 750 12059); ECN 853-2182 30126 dated 18 July 2003. Supersedes data of 28 October 1999 (9397 750 06552). Modifications: • Corrections to block diagram drawing
_1	19991028	Product data (9397 750 06552); ECN: 853-2182 22598 of 28 October 1999

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Data sheet status

Level	Data sheet status ^[1]	Product status ^{[2] [3]}	Definitions
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
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[3] For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

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Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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Contact information

For additional information please visit

<http://www.semiconductors.philips.com>. Fax: +31 40 27 24825

For sales offices addresses send e-mail to:

sales.addresses@www.semiconductors.philips.com.

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