

SN54ABT543A, SN74ABT543A OCTAL REGISTERED TRANSCEIVERS WITH 3-STATE OUTPUTS

SCBS157F – JANUARY 1991 – REVISED MAY 1997

- State-of-the-Art *EPIC-II*[™] BiCMOS Design Significantly Reduces Power Dissipation
- ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Typical V_{OLP} (Output Ground Bounce) < 1 V at $V_{CC} = 5$ V, $T_A = 25^\circ\text{C}$
- High-Drive Outputs (–32-mA I_{OH} , 64-mA I_{OL})
- Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) Packages, Ceramic Chip Carriers (FK), Ceramic Flat (W) Package, and Plastic (NT) and Ceramic (JT) DIPs

description

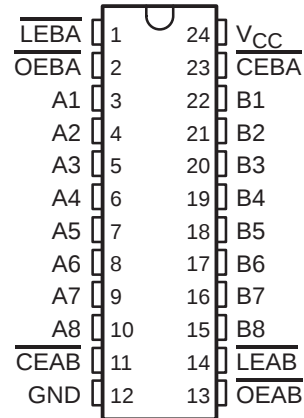
The 'ABT543A octal transceivers contain two sets of D-type latches for temporary storage of data flowing in either direction. Separate latch-enable ($\overline{\text{LEAB}}$ or $\overline{\text{LEBA}}$) and output-enable ($\overline{\text{OEAB}}$ or $\overline{\text{OEBA}}$) inputs are provided for each register to permit independent control in either direction of data flow.

The A-to-B enable ($\overline{\text{CEAB}}$) input must be low to enter data from A or to output data from B. If $\overline{\text{CEAB}}$ is low and $\overline{\text{LEAB}}$ is low, the A-to-B latches are transparent; a subsequent low-to-high transition of $\overline{\text{LEAB}}$ puts the A latches in the storage mode. With $\overline{\text{CEAB}}$ and $\overline{\text{OEAB}}$ both low, the 3-state B outputs are active and reflect the data present at the output of the A latches. Data flow from B to A is similar, but requires using the $\overline{\text{CEBA}}$, $\overline{\text{LEBA}}$, and $\overline{\text{OEBA}}$ inputs.

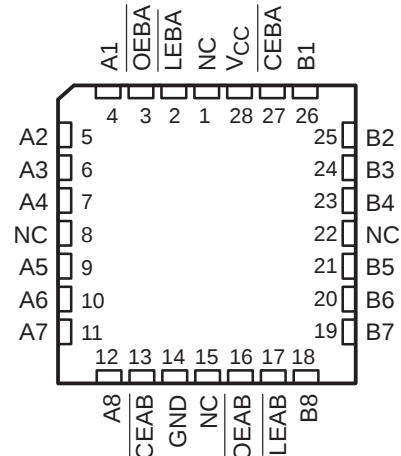
To ensure the high-impedance state during power up or power down, $\overline{\text{OE}}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN54ABT543A is characterized for operation over the full military temperature range of -55°C to 125°C . The SN74ABT543A is characterized for operation from -40°C to 85°C .

SN54ABT543A . . . JT OR W PACKAGE
SN74ABT543A . . . DB, DW, NT, OR PW PACKAGE
(TOP VIEW)



SN54ABT543A . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection



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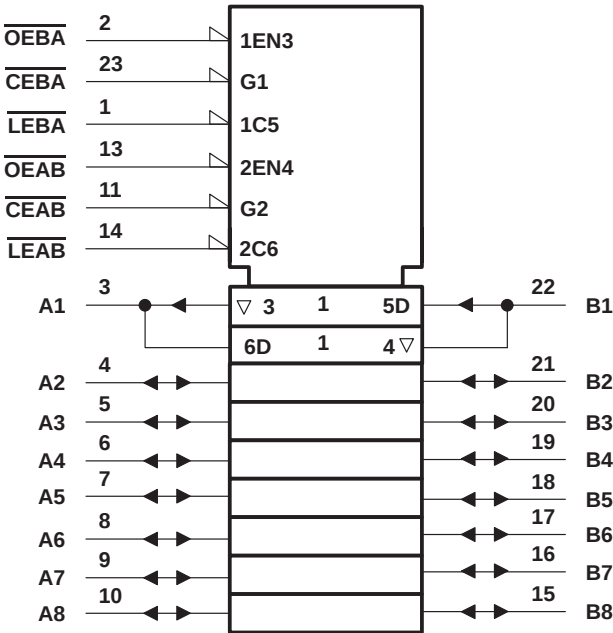
SN54ABT543A, SN74ABT543A
OCTAL REGISTERED TRANSCEIVERS
WITH 3-STATE OUTPUTS

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FUNCTION TABLE†				
INPUTS				OUTPUT B
CEAB	LEAB	OEAB	A	
H	X	X	X	Z
X	X	H	X	Z
L	H	L	X	B ₀ ‡
L	L	L	L	L
L	L	L	H	H

† A-to-B data flow is shown; B-to-A flow control is the same except that it uses CEBA, LEBA, and OEBA.
‡ Output level before the indicated steady-state input conditions were established

logic symbols§



§ This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the DB, DW, JT, NT, PW, and W packages.

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The diagram illustrates the internal logic of the B1 channel. It features four 3-input AND gates at the top, each with one active-low input (OEBA, CEBA, LEBA, OEAB) and two active-low inputs (13, 11, 14). The outputs of these AND gates are connected to a network of inverters, buffers (C1, 1D), and multiplexers. The final output is B1 (22). A bracket at the bottom indicates that similar logic exists for the other six channels.

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SN54ABT543A, SN74ABT543A

OCTAL REGISTERED TRANSCEIVERS

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recommended operating conditions (see Note 3)

			SN54ABT543A		SN74ABT543A		UNIT
			MIN	MAX	MIN	MAX	
V _{CC}	Supply voltage		4.5	5.5	4.5	5.5	V
V _{IH}	High-level input voltage		2		2		V
V _{IL}	Low-level input voltage			0.8		0.8	V
V _I	Input voltage		0	V _{CC}	0	V _{CC}	V
I _{OH}	High-level output current			–24		–32	mA
I _{OL}	Low-level output current			48		64	mA
Δt/Δv	Input transition rise or fall rate	Outputs enabled		5		5	ns/V
T _A	Operating free-air temperature		–55	125	–40	85	°C

NOTE 3: Unused pins (input or I/O) must be held high or low to prevent them from floating.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T _A = 25°C			SN54ABT543A		SN74ABT543A		UNIT
			MIN	TYP [†]	MAX	MIN	MAX	MIN	MAX	
V _{IK}		V _{CC} = 4.5 V, I _I = –18 mA			–1.2		–1.2		–1.2	V
V _{OH}		V _{CC} = 4.5 V, I _{OH} = –3 mA	2.5			2.5		2.5		V
		V _{CC} = 5 V, I _{OH} = –3 mA	3			3		3		
		V _{CC} = 4.5 V, I _{OH} = –24 mA	2			2				
		V _{CC} = 4.5 V, I _{OH} = –32 mA	2*					2		
V _{OL}		V _{CC} = 4.5 V, I _{OL} = 48 mA			0.55		0.55			V
		V _{CC} = 4.5 V, I _{OL} = 64 mA			0.55*				0.55	
V _{hys}				100						mV
I _I	Control inputs	V _{CC} = 5.5 V, V _I = V _{CC} or GND			±1		±1		±1	μA
	A or B ports				±100		±100		±100	
I _{OZH} [‡]		V _{CC} = 5.5 V, V _O = 2.7 V			10 [§]		10 [§]		10 [§]	μA
I _{OZL} [‡]		V _{CC} = 5.5 V, V _O = 0.5 V			–10 [§]		–10 [§]		–10 [§]	μA
I _{off}		V _{CC} = 0, V _I or V _O ≤ 4.5 V			±100				±100	μA
I _{CEX}		V _{CC} = 5.5 V, V _O = 5.5 V, Outputs high			50		50		50	μA
I _O [¶]		V _{CC} = 5.5 V, V _O = 2.5 V	–50*	–100	–180*	–50	–200	–50	–180	mA
I _{CC}	A or B ports	V _{CC} = 5.5 V, I _O = 0, V _I = V _{CC} or GND, Outputs high		1	250*		350		250	μA
		V _{CC} = 5.5 V, I _O = 0, V _I = V _{CC} or GND, Outputs low		24	30*		34		30	mA
		V _{CC} = 5.5 V, I _O = 0, V _I = V _{CC} or GND, Outputs disabled		0.5	250*		350		250	μA
ΔI _{CC} [#]		V _{CC} = 5.5 V, One input at 3.4 V, Other inputs at V _{CC} or GND			1.5		1.5		1.5	mA
C _i	Control inputs	V _I = 2.5 V or 0.5 V			4					pF
C _{io}	A or B ports	V _O = 2.5 V or 0.5 V			7					pF

* On products compliant to MIL-PRF-38535, this parameter does not apply.

† All typical values are at V_{CC} = 5 V.

‡ The parameters I_{OZH} and I_{OZL} include the input leakage current.

§ This data sheet limit may vary among suppliers.

¶ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.



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timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)

				SN54ABT543A		UNIT		
				$V_{CC} = 5\text{ V}$, $T_A = 25^{\circ}\text{C}$			MIN	MAX
				MIN	MAX			
t_W	Pulse duration, $\overline{LEAB}$ or $\overline{LEBA}$ low			3.5	3.5	ns		
t_{su}	Setup time	Data before $\overline{LEAB}$ or $\overline{LEBA}\uparrow$	High	2.5	2.5	ns		
			Low	3	3			
		Data before $\overline{CEAB}$ or $\overline{CEBA}\uparrow$	High	2.5	2.5			
			Low	3	3			
t_h	Hold time	Data after $\overline{LEAB}$ or $\overline{LEBA}\uparrow$	1	1	ns			
		Data after $\overline{CEAB}$ or $\overline{CEBA}\uparrow$	1	1				

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)

				SN74ABT543A		UNIT		
				$V_{CC} = 5\text{ V}$, $T_A = 25^{\circ}\text{C}$			MIN	MAX
				MIN	MAX			
t_W	Pulse duration, $\overline{LEAB}$ or $\overline{LEBA}$ low			3.5	3.5	ns		
t_{su}	Setup time	Data before $\overline{LEAB}$ or $\overline{LEBA}\uparrow$	High	3.5	3.5	ns		
			Low	3	3			
		Data before $\overline{CEAB}$ or $\overline{CEBA}\uparrow$	High	3.5	3.5			
			Low	3	3			
t_h	Hold time	Data after $\overline{LEAB}$ or $\overline{LEBA}\uparrow$	0.5	0.5	ns			
		Data after $\overline{CEAB}$ or $\overline{CEBA}\uparrow$	0.5	0.5				

SN54ABT543A, SN74ABT543A

OCTAL REGISTERED TRANSCEIVERS

WITH 3-STATE OUTPUTS

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switching characteristics over recommended ranges of supply voltage and operating free-air temperature, $C_L = 50$ pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54ABT543A					UNIT
			V _{CC} = 5 V, T _A = 25°C			MIN	MAX	
			MIN	TYP	MAX			
t _{PLH}	A or B	B or A	1.6 [†]	4.4	4.4	1.6 [†]	5.5	ns
t _{PHL}			1.6	4.4	5.1	1.6	6.2	
t _{PLH}	$\overline{LEBA}$ or $\overline{LEAB}$	A or B	1.6 [†]	4.1	5.1	1.6 [†]	6.6	ns
t _{PHL}			1.6	4.6	5.4	1.6	6.4	
t _{PZH}	$\overline{OEBA}$ or $\overline{OEAB}$	A or B	1.4	3.9	4.1	1.4	5.1	ns
t _{PZL}			2	5	4.9	2	5.8	
t _{PHZ}	$\overline{OEBA}$ or $\overline{OEAB}$	A or B	2.5 [†]	5.9	5.8	2.5 [†]	6.9	ns
t _{PLZ}			2.5 [†]	5.5	6.1	2.5 [†]	7.6	
t _{PZH}	$\overline{CEBA}$ or $\overline{CEAB}$	A or B	1.4	3.9	4.7	1.4	5.6	ns
t _{PZL}			2	5	5.7	2	6.2	
t _{PHZ}	CEBA or CEAB	A or B	3.2 [†]	5.9	6.5	3.2 [†]	7.3	ns
t _{PLZ}			2.5 [†]	5.5	6.7	2.5 [†]	7.8	

[†] This data sheet limit may vary among suppliers.

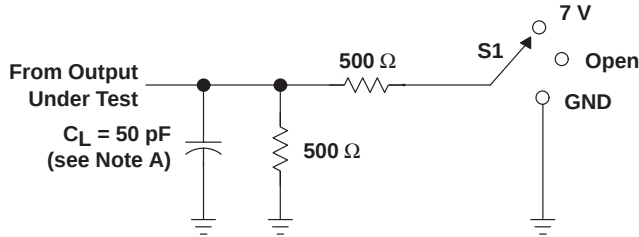
switching characteristics over recommended ranges of supply voltage and operating free-air temperature, $C_L = 50$ pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN74ABT543A					UNIT
			V _{CC} = 5 V, T _A = 25°C			MIN	MAX	
			MIN	TYP	MAX			
t _{PLH}	A or B	B or A	1.8 [†]	4.4	5.9	1.8 [†]	6.9	ns
t _{PHL}			1.9	4.4	5.9	1.9	6.9	
t _{PLH}	$\overline{LEBA}$ or $\overline{LEAB}$	A or B	1.5 [†]	4.1	5.6	1.5 [†]	6.6	ns
t _{PHL}			2.1	4.6	6.1	2.1	7.1	
t _{PZH}	$\overline{OEBA}$ or $\overline{OEAB}$	A or B	1.4	3.9	5.4	1.4	6.4	ns
t _{PZL}			2.5	5	6.5	2.5	7.5	
t _{PHZ}	$\overline{OEBA}$ or $\overline{OEAB}$	A or B	2.5 [†]	5.9	7.4	2.5 [†]	8.4	ns
t _{PLZ}			2.5 [†]	5.5	7	2.5 [†]	8	
t _{PZH}	$\overline{CEBA}$ or $\overline{CEAB}$	A or B	1.4	3.9	5.4	1.4	6.4	ns
t _{PZL}			2.5	5	6.5	2.5	7.5	
t _{PHZ}	$\overline{CEBA}$ or $\overline{CEAB}$	A or B	2.9 [†]	5.9	7.4	2.9 [†]	8.4	ns
t _{PLZ}			2.4 [†]	5.5	7	2.4 [†]	8	

[†] This data sheet limit may vary among suppliers.

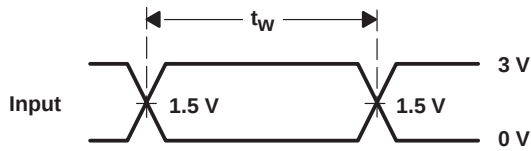


PARAMETER MEASUREMENT INFORMATION

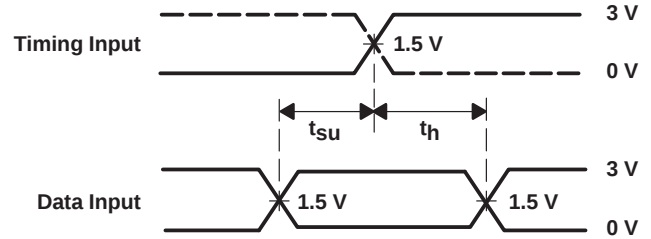


LOAD CIRCUIT

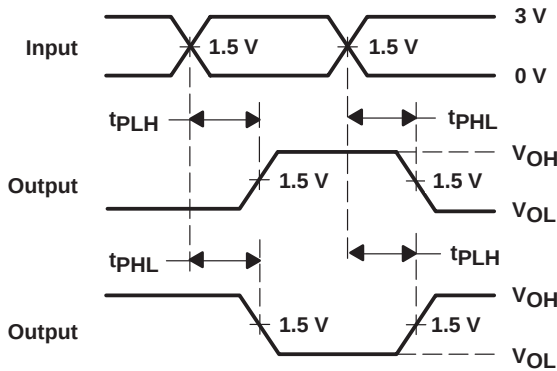
TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	Open



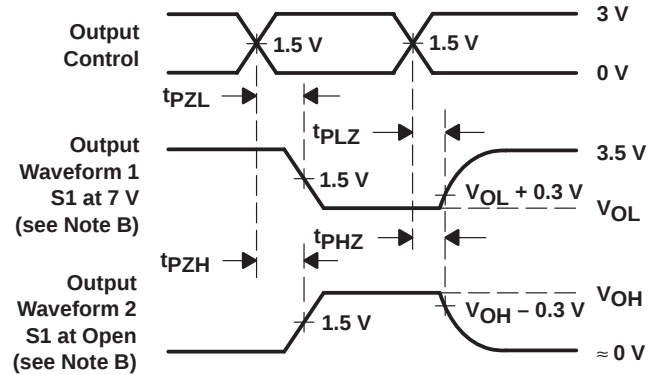
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

- NOTES: A. C_L includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2.5 \text{ ns}$, $t_f \leq 2.5 \text{ ns}$.
- D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

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PRODUCT SUPPORT: [TRAINING](#)

SN54ABT543A, Octal Registered Transceiver With 3-State Outputs
DEVICE STATUS: ACTIVE

PARAMETER NAME	SN54ABT543A	SN74ABT543A
Voltage Nodes (V)	5	5
Vcc range (V)	4.5 to 5.5	4.5 to 5.5
Input Level	TTL	TTL
Output Level	TTL	TTL
Output Drive (mA)		-32/64
No. of Outputs	8	8
Logic	True	True
Static Current		15.12
th (ns)		0.5
tpd max (ns)		6.2
tsu (ns)		3.5

FEATURES

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- State-of-the-Art **EPIC-II B™** BiCMOS Design Significantly Reduces Power Dissipation
- ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
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EPIC-IIB is a trademark of Texas Instruments Incorporated.

DESCRIPTION

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TECHNICAL DOCUMENTS

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Product Folder: SN54ABT543A, Octal Registered Transceiver With 3-State Outputs

To download a document to your hard drive, right-click on the link and choose 'Save'.

DATASHEET

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Full datasheet in Acrobat PDF: [sn54abt543a.pdf](#) (127 KB,Rev.F) (Updated: 05/01/1997)

APPLICATION NOTES

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View Application Notes for [Digital Logic](#)

- [Advanced BiCMOS Technology \(ABT\) Logic Characterization Information \(Rev. B\)](#) (SCBA008B - Updated: 06/01/1997)
- [Advanced BiCMOS Technology \(ABT\) Logic Enables Optimal System Design \(Rev. A\)](#) (SCBA001A - Updated: 03/01/1997)
- [Bus-Interface Devices With Output-Damping Resistors Or Reduced-Drive Outputs \(Rev. A\)](#) (SCBA012A - Updated: 08/01/1997)
- [Designing With Logic \(Rev. C\)](#) (SDYA009C - Updated: 06/01/1997)
- [Evaluation of Nickel/Palladium/Gold-Finished Surface-Mount Integrated Circuits](#) (SZZA026 - Updated: 06/20/2001)
- [Family of Curves Demonstrating Output Skews for Advanced BiCMOS Devices \(Rev. A\)](#) (SCBA006A - Updated: 12/01/1996)
- [Implications of Slow or Floating CMOS Inputs \(Rev. C\)](#) (SCBA004C - Updated: 02/01/1998)
- [Input and Output Characteristics of Digital Integrated Circuits](#) (SDYA010 - Updated: 10/01/1996)
- [Live Insertion](#) (SDYA012 - Updated: 10/01/1996)
- [Power-Up 3-State \(PU3S\) Circuits in TI Standard Logic Devices](#) (SZZA033 - Updated: 05/10/2002)
- [Quad Flatpack No-Lead Logic Packages \(Rev. C\)](#) (SCBA017C - Updated: 11/22/2002)
- [TI IBIS File Creation, Validation, and Distribution Processes](#) (SZZA034 - Updated: 08/29/2002)
- [Understanding Advanced Bus-Interface Products Design Guide](#) (SCAA029, 253 KB - Updated: 05/01/1996)
- [Understanding and Interpreting Texas Instruments Standard-Logic Products Data Sh \(Rev. A\)](#) (SZZA036A - Updated: 02/27/2003)

MORE LITERATURE

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- [Enhanced Plastic Portfolio Brochure](#) (SGZB004, 387 KB - Updated: 08/19/2002)
- [Logic Reference Guide](#) (SCYB004, 1032 KB - Updated: 10/23/2001)
- [MicroStar Junior BGA Design Summary](#) (SCET004, 167 KB - Updated: 07/28/2000)
- [Military Brief](#) (SGYN138, 803 KB - Updated: 10/10/2000)
- [Overview of IEEE Std 91-1984, Explanation of Logic Symbols Training Booklet \(Rev. A\)](#) (SDYZ001A, 138 KB - Updated: 07/01/1996)
- [Palladium Lead Finish User's Manual](#) (SDYV001, 2041 KB - Updated: 11/01/1996)
- [QML Class V Space Products Military Brief \(Rev. A\)](#) (SGZN001A, 257 KB - Updated: 10/07/2002)

USER GUIDES

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- [LOGIC Pocket Data Book](#) (SCYD013, 4837 KB - Updated: 12/05/2002)

PRICING/AVAILABILITY/PKG

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DEVICE INFORMATION Updated Daily								TI INVENTORY STATUS As Of 09:00 AM GMT, 17 Apr 2003			REPORTED DISTRIBUTOR INVENTORY As Of 09:00 AM GMT, 17 Apr 2003			
ORDERABLE DEVICE	STATUS	PACKAGE TYPE PINS		TEMP (*C)	DSCC. NUMBER	PRODUCT CONTENT	BUDGETARY PRICING QTY \$US	STD PACK QTY	IN STOCK	IN PROGRESS QTY DATE	LEAD TIME	DISTRIBUTOR COMPANY REGION	IN STOCK	PURCHASE
5962-9231402Q3A	ACTIVE	LCCC (FK)	28	-55 TO 125		View Contents	1KU 8.08	1	27*	3556 20 May	8 WKS	Avnet Americas	2	BUY NOW
										>10k 27 May				
5962-9231402QKA	ACTIVE	CFP (W)	24	-55 TO 125		View Contents	1KU 8.58	1	15*	>10k 20 May	8 WKS	None Reported View Distributors		
5962-9231402QLA	ACTIVE	CDIP (JT)	24	-55 TO 125		View Contents	1KU 4.86	1	89*	>10k 20 May	8 WKS	Avnet Americas	35	BUY NOW
SNJ54ABT543AFK	ACTIVE	LCCC (FK)	28	-55 TO 125	5962-9231402Q3A	View Contents	1KU 8.08	1	113*	387 12 May	8 WKS	None Reported View Distributors		

									3801 20 May					
									>10k 27 May					
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