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The circuit diagram shows an instrumentation amplifier configuration using two LMC6044 operational amplifiers. The input signal V_{IN} is applied across a 10k potentiometer (R2). The wiper of R2 is connected to the non-inverting input (+) of the top LMC6044. The other end of R2 is connected to the inverting input (-) of the bottom LMC6044. Both inputs are also connected to resistors R1 (44.2k) and R5 (44.2k), which are tied together at their other ends. The output of the top op-amp is connected to resistor R3 (10k), and the output of the bottom op-amp is connected to resistor R6 (10k). These two nodes are connected to a second LMC6044 configured as a voltage follower. Its non-inverting input (+) is connected to the junction of R3 and R6, while its inverting input (-) is connected to ground through a 91k resistor (R7) and a 20k potentiometer. The final output voltage V_{OUT} is taken from the output of this second op-amp.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Differential Input Voltage	±Supply Voltage
Supply Voltage ($V^+ - V^-$)	16V
Output Short Circuit to V^+	(Note 12)
Output Short Circuit to V^-	(Note 2)
Lead Temperature (Soldering, 10 sec.)	260°C
Current at Input Pin	±5 mA
Current at Output Pin	±18 mA
Current at Power Supply Pin	35 mA
Power Dissipation	(Note 3)
Storage Temperature Range	–65°C to +150°C

Junction Temperature (Note 3)	110°C
ESD Tolerance (Note 4)	500V
Voltage at I/O Pin (V^+)	+0.3V, (V^-) –0.3V

Operating Ratings

Temperature Range	LMC6044AI, LMC6044I	–40°C ≤ T_J ≤ +85°C
Supply Voltage		4.5V ≤ V^+ ≤ 15.5V
Power Dissipation		(Note 10)
Thermal Resistance (θ_{JA}), (Note 11)		
14-Pin DIP		85°C/W
14-Pin SO		115°C/W

Electrical Characteristics

Unless otherwise specified, all limits guaranteed for $T_A = T_J = 25^\circ\text{C}$. **Boldface** limits apply at the temperature extremes. $V^+ = 5\text{V}$, $V^- = 0\text{V}$, $V_{CM} = 1.5\text{V}$, $V_O = V^+/2$, and $R_L > 1\text{M}$ unless otherwise specified.

Symbol	Parameter	Conditions	Typical (Note 5)	LMC6044AI	LMC6044I	Units (Limit)
				Limit (Note 6)	Limit (Note 6)	
V_{OS}	Input Offset Voltage		1	3 3.3	6 6.3	mV max
TCV_{OS}	Input Offset Voltage Average Drift		1.3			$\mu\text{V}/^\circ\text{C}$
I_B	Input Bias Current		0.002	4	4	pA max
I_{OS}	Input Offset Current		0.001	2	2	pA max
R_{IN}	Input Resistance		>10			Tera Ω
CMRR	Common Mode Rejection Ratio	$0\text{V} \leq V_{CM} \leq 12.0\text{V}$ $V^+ = 15\text{V}$	75	68 66	62 60	dB min
+PSRR	Positive Power Supply Rejection Ratio	$5\text{V} \leq V^+ \leq 15\text{V}$ $V_O = 2.5\text{V}$	75	68 66	62 60	dB min
–PSRR	Negative Power Supply Rejection Ratio	$0\text{V} \leq V^- \leq -10\text{V}$ $V_O = 2.5\text{V}$	94	84 83	74 73	dB min
CMR	Input Common-Mode Voltage Range	$V^+ = 5\text{V} \text{ \& } 15\text{V}$ For CMRR ≥ 50 dB	–0.4	–0.1 0	–0.1 0	V max
			$V^+ - 1.9\text{V}$	$V^+ - 2.3\text{V}$ $V^+ - 2.5\text{V}$	$V^+ - 2.3\text{V}$ $V^+ - 2.4\text{V}$	V min
A_V	Large Signal Voltage Gain	$R_L = 100\text{ k}\Omega$ (Note 7)	Sourcing	1000 300	300 200	V/mV min
			Sinking	500 120	90 70	V/mV min
		$R_L = 25\text{ k}\Omega$ (Note 7)	Sourcing	1000 160	100 80	V/mV min
			Sinking	250 60	50 40	V/mV min

Electrical Characteristics (Continued)

Unless otherwise specified, all limits guaranteed for $T_A = T_J = 25^\circ\text{C}$. **Boldface** limits apply at the temperature extremes. $V^+ = 5\text{V}$, $V^- = 0\text{V}$, $V_{CM} = 1.5\text{V}$, $V_O = V^+/2$, and $R_L > 1\text{M}$ unless otherwise specified.

Symbol	Parameter	Conditions	Typical (Note 5)	LMC6044AI	LMC6044I	Units (Limit)
				Limit (Note 6)	Limit (Note 6)	
V_O	Output Swing	$V^+ = 5\text{V}$ $R_L = 100\text{ k}\Omega$ to 2.5V	4.987	4.970 4.950	4.940 4.910	V min
			0.004	0.030 0.050	0.060 0.090	V max
		$V^+ = 5\text{V}$ $R_L = 25\text{ k}\Omega$ to 2.5V	4.980	4.920 4.870	4.870 4.820	V min
			0.010	0.080 0.130	0.130 0.180	V max
		$V^+ = 15\text{V}$ $R_L = 100\text{ k}\Omega$ to $V^+/2$	14.970	14.920 14.880	14.880 14.820	V min
			0.007	0.030 0.050	0.060 0.090	V max
		$V^+ = 15\text{V}$ $R_L = 25\text{ k}\Omega$ to $V^+/2$	14.950	14.900 14.850	14.850 14.800	V min
			0.022	0.100 0.150	0.150 0.200	V max
I_{SC}	Output Current $V^+ = 5\text{V}$	Sourcing, $V_O = 0\text{V}$	22	16 10	13 8	mA min
		Sinking, $V_O = 5\text{V}$	21	16 8	13 8	mA min
I_{SC}	Output Current $V^+ = 15\text{V}$	Sourcing, $V_O = 0\text{V}$	40	15 10	15 10	mA min
		Sinking, $V_O = 13\text{V}$ (Note 12)	39	24 8	21 8	mA min
I_S	Supply Current	Four Amplifiers $V_O = 1.5\text{V}$	40	65 72	75 82	μA max
		Four Amplifiers $V^+ = 15\text{V}$	52	85 94	98 107	μA max

AC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for $T_A = T_J = 25^\circ\text{C}$. **Boldface** limits apply at the temperature extremes. $V^+ = 5\text{V}$, $V^- = 0\text{V}$, $V_{CM} = 1.5\text{V}$, $V_O = V^+/2$, and $R_L > 1\text{M}$ unless otherwise specified.

Symbol	Parameter	Conditions	Typical (Note 5)	LMC6044AI	LMC6044I	Units (Limit)
				Limit (Note 6)	Limit (Note 6)	
SR	Slew Rate	(Note 8)	0.02	0.015 0.010	0.010 0.007	V/ μs min
GBW	Gain-Bandwidth Product		0.10			MHz
ϕ_m	Phase Margin		60			Deg
	Amp-to-Amp Isolation	(Note 9)	115			dB
e_n	Input-Referred Voltage Noise	$F = 1\text{ kHz}$	83			nV/ $\sqrt{\text{Hz}}$
i_n	Input-Referred Current Noise	$F = 1\text{ kHz}$	0.0002			pA/ $\sqrt{\text{Hz}}$

AC Electrical Characteristics (Continued)

Unless otherwise specified, all limits guaranteed for $T_A = T_J = 25^\circ\text{C}$. **Boldface** limits apply at the temperature extremes. $V^+ = 5\text{V}$, $V^- = 0\text{V}$, $V_{CM} = 1.5\text{V}$, $V_O = V^+/2$, and $R_L > 1\text{M}$ unless otherwise specified.

Symbol	Parameter	Conditions	Typical (Note 5)	LMC6044AI	LMC6044I	Units (Limit)
				Limit (Note 6)	Limit (Note 6)	
T.H.D.	Total Harmonic Distortion	$F = 1\text{ kHz}$, $A_V = -5$ $R_L = 100\text{ k}\Omega$, $V_O = 2\text{ V}_{pp}$ $\pm 5\text{V}$ Supply	0.01			%

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed.

Note 2: Applies to both single-supply and split-supply operation. Continuous short circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature of 110°C . Output currents in excess of $\pm 30\text{ mA}$ over long term may adversely affect reliability.

Note 3: The maximum power dissipation is a function of $T_{J(max)}$, θ_{JA} , and T_A . The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(max)} - T_A)/\theta_{JA}$.

Note 4: Human body model, $1.5\text{ k}\Omega$ in series with 100 pF .

Note 5: Typical Values represent the most likely parametric norm.

Note 6: All limits are guaranteed at room temperature (standard type face) or at operating temperature extremes (bold face type).

Note 7: $V^+ = 15\text{V}$, $V_{CM} = 7.5\text{V}$ and R_L connected to 7.5V . For Sourcing tests, $7.5\text{V} \leq V_O \leq 11.5\text{V}$. For Sinking tests, $2.5\text{V} \leq V_O \leq 7.5\text{V}$.

Note 8: $V^+ = 15\text{V}$. Connected as Voltage Follower with 10V step input. Number specified in the slower of the positive and negative slew rates.

Note 9: Input referred $V^+ = 15\text{V}$ and $R_L = 100\text{ k}\Omega$ connected to $V^+/2$. Each amp excited in turn with 100 Hz to produce $V_O = 12\text{ V}_{pp}$.

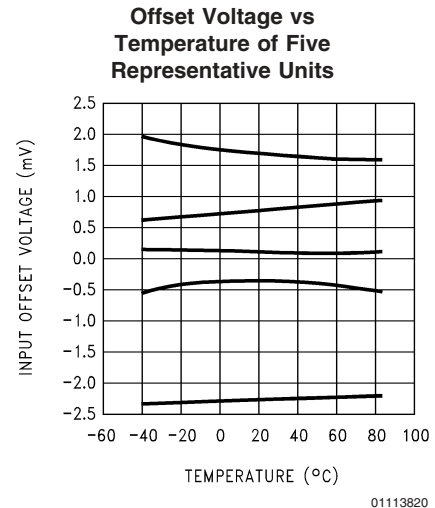
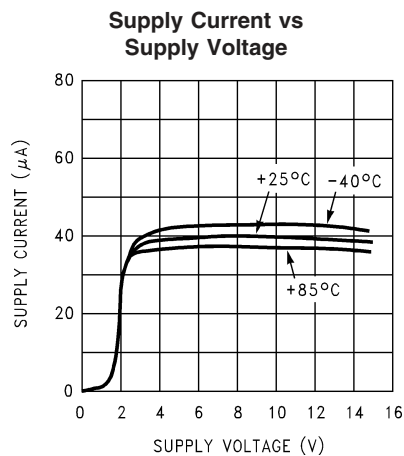
Note 10: For operating at elevated temperatures, the device must be derated based on the thermal resistance θ_{JA} with $P_D = (T_J - T_A)/\theta_{JA}$.

Note 11: All numbers apply for packages soldered directly into a PC board.

Note 12: Do not connect output to V^+ when V^+ is greater than 13V or reliability may be adversely affected.

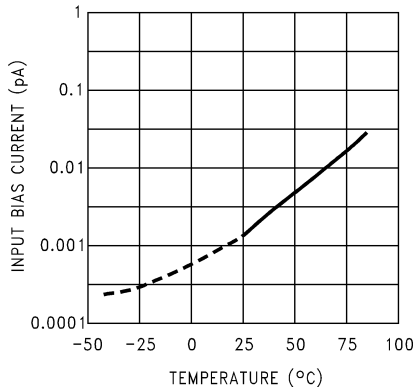
Typical Performance Characteristics

$V_S = \pm 7.5\text{V}$, $T_A = 25^\circ\text{C}$ unless otherwise specified



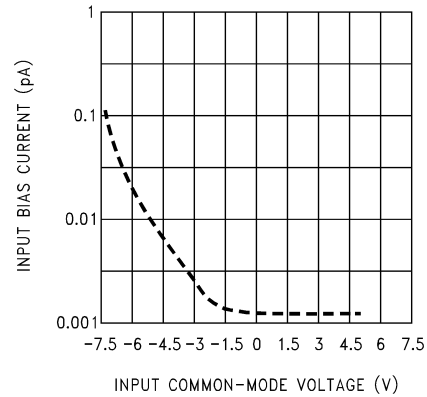
Typical Performance Characteristics $V_S = \pm 7.5V$, $T_A = 25^\circ C$ unless otherwise specified (Continued)

Input Bias Current vs Temperature



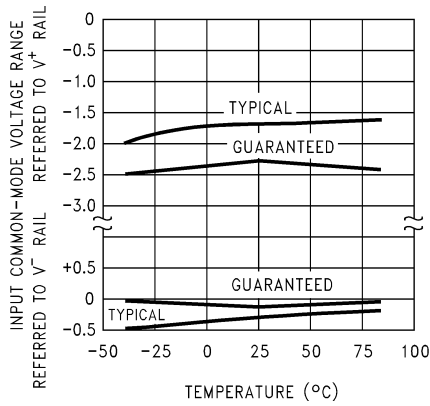
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Input Bias Current vs Input Common-Mode Voltage



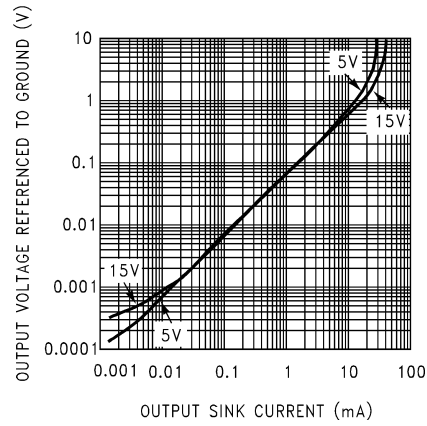
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Input Common-Mode Voltage Range vs Temperature



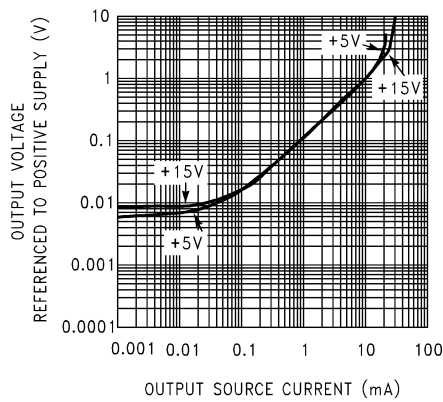
01113823

Output Characteristics Current Sinking



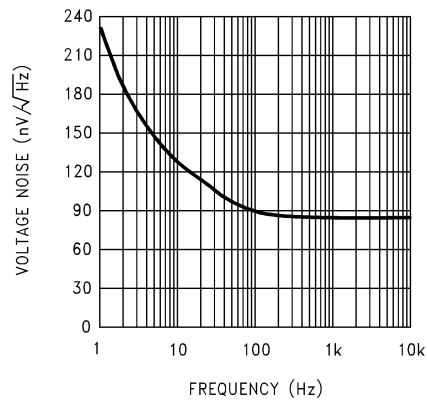
01113824

Output Characteristics Current Sourcing



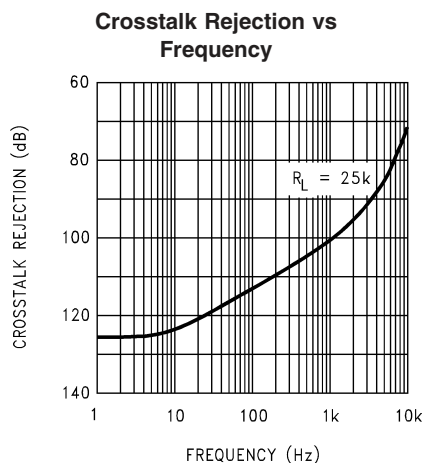
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Output Characteristics vs Frequency

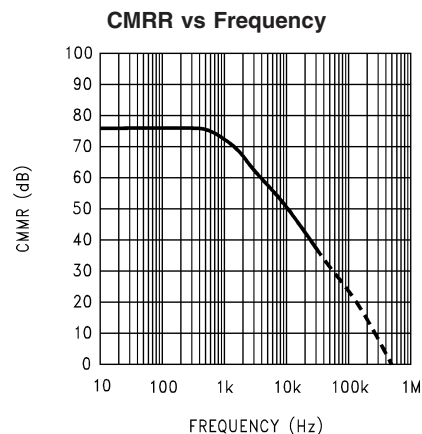


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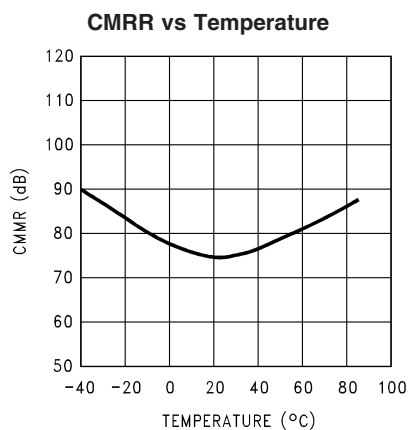
Typical Performance Characteristics $V_S = \pm 7.5V$, $T_A = 25^\circ C$ unless otherwise specified (Continued)



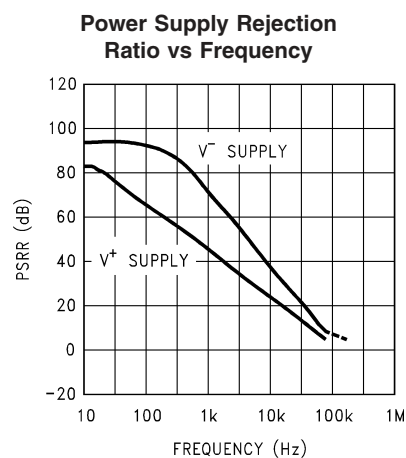
01113827



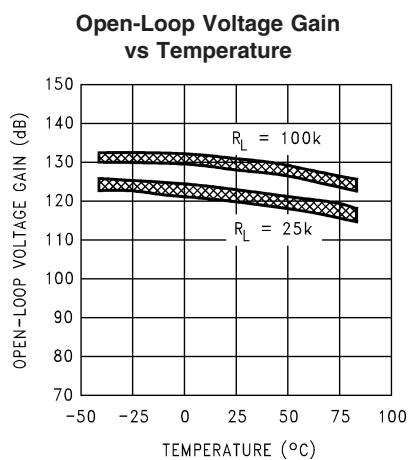
01113828



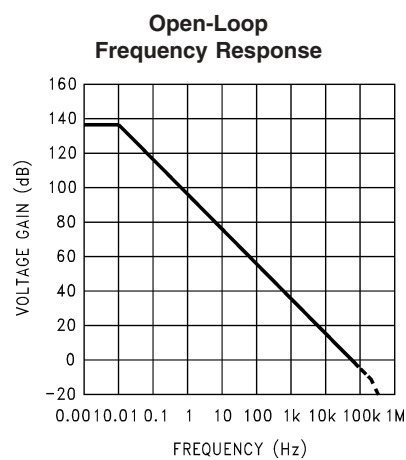
01113829



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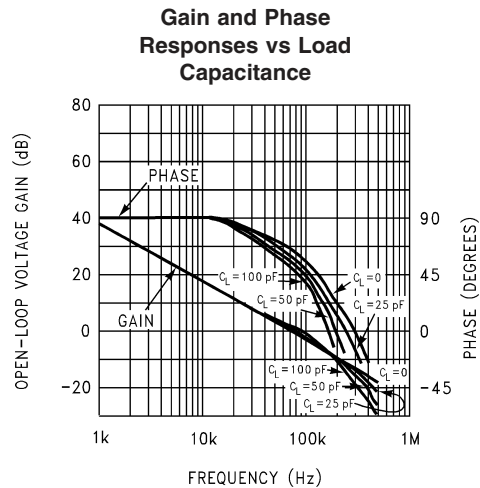


01113831

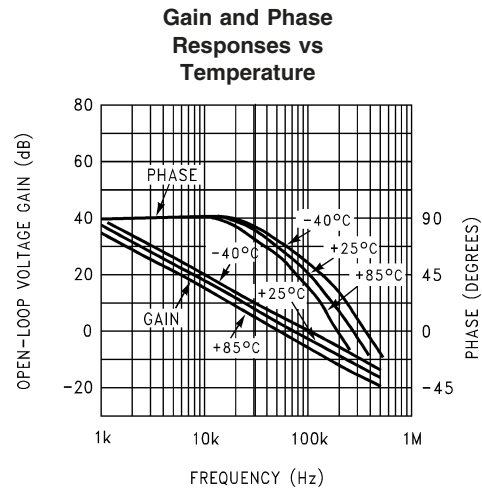


01113832

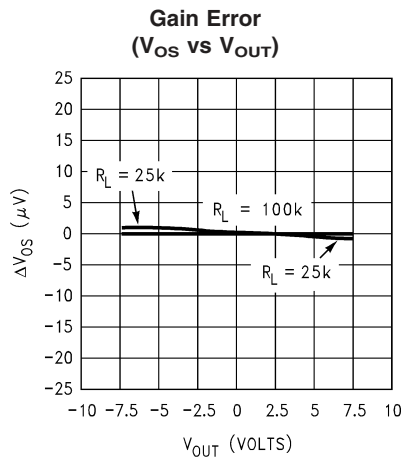
Typical Performance Characteristics $V_S = \pm 7.5V$, $T_A = 25^\circ C$ unless otherwise specified (Continued)



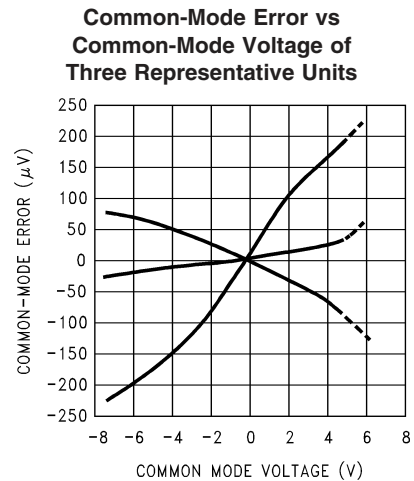
01113833



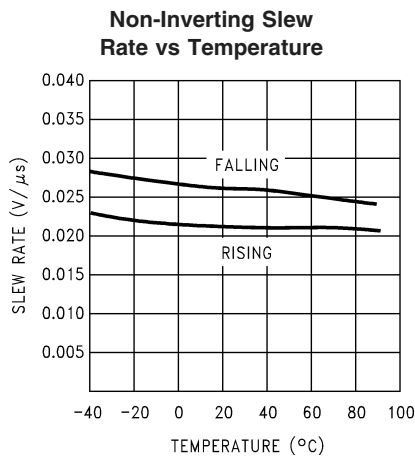
01113834



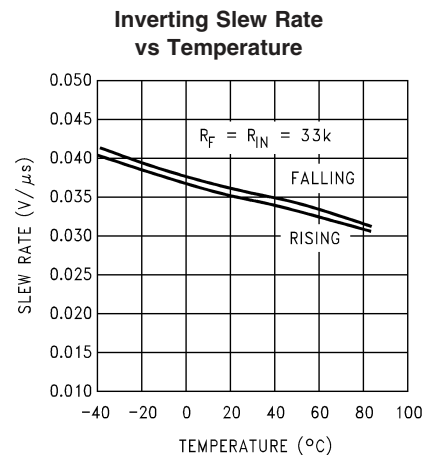
01113835



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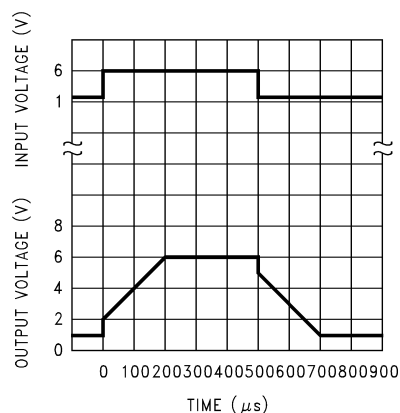
01113837



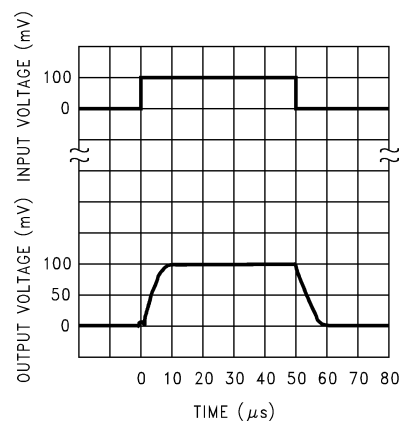
01113838

Typical Performance Characteristics $V_S = \pm 7.5V$, $T_A = 25^\circ C$ unless otherwise specified (Continued)

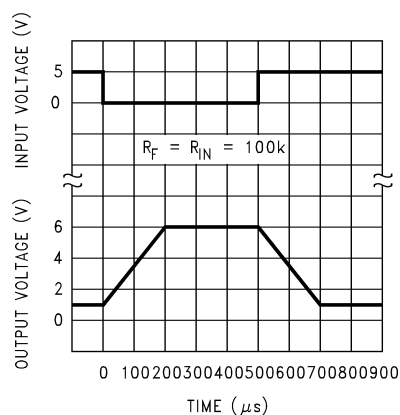
Non-Inverting Large Signal Pulse Response ($A_V = +1$)



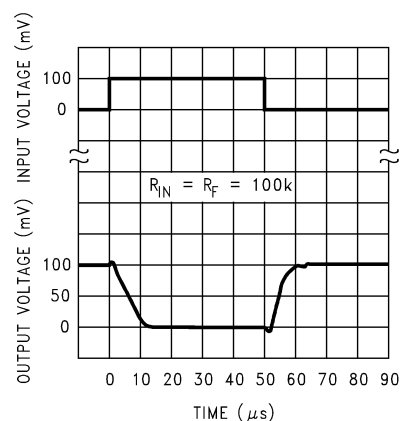
Non-Inverting Small Signal Pulse Response



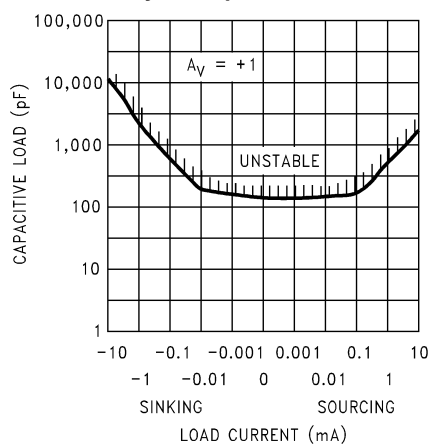
Inverting Large-Signal Pulse Response



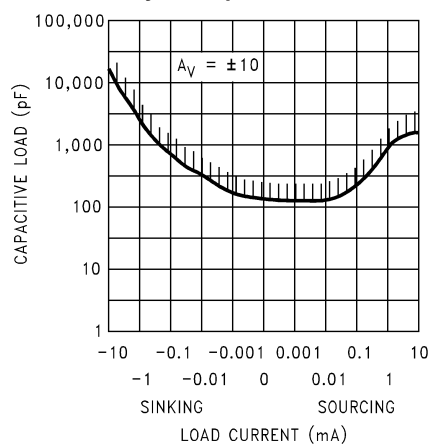
Inverting Small Signal Pulse Response



Stability vs Capacitive Load ($A_V = +1$)



Stability vs Capacitive Load ($A_V = \pm 10$)



Application Hints

AMPLIFIER TOPOLOGY

The LMC6044 incorporates a novel op-amp design topology that enables it to maintain rail to rail output swing even when driving a large load. Instead of relying on a push-pull unity gain output buffer stage, the output stage is taken directly from the internal integrator, which provides both low output impedance and large gain. Special feed-forward compensation design techniques are incorporated to maintain stability over a wider range of operating conditions than traditional micropower op-amps. These features make the LMC6044 both easier to design with, and provide higher speed than products typically found in this ultra-low power class.

COMPENSATING FOR INPUT CAPACITANCE

It is quite common to use large values of feedback resistance with amplifiers with ultra-low input current, like the LMC6044.

Although the LMC6044 is highly stable over a wide range of operating conditions, certain precautions must be met to achieve the desired pulse response when a large feedback resistor is used. Large feedback resistors and even small values of input capacitance, due to transducers, photodiodes, and circuits board parasitics, reduce phase margins. When high input impedance are demanded, guarding of the LMC6044 is suggested. Guarding input lines will not only reduce leakage, but lowers stray input capacitance as well. (See **Printed-Circuit-Board Layout for High Impedance Work.**)

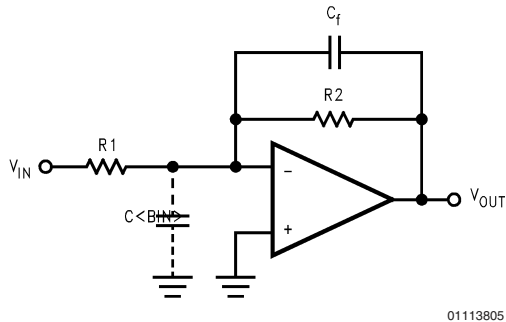


FIGURE 1. Canceling the Effect of Input Capacitance

The effect of input capacitance can be compensated for by adding a capacitor. Adding a capacitor, C_f , around the feedback resistor (as in Figure 1) such that:

$$\frac{1}{2\pi R_1 C_{IN}} \geq \frac{1}{2\pi R_2 C_f}$$

or

$$R_1 C_{IN} \leq R_2 C_f$$

Since it is often difficult to know the exact value of C_{IN} , C_f can be experimentally adjusted so that the desired pulse response is achieved. Refer to the LMC660 and the LMC662 for a more detailed discussion on compensating for input capacitance.

CAPACITIVE LOAD TOLERANCE

Direct capacitive loading will reduce the phase margin of many op-amps. A pole in the feedback loop is created by the combination of the op-amp's output impedance and the capacitive load. This pole induces phase lag at the unity-gain crossover frequency of the amplifier resulting in either an oscillatory or underdamped pulse response. With a few external components, op amps can easily indirectly drive capacitive loads, as shown in Figure 2.

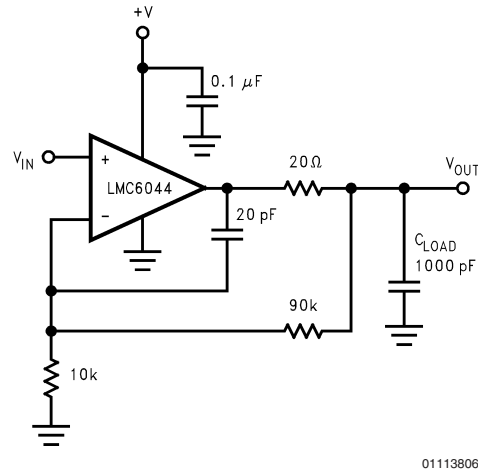


FIGURE 2. LMC6044 Noninverting Gain of 10 Amplifier, Compensated to Handle Capacitive Loads

In the circuit of Figure 2, R_1 and C_1 serve to counteract the loss of phase margin by feeding the high frequency component of the output signal back to the amplifier's inverting input, thereby preserving phase margin in the overall feedback loop.

Capacitive load driving capability is enhanced by using a pull up resistor to V^+ (Figure 3). Typically, a pull up resistor conducting 10 μA or more will significantly improve capacitive load responses. The value of the pull up resistor must be determined based on the current sinking capability of the amplifier with respect to the desired output swing. Open loop gain of the amplifier can also be affected by the pull up resistor (see Electrical Characteristics).

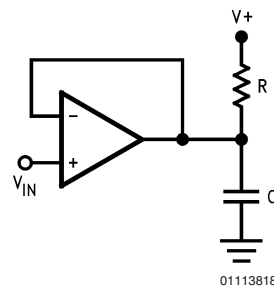


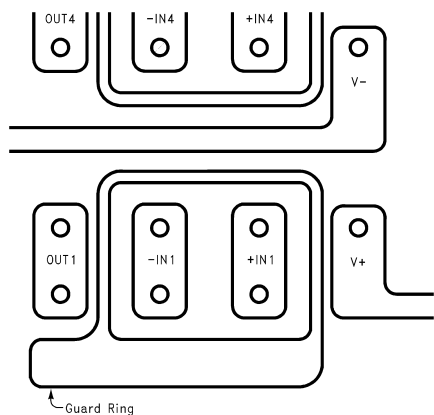
FIGURE 3. Compensating for Large Capacitive Loads with a Pull Up Resistor

PRINTED-CIRCUIT-BOARD LAYOUT FOR HIGH-IMPEDANCE WORK

It is generally recognized that any circuit which must operate with less than 1000 pA of leakage current requires special layout of the PC board. When one wishes to take advantage

Application Hints (Continued)

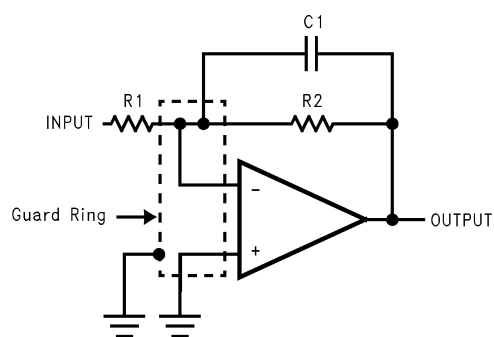
of the ultra-low bias current of the LMC6044, typically less than 2 fA, it is essential to have an excellent layout. Fortunately, the techniques of obtaining low leakages are quite simple. First, the user must not ignore the surface leakage of the PC board, even though it may sometimes appear acceptably low, because under conditions of high humidity or dust or contamination, the surface leakage will be appreciable.



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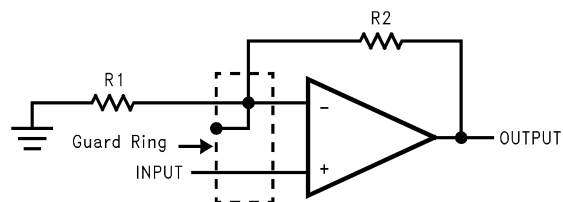
FIGURE 4. Example of Guard Ring in P.C. Board Layout

To minimize the effect of any surface leakage, lay out a ring of foil completely surrounding the LMC6044's inputs and the terminals of capacitors, diodes, conductors, resistors, relay terminals, etc. connected to the op-amp's inputs, as in *Figure 4*. To have a significant effect, guard rings should be placed on both the top and bottom of the PC board. This PC foil must then be connected to a voltage which is at the same voltage as the amplifier inputs, since no leakage current can flow between two points at the same potential. For example, a PC board trace-to-pad resistance of $10^{12}\Omega$, which is normally considered a very large resistance, could leak 5 pA if the trace were a 5V bus adjacent to the pad of the input. This would cause a 100 times degradation from the LMC6044's actual performance. However, if a guard ring is held within 5 mV of the inputs, then even a resistance of $10^{11}\Omega$ would cause only 0.05 pA of leakage current. See *Figure 5* for typical connections of guard rings for standard op-amp configurations.



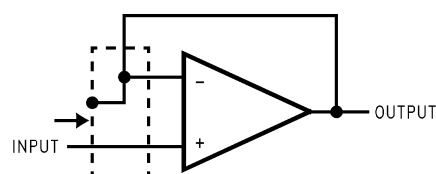
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Inverting Amplifier



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Non-Inverting Amplifier



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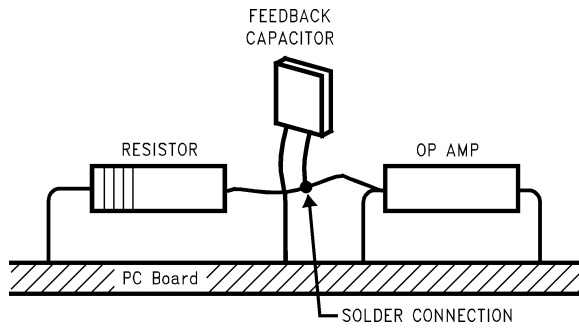
Follower

FIGURE 5. Typical Connections of Guard Rings

The designer should be aware that when it is inappropriate to lay out a PC board for the sake of just a few circuits, there is another technique which is even better than a guard ring on a PC board: Don't insert the amplifier's input pin into the board at all, but bend it up in the air and use only air as an insulator. Air is an excellent insulator. In this case you may have to forego some of the advantages of PC board construction, but the advantages are sometimes well worth the effort of using point-to-point up-in-the-air wiring. See *Figure 6*.

Typical Single-Supply Applications

($V_+ = 5.0 V_{DC}$)



(Input pins are lifted out of PC board and soldered directly to components. All other pins connected to PC board.)

FIGURE 6. Air Wiring

The extremely high input impedance, and low power consumption, of the LMC6044 make it ideal for applications that require battery-powered instrumentation amplifiers. Examples of these type of applications are hand-held pH probes, analytic medical instruments, magnetic field detectors, gas detectors, and silicon based pressure transducers. The circuit in *Figure 7* is recommended for applications where the common-mode input range is relatively low and the differential gain will be in the range of 10 to 1000. This two op-amp instrumentation amplifier features an independent adjustment of the gain and common-mode rejection trim, and a total quiescent supply current of less than 40 μA .

To maintain ultra-high input impedance, it is advisable to use ground rings and consider PC board layout an important part of the overall system design (see Printed-Circuit-Board Layout for High Impedance Work). Referring to *Figure 7*, the input voltages are represented as a common-mode input V_{CM} plus a differential input V_D . Rejection of the common-mode component of the input is accomplished by making the ratio of R_1/R_2 equal to R_3/R_4 . So that where,

$$\frac{R_3}{R_4} = \frac{R_2}{R_1}$$

$$V_{OUT} = \frac{R_4}{R_3} \left(1 + \frac{R_3}{R_4} + \frac{R_2 + R_3}{R_O} \right) V_D$$

A suggested design guideline is to minimize the difference of value between R_1 through R_4 . This will often result in improved resistor tempco, amplifier gain, and CMRR over temperature. If $R_N = R_1 = R_2 = R_3 = R_4$ then the gain equation can be simplified:

$$V_{OUT} = 2 \left(1 + \frac{R_N}{R_O} \right) V_D$$

Due to the “zero-in, zero-out” performance of the LMC6044, and output swing rail-rail, the dynamic range is only limited to the input common-mode range of $0V$ to $V_S - 2.3V$, worst case at room temperature. This feature of the LMC6044 makes it an ideal choice for low-power instrumentation systems.

A complete instrumentation amplifier designed for a gain of 100 is shown in *Figure 8*. Provisions have been made for low sensitivity trimming of CMRR and gain.

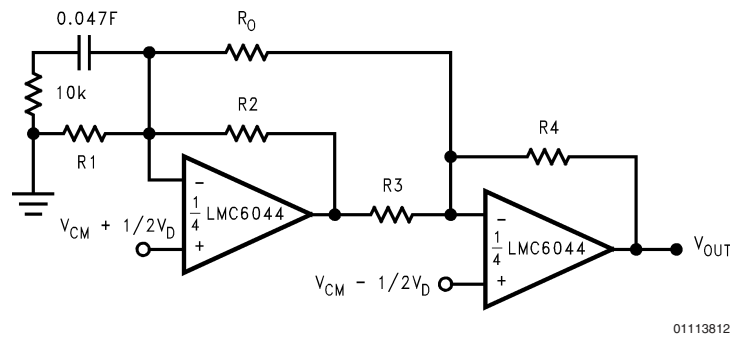
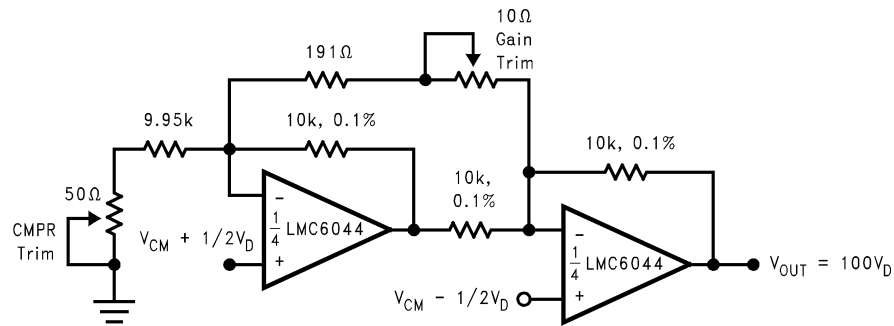


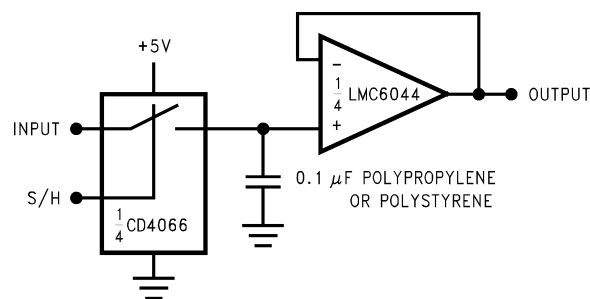
FIGURE 7. Two Op-Amp Instrumentation Amplifier

Typical Single-Supply Applications ($V_+ = 5.0 V_{DC}$) (Continued)



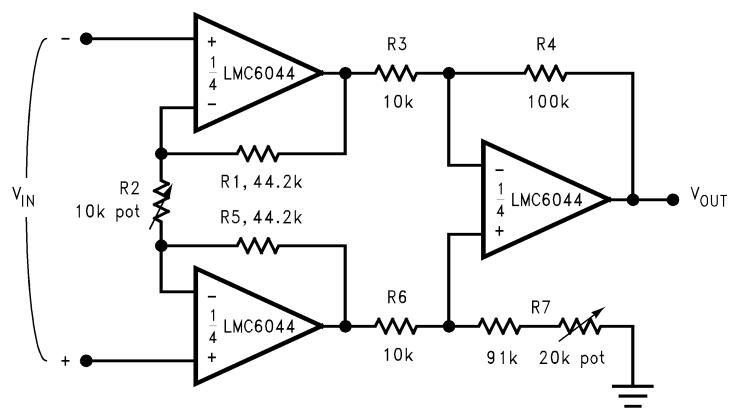
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FIGURE 8. Low-Power Two-Op-Amp Instrumentation Amplifier



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FIGURE 9. Low-Leakage Sample-and-Hold

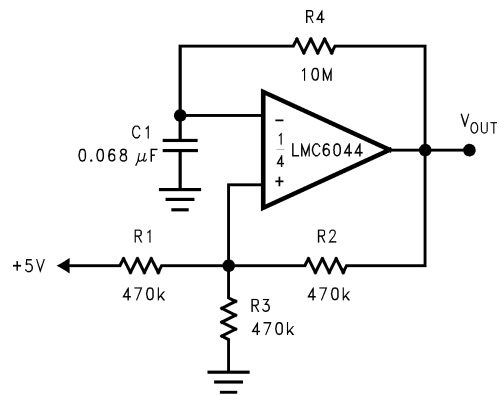


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FIGURE 10. Instrumentation Amplifier

Typical Single-Supply Applications

($V_+ = 5.0\text{ V}_{\text{DC}}$) (Continued)

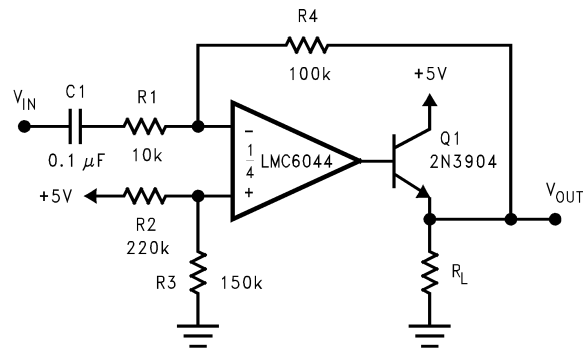


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FIGURE 11. 1 Hz Square-Wave Oscillator

Ordering Information

Package	Temperature Range	NSC Drawing	Transport Media
	Industrial -40°C to +85°C		
14-Pin Small Outline	LMC6044AIM, LMC6044AIMX	M14A	Rail Tape and Reel
14-Pin Molded DIP	LMC6044AIN LMC6044IN	N14A	Rail

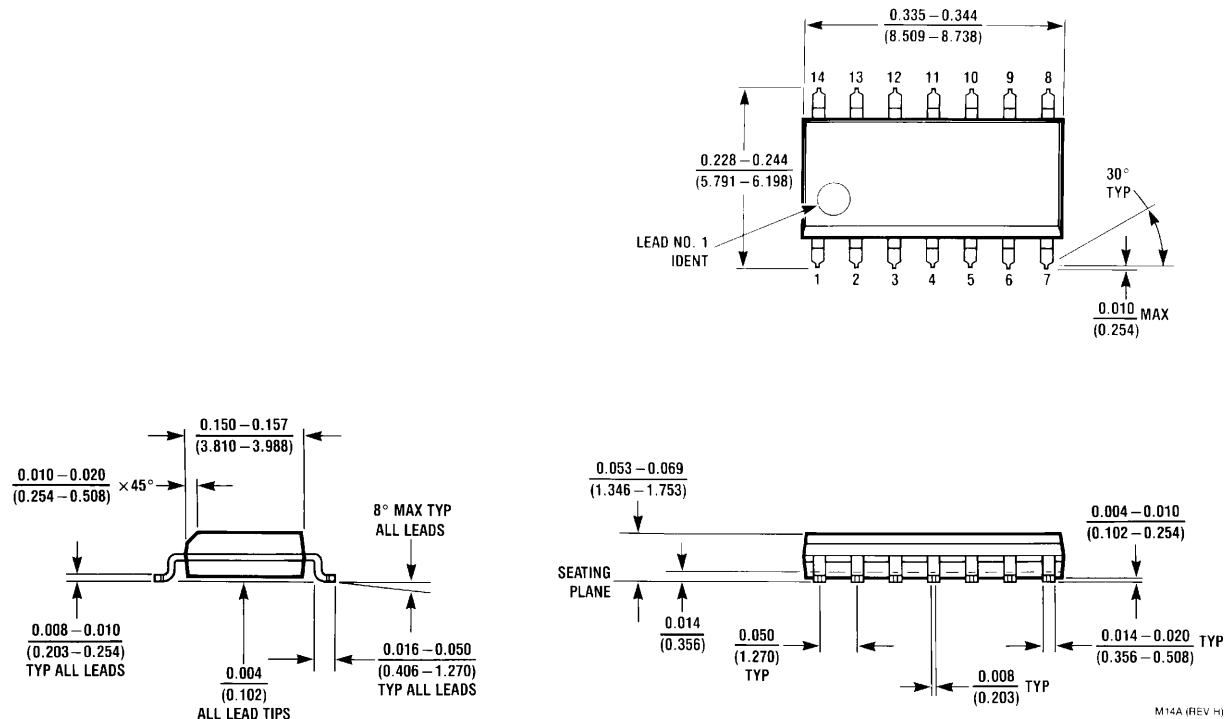


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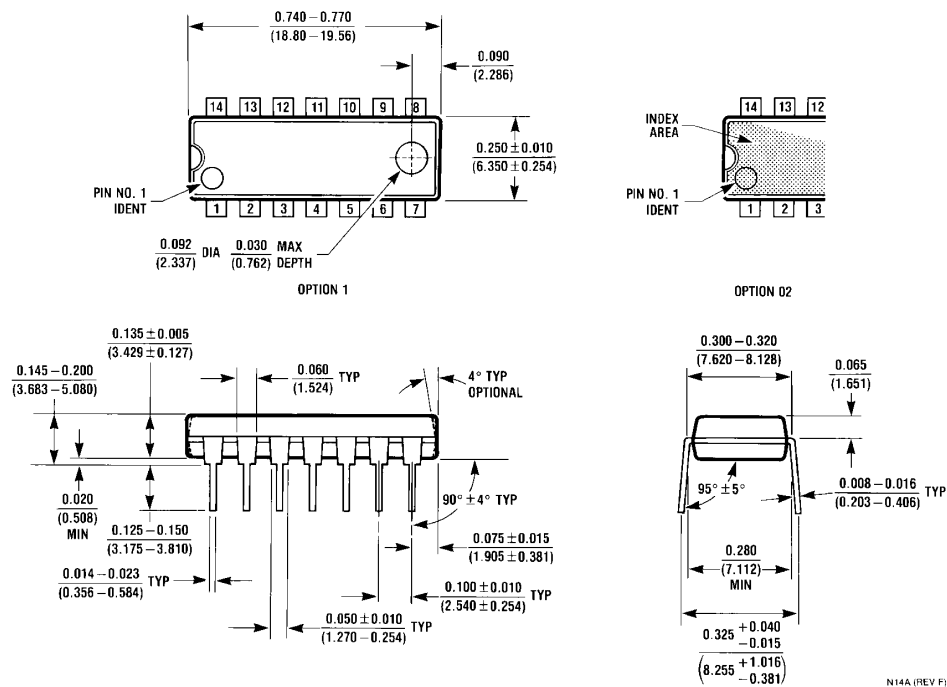
FIGURE 12. AC Coupled Power Amplifier

Physical Dimensions inches (millimeters)

unless otherwise noted



14-Pin Small Outline
Order Package Number LMC6044AIM, LMC6044AIMX, LMC6044IM or LMC6044IMX
NS Package Number M14A



14-Pin Molded DIP
Order Package Number LMC6044AIN or LMC6044IN
NS Package Number N14A

Notes

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