

BUILT-IN PROGRAMMABLE ROM VERSION

4.1 Overview

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In addition to the mask ROM versions, there are other members of the 7470 Series called built-in programmable ROM versions which are microcomputers with built-in programmable ROM. One version, the window-type EPROM version, has an built-in EPROM that can be written to and erased. Another version is a one-time programmable microcomputer whose built-in PROM can be written to but not erased. Since the functions of the built-in EPROM and one-time programmable versions are exactly the same, apart from whether the ROM contents can be erased, they are both referred to as built-in PROM versions in this manual.

The built-in PROM versions have functions similar to those of the mask ROM versions, but they also have a EPROM mode that enables writing to built-in PROM.

Seven built-in PROM versions of the 7470 Series are available: the M37470E4-XXXSP (one-time programmable), the M37470E8-XXXSP (one-time programmable), the M37471E4-XXXSP/FP (one-time programmable), the M37471E8-XXXSP/FP (one-time programmable), and the M37471E8SS (window version). A brief outline of the specifications of these microcomputers is given in Table 4.1.1.

Table 4.1.1 Functions of built-in PROM versions (M37470E4-XXXSP, M37470E8-XXXSP, M37471E4-XXXSP/FP, M37471E8-XXXSP/FP, and M37471E8SS)

Parameter			Functions		
			M37470E4-XXXSP and M37470E8-XXXSP	M37471E4-XXXSP, M37471E8-XXXSP and M37471E8SS	M37471E4-XXXFP and M37471E8-XXXFP
Basic instructions			69		
Instruction execution time			1.0μs (minimum instructions, at 4MHz)		
Clock frequency			4MHz		
Memory size	PROM (Note 4)		8192 bytes (Note 1)		
	RAM		192 bytes (Note 2)		
Input/Output ports	P0, P1	I/O	8-bit × 2	8-bit × 2	
	P2	I/O	4-bit × 1	8-bit × 1	
	P3	Input	4-bit × 1	4-bit × 1	
	P4	I/O	2-bit × 1	4-bit × 1	
	P5	Input	—	4-bit × 1	
Serial I/O			8-bit × 1		
Timer			8-bit × 4 (with 8-bit latch)		
A-D converter			8-bit × 1 (4-channel)	8-bit × 1 (8-channel)	
Subroutine nesting			96 (max.) (Note 3)		
Interrupt			External 5, internal 6 and software 1		
Clock generating circuit			1 built-in (with external ceramic or quartz crystal oscillator)	2 built-in (with external ceramic or quartz crystal oscillator)	
Power supply			2.7 to 5.5V		
Power dissipation (typ.)			17.5mW (at 4MHz)		
Input/Output characteristics	Input/Output voltage		5V		
	Output current		-5 to 10mA (P0, P1, P2 and P4: CMOS 3-state)		
Operating temperature range			-20 to 85°C		
Device structure			CMOS silicon gate		
Package	One-time programmable		32-pin shrink plastic molded DIP	42-pin shrink plastic molded DIP	56-pin plastic molded QFP
	Window type		—	42-pin shrink ceramic DIP	—

Note 1 : 16384 bytes for M37470E8-XXXSP, M37471E8-XXXSP/FP and M37471E8SS.

2 : 384 bytes for M37470E8-XXXSP, M37471E8-XXXSP/FP and M37471E8SS.

3 : 192 (max.) for M37470E8-XXXSP, M37471E8-XXXSP/FP and M37471E8SS.

4 : Voltage of writing to PROM is 12.5V (corresponding to M5L27256).

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4.2 Pin configuration

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Figure 4.2.1 shows the pin configuration of M37470E4-XXXSP and M37470E8-XXXSP, Figure 4.2.2 shows the pin configuration of M37471E4-XXXSP, M37471E8-XXXSP and M37471E8SS, and Figure 4.2.3 shows the pin configuration of M37471E4-XXXFP and M37471E8-XXXFP. The built-in PROM versions have pin-compatibility with the mask ROM version.

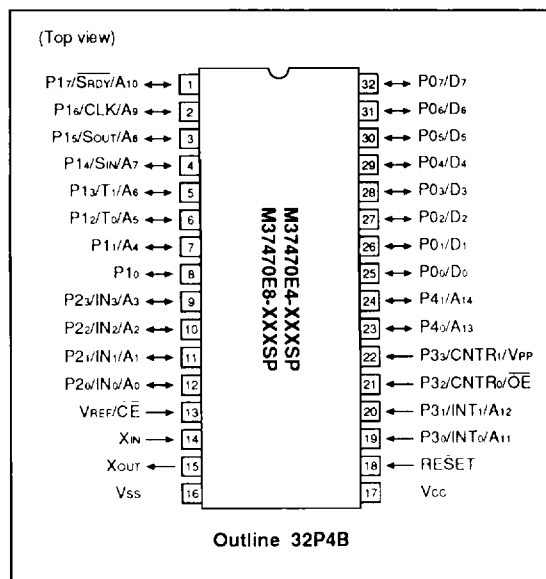


Fig.4.2.1 Pin configuration (M37470E4-XXXSP and M37470E8-XXXSP)

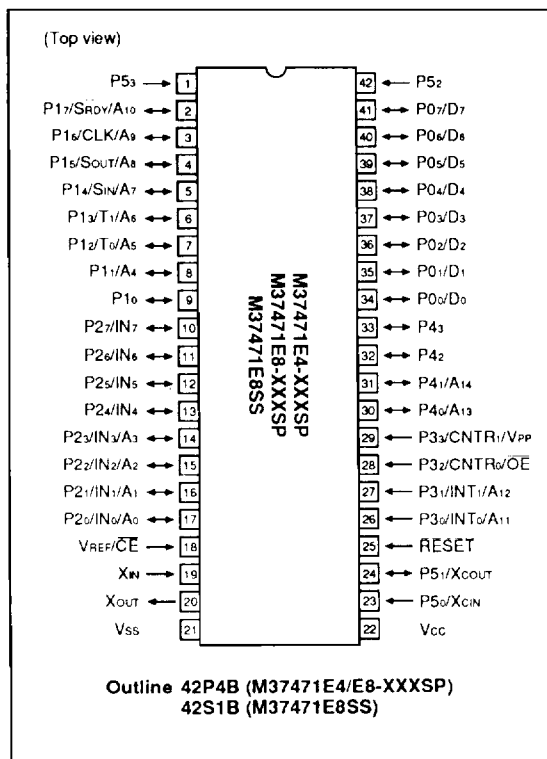


Fig.4.2.2 Pin configuration (M37471E4-XXXSP, M37471E8-XXXSP and M37471E8SS)

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4.3 Block diagram

4.3 Block diagram

Figures 4.3.1 to 4.3.3 shows the block diagrams of M37470E4-XXXSP, M37470E8-XXXSP, M37471E4-XXXSP, M37471E8-XXXSP, M37471E8SS, M37471E4-XXXFP, and M37471E8-XXXFP.

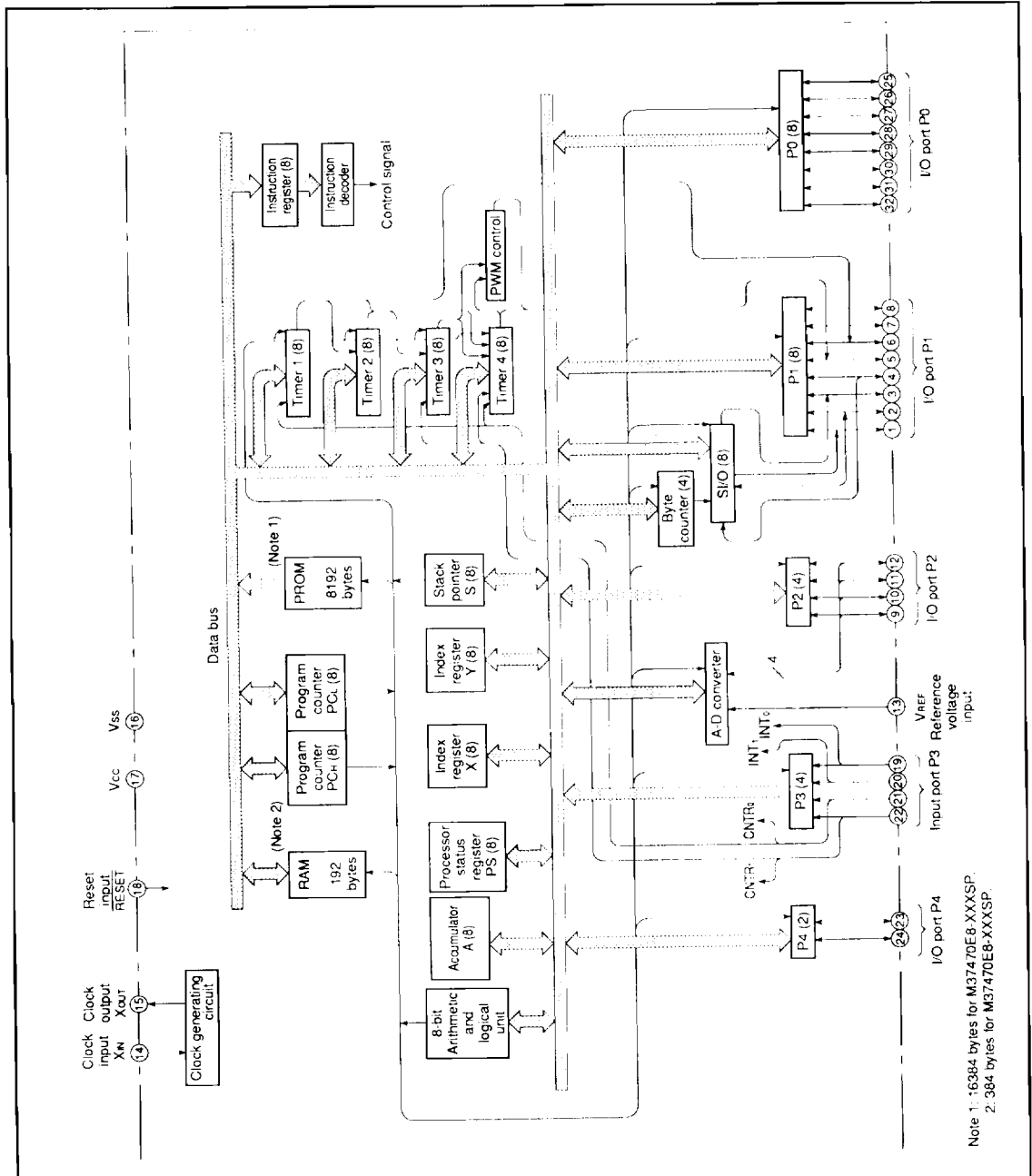


Fig.4.3.1 Block diagram of M37470E4-XXXSP and M37470E8-XXXSP

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4.3 Block diagram

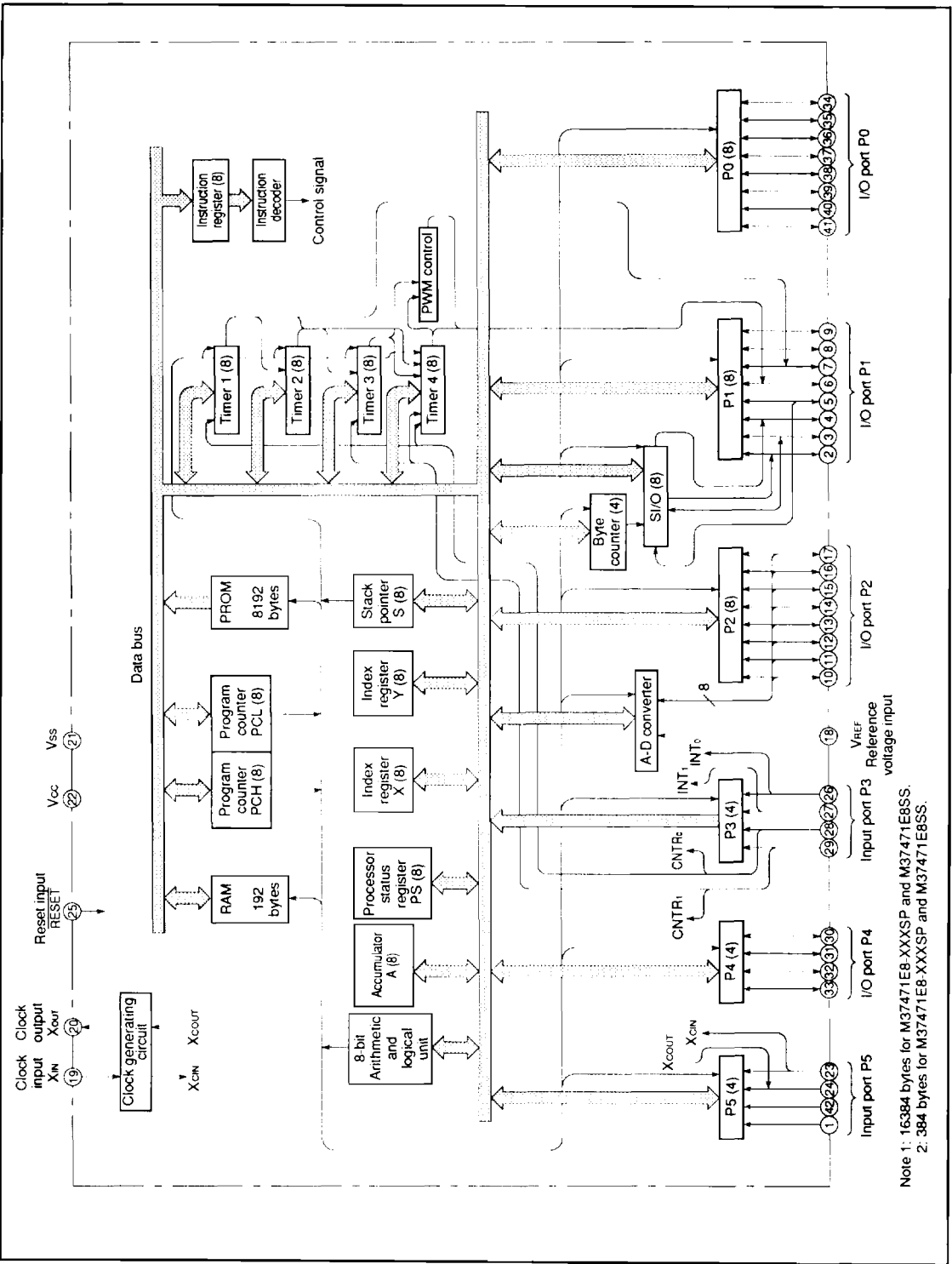


Fig.4.3.2 Block diagram of M37471E4-XXXSP and M37471E8-XXXSP(M37471E8SS)

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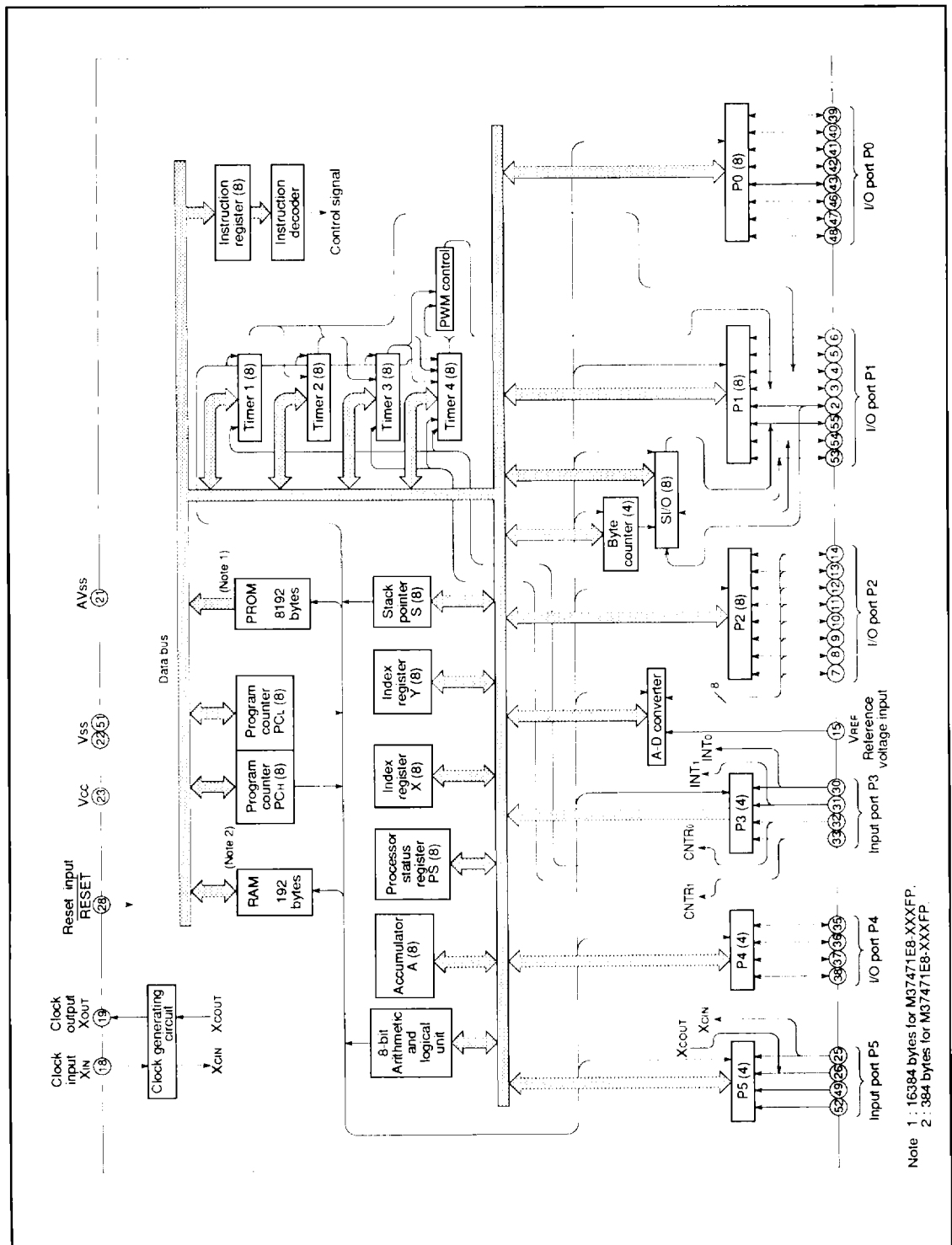


Fig.4.3.3 Block diagram of M37471E4-XXXXFP and M37471E8-XXXXFP

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4.4 EPROM mode

4.4 EPROM mode

4.4.1 EPROM mode

The built-in PROM versions of the 7470 Series have an EPROM mode in addition to the ordinary operating mode. Use EPROM mode to write to, read from, and erase built-in PROM, in the same way as in the M5L27256 (EPROM device).

The pin assignments in EPROM mode are shown in Table 4.4.1, and pin connection diagrams are shown in Figures 4.4.1 to 4.4.3.

Table 4.4.1 Pin correspondence at the EPROM mode

Device type name	Built-in PROM version	M5L27256
Pin name	Vcc	Vcc
	P33	VPP
	Vss	Vss
	P11 to P17, P20 to P23 P30, P31, P40, P41	A0 to A14
	P00 to P07	D0 to D7
	VREF	CE
	P32	OE

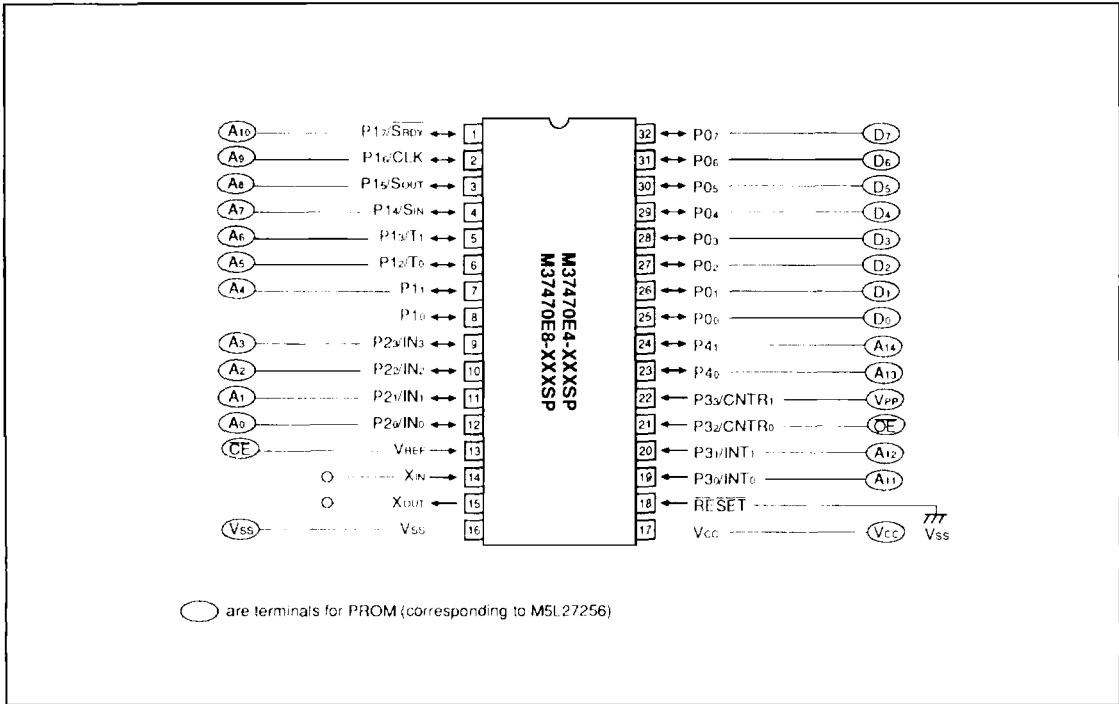


Fig.4.4.1 Pin connection at EPROM mode (M37470E4-XXXSP and M37470E8-XXXSP)

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4.4 EPROM mode

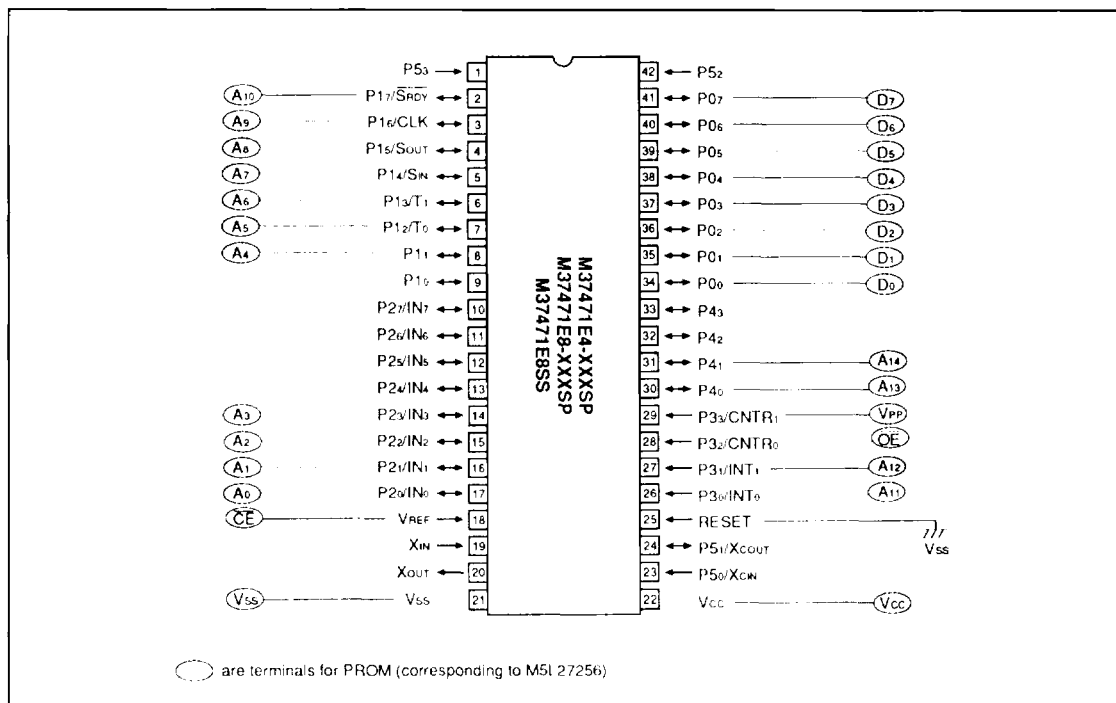


Fig.4.4.2 Pin connection at EPROM mode (M37471E4-XXXSP, M37471E8-XXXSP and M37471E8SS)

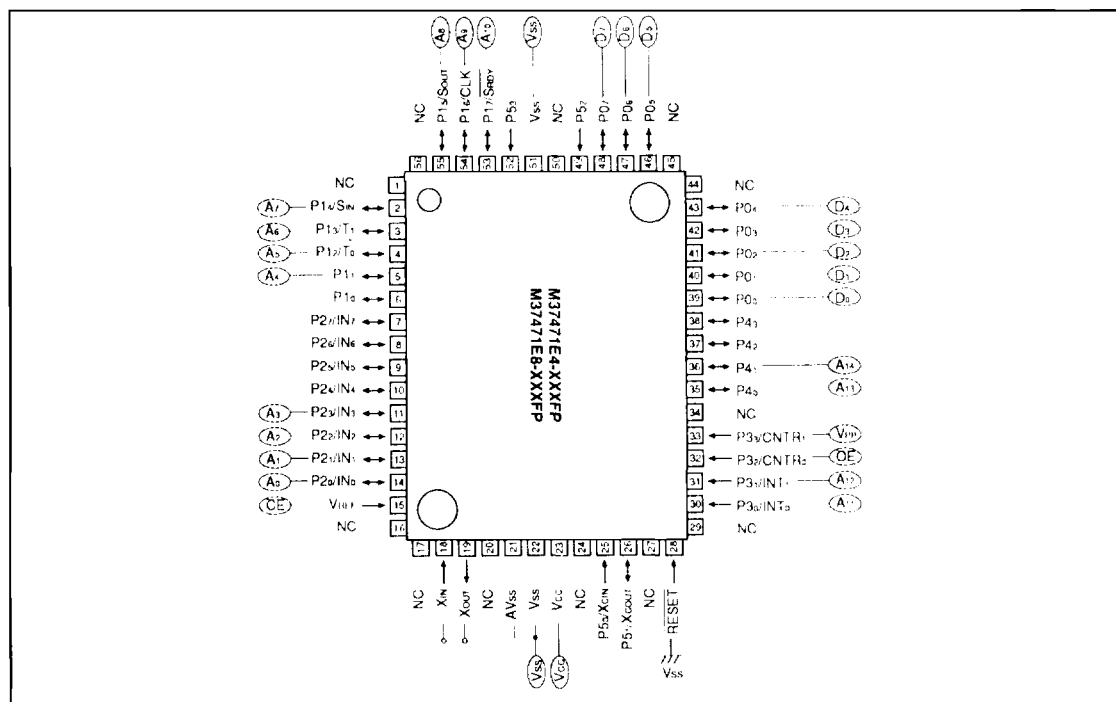


Fig.4.4.3 Pin connection at EPROM mode (M37471E4-XXXFP and M37471E8-XXXFP)

BUILT-IN PROGRAMMABLE ROM VERSION

4.4 EPROM mode

4.4.2 Pin description

Table 4.4.2 shows the pin description at ordinary operating mode and EPROM mode.

Table 4.4.2 Pin description

Pin	Name	Mode	Function
Vcc, Vss	Supply voltage	Ordinary operation/ EPROM	Supply 2.7 to 5.5V to Vcc, and 0V to Vss.
AVss	Analog power supply	Ordinary operation/ EPROM	Acts as ground level input pin for A-D converter. Same voltage as Vss is applied. (Note 1)
VREF	Reference voltage input	Ordinary operation	Acts as reference voltage input pin for the A-D converter.
	Mode input	EPROM	Becomes CE input.
RESET	Reset input	Ordinary operation	Specifies reset when held at "L" for at least 2 μ s.
		EPROM	Connect to Vss.
XIN	Clock input	Ordinary operation/ EPROM	Acts as input and output pins interfacing with the internal clock generating circuit. Connect a ceramic resonator or crystal oscillator between the XIN and XOUT pins to set the oscillator frequency. An internal feedback resistor is connected between the XIN and XOUT pins.
XOUT	Clock output	Ordinary operation/ EPROM	If an external clock is used, connect the clock source to the XIN pin and leave the XOUT pin open.
P0 $\bar{0}$ –P0 $\bar{7}$	I/O port P0	Ordinary operation	Acts as 8-bit I/O port with CMOS output format. When input port is selected, these pins can be connected individually to pull-up transistors. A key on wakeup function is also provided.
	Data I/O D $\bar{0}$ –D $\bar{7}$	EPROM	Becomes data(D $\bar{0}$ –D $\bar{7}$) I/O.
P1 $\bar{0}$ –P1 $\bar{7}$	I/O port P1	Ordinary operation	Acts as 8-bit I/O port with CMOS output format. When input port is selected, these pins can be connected in groups of four to pull-up transistors. P1 $\bar{2}$ and P1 $\bar{3}$ can also be used as timer outputs T $\bar{0}$ and T $\bar{1}$, and P1 $\bar{4}$, P1 $\bar{5}$, P1 $\bar{6}$, and P1 $\bar{7}$ can also be used as SIN, SOUT, CLK, and SRDY of the serial I/O function. SOUT and SRDY outputs can be set to N-channel open drain output.
	Address input A $\bar{4}$ –A $\bar{10}$	EPROM	Pins P1 $\bar{1}$ to P1 $\bar{7}$ are address(A $\bar{4}$ –A $\bar{10}$) input pins. Leave P1 $\bar{0}$ pin open.
P2 $\bar{0}$ –P2 $\bar{7}$ (Note 2)	I/O port P2	Ordinary operation	Acts as 8-bit I/O port with CMOS output format. When input port is selected, these pins can be connected in groups of four to pull-up transistors. These pins can also be used as analog inputs IN $\bar{0}$ to IN $\bar{7}$.
	Address input A $\bar{0}$ –A $\bar{3}$	EPROM	Pins P2 $\bar{0}$ to P2 $\bar{3}$ are address(A $\bar{0}$ –A $\bar{3}$) input pins. Leave P2 $\bar{4}$ to P2 $\bar{7}$ open.

Note 1: For 56-pin QFP type only.

2: At M37470E4-XXXSP and M37470E8-XXXSP, there are 4-bit as P2 $\bar{0}$ –P2 $\bar{3}$ (IN $\bar{0}$ –IN $\bar{3}$) only.

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4.4 EPROM mode

Table 4.4.2 Pin description

Pin	Name	Mode	Function
P30-P33	Input port P3	Ordinary operation	Acts as 4-bit input port. P30 and P31 can also be used as external interrupt input pins INT0 and INT1, and P32 and P33 can also be used as timer input pins CNTR0 and CNTR1.
	Address input A11, A12 Mode input VPP input	EPROM	Pins P30 and P31 are address(A11, A12) input pins. P32 becomes OE input pin. P33 becomes VPP input pin. At programming and program verifying, supply VPP level into this pin.
P40-P43 (Note 2)	I/O port P4	Ordinary operation	Acts as 4-bit I/O port with CMOS output format. When input port is selected, these pins can be connected in groups of four to pull-up transistors.
	Address input A13, A14	EPROM	Pins P40 and P41 are address(A13, A14) input pins. Leave pins P42 and P43 open.
P50-P53 (Note 3)	Input port P5	Ordinary operation	Acts as 4-bit input port that can be connected as a group of four pins to pull-up transistors. P50 and P51 can also be used as the XCIN and Xcout pins for the clock-function clock generating circuit. When using these pins as XCIN and Xcout pins, an internal feedback resistor is connected between them. To enable external clock input, connect the clock source to the XCIN pin and leave the Xcout pin open.
		EPROM	Setting to open.

Note 2: At M37470E4-XXXSP and M37470E8-XXXSP, there are 2-bit as P40 and P41 only.

3: At M37470E4-XXXSP and M37470E8-XXXSP, there are nothing.

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4.4 EPROM mode

4.4.3 Reading, writing, and erasure of built-in PROM

Activate EPROM mode in the built-in PROM versions by forcing the RESET pin to "L". In EPROM mode, the built-in PROM can be read from, written to, and erased, as described below.

(1) Reading

Apply 0V to the RESET pin and 5V to the VCC pin.

Input the address signal (A0 to A14) and set the CE and OE pins to "L"—the PROM contents will appear at the data I/O pins (D0 to D7). If the CE pin or the OE pin is set to "H", the data I/O pins will float.

(2) Writing

Apply 0V to the RESET pin and 6V to the VCC pin.

Set the OE pin to "H" and apply VPP to the VPP pin to activate program mode. Set the address to be written to by the address input pins (A0 to A14) and input the data in parallel through the data I/O pins (D0 to D7). When the CE pin is set to "L" in this status, the data is written to PROM.

(3) Erasure

Only the built-in EPROM version that has an erasure window on the package's top surface (M37471E8SS) can be erased. To erase the EPROM, shine an ultraviolet light source of wavelength 2537Å onto the window for a minimum dose of 15W·s/cm².

Note the following points when writing data with a PROM writer:

- M37470E4-XXXSP, and M37471E4-XXXSP/FP

When using a PROM writer, the address range should be between 6000₁₆ and 7FFF₁₆. Read/write operations on addresses 0000₁₆ to 5FFF₁₆ cannot be performed correctly.

- M37470E8-XXXSP, M37471E8-XXXSP/FP and M37471E8SS

When using a PROM writer, the address range should be between 4000₁₆ and 7FFF₁₆. When data is written between addresses 0000₁₆ and 7FFF₁₆, fill addresses 0000₁₆ to 3FFF₁₆ with FF₁₆.

Table 4.4.3 Input/Output signal at each mode

Mode \ Pin name	CE	OE	VPP	VCC	RESET	D0~D7
Read	V _{IL}	V _{IL}	VCC	VCC	0V	Output
Output disable	V _{IL}	V _{IH}	VCC			Floating
Write	V _{IL}	V _{IH}	12.5V			Input
Verify	V _{IH}	V _{IL}	12.5V			Output
Write disable	V _{IH}	V _{IH}	12.5V			Floating

Note : V_{IL} means "L" input voltage, V_{IH} means "H" input voltage.

BUILT-IN PROGRAMMABLE ROM VERSION

4.4 EPROM mode

4.4.4 Notes on handling

- (1) Sunlight and fluorescent light include wavelengths that will erase written data. When using the window version of the 7470 Series in read mode, always cover the transparent glass window with a light-proof seal.
 - (2) Mitsubishi provides light-proof seals designed to cover the transparent glass window of the window version. Make sure that the seal does not touch the lead pins of the microcomputer.
 - (3) Before erasing the window version, clean the transparent glass of the window. Dirt such as grease from hands and glue may hinder the passage of ultraviolet light and affect the erasure characteristics.
 - (4) Writing involves the use of high voltages, so make sure that excessive voltages are not used. Pay particular attention when turning on the power source.
 - (5) Mitsubishi does not test or screen any writing to PROM in blank one-time programmable microcomputers^{**} after they have left the factory. To improve reliability after writing, we recommend that these microcomputers are written to and tested in the sequence shown in the flow diagram of Figure 4.4.4.
- (^{**}1: Blank microcomputers have nothing written in PROM when they leave the factory.)

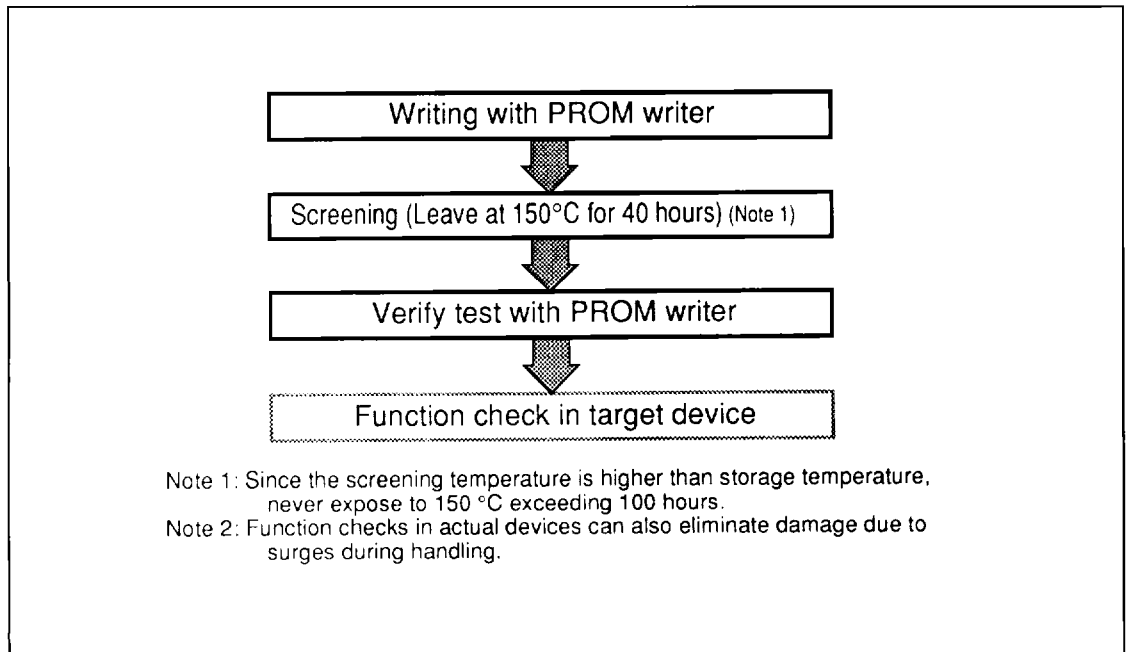


Fig.4.4.4 Writing and test for blank one-time programmable type

BUILT-IN PROGRAMMABLE ROM VERSION

4.5 Electric Characteristics

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4.5.1 Electric characteristics of M37470E4-XXXSP and M37470E8-XXXSP

Absolute maximum ratings

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage	With respect to V_{SS} Output transistors are at "OFF" state.	-0.3 to 7	V
V_I	Input voltage X_{IN}		-0.3 to $V_{CC}+0.3$	V
V_I	Input voltage $P0_0-P0_7, P1_0-P1_7, P2_0-P2_3, P3_0-P3_3, P4_0-P4_1, V_{REF}, RESET$		-0.3 to $V_{CC}+0.3$ (Note 1)	V
V_O	Output voltage $P0_0-P0_7, P1_0-P1_7, P2_0-P2_3, P4_0-P4_1, X_{OUT}$		-0.3 to $V_{CC}+0.3$	V
P_d	Power dissipation	$T_a=25^\circ\text{C}$	1000	mW
T_{opr}	Operating temperature		-20 to 85	$^\circ\text{C}$
T_{stg}	Storage temperature		-40 to 150	$^\circ\text{C}$

Note 1: At writing to PROM, the value for $P3_3$ is 13V.

Recommended operating conditions ($V_{CC}=2.7$ to 5.5V , $V_{SS}=0\text{V}$, $T_a=-20$ to 85°C , unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
V_{CC}	Supply voltage	2.7	5	5.5	V
V_{SS}	Supply voltage		0		V
V_{IH}	"H" input voltage $P0_0-P0_7, P1_0-P1_7, P3_0-P3_3, RESET, X_{IN}$	$0.8V_{CC}$		V_{CC}	V
V_{IH}	"H" input voltage $P2_0-P2_3, P4_0-P4_1$	$0.7V_{CC}$		V_{CC}	V
V_{IL}	"L" input voltage $P0_0-P0_7, P1_0-P1_7, P3_0-P3_3$	0		$0.2V_{CC}$	V
V_{IL}	"L" input voltage $P2_0-P2_3, P4_0-P4_1$	0		$0.25V_{CC}$	V
V_{IL}	"L" input voltage X_{IN}	0		$0.16V_{CC}$	V
V_{IL}	"L" input voltage $RESET$	0		$0.12V_{CC}$	V
$I_{OH(sum)}$	"H" sum output current $P0_0-P0_7, P4_0-P4_1$			-30	mA
$I_{OH(sum)}$	"H" sum output current $P1_0-P1_7, P2_0-P2_3$			-30	mA
$I_{OL(sum)}$	"L" sum output current $P0_0-P0_7, P4_0-P4_1$			60	mA
$I_{OL(sum)}$	"L" sum output current $P1_0-P1_7, P2_0-P2_3$			60	mA
$I_{OH(peak)}$	"H" peak output current $P0_0-P0_7, P1_0-P1_7, P2_0-P2_3, P4_0-P4_1$			-10	mA
$I_{OL(peak)}$	"L" peak output current $P0_0-P0_7, P1_0-P1_7, P2_0-P2_3, P4_0-P4_1$			20	mA
$I_{OH(avg)}$	"H" average output current $P0_0-P0_7, P1_0-P1_7, P2_0-P2_3, P4_0-P4_1$ (Note 3)			-5	mA
$I_{OL(avg)}$	"L" average output current $P0_0-P0_7, P1_0-P1_7, P2_0-P2_3, P4_0-P4_1$ (Note 3)			10	mA
$f_{(CNTR)}$	Timer input frequency $CNTR_0$ ($P3_2$), $CNTR_1$ ($P3_3$) (Note 2)			1	MHz
$f_{(CLK)}$	Serial I/O clock input frequency $CLK(P1_6)$ (Note 2)			1	MHz
$f_{(XIN)}$	Clock oscillating frequency (Note 2)			4	MHz

Note 2: Oscillation frequency is at 50% duty cycle.

3: The average output current $I_{OH(avg)}$ and $I_{OL(avg)}$ are the average value during a 100ms.

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4.5 Electric Characteristics

Electrical characteristics ($V_{CC}=2.7$ to $5.5V$, $V_{SS}=0V$, $T_a=-20$ to $85^{\circ}C$, unless otherwise noted)

Symbol	Parameter	Test Conditions		Limits			Unit
				Min.	Typ.	Max.	
V _{OH}	"H" output voltage P0 ₀ –P0 ₇ , P1 ₀ –P1 ₇ , P2 ₀ –P2 ₃ , P4 ₀ , P4 ₁	V _{CC} =5V, I _{OH} =–5mA V _{CC} =3V, I _{OH} =–1.5mA	3 2				V
V _{OL}	"L" output voltage P0 ₀ –P0 ₇ , P1 ₀ –P1 ₇ , P2 ₀ –P2 ₃ , P4 ₀ , P4 ₁	V _{CC} =5V, I _{OL} =10mA V _{CC} =3V, I _{OL} =3mA				2 1	V
V _{T+} –V _{T–}	Hysteresis P0 ₀ –P0 ₇ , P3 ₀ –P3 ₃	V _{CC} =5V V _{CC} =3V		0.5 0.3			V
V _{T+} –V _{T–}	Hysteresis RESET	V _{CC} =5V V _{CC} =3V		0.5 0.3			V
V _{T+} –V _{T–}	Hysteresis P1 ₆ /CLK	use as CLK input V _{CC} =5V V _{CC} =3V		0.5 0.3			V
I _{IL}	"L" input current P0 ₀ –P0 ₇ , P1 ₀ –P1 ₇ , P3 ₀ –P3 ₂ , P4 ₀ , P4 ₁	V _I =0V, not use pull-up transistor V _{CC} =5V V _{CC} =3V				–5 –3	μA
		V _I =0V, use pull-up transistor V _{CC} =5V V _{CC} =3V	–0.25 –0.08	–0.5 –0.18	–1.0 –0.35	mA	
I _{IL}	"L" input current P3 ₃	V _I =0V V _{CC} =5V V _{CC} =3V				–5 –3	μA
I _{IL}	"L" input current P2 ₀ –P2 ₃	V _I =0V, not use as analog input, not use pull-up transistor V _{CC} =5V V _{CC} =3V				–5 –3	μA
			V _I =0V, not use as analog input, use pull-up transistor V _{CC} =5V V _{CC} =3V	–0.25 –0.08	–0.5 –0.18	–1.0 –0.35	mA
I _{IL}	"L" input current RESET, X _N	V _I =0V (X _N is at stop mode) V _{CC} =5V V _{CC} =3V				–5 –3	μA
I _{IH}	"H" input current P0 ₀ –P0 ₇ , P1 ₀ –P1 ₇ , P3 ₀ –P3 ₂ , P4 ₀ , P4 ₁	V _I =V _{CC} , not use pull-up transistor V _{CC} =5V V _{CC} =3V				5 3	μA
I _{IH}	"H" input current P3 ₃	V _I =V _{CC} V _{CC} =5V V _{CC} =3V				5 3	μA
I _{IH}	"H" input current P2 ₀ –P2 ₃	V _I =V _{CC} , not use as analog input, not use pull-up transistor V _{CC} =5V V _{CC} =3V				5 3	μA
I _{IH}	"H" input current RESET, X _{IN}	V _I =V _{CC} , (X _N is at stop mode) V _{CC} =5V V _{CC} =3V				5 3	μA
I _{CC}	Supply current	At normal operation, A-D conversion is not executed f(X _{IN})=4MHz	V _{CC} =5V		3.5	7	mA
			V _{CC} =3V		1.8	3.6	
		At normal operation, A-D conversion is executed f(X _{IN})=4MHz	V _{CC} =5V		4	8	
			V _{CC} =3V		2	4	
		At wait mode, f(X _{IN})=4MHz	V _{CC} =5V		1	2	
			V _{CC} =3V		0.5	1	
V _{RAM}	RAM retention voltage	Stop all oscillation V _{CC} =5V	T _a =25°C		0.1	1	μA
			T _a =85°C		1	10	
V _{RAM}	RAM retention voltage	Stop all oscillation	2				V

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4.5 Electric Characteristics

A-D converter characteristics

($V_{CC}=2.7$ to $5.5V$, $V_{SS}=0V$, $T_a=-20$ to $85^{\circ}C$, $f(X_{IN})=4MHz$, unless otherwise noted)

Symbol	Parameter	Test Conditions	Limits			Unit
			Min.	Typ.	Max.	
—	Resolution				8	bits
—	Non-linearity error				± 2	LSB
—	Differential non-linearity error				± 0.9	LSB
V_{0T}	Zero transition error	$V_{CC}=V_{REF}=5.12V$, $I_{OL(sum)}=0mA$ $V_{CC}=V_{REF}=3.072V$, $I_{OL(sum)}=0mA$			2 3	LSB
V_{FST}	Full-scale transition error	$V_{CC}=V_{REF}=5.12V$ $V_{CC}=V_{REF}=3.072V$			4 7	LSB
t_{CONV}	Conversion time				25	μs
V_{VREF}	Reference input voltage		$0.5V_{CC}$		V_{CC}	V
R_{LADDER}	Ladder resistance value		2	5	10	$k\Omega$
V_{IA}	Analog input voltage		0		V_{REF}	V

BUILT-IN PROGRAMMABLE ROM VERSION

4.5 Electric Characteristics

4.5.2 Electric characteristics of M37471E4-XXXSP/FP, M37471E8-XXXSP/FP and M37471E8SS

Absolute maximum ratings

Symbol	Parameter	Conditions	Ratings	Unit
V _{CC}	Supply voltage	With respect to V _{SS} Output transistors are at "OFF" state.	-0.3 to 7	V
V _I	Input voltage X _{IN}		-0.3 to V _{CC} +0.3	V
V _I	Input voltage P0 ₀ -P0 ₇ , P1 ₀ -P1 ₇ , P2 ₀ -P2 ₇ , P3 ₀ -P3 ₃ , P4 ₀ -P4 ₃ , P5 ₀ -P5 ₃ , V _{REF} , RESET		-0.3 to V _{CC} +0.3 (Note 1)	V
V _O	Output voltage P0 ₀ -P0 ₇ , P1 ₀ -P1 ₇ , P2 ₀ -P2 ₇ , P4 ₀ -P4 ₃ , X _{OUT}		-0.3 to V _{CC} +0.3	V
P _d	Power dissipation	T _a =25°C	1000(Note 2)	mW
T _{opr}	Operating temperature		-20 to 85	°C
T _{stg}	Storage temperature		-40 to 150	°C

Note 1: At writing to PROM, the value for P3₃ is 13V.

2: 500mW for M37471E4-XXXFP and M37471E8-XXXFP.

Recommended operating conditions (V_{CC}=2.7 to 5.5V, V_{SS}=AV_{SS}=0V, T_a=-20 to 85°C, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
V _{CC}	Supply voltage	2.7	5	5.5	V
V _{SS}	Supply voltage		0		V
AV _{SS}	Analog supply voltage		0		V
V _{IH}	"H" input voltage P0 ₀ -P0 ₇ , P1 ₀ -P1 ₇ , P3 ₀ -P3 ₃ , RESET, X _N	0.8V _{CC}		V _{CC}	V
V _{IH}	"H" input voltage P2 ₀ -P2 ₇ , P4 ₀ -P4 ₃ , P5 ₀ -P5 ₃ (Note 3)	0.7V _{CC}		V _{CC}	V
V _{IL}	"L" input voltage P0 ₀ -P0 ₇ , P1 ₀ -P1 ₇ , P3 ₀ -P3 ₃	0		0.2V _{CC}	V
V _{IL}	"L" input voltage P2 ₀ -P2 ₇ , P4 ₀ -P4 ₃ , P5 ₀ -P5 ₃ (Note 3)	0		0.25V _{CC}	V
V _{IL}	"L" input voltage X _N	0		0.16V _{CC}	V
V _{IL}	"L" input voltage RESET	0		0.12V _{CC}	V
I _{OH} (sum)	"H" sum output current P0 ₀ -P0 ₇ , P4 ₀ -P4 ₃			-30	mA
I _{OH} (sum)	"H" sum output current P1 ₀ -P1 ₇ , P2 ₀ -P2 ₇			-30	mA
I _{OL} (sum)	"L" sum output current P0 ₀ -P0 ₇ , P4 ₀ -P4 ₃			60	mA
I _{OL} (sum)	"L" sum output current P1 ₀ -P1 ₇ , P2 ₀ -P2 ₇			60	mA
I _{OH} (peak)	"H" peak output current P0 ₀ -P0 ₇ , P1 ₀ -P1 ₇ , P2 ₀ -P2 ₇ , P4 ₀ -P4 ₃			-10	mA
I _{OL} (peak)	"L" peak output current P0 ₀ -P0 ₇ , P1 ₀ -P1 ₇ , P2 ₀ -P2 ₇ , P4 ₀ -P4 ₃			20	mA
I _{OH} (avg)	"H" average output current P0 ₀ -P0 ₇ , P1 ₀ -P1 ₇ , P2 ₀ -P2 ₇ , P4 ₀ -P4 ₃ (Note 6)			-5	mA
I _{OL} (avg)	"L" average output current P0 ₀ -P0 ₇ , P1 ₀ -P1 ₇ , P2 ₀ -P2 ₇ , P4 ₀ -P4 ₃ (Note 6)			10	mA
f _(CNTR)	Timer input frequency CNTR ₀ (P3 ₂), CNTR ₁ (P3 ₃) (Note 4)			1	MHz
f _(CLK)	Serial I/O clock input frequency CLK(P1 ₆) (Note 4)			1	MHz
f _(XIN)	Clock oscillating frequency (Note 4)			4	MHz
f _(XCIN)	Clock oscillating frequency for clock function (Note 4, 5)		32	50	kHz

Note 3: It is except to use P5₀ as X_{CIN}.

4: Oscillation frequency is at 50% duty cycle.

5: When used in the low-speed mode, the clock oscillating frequency for clock function should be f_(XCIN)<f_(XIN)/3.

6: The average output current I_{OH}(avg) and I_{OL}(avg) are the average value during a 100ms.

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4.5 Electric Characteristics

Electrical characteristics ($V_{CC}=2.7$ to $5.5V$, $V_{SS}=AV_{SS}=0V$, $T_a=-20$ to $85^{\circ}C$, unless otherwise noted)

Symbol	Parameter	Test Conditions	Limits			Unit	
			Min.	Typ.	Max.		
V _{OH}	“H” output voltage P0 ₀ –P0 ₇ , P1 ₀ –P1 ₇ , P2 ₀ –P2 ₇ , P4 ₀ –P4 ₃	V _{CC} =5V, I _{OH} =–5mA	3			V	
		V _{CC} =3V, I _{OH} =–1.5mA	2				
V _{OL}	“L” output voltage P0 ₀ –P0 ₇ , P1 ₀ –P1 ₇ , P2 ₀ –P2 ₇ , P4 ₀ –P4 ₃	V _{CC} =5V, I _{OL} =10mA			2	V	
		V _{CC} =3V, I _{OL} =3mA			1		
V _{T+} –V _{T–}	Hysteresis P0 ₀ –P0 ₇ , P3 ₀ –P3 ₃	V _{CC} =5V		0.5		V	
		V _{CC} =3V		0.3			
V _{T+} –V _{T–}	Hysteresis RESET	V _{CC} =5V		0.5		V	
		V _{CC} =3V		0.3			
V _{T+} –V _{T–}	Hysteresis P1 ₆ /CLK	use as CLK input	V _{CC} =5V	0.5		V	
			V _{CC} =3V	0.3			
I _{IL}	“L” input current P0 ₀ –P0 ₇ , P1 ₀ –P1 ₇ , P3 ₀ –P3 ₂ , P4 ₀ –P4 ₃ , P5 ₀ –P5 ₃	V _I =0V, not use pull-up transistor	V _{CC} =5V		–5	μA	
			V _{CC} =3V		–3		
		V _I =0V, use pull-up transistor	V _{CC} =5V	–0.25	–0.5	–1.0	mA
			V _{CC} =3V	–0.08	–0.18	–0.35	
I _{IL}	“L” input current P3 ₃	V _I =0V	V _{CC} =5V		–5	μA	
			V _{CC} =3V		–3		
I _{IL}	“L” input current P2 ₀ –P2 ₇	V _I =0V, not use as analog input, not use pull-up transistor	V _{CC} =5V		–5	μA	
			V _{CC} =3V		–3		
		V _I =0V, not use as analog input, use pull-up transistor	V _{CC} =5V	–0.25	–0.5	–1.0	mA
			V _{CC} =3V	–0.08	–0.18	–0.35	
I _{IL}	“L” input current RESET, X _N	V _I =0V (X _N is at stop mode)	V _{CC} =5V		–5	μA	
			V _{CC} =3V		–3		
I _{IH}	“H” input current P0 ₀ –P0 ₇ , P1 ₀ –P1 ₇ , P3 ₀ –P3 ₂ , P4 ₀ –P4 ₃ , P5 ₀ –P5 ₃	V _I =V _{CC} , not use pull-up transistor	V _{CC} =5V		5	μA	
			V _{CC} =3V		3		
I _{IH}	“H” input current P3 ₃	V _I =V _{CC}	V _{CC} =5V		5	μA	
			V _{CC} =3V		3		
I _{IH}	“H” input current P2 ₀ –P2 ₇	V _I =V _{CC} , not use as analog input, not use pull-up transistor	V _{CC} =5V		5	μA	
			V _{CC} =3V		3		
I _{IH}	“H” input current RESET, X _N	V _I =V _{CC} , (X _N is at stop mode)	V _{CC} =5V		5	μA	
			V _{CC} =3V		3		
I _{CC}	Supply current	At normal operation, A-D conversion is not executed f(X _{IN})=4MHz	V _{CC} =5V		3.5	7	mA
			V _{CC} =3V		1.8	3.6	
		At normal operation, A-D conversion is executed f(X _{IN})=4MHz	V _{CC} =5V		4	8	
			V _{CC} =3V		2	4	
		At low- speed mode, X _{COU} T is low-power mode, A-D conversion is not executed f(X _{IN})=0Hz, f(X _{CN})=32kHz, T _a =25°C	V _{CC} =5V		30	80	μA
			V _{CC} =3V		15	40	
		At wait mode, f(X _{IN})=4MHz	V _{CC} =5V		1	2	mA
			V _{CC} =3V		0.5	1	
		At wait mode, f(X _{IN})=0Hz, f(X _{CN})=32kHz, X _{COU} T is low-power mode, T _a =25°C	V _{CC} =5V		3	12	μA
			V _{CC} =3V		2	8	
Stop all oscillation	T _a =25°C		0.1	1			
	V _{CC} =5V T _a =85°C		1	10			
V _{RAM}	RAM retention voltage	Stop all oscillation		2		V	

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4.5 Electric Characteristics

A-D converter characteristics

($V_{CC}=2.7$ to $5.5V$, $V_{SS}=AV_{SS}=0V$, $T_a=-20$ to $85^{\circ}C$, $f(X_N)=4MHz$, unless otherwise noted)

Symbol	Parameter	Test Condition	Limits			Unit
			Min.	Typ.	Max.	
—	Resolution				8	bits
—	Non-linearity error				± 2	LSB
—	Differential non-linearity error				± 0.9	LSB
V_{DT}	Zero transition error	$V_{CC}=V_{REF}=5.12V$, $I_{OL(sum)}=0mA$			2	LSB
		$V_{CC}=V_{REF}=3.072V$, $I_{OL(sum)}=0mA$			3	
V_{FST}	Full-scale transition error	$V_{CC}=V_{REF}=5.12V$			4	LSB
		$V_{CC}=V_{REF}=3.072V$			7	
t_{CONV}	Conversion time				25	μs
V_{VREF}	Reference input voltage		$0.5V_{CC}$		V_{CC}	V
R_{LADDER}	Ladder resistance value		2	5	10	$k\Omega$
V_{IA}	Analog input voltage		0		V_{REF}	V