

Hex 3-State Inverting Buffer with Separate 2-Bit and 4-Bit Sections

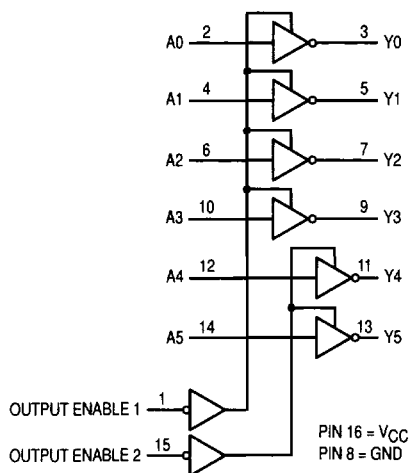
High-Performance Silicon-Gate CMOS

The MC74HC368 is identical in pinout to the LS368. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

This device is arranged into 2-bit and 4-bit sections, each having its own active-low Output Enable. When either of the enables is high, the affected buffer outputs are placed into high-impedance states. The HC368 has inverting outputs.

- Output Drive Capability: 15 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2 to 6 V
- Low Input Current: 1 μ A
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 80 FETs or 20 Equivalent Gates

LOGIC DIAGRAM



MC74HC368



N SUFFIX
PLASTIC PACKAGE
CASE 648-08

ORDERING INFORMATION

MC74HCXXN Plastic

PIN ASSIGNMENT

OUTPUT ENABLE 1	1	16	VCC
A0	2	15	OUTPUT ENABLE 2
Y0	3	14	A5
A1	4	13	Y5
Y1	5	12	A4
A2	6	11	Y4
Y2	7	10	A3
GND	8	9	Y3

FUNCTION TABLE

Inputs		Output
Enable 1, Enable 2	A	Y
L	L	H
L	H	L
H	X	Z

X = don't care
Z = high-impedance



MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	-0.5 to $+7.0$	V
V_{in}	DC Input Voltage (Referenced to GND)	-1.5 to $V_{CC} + 1.5$	V
V_{out}	DC Output Voltage (Referenced to GND)	-0.5 to $V_{CC} + 0.5$	V
I_{in}	DC Input Current, per Pin	± 20	mA
I_{out}	DC Output Current, per Pin	± 35	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	± 75	mA
P_D	Power Dissipation in Still Air Plastic DIP†	750	mW
T_{stg}	Storage Temperature	-65 to $+150$	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP)	260	°C

* Maximum Ratings are those values beyond which damage to the device may occur.

Functional operation should be restricted to the Recommended Operating Conditions.

† Derating — Plastic DIP: -10 mW/°C from 65° to 125° C

For high frequency or heavy load considerations, see Chapter 2.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $GND \leq (V_{in} \text{ or } V_{out}) \leq V_{CC}$. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit	
V _{CC}	DC Supply Voltage (Referenced to GND)	2.0	6.0	V	
V _{in} , V _{out}	DC Input Voltage, Output Voltage (Referenced to GND)	0	V _{CC}	V	
T _A	Operating Temperature, All Package Types	− 55	+ 125	°C	
t _r , t _f	Input Rise and Fall Time (Figure 1)	V _{CC} ≈ 2.0 V V _{CC} ≈ 4.5 V V _{CC} ≈ 6.0 V	0 0 0	1000 500 400	ns

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V_{CC} V	Guaranteed Limit			Unit
				-55 to 25° C	$\leq 85^\circ$ C	$\leq 125^\circ$ C	
V_{IH}	Minimum High-Level Input Voltage	$V_{out} = 0.1$ V $ I_{out} \leq 20$ μ A	2.0 4.5 6.0	1.5 3.15 4.2	1.5 3.15 4.2	1.5 3.15 4.2	V
V_{IL}	Maximum Low-Level Input Voltage	$V_{out} = V_{CC} - 0.1$ V $ I_{out} \leq 20$ μ A	2.0 4.5 6.0	0.3 0.9 1.2	0.3 0.9 1.2	0.3 0.9 1.2	V
V_{OH}	Minimum High-Level Output Voltage	$V_{in} = V_{IL}$ $ I_{out} \leq 20$ μ A	2.0 4.5 6.0	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	V
		$V_{in} = V_{IL}$ $ I_{out} \leq 6.0$ mA $ I_{out} \leq 7.8$ mA	4.5 6.0	3.98 5.48	3.84 5.34	3.70 5.20	
V_{OL}	Maximum Low-Level Output Voltage	$V_{in} = V_{IH}$ $ I_{out} \leq 20$ μ A	2.0 4.5 6.0	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	V
		$V_{in} = V_{IH}$ $ I_{out} \leq 6.0$ mA $ I_{out} \leq 7.8$ mA	4.5 6.0	0.26 0.26	0.33 0.33	0.40 0.40	
I_{in}	Maximum Input Leakage Current	$V_{in} = V_{CC}$ or GND	6.0	± 0.1	± 1.0	± 1.0	μ A
I_{OZ}	Maximum Three-State Leakage Current	Output in High-Impedance State $V_{in} = V_{IL}$ or V_{IH} $V_{out} = V_{CC}$ or GND	6.0	± 0.5	± 5.0	± 10	μ A
I_{CC}	Maximum Quiescent Supply Current (per Package)	$V_{in} = V_{CC}$ or GND $I_{out} = 0$ μ A	6.0	8	80	160	μ A

NOTE: Information on typical parametric values can be found in Chapter 2.

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AC ELECTRICAL CHARACTERISTICS (C_L = 50 pF, Input t_r = t_f = 6 ns)

Symbol	Parameter	V _{CC} V	Guaranteed Limit			Unit
			− 55 to 25°C	≤ 85°C	≤ 125°C	
t _{PLH} , t _{PHL}	Maximum Propagation Delay, Input A to Output Y (Figures 1 and 3)	2.0 4.5 6.0	95 19 16	120 24 20	145 29 25	ns
t _{PLZ} , t _{PHZ}	Maximum Propagation Delay, Output Enable to Output Y (Figures 2 and 4)	2.0 4.5 6.0	175 35 30	220 44 37	265 53 45	ns
t _{PZL} , t _{PZH}	Maximum Propagation Delay, Output Enable to Output Y (Figures 2 and 4)	2.0 4.5 6.0	190 38 32	240 48 41	285 57 48	ns
t _{TLH} , t _{THL}	Maximum Output Transition Time, Any Output (Figures 1 and 3)	2.0 4.5 6.0	60 12 10	75 15 13	90 18 15	ns
C _{in}	Maximum Input Capacitance	—	10	10	10	pF
C _{out}	Maximum Three-State Output Capacitance (Output in High-Impedance State)	—	15	15	15	pF

NOTES:

1. For propagation delays with loads other than 50 pF, see Chapter 2.
2. Information on typical parametric values can be found in Chapter 2.

C _{PD}	Power Dissipation Capacitance (Per Buffer)*	Typical @ 25°C, V _{CC} = 5.0 V	pF
		40	

* Used to determine the no-load dynamic power consumption: P_D = C_{PD} V_{CC}²f + I_{CC} V_{CC}. For load considerations, see Chapter 2.

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SWITCHING WAVEFORMS

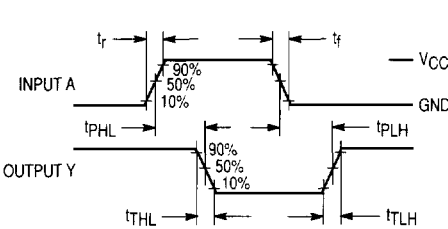


Figure 1.

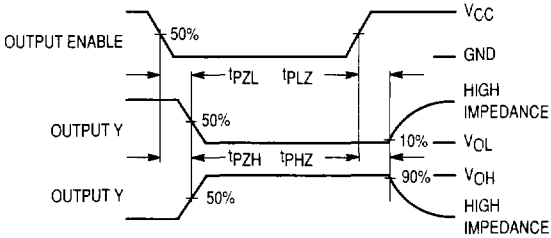
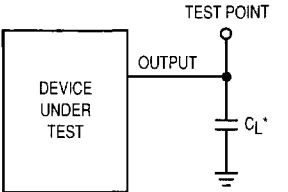


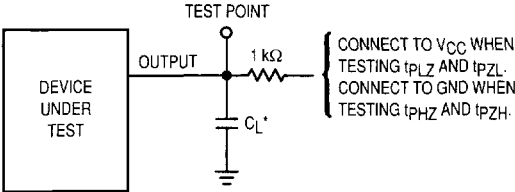
Figure 2.

TEST CIRCUITS



* Includes all probe and jig capacitance

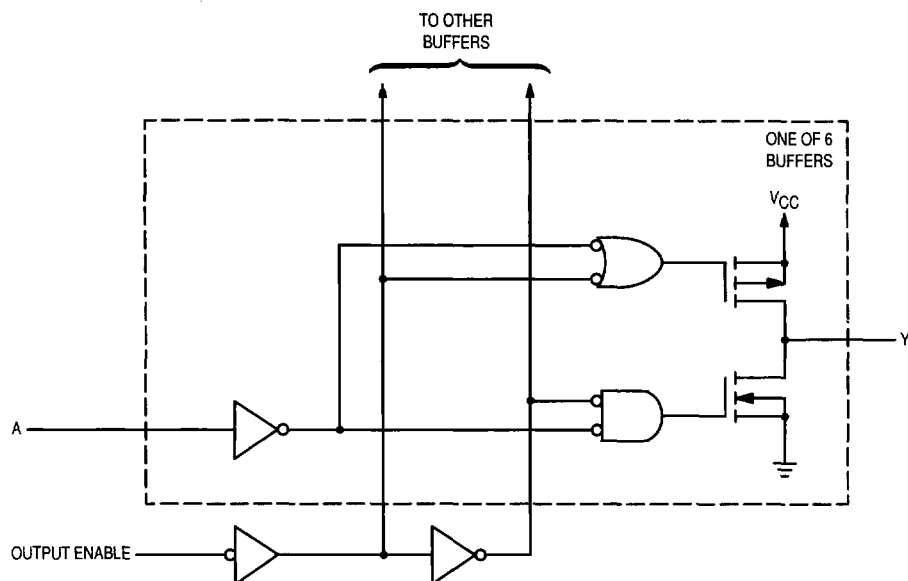
Figure 3.



* Includes all probe and jig capacitance

Figure 4.

LOGIC DETAIL



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