

AD394

1.1 Scope.

This specification covers the detail requirements for a hybrid quad 12-bit voltage output CMOS D/A converter with individual DAC reference inputs.

1.2 Part Number.

The complete part number per Table 1 of this specification is as follows:

Device	Part Number
-1	AD394SD/883B
-2	AD394TD/883B

1.2.3 Case Outline.

See Appendix 1 of General Specification ADI-H-1000: package outline: DH-28A.

1.3 Absolute Maximum Ratings. ($T_A = +25^{\circ}\text{C}$ unless otherwise noted)

$+V_S$ to DGND		-0.3V to $+17\text{V}$
$-V_S$ to DGND		$+0.3\text{V}$ to -17V
Digital Inputs (Pins 1-16) to DGND		-0.3V to $+7\text{V}$
V_{REFIN} to DGND		$\pm 25\text{V}$
AGND to DGND		-0.3V to $+V_S$
Analog Outputs (Pins 18, 21, 24, 27)		Indefinite
	Short to AGND or DGND Momentary	Short to $\pm V_S$
Operating Temperature Range (Ambient)		-55°C to $+125^{\circ}\text{C}$
Storage Temperature Range		-65°C to $+150^{\circ}\text{C}$
Lead Temperature (Soldering 10secs)		$+300^{\circ}\text{C}$

1.5 Thermal Characteristics.

Thermal Resistance $\theta_{\text{JC}} = 8^{\circ}\text{C}/\text{W}$ typ
 $\theta_{\text{JA}} = 25^{\circ}\text{C}/\text{W}$ typ

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Table 1.

Test	Symbol	Device	Design Limit @ 25°C/(−55°C to +125°C)	Sub Group 1	Sub Group 2, 3	Sub Group 4	Test Condition ¹	Units
Data Input Voltage High End Point Electrical	V _{IH}	−1, 2 −1, 2	2.4/(2.4) 5.5/(5.5)	2.4		2.4	Test Limits Apply to Pins 1–12. Design Limits Apply to Pins 13–16.	+ V min + V max + V min
Data Input Voltage Low End Point Electrical	V _{IL}	−1, 2 −1, 2	0.0/(0.0) 0.8/(0.8)	0.8		0.8	Test Limits Apply to Pins 1–12. Design Limits Apply to Pins 13–16.	+ V min + V max + V min
Input Current High	I _{IH}	−1, 2	40/(40)			40	V _{IN} = 0V or +5V	± μA max
Input Current Low End Point Electrical	I _{IL} I _{IH} , I _{IL}	−1, 2 −1, 2	40/(40)	40		40	V _{IN} = 0V or +5V	± μA max
Output Voltage Range ²	V _{OUT}	−1, 2	11/(11) 11/(11)			10 10	Output Voltage Equals −REFIN to +REFIN	− V min + V max
Output Current Range	I _{OR}	−1, 2	5/(5)					± mA min
Gain Error End Point Electrical	A _E	−1 −2 −1, 2	0.1 0.05	0.1 0.2		0.05	External + 10.000V REF Bit Code = 1111 1111 1111	± %FSR ³ max
Gain Error Temperature Coefficient	TC _{AE}	−1 −2	/(10) /(5)		10 5		External + 10.000V REF Bit Code = 1111 1111 1111	± ppm/°C max
Offset Error End Point Electrical	V _{OS}	−1 −2 −1, 2	0.05 0.025	0.05 0.1		0.025	External + 10.000V REF Bit Code = 0000 0000 0000	± %FSR max
Offset Temperature Coefficient	TC _{BPZ}	−1 −2	/(10) /(5)		10 5		External + 10.000V REF Bit Code = 0000 0000 0000	± ppm/°C max
Differential Linearity Error ⁴ End Point Electrical	DLE	−1 −2 −1, 2	3/4 1/2	3/4 1.5	1 1	1/2		± LSB max
Linearity Error ⁵ End Point Electrical	TC _{LE}	−1 −2 −1, 2	3/4 1/2	3/4 1/2 1	3/4 1/2			± LSB max
Power Supply Voltages ²	V _S	−1, 2 −1, 2	13.5/(13.5) 16.5/(16.5)	15 15	15 15			− V min V max
Power Supply Currents	I _{CC}	−1, 2	28/(35)			28	Data Input Bits = 1111 1111 1111 R _L = ∞	− mA max
	I _{EE}		22/(22)			22	Data Input Bits = 1111 1111 1111 R _L = ∞	+ mA max
Power Supply Gain Sensitivity Δ Gain/ ΔV _S (+V _S and −V _S)	PSRR	−1, 2	0.006			0.006	Input Bits = 1111 1111 1111 V _S = ±15V ±10%	± %FS/%
Timing Specifications Chip Select	t _{CS}	−1, 2	170				See Figure 1	ns min
Data Access Time	t _{DA}	−1, 2	0				See Figure 1	ns min
Data Setup Time	t _{DS}	−1, 2	150				See Figure 1	ns min
Data Hold Time	t _{DH}	−1, 2	5				See Figure 1	ns min

NOTES

¹T_A = +25°C and ±V_S = ±15V, V_{REFIN} = +10V.

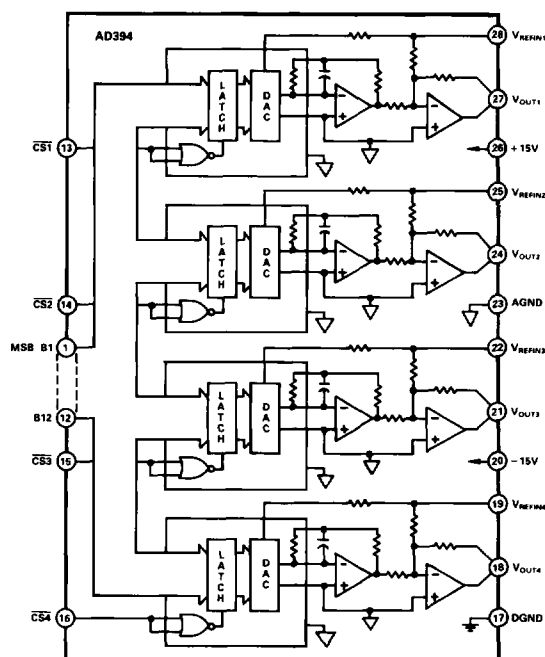
²The AD394 can be used with supplies as low as ±11.4V. See page 6, Figure 10 of product data sheet.

³FSR means Full-Scale Range and is equal to 20V for a ±10V bipolar range and 10V for 0 to 10V unipolar range.

⁴Monotonicity is tested for over the full military temperature.

⁵Integral nonlinearity is a measure of the maximum deviation from a straight line passing through the end points of the transfer function.

3.2.1 Functional Block Diagram and Terminal Assignments.



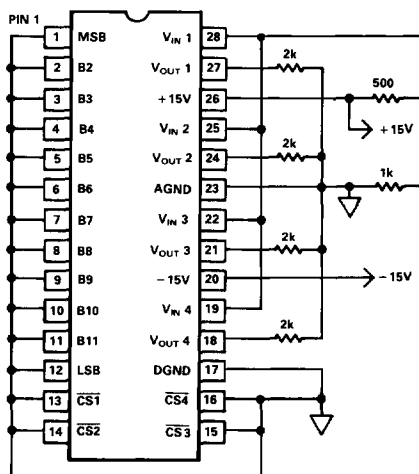
AD394 Functional Block Diagram

3.2.4 Microcircuit Technology Group.

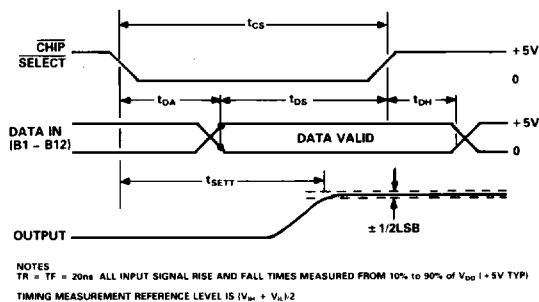
This microcircuit is covered by technology group (I).

4.2.1 Life Test/Burn-In Circuit.

Steady state life test is per MIL-STD-883 Method 1005. Burn-in is per MIL-STD-883 Method 1015 test condition (B).



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WRITE MODE
 $\overline{CS}$ LOW, DAC RESPONDS TO
 DATA BUS (db0-db11) INPUTS

HOLD MODE MODE SELECTION
 $\overline{CS}$ HIGH, DATA BUS (db0-db11) IS
 LOCKED OUT, DAC HOLDS LAST DATA
 PRESENT WHEN $\overline{CS}$ ASSUMED
 HIGH STATE

Figure 1. Timing Diagram

Table 2. DAC Select Matrix

$\overline{CS1}$	$\overline{CS2}$	$\overline{CS3}$	$\overline{CS4}$	Operation
1	1	1	1	All DACs Latched
0	1	1	1	Load DAC 1 From Data Bus
1	0	1	1	Load DAC 2 From Data Bus
1	1	0	1	Load DAC 3 From Data Bus
1	1	1	0	Load DAC 4 From Data Bus
0	0	0	0	All DACs Simultaneously Loaded

Table 3. AD394 Bipolar Code Table

DATA INPUT	ANALOG OUTPUT	ANALOG OUTPUT VOLTAGE $V_{REFIN} = +10$ VOLTS
1111 1111 1111	$+1 \cdot (V_{REFIN}) \left\{ \frac{2047}{2048} \right\}$	+9.9951V + FULL SCALE - 1LSB
1100 0000 0000	$+1 \cdot (V_{REFIN}) \left\{ \frac{1024}{2048} \right\}$	+5.000V + 1/2 SCALE
1000 0000 0001	$+1 \cdot (V_{REFIN}) \left\{ \frac{1}{2048} \right\}$	+4.88mV + 1LSB
1000 0000 0000	$+1 \cdot (V_{REFIN}) \left\{ \frac{0}{2048} \right\}$	+0.000V ZERO
0111 1111 1111	$-1 \cdot (V_{REFIN}) \left\{ \frac{1}{2048} \right\}$	-4.88mV - 1LSB
0100 0000 0000	$-1 \cdot (V_{REFIN}) \left\{ \frac{1024}{2048} \right\}$	-5.000V - 1/2 SCALE
0000 0000 0000	$-1 \cdot (V_{REFIN}) \left\{ \frac{2048}{2048} \right\}$	-10.000V - FULL SCALE