

# TFA9891

## 9.5 V boosted audio system with adaptive sound maximizer and speaker protection

Rev. 1 — 21 December 2016

Product short data sheet

### 1. General description

---

The TFA9891 is a high efficiency class-D audio amplifier with a sophisticated speaker boost and protection algorithm. It can deliver 7.2 W peak output power to an 8  $\Omega$  speaker, at a supply voltage of 3.6 V. The internal boost converter raises the supply voltage to 9.5 V, providing ample headroom for major improvements in sound quality.

A safe working environment is provided for the speaker under all operating conditions. The TFA9891 maximizes acoustic output while ensuring that the diaphragm displacement and voice coil temperature do not exceed their rated limits. This function is based on a speaker box model that operates in all loudspeaker environments (e.g. free air, closed box or vented box). Furthermore, advanced signal processing ensures that the quality of the audio signal is never degraded by unwanted clipping or distortion in the amplifier or speaker. An integrated Dynamic Range Compressor (DRC) allows the speaker to operate at the highest possible power rating without suffering physical damage.

Unlike competing solutions, the adaptive sound maximizer algorithm uses feedback to calculate both the temperature and the excursion. It allows the TFA9891 to adapt to changes in the acoustic environment.

Internal intelligent DC-to-DC conversion boosts the supply rail to provide additional headroom and power output. The supply voltage is only raised when necessary. It maximizes the output power of the class-D audio amplifier while limiting quiescent power consumption.

The TFA9891 also incorporates advanced battery protection. By limiting the supply current when the battery voltage is low, it prevents the audio system from drawing excessive load currents from the battery. Drawing excessive load currents from the battery could cause a system undervoltage. The advanced processor minimizes the impact of a falling battery voltage on the audio quality, by preventing distortion as the battery discharges.

The device features low RF susceptibility because it has a digital input interface that is insensitive to clock jitter. The second order closed loop architecture used in a class-D audio amplifier provides excellent audio performance and high supply voltage ripple rejection. The audio input interface is I<sup>2</sup>S and the control settings are communicated via an I<sup>2</sup>C-bus interface.

The device also provides the speaker with robust protection against ESD damage. In a typical application, no additional components are required to withstand a 15 kV discharge on the speaker.

The TFA9891 is available in a 49-bump WLCSP (Wafer Level Chip-Size Package) with a 400  $\mu$ m pitch.



## 2. Features and benefits

- Sophisticated speaker-boost and protection algorithm that maximizes speaker performance while protecting the speaker:
  - ◆ Fully embedded software, no additional license fee or porting required
  - ◆ Total integrated solution that includes DSP, amplifier, DC-to-DC, sensing and more
- Adaptive excursion control which guarantees that the speaker membrane excursion never exceeds its rated limit
- Multiband Dynamic Range Compressor (DRC) allows independent control of up to three frequency bands
- Audio enhancement
- Real-time temperature protection - direct measurement ensures that voice coil temperature never exceeds its rated limit
- Environmentally aware - automatically adapts speaker parameters to acoustic and thermal changes including compensation for speaker box leakage
- Output power: 3.6 W (RMS) into 8  $\Omega$  at 3.6 V supply voltage (THD = 1 %)
- Clip avoidance - DSP algorithm prevents clipping even with sagging supply voltage
- Bandwidth extension option to increase low frequency response
- Compatible with standard acoustic echo canceler (s)
- High efficiency and low-power dissipation
- Wide supply voltage range (fully operational from 2.7 V to 5.5 V)
- Two I<sup>2</sup>S inputs to support two audio sources or one Pulse Density Modulation (PDM) input
- A third I<sup>2</sup>S input dedicated to inter-chip communications
- I<sup>2</sup>C-bus control interface (400 kHz)
- Speaker current and voltage monitoring (via the I<sup>2</sup>S-bus or PDM output) for Acoustic Echo Cancellation (AEC) at the host
- Fully short-circuit proof across the load and to the supply lines
- Sample frequencies from 8 kHz to 48 kHz supported in I<sup>2</sup>S mode and 16 kHz to 48 kHz in PDM mode
- 3-bit clock/word select ratios supported (32x, 48x, and 64x) in I<sup>2</sup>S mode
- Bit clock speed from 2.048 MHz up to 6.144 MHz in PDM mode
- Option to route I<sup>2</sup>S input directly to I<sup>2</sup>S output allowing a second I<sup>2</sup>S output slave device to be used in combination with TFA9891
- TDM interface supported (with limited functionality)
- Volume control
- Low RF susceptibility
- Input clock jitter insensitive interface
- Thermally protected
- 15 kV system-level ESD protection without external components

### 3. Applications

- Mobile phones, Tablets
- Portable Navigation Devices (PND)
- Notebooks/netbooks
- MP3 players and portable media players
- Small audio systems

### 4. Quick reference data

Table 1. Quick reference data

| Symbol              | Parameter              | Conditions                                                                                                                                                                              | Min  | Typ | Max  | Unit |
|---------------------|------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------|-----|------|------|
| V <sub>BAT</sub>    | battery supply voltage | on pin VBAT                                                                                                                                                                             | 2.7  | -   | 5.5  | V    |
| V <sub>DDD</sub>    | digital supply voltage | on pin VDDD                                                                                                                                                                             | 1.65 | 1.8 | 1.95 | V    |
| I <sub>BAT</sub>    | battery supply current | on pin VBAT and in DC-to-DC converter coil; operating modes with load; DC-to-DC converter in adaptive boost mode (no output signal, V <sub>BAT</sub> = 3.6 V, V <sub>DDD</sub> = 1.8 V) | -    | 4   | -    | mA   |
|                     |                        | power-down mode                                                                                                                                                                         | -    | 1   | -    | μA   |
| I <sub>DDD</sub>    | digital supply current | on pin VDDD; operating modes; speaker boost protection activated                                                                                                                        | -    | 20  | -    | mA   |
|                     |                        | on pin VDDD; operating modes; CoolFlux DSP bypassed                                                                                                                                     | -    | 7   | -    | mA   |
|                     |                        | on pin VDDD; power-down mode; BCK1 = WS1 = DATA1 = BCK2 = WS2 = DATA2 = DATA3 = 0 V                                                                                                     | -    | 10  | -    | μA   |
| P <sub>0(RMS)</sub> | RMS output power       | THD+N = 1 %; CLIP = 0                                                                                                                                                                   |      |     |      |      |
|                     |                        | R <sub>L</sub> = 8 Ω; f <sub>s</sub> = 48 kHz                                                                                                                                           | -    | 3.6 | -    | W    |
|                     |                        | R <sub>L</sub> = 8 Ω; f <sub>s</sub> = 32 kHz                                                                                                                                           | -    | 3.7 | -    | W    |

### 5. Ordering information

Table 2. Ordering information

| Type number | Package |                                                                                             |         |
|-------------|---------|---------------------------------------------------------------------------------------------|---------|
|             | Name    | Description                                                                                 | Version |
| TFA9891UK   | WLCSP49 | wafer level chip-scale package; 49 bumps; 3.43 × 2.98 × 0.56 mm (backside coating included) | TFA9891 |

6. Block diagram

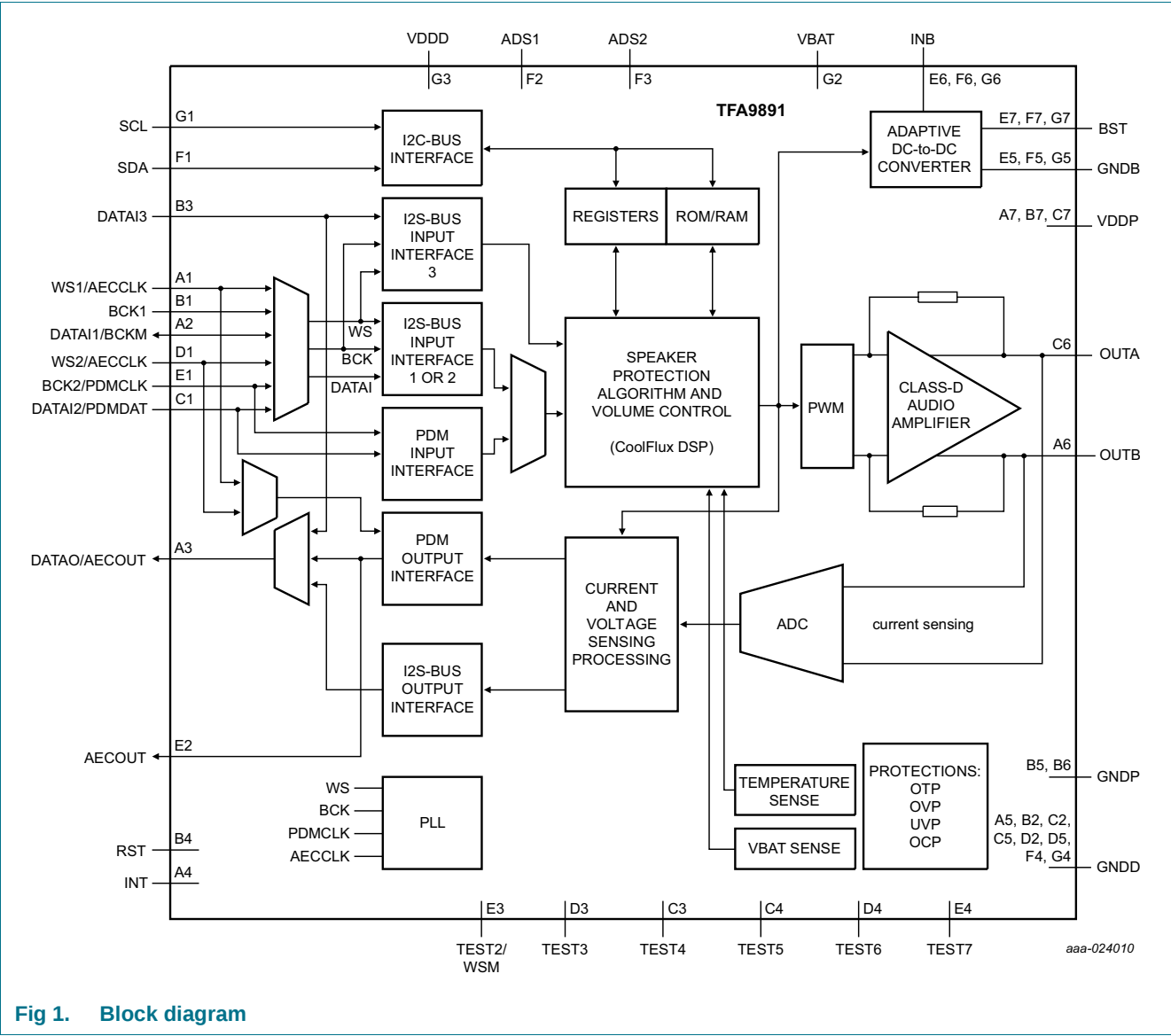
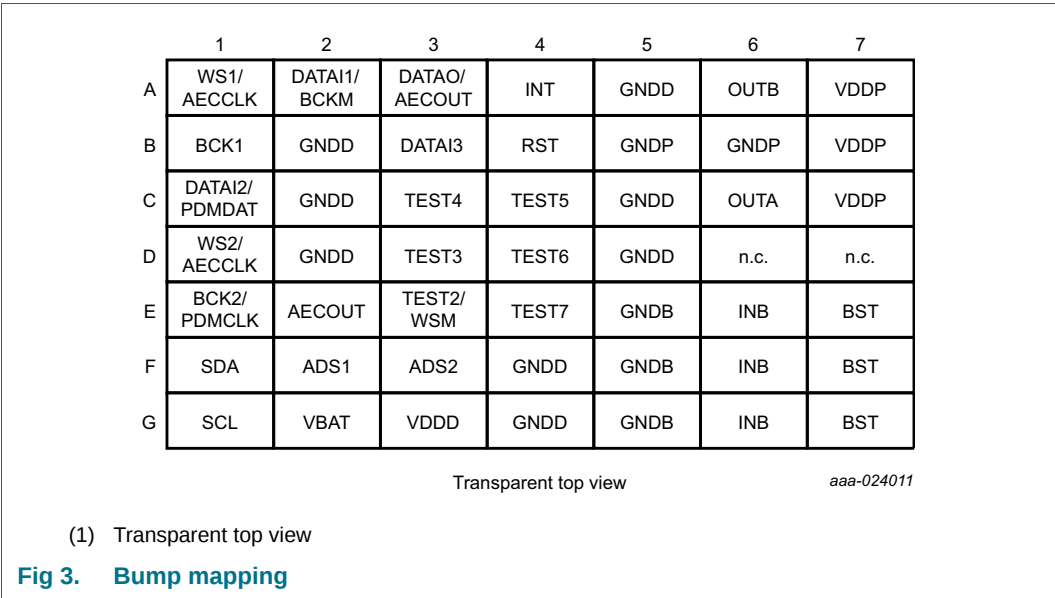
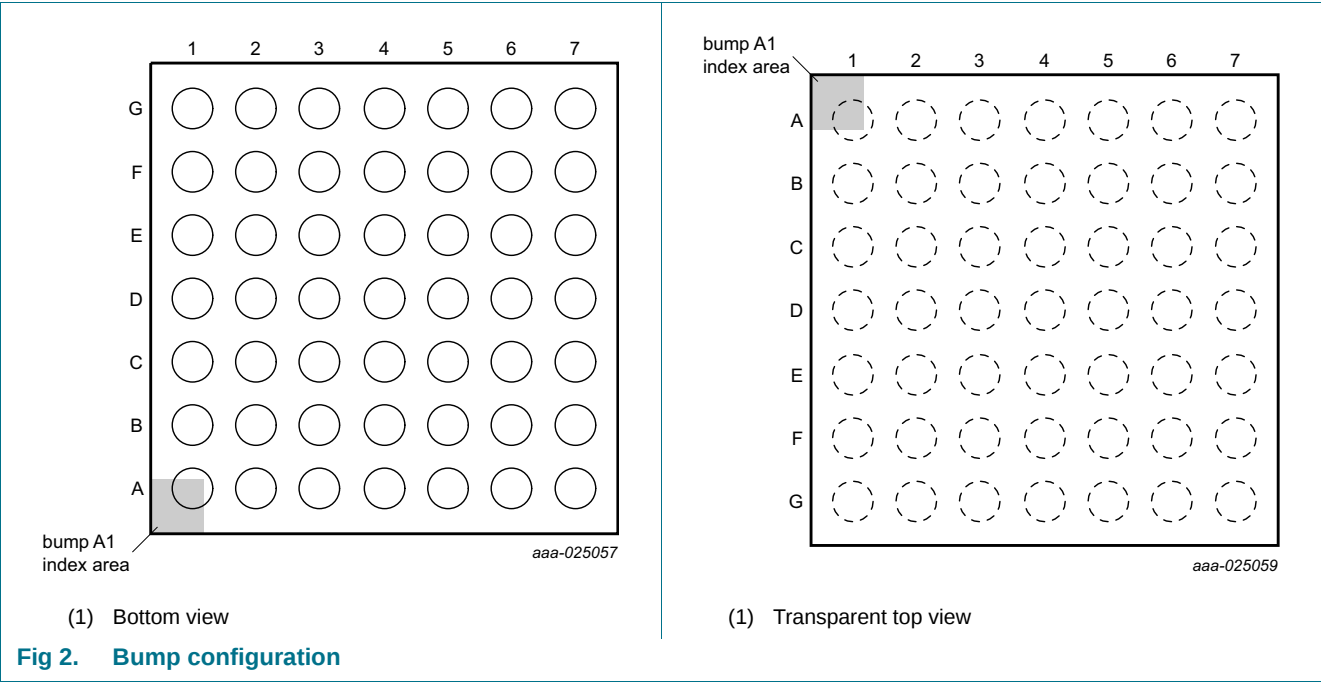


Fig 1. Block diagram

7. Pinning information

7.1 Pinning



## 7.2 Pin description

Table 3. Pin description

| Symbol        | Pin | Type | Description                                                                                                                                                             |
|---------------|-----|------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| WS1/AECCLK    | A1  | I    | I <sup>2</sup> S mode: Digital audio word select input 1 for I <sup>2</sup> S interface 1<br>PDM mode: PDM input clock used for AEC reference output (in mono)          |
| DATAI1/BCKM   | A2  | I/O  | I <sup>2</sup> S mode: Digital audio data input 1 for I <sup>2</sup> S interface 1<br>PDM mode: Master I <sup>2</sup> S audio bit clock output for stereo gain exchange |
| DATAO/AECOUT  | A3  | O    | I <sup>2</sup> S mode: Digital audio data output<br>PDM mode mono: AEC PDM output<br>PDM mode stereo: Gain exchange between 2x devices                                  |
| INT           | A4  | O    | interrupt output                                                                                                                                                        |
| GNDD          | A5  | P    | digital ground                                                                                                                                                          |
| OUTB          | A6  | O    | inverting output                                                                                                                                                        |
| VDDP          | A7  | P    | power supply voltage                                                                                                                                                    |
| BCK1          | B1  | I    | digital audio bit clock input 1 for I <sup>2</sup> S interface 1                                                                                                        |
| GNDD          | B2  | P    | digital ground                                                                                                                                                          |
| DATAI3        | B3  | I    | digital audio data input 3 for I <sup>2</sup> S interface 3                                                                                                             |
| RST           | B4  | I    | reset input                                                                                                                                                             |
| GNDD          | B5  | P    | power ground                                                                                                                                                            |
| GNDD          | B6  | P    | power ground                                                                                                                                                            |
| VDDP          | B7  | P    | power supply voltage                                                                                                                                                    |
| DATAI2/PDMDAT | C1  | I    | I <sup>2</sup> S mode: Digital audio data input 2 for I <sup>2</sup> S interface 2<br>PDM mode: PDM audio data stream input                                             |
| GNDD          | C2  | P    | digital ground                                                                                                                                                          |
| TEST4         | C3  | O    | test signal input 4; for test purposes only, connect to PCB ground                                                                                                      |
| TEST5         | C4  | O    | test signal input 5; for test purposes only, connect to PCB ground                                                                                                      |
| GNDD          | C5  | P    | digital ground                                                                                                                                                          |
| OUTA          | C6  | O    | non-inverting output                                                                                                                                                    |
| VDDP          | C7  | P    | power supply voltage                                                                                                                                                    |
| WS2/AECCLK    | D1  | I    | I <sup>2</sup> S mode: Digital audio word select input 2 for I <sup>2</sup> S interface 2<br>PDM mode: PDM input clock used for AEC reference output (in stereo)        |
| GNDD          | D2  | P    | digital ground                                                                                                                                                          |
| TEST3         | D3  | O    | test signal input 3; for test purposes only, connect to PCB ground                                                                                                      |
| TEST6         | D4  | O    | test signal input 6; for test purposes only, connect to PCB ground                                                                                                      |
| GNDD          | D5  | P    | digital ground                                                                                                                                                          |
| n.c.          | D6  | -    | not connected <sup>[1]</sup>                                                                                                                                            |
| n.c.          | D7  | -    | not connected <sup>[1]</sup>                                                                                                                                            |

## 9.5 V boosted audio system with adaptive sound maximizer and speaker protection

Table 3. Pin description ...continued

| Symbol      | Pin | Type | Description                                                                                                                                                |
|-------------|-----|------|------------------------------------------------------------------------------------------------------------------------------------------------------------|
| BCK2/PDMCLK | E1  | I    | I <sup>2</sup> S mode: Digital audio bit clock input 2 for I <sup>2</sup> S interface 2<br>PDM mode: PDM clock input for audio data stream                 |
| AECOUT      | E2  | O    | PDM stereo: AEC PDM output<br>I <sup>2</sup> S mode or PDM mono mode: Pin is tristated internally; must be tied to GNDD externally                         |
| TEST2/WSM   | E3  | O    | I <sup>2</sup> S mode: Test signal input 2; connect to PCB ground<br>PDM mode: Master audio word select output for stereo gain exchange between 2x devices |
| TEST7       | E4  | O    | test signal input 7; for test purposes only, connect to PCB ground                                                                                         |
| GNDB        | E5  | P    | boosted ground                                                                                                                                             |
| INB         | E6  | P    | DC-to-DC boost converter input                                                                                                                             |
| BST         | E7  | O    | boosted supply voltage output                                                                                                                              |
| SDA         | F1  | I/O  | I <sup>2</sup> C-bus data input/output                                                                                                                     |
| ADS1        | F2  | I    | address select input 1                                                                                                                                     |
| ADS2        | F3  | I    | address select input 2                                                                                                                                     |
| GNDD        | F4  | P    | digital ground                                                                                                                                             |
| GNDB        | F5  | P    | boosted ground                                                                                                                                             |
| INB         | F6  | P    | DC-to-DC boost converter input                                                                                                                             |
| BST         | F7  | O    | boosted supply voltage output                                                                                                                              |
| SCL         | G1  | I    | I <sup>2</sup> C-bus clock input                                                                                                                           |
| VBAT        | G2  | P    | battery supply voltage sense input                                                                                                                         |
| VDDD        | G3  | P    | digital supply voltage                                                                                                                                     |
| GNDD        | G4  | P    | digital ground                                                                                                                                             |
| GNDB        | G5  | P    | boosted ground                                                                                                                                             |
| INB         | G6  | P    | DC-to-DC boost converter input                                                                                                                             |
| BST         | G7  | O    | boosted supply voltage output                                                                                                                              |

[1] Can be used to simplify routing to pin OUTA (see [Table 3](#)).

## 8. Functional description

The TFA9891 is a highly efficient mono Bridge Tied Load (BTL) class-D audio amplifier with a sophisticated SpeakerBoost protection algorithm. [Figure 1](#) is a block diagram of the TFA9891.

In I2S mode, TFA9891 contains three I2S data inputs and one I2S data output. Two of the I2S inputs, DATAI1 and DATAI2, can be selected as the audio input stream. The third I2S input, DATAI3, is provided to support stereo applications. The selected WS/BCK signal is used to internally clock DATAI3 (at the output of the MUX controlled by ISEL; see [Figure 1](#)).

A 'pass-through' option allows one of the I2S input interfaces to be connected directly to the I2S output. It allows I2S output slave device such as codec connected in parallel with TFA9891 to be routed directly to the audio host via I2S output.

In PDM mode, the TFA9891 features one PDM input interface for audio stream and one PDM output interface to provide AEC voltage or current reference. It also has one I2S input (DATAI3) and one I2S output interface (DATAO). In this mode, the I2S input/output interfaces are dedicated to communication between two devices for gain and synchronization on stereo platforms.

Regardless of active mode (I2S or PDM), the I2S output signal on DATAO can be configured to transmit DSP output signal, amplifier output current information, DATAI3 left or right signal information (bypass) or amplifier gain information. The gain information can be used to facilitate communication between two devices in stereo applications.

A SpeakerBoost protection algorithm, running on a CoolFlux Digital Signal Processor (DSP) core maximizes the acoustical output of the speaker. The algorithm also limits membrane excursion and voice coil temperature to a safe level. The mechanical protection implemented guarantees that the speaker membrane excursion never exceeds its rated limit, to accuracy of 10 %. Thermal protection guarantees that the voice coil temperature never exceeds its rated limit, to accuracy of  $\pm 10$  °C. Furthermore, advanced signal processing ensures that the audio quality remains acceptable always.

The protection algorithm implements an adaptive loudspeaker model that is used to predict the extent of membrane excursion. The model is continuously updated to ensure that the protection scheme remains effective even when speaker parameter values change or the acoustic enclosure is modified.

Output sound pressure levels are boosted within given mechanical, thermal and quality limits. An optional bandwidth extension mode extends the low frequency response up to a predefined limit before maximizing the output level. This mode is suitable for listening to high-quality music in quiet environments.

The frequency response of the TFA9891 can be modified via ten fully programmable cascaded second-order biquad filters. The first two biquads are processed with 48-bit double precision; biquads 3 to 8 are processed with 24-bit single precision.

At low battery voltage levels, the gain is automatically reduced to limit battery current. The SpeakerBoost protection algorithm or the host application (external) controls the output volume. In the latter case, the boost features of the SpeakerBoost protection algorithm must be disabled to avoid neutralizing external volume control.

---

**9.5 V boosted audio system with adaptive sound maximizer and speaker protection**

The SpeakerBoost protection algorithm output is converted into two pulse width modulated (PWM) signals which are injected into the class-D audio amplifier. The 3-level PWM scheme supports filterless speaker drive.

An adaptive DC-to-DC converter boosts the battery supply voltage in line with the output of the SpeakerBoost protection algorithm. It switches to follower mode ( $V_{bst} = V_{BAT}$ ; no boost) when the audio output voltage is lower than the battery voltage.

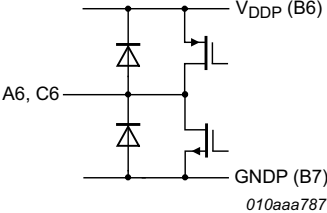
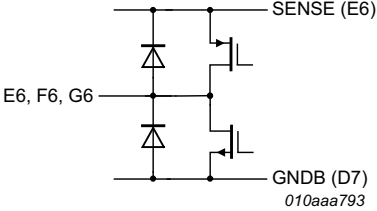
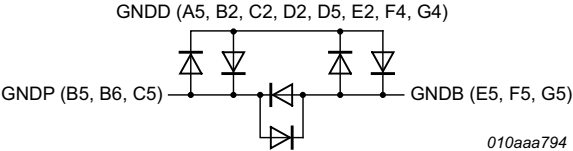
## 9. Internal circuitry

Table 4. Internal circuitry

| Pin                        | Symbol                                      | Equivalent circuit |
|----------------------------|---------------------------------------------|--------------------|
| C1, C4, D1, D3, E1, F2, F3 | DATAI2, TEST5, WS2, TEST3, BCK2, ADS1, ADS2 |                    |
| A1, A2, A4, B1, B3, E3, G1 | WS1, DATAI1, INT, BCK1, DATAI3, TEST2, SCL, |                    |
| C3                         | TEST4                                       |                    |
| F1                         | SDA                                         |                    |
| A3, E2                     | DATAO, AECOUT                               |                    |

9.5 V boosted audio system with adaptive sound maximizer and speaker protection

Table 4. Internal circuitry ...continued

| Pin                                                | Symbol           | Equivalent circuit                                                                  |
|----------------------------------------------------|------------------|-------------------------------------------------------------------------------------|
| A6, C6                                             | OUTB, OUTA       |   |
| E6, F6, G6                                         | i.c.             |   |
| A5, B2, B5, B6, C2, C5, D2, D5, E5, F4, F5, G4, G5 | GNDD, GNDB, GNDD |  |

## 10. I<sup>2</sup>C-bus interface and register settings

The TFA9891 supports the 400 kHz I<sup>2</sup>C-bus microcontroller interface mode standard. The I<sup>2</sup>C-bus is used to control the TFA9891 and to transmit and receive data. The TFA9891 can only operate in I<sup>2</sup>C slave mode, as a slave receiver or as a slave transmitter.

### 10.1 TFA9891 addressing

The TFA9891 is accessed via an 8-bit code; see [Table 5](#). Bits 1 to 7 contain the device address. Bit 0 (R/W) indicates whether a read (1) or a write (0) operation has been requested. Four separate addresses are supported for stereo applications. Address selection is via pins ADS1 and ADS2. The levels on pins ADS1 and ADS2 determine the values of bits 1 and 2, respectively, of the device address, as detailed in [Table 5](#). The generic address is independent of pins ADS1 and ADS2.

**Table 5.** Address selection via pins ADS1 and ADS2

| ADS2 pin voltage (V) | ADS1 pin voltage (V) | Address                    | Function       |
|----------------------|----------------------|----------------------------|----------------|
| 0                    | 0                    | 01101000                   | for write mode |
|                      |                      | 01101001                   | for read mode  |
| 0                    | V <sub>DDD</sub>     | 01101010                   | for write mode |
|                      |                      | 01101011                   | for read mode  |
| V <sub>DDD</sub>     | 0                    | 01101100                   | for write mode |
|                      |                      | 01101101                   | for read mode  |
| V <sub>DDD</sub>     | V <sub>DDD</sub>     | 01101110                   | for write mode |
|                      |                      | 01101111                   | for read mode  |
| don't care           | don't care           | 00011100 (generic address) | for write mode |
| don't care           | don't care           | 00011101 (generic address) | for read mode  |

### 10.2 I<sup>2</sup>C-bus write cycle

The sequence of events that is followed when writing data to the I<sup>2</sup>C-bus registers of TFA9891 is specified in [Table 6](#). 1 byte is transmitted at a time. Each register stores 2 bytes of data. Data is always written in byte pairs. Data transfer is always MSB first.

The write cycle sequence using SDA is as follows:

- The microcontroller asserts a start condition (S).
- The microcontroller transmits the 7-bit device address of the TFA9891, followed by the R/W bit set to 0.
- The TFA9891 asserts an acknowledge (A).
- The microcontroller transmits the 8-bit TFA9891 register address to which the first data byte is written.
- The TFA9891 asserts an acknowledge.
- The microcontroller transmits the first byte (the most significant byte).
- The TFA9891 asserts an acknowledge.
- The microcontroller transmits the second byte (the least significant byte).
- The TFA9891 asserts an acknowledge.

## 9.5 V boosted audio system with adaptive sound maximizer and speaker protection

- The microcontroller can either assert the stop condition (P) or continue transmitting data by sending another pair of data bytes, repeating the sequence from step 6. In the latter case, the targeted register address has been auto-incremented by the TFA9891.

Table 6. I<sup>2</sup>C-bus write cycle

| Start | TFA9891 address                    | R/W | ACK <sup>[1]</sup> | TFA9891 first register address | ACK <sup>[1]</sup> | MSB | ACK <sup>[1]</sup> | LSB | ACK <sup>[1]</sup> | More data... | Stop |
|-------|------------------------------------|-----|--------------------|--------------------------------|--------------------|-----|--------------------|-----|--------------------|--------------|------|
| S     | 01101A <sub>2</sub> A <sub>1</sub> | 0   | A                  | ADDR                           | A                  | MS1 | A                  | LS1 | A                  | <....>       | P    |

[1] ACK stands for acknowledge.

10.3 I<sup>2</sup>C-bus read cycle

The sequence of events that is followed when reading data from the I<sup>2</sup>C-bus registers of TFA9891 is specified in Table 7. 1 byte is transmitted at a time. Each of the registers stores 2 bytes of data. Data is always written in byte pairs. Data transfer is always MSB first.

The read cycle sequence using SDA is as follows:

- The microcontroller asserts a start condition (S)
- The microcontroller transmits the 7-bit device address of the TFA9891, followed by the R/W bit set to 0
- The TFA9891 asserts an acknowledge (A)
- The microcontroller transmits the 8 bit TFA9891 register address from which the first data byte is read
- The TFA9891 asserts an acknowledge
- The microcontroller asserts a repeated start (Sr)
- The microcontroller retransmits the device address followed by the R/W bit set to 1
- The TFA9891 asserts an acknowledge
- The TFA9891 transmits the first byte (the MSB)
- The microcontroller asserts an acknowledge
- The TFA9891 transmits the second byte (the LSB)
- The microcontroller asserts either an acknowledge or a negative acknowledge (NA)
  - If the microcontroller asserts an acknowledge, TFA9891 auto increments the target register address and steps 9 to 12 are repeated
  - If the microcontroller asserts a negative acknowledge, the TFA9891 frees the I<sup>2</sup>C-bus and the microcontroller generates a stop condition (P)

Table 7. I<sup>2</sup>C-bus read cycle

| Start | TFA9891 address                    | R/W | ACK | First register address | ACK | Repeated start | TFA9891 address                    | R/W | ACK | MSB | ACK | LSB | ACK | More data... | ACK | Stop |
|-------|------------------------------------|-----|-----|------------------------|-----|----------------|------------------------------------|-----|-----|-----|-----|-----|-----|--------------|-----|------|
| S     | 01101A <sub>2</sub> A <sub>1</sub> | 0   | A   | ADDR                   | A   | Sr             | 11011A <sub>2</sub> A <sub>1</sub> | 1   | A   | MS1 | A   | LS1 | A   | <....>       | NA  | P    |

## 11. Limiting values

**Table 8. Limiting values**

*In accordance with the Absolute Maximum Rating System (IEC 60134).*

| Symbol           | Parameter                       | Conditions                              | Min  | Max   | Unit |
|------------------|---------------------------------|-----------------------------------------|------|-------|------|
| V <sub>BAT</sub> | battery supply voltage          | on pin VBAT                             | −0.3 | +5.5  | V    |
| V <sub>bst</sub> | boost voltage                   | on pin BST                              | −0.3 | +11   | V    |
| V <sub>INB</sub> | voltage on pin INB              | on pin INB                              | −0.3 | +11   | V    |
| V <sub>DDP</sub> | power supply voltage            | on pin VDDP                             | −0.3 | +11   | V    |
| V <sub>DDD</sub> | digital supply voltage          | on pin VDDD                             | −0.3 | +1.95 | V    |
| T <sub>j</sub>   | junction temperature            |                                         | -    | +150  | °C   |
| T <sub>stg</sub> | storage temperature             |                                         | −55  | +150  | °C   |
| T <sub>amb</sub> | ambient temperature             |                                         | −40  | +85   | °C   |
| V <sub>ESD</sub> | electrostatic discharge voltage | according to Human Body Model (HBM)     | −2   | +2    | kV   |
|                  |                                 | according to Charged Device Model (CDM) | −500 | +500  | V    |
| Amplifier output |                                 |                                         |      |       |      |
| V <sub>O</sub>   | output voltage                  | on pin OUTA and pin OUTB                | −0.3 | +11   | V    |

## 12. Thermal characteristics

**Table 9. Thermal characteristics**

| Symbol               | Parameter                                   | Conditions                   | Typ | Max | Unit |
|----------------------|---------------------------------------------|------------------------------|-----|-----|------|
| R <sub>th(j-a)</sub> | thermal resistance from junction to ambient | four layer application board | 40  | 60  | K/W  |

## 13. Characteristics

### 13.1 I<sup>2</sup>C timing characteristics

**Table 10. I<sup>2</sup>C-bus interface characteristics; see Figure 4**

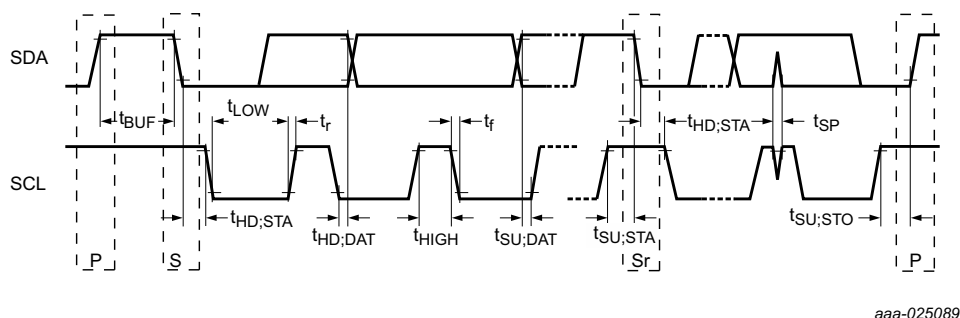
All parameters are guaranteed for  $V_{BAT} = 3.6\text{ V}$ ;  $V_{DDD} = 1.8\text{ V}$ ;  $V_{DDP} = V_{bst} = 9.5\text{ V}$ , adaptive boost mode;  $L_{BST} = 1\text{ }\mu\text{H}$ ;  $R_L = 8\text{ }\Omega$ ;  $L_L = 40\text{ }\mu\text{H}$ ;  $f_i = 1\text{ kHz}$ ;  $f_s = 48\text{ kHz}$ ;  $T_{amb} = 25\text{ }^\circ\text{C}$ ; default settings, unless otherwise specified.

| Symbol       | Parameter                                                         | Conditions              | Min            | Typ | Max | Unit          |
|--------------|-------------------------------------------------------------------|-------------------------|----------------|-----|-----|---------------|
| $f_{SCL}$    | SCL clock frequency                                               |                         | -              | -   | 400 | kHz           |
| $t_{LOW}$    | LOW period of the SCL clock                                       |                         | 1.3            | -   | -   | $\mu\text{s}$ |
| $t_{HIGH}$   | HIGH period of the SCL clock                                      |                         | 0.6            | -   | -   | $\mu\text{s}$ |
| $t_r$        | rise time                                                         | SDA and SCL signals [2] | $20 + 0.1 C_b$ | -   | -   | ns            |
| $t_f$        | fall time                                                         | SDA and SCL signals [2] | $20 + 0.1 C_b$ | -   | -   | ns            |
| $t_{HD;STA}$ | hold time (repeated) START condition                              | [3]                     | 0.6            | -   | -   | $\mu\text{s}$ |
| $t_{SU;STA}$ | set-up time for a repeated START condition                        |                         | 0.6            | -   | -   | $\mu\text{s}$ |
| $t_{SU;STO}$ | set-up time for STOP condition                                    |                         | 0.6            | -   | -   | $\mu\text{s}$ |
| $t_{BUF}$    | bus free time between a STOP and START condition                  |                         | 1.3            | -   | -   | $\mu\text{s}$ |
| $t_{SU;DAT}$ | data set-up time                                                  |                         | 100            | -   | -   | ns            |
| $t_{HD;DAT}$ | data hold time                                                    |                         | 0              | -   | -   | $\mu\text{s}$ |
| $t_{SP}$     | pulse width of spikes that must be suppressed by the input filter |                         | 0              | -   | 50  | ns            |
| $C_b$        | capacitive load for each bus line                                 |                         | -              | -   | 400 | pF            |

[1]  $L_{BST}$  = boost converter inductance;  $R_L$  = load resistance;  $L_L$  = load inductance.

[2]  $C_b$  is the total capacitance of one bus line in pF. The maximum capacitive load for each bus line is 400 pF.

[3] After this period, the first clock pulse is generated.



**Fig 4. I<sup>2</sup>C timing**

13.2 I<sup>2</sup>S timing characteristics

**Table 11.** I<sup>2</sup>S bus interface characteristics; see Figure 5  
All parameters are guaranteed for  $V_{BAT} = 3.6\text{ V}$ ;  $V_{DDD} = 1.8\text{ V}$ ;  $V_{DDP} = V_{bst} = 9.5\text{ V}$ , adaptive boost mode;  $L_{BST} = 1\text{ }\mu\text{H}$ ;  $R_L = 8\text{ }\Omega$ ;  $L_L = 40\text{ }\mu\text{H}$ ;  $f_i = 1\text{ kHz}$ ;  $f_s = 48\text{ kHz}$ ;  $T_{amb} = 25\text{ }^\circ\text{C}$ ; default settings, unless otherwise specified.

| Symbol    | Parameter          | Conditions              | Min             | Typ | Max             | Unit |
|-----------|--------------------|-------------------------|-----------------|-----|-----------------|------|
| $f_s$     | sampling frequency | on pin WS [2]           | 8               | -   | 48              | kHz  |
| $f_{clk}$ | clock frequency    | on pin BCK [2]          | $32 \times f_s$ | -   | $64 \times f_s$ | Hz   |
| $t_{su}$  | set-up time        | WS edge to BCK HIGH [3] | 10              | -   | -               | ns   |
|           |                    | DATA edge to BCK HIGH   | 10              | -   | -               | ns   |
| $t_h$     | hold time          | BCK HIGH to WS edge [3] | 10              | -   | -               | ns   |
|           |                    | BCK HIGH to DATA edge   | 10              | -   | -               | ns   |

- [1]  $L_{BST}$  = boost converter inductance;  $R_L$  = load resistance;  $L_L$  = load inductance.  
[2] The I<sup>2</sup>S bit clock input (BCK) is used as a clock input for the DSP, as well as for the amplifier and the DC-to-DC converter. Both BCK and WS signals should be present for the clock to operate correctly.  
[3] This parameter is not tested during production; design guarantees the value and is checked during product validation.

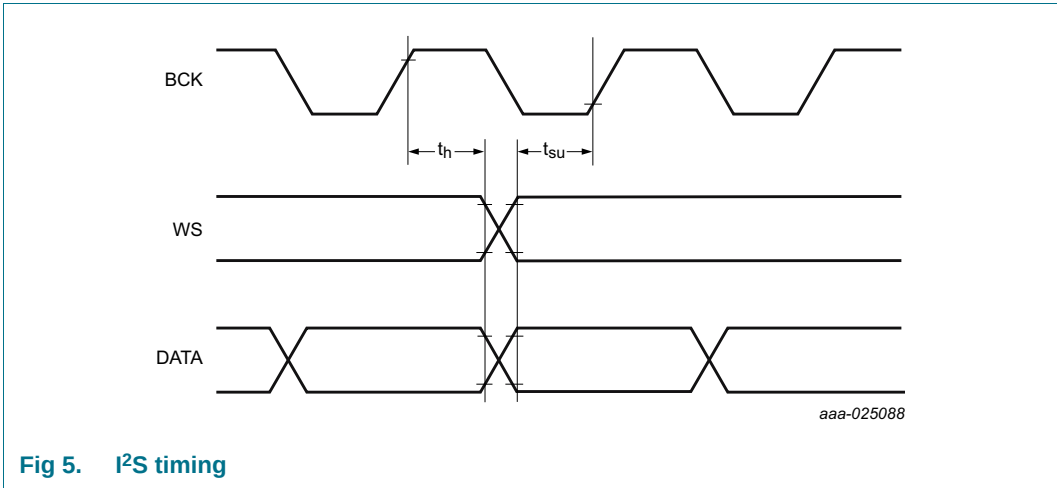


Fig 5. I<sup>2</sup>S timing

14. Package outline

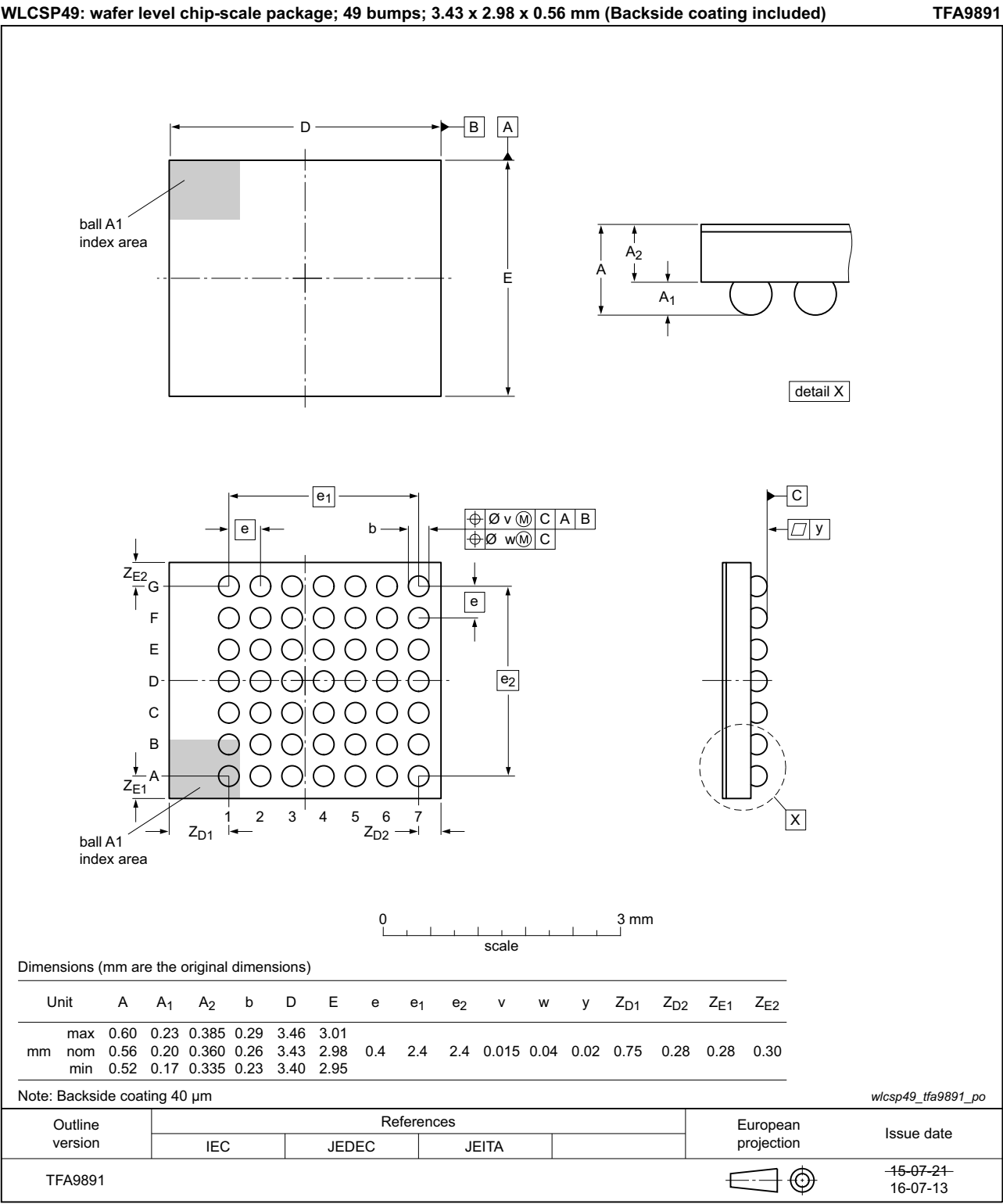


Fig 6. Package outline TFA9891 (WLCSP49)

## 15. Soldering of WLCSP packages

### 15.1 Introduction to soldering WLCSP packages

This text provides a very brief insight into a complex technology. A more in-depth account of soldering WLCSP (Wafer Level Chip-Size Packages) can be found in application note AN10439 "Wafer Level Chip Scale Package" and in application note AN10365 "Surface mount reflow soldering description".

Wave soldering is not suitable for this package.

All NXP WLCSP packages are lead-free.

### 15.2 Board mounting

Board mounting of a WLCSP requires several steps:

1. Solder paste printing on the PCB
2. Component placement with a pick and place machine
3. The reflow soldering itself

### 15.3 Reflow soldering

Key characteristics in reflow soldering are:

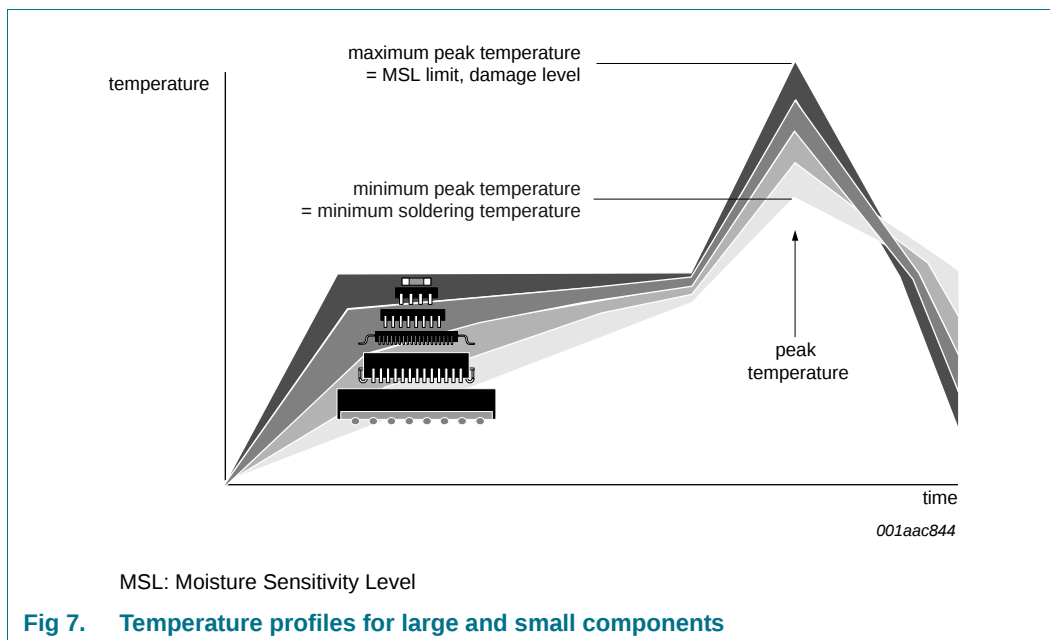
- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see [Figure 7](#)) than a SnPb process, thus reducing the process window
- Solder paste printing issues, such as smearing, release, and adjusting the process window for a mix of large and small components on one board
- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature), and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic) while being low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with [Table 12](#).

**Table 12. Lead-free process (from J-STD-020D)**

| Package thickness (mm) | Package reflow temperature (°C) |             |        |
|------------------------|---------------------------------|-------------|--------|
|                        | Volume (mm <sup>3</sup> )       |             |        |
|                        | < 350                           | 350 to 2000 | > 2000 |
| < 1.6                  | 260                             | 260         | 260    |
| 1.6 to 2.5             | 260                             | 250         | 245    |
| > 2.5                  | 250                             | 245         | 245    |

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see [Figure 7](#).



For further information on temperature profiles, refer to application note AN10365 “Surface mount reflow soldering description”.

### 15.3.1 Stand off

The stand off between the substrate and the chip is determined by:

- The amount of printed solder on the substrate
- The size of the solder land on the substrate
- The bump height on the chip

The higher the stand off, the better the stresses are released due to TEC (Thermal Expansion Coefficient) differences between substrate and chip.

### 15.3.2 Quality of solder joint

A flip-chip joint is considered to be a good joint when the entire solder land has been wetted by the solder from the bump. The surface of the joint should be smooth and the shape symmetrical. The soldered joints on a chip should be uniform. Voids in the bumps after reflow can occur during the reflow process in bumps with high ratio of bump diameter to bump height, i.e. low bumps with large diameter. No failures have been found to be related to these voids. Solder joint inspection after reflow can be done with X-ray to monitor defects such as bridging, open circuits and voids.

### 15.3.3 Rework

In general, rework is not recommended. By rework we mean the process of removing the chip from the substrate and replacing it with a new chip. If a chip is removed from the substrate, most solder balls of the chip will be damaged. In that case it is recommended not to re-use the chip again.

Device removal can be done when the substrate is heated until it is certain that all solder joints are molten. The chip can then be carefully removed from the substrate without damaging the tracks and solder lands on the substrate. Removing the device must be done using plastic tweezers, because metal tweezers can damage the silicon. The surface of the substrate should be carefully cleaned and all solder and flux residues and/or underfill removed. When a new chip is placed on the substrate, use the flux process instead of solder on the solder lands. Apply flux on the bumps at the chip side as well as on the solder pads on the substrate. Place and align the new chip while viewing with a microscope. To reflow the solder, use the solder profile shown in application note AN10365 “Surface mount reflow soldering description”.

#### 15.3.4 Cleaning

Cleaning can be done after reflow soldering.

## 16. Abbreviations

Table 13. Abbreviations

| Acronym | Description                       |
|---------|-----------------------------------|
| AEC     | Acoustic Echo Cancellation        |
| API     | Application Programming Interface |
| DRC     | Dynamic Range Compressor          |
| PLL     | Phased Locked Loop                |
| PND     | Portable Navigation Devices       |
| OSR     | Over Sampling Ration              |
| RPC     | Remote Procedure Call             |
| WLCSP   | Wafer Level Chip-Size Package     |

## 17. Revision history

Table 14. Revision history

| Document ID     | Release date | Data sheet status        | Change notice | Supersedes |
|-----------------|--------------|--------------------------|---------------|------------|
| TFA9891_SDS v.1 | 20161221     | Product short data sheet | -             | -          |

## 18. Legal information

### 18.1 Data sheet status

| Document status <sup>[1][2]</sup> | Product status <sup>[3]</sup> | Definition                                                                            |
|-----------------------------------|-------------------------------|---------------------------------------------------------------------------------------|
| Objective [short] data sheet      | Development                   | This document contains data from the objective specification for product development. |
| Preliminary [short] data sheet    | Qualification                 | This document contains data from the preliminary specification.                       |
| Product [short] data sheet        | Production                    | This document contains the product specification.                                     |

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nxp.com>.

### 18.2 Definitions

**Draft** — The document is a draft version only. The content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included herein and shall have no liability for the consequences of use of such information.

**Short data sheet** — A short data sheet is an extract from a full data sheet with the same product type number(s) and title. A short data sheet is intended for quick reference only and should not be relied upon to contain detailed and full information. For detailed and full information see the relevant full data sheet, which is available on request via the local NXP Semiconductors sales office. In case of any inconsistency or conflict with the short data sheet, the full data sheet shall prevail.

**Product specification** — The information and data provided in a Product data sheet shall define the specification of the product as agreed between NXP Semiconductors and its customer, unless NXP Semiconductors and customer have explicitly agreed otherwise in writing. In no event however, shall an agreement be valid in which the NXP Semiconductors product is deemed to offer functions and qualities beyond those described in the Product data sheet.

### 18.3 Disclaimers

**Limited warranty and liability** — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information. NXP Semiconductors takes no responsibility for the content in this document if provided by an information source outside of NXP Semiconductors.

In no event shall NXP Semiconductors be liable for any indirect, incidental, punitive, special or consequential damages (including - without limitation - lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges) whether or not such damages are based on tort (including negligence), warranty, breach of contract or any other legal theory.

Notwithstanding any damages that customer might incur for any reason whatsoever, NXP Semiconductors' aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the *Terms and conditions of commercial sale* of NXP Semiconductors.

**Short data sheet** — A short data sheet is an extract from a full data sheet with the same product type number(s) and title. A short data sheet is intended for quick reference only and should not be relied upon to contain detailed and full information. For detailed and full information see the relevant full data sheet, which is available on request via the local NXP Semiconductors sales office. In case of any inconsistency or conflict with the short data sheet, the full data sheet shall prevail.

**Suitability for use** — NXP Semiconductors products are not designed, authorized or warranted to be suitable for use in life support, life-critical or safety-critical systems or equipment, nor in applications where failure or malfunction of an NXP Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental damage. NXP Semiconductors and its suppliers accept no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

**Applications** — Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Customers are responsible for the design and operation of their applications and products using NXP Semiconductors products, and NXP Semiconductors accepts no liability for any assistance with applications or customer product design. It is customer's sole responsibility to determine whether the NXP Semiconductors product is suitable and fit for the customer's applications and products planned, as well as for the planned application and use of customer's third party customer(s). Customers should provide appropriate design and operating safeguards to minimize the risks associated with their applications and products.

NXP Semiconductors does not accept any liability related to any default, damage, costs or problem which is based on any weakness or default in the customer's applications or products, or the application or use by customer's third party customer(s). Customer is responsible for doing all necessary testing for the customer's applications and products using NXP Semiconductors products in order to avoid a default of the applications and the products or of the application or use by customer's third party customer(s). NXP does not accept any liability in this respect.

**Limiting values** — Stress above one or more limiting values (as defined in the Absolute Maximum Ratings System of IEC 60134) will cause permanent damage to the device. Limiting values are stress ratings only and (proper) operation of the device at these or any other conditions above those given in the Recommended operating conditions section (if present) or the Characteristics sections of this document is not warranted. Constant or repeated exposure to limiting values will permanently and irreversibly affect the quality and reliability of the device.

**Terms and conditions of commercial sale** — NXP Semiconductors products are sold subject to the general terms and conditions of commercial sale, as published at <http://www.nxp.com/profile/terms>, unless otherwise agreed in a valid written individual agreement. In case an individual agreement is concluded only the terms and conditions of the respective agreement shall apply. NXP Semiconductors hereby expressly objects to applying the customer's general terms and conditions with regard to the purchase of NXP Semiconductors products by customer.

**No offer to sell or license** — Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights.

## 9.5 V boosted audio system with adaptive sound maximizer and speaker protection

**Export control** — This document as well as the item(s) described herein may be subject to export control regulations. Export might require a prior authorization from competent authorities.

**Quick reference data** — The Quick reference data is an extract of the product data given in the Limiting values and Characteristics sections of this document, and as such is not complete, exhaustive or legally binding.

**Non-automotive qualified products** — Unless this data sheet expressly states that this specific NXP Semiconductors product is automotive qualified, the product is not suitable for automotive use. It is neither qualified nor tested in accordance with automotive testing or application requirements. NXP Semiconductors accepts no liability for inclusion and/or use of non-automotive qualified products in automotive equipment or applications.

In the event that customer uses the product for design-in and use in automotive applications to automotive specifications and standards, customer (a) shall use the product without NXP Semiconductors' warranty of the product for such automotive applications, use and specifications, and (b) whenever customer uses the product for automotive applications beyond

NXP Semiconductors' specifications such use shall be solely at customer's own risk, and (c) customer fully indemnifies NXP Semiconductors for any liability, damages or failed product claims resulting from customer design and use of the product for automotive applications beyond NXP Semiconductors' standard warranty and NXP Semiconductors' product specifications.

**Translations** — A non-English (translated) version of a document is for reference only. The English version shall prevail in case of any discrepancy between the translated and English versions.

## 18.4 Trademarks

Notice: All referenced brands, product names, service names and trademarks are the property of their respective owners.

**I<sup>2</sup>C-bus** — logo is a trademark of NXP B.V.

**CoolFlux** — is a trademark of NXP B.V.

**CoolFlux DSP** — is a trademark of NXP B.V.

## 19. Contact information

For more information, please visit: <http://www.nxp.com>

For sales office addresses, please send an email to: [salesaddresses@nxp.com](mailto:salesaddresses@nxp.com)

## 20. Contents

|           |                                                                     |           |
|-----------|---------------------------------------------------------------------|-----------|
| <b>1</b>  | <b>General description</b> . . . . .                                | <b>1</b>  |
| <b>2</b>  | <b>Features and benefits</b> . . . . .                              | <b>2</b>  |
| <b>3</b>  | <b>Applications</b> . . . . .                                       | <b>3</b>  |
| <b>4</b>  | <b>Quick reference data</b> . . . . .                               | <b>3</b>  |
| <b>5</b>  | <b>Ordering information</b> . . . . .                               | <b>3</b>  |
| <b>6</b>  | <b>Block diagram</b> . . . . .                                      | <b>4</b>  |
| <b>7</b>  | <b>Pinning information</b> . . . . .                                | <b>5</b>  |
| 7.1       | Pinning . . . . .                                                   | 5         |
| 7.2       | Pin description . . . . .                                           | 6         |
| <b>8</b>  | <b>Functional description</b> . . . . .                             | <b>8</b>  |
| <b>9</b>  | <b>Internal circuitry</b> . . . . .                                 | <b>10</b> |
| <b>10</b> | <b>I<sup>2</sup>C-bus interface and register settings</b> . . . . . | <b>12</b> |
| 10.1      | TFA9891 addressing . . . . .                                        | 12        |
| 10.2      | I <sup>2</sup> C-bus write cycle . . . . .                          | 12        |
| 10.3      | I <sup>2</sup> C-bus read cycle . . . . .                           | 13        |
| <b>11</b> | <b>Limiting values</b> . . . . .                                    | <b>14</b> |
| <b>12</b> | <b>Thermal characteristics</b> . . . . .                            | <b>14</b> |
| <b>13</b> | <b>Characteristics</b> . . . . .                                    | <b>15</b> |
| 13.1      | I <sup>2</sup> C timing characteristics . . . . .                   | 15        |
| 13.2      | I <sup>2</sup> S timing characteristics . . . . .                   | 16        |
| <b>14</b> | <b>Package outline</b> . . . . .                                    | <b>17</b> |
| <b>15</b> | <b>Soldering of WLCSP packages</b> . . . . .                        | <b>18</b> |
| 15.1      | Introduction to soldering WLCSP packages . . . . .                  | 18        |
| 15.2      | Board mounting . . . . .                                            | 18        |
| 15.3      | Reflow soldering . . . . .                                          | 18        |
| 15.3.1    | Stand off . . . . .                                                 | 19        |
| 15.3.2    | Quality of solder joint . . . . .                                   | 19        |
| 15.3.3    | Rework . . . . .                                                    | 19        |
| 15.3.4    | Cleaning . . . . .                                                  | 20        |
| <b>16</b> | <b>Abbreviations</b> . . . . .                                      | <b>20</b> |
| <b>17</b> | <b>Revision history</b> . . . . .                                   | <b>21</b> |
| <b>18</b> | <b>Legal information</b> . . . . .                                  | <b>22</b> |
| 18.1      | Data sheet status . . . . .                                         | 22        |
| 18.2      | Definitions . . . . .                                               | 22        |
| 18.3      | Disclaimers . . . . .                                               | 22        |
| 18.4      | Trademarks . . . . .                                                | 23        |
| <b>19</b> | <b>Contact information</b> . . . . .                                | <b>23</b> |
| <b>20</b> | <b>Contents</b> . . . . .                                           | <b>24</b> |

Please be aware that important notices concerning this document and the product(s) described herein, have been included in section 'Legal information'.

© NXP Semiconductors N.V. 2016.

All rights reserved.

For more information, please visit: <http://www.nxp.com>

For sales office addresses, please send an email to: [salesaddresses@nxp.com](mailto:salesaddresses@nxp.com)

Date of release: 21 December 2016

Document identifier: TFA9891