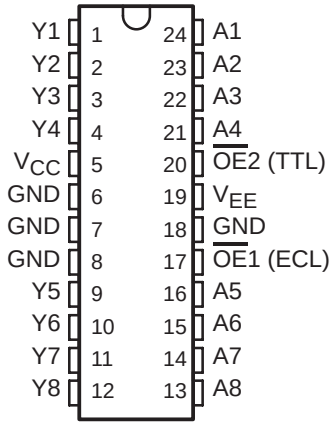
- **100K Compatible**
- **ECL and TTL Control Inputs**
- **Noninverting Outputs**
- **Flow-Through Architecture Optimizes PCB Layout**
- **Center Pin V_{CC}, V_{EE}, and GND Configurations Minimize High-Speed Switching Noise**
- **Package Options Include "Small Outline" Packages and Standard Plastic 300-mil DIPs**

DW OR NT PACKAGE
(T0P VIEW)



description

This octal ECL-to-TTL translator is designed to provide a efficient translation between a 100K ECL signal environment to a TTL signal environment. This device is designed specifically to improve the performance and density of ECL-to-TTL CPU/bus-oriented functions such as memory-address drivers, clock drivers, and bus-oriented receivers and transmitters.

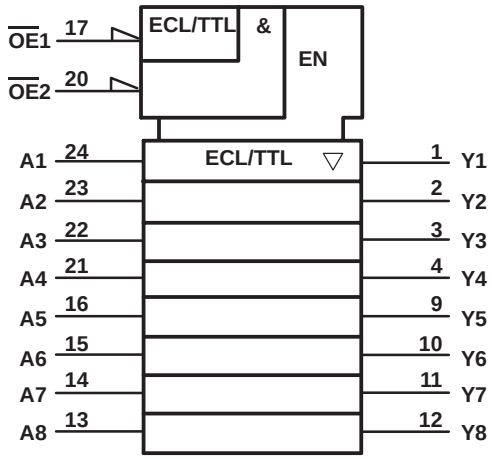
Two output-enable pins, $\overline{OE}1$ and $\overline{OE}2$ are provided. These control inputs are ANDed together with $\overline{OE}1$ being ECL compatible and $\overline{OE}2$ being TTL compatible. This offers the choice of controlling the outputs of the device from either a TTL or ECL signal environment.

The SN100KT5541 is characterized for operation from 0°C to 85°C.

FUNCTION TABLE

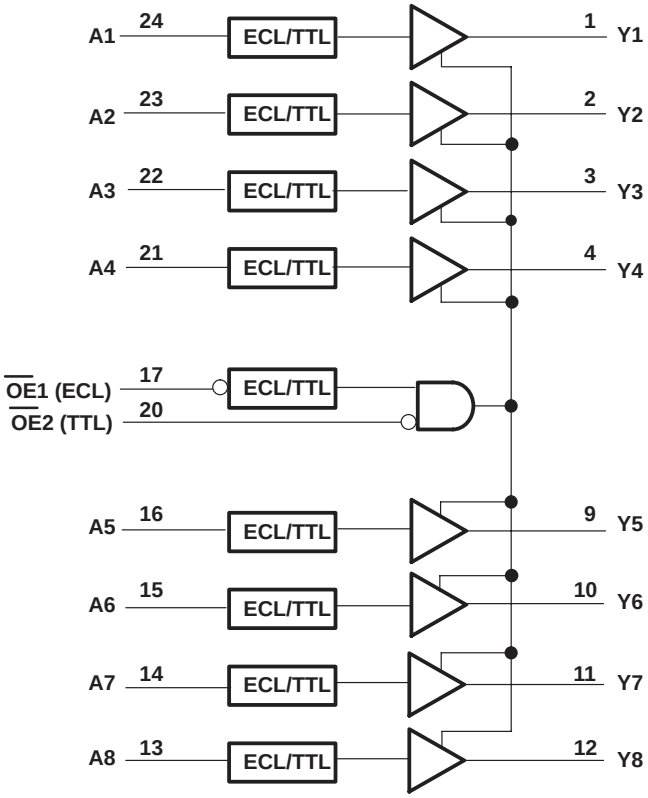
OUTPUT ENABLE		DATA INPUT	OUTPUT (TTL)
$\overline{OE}1$	$\overline{OE}2$	A	Y
X	H	X	Z
H	X	X	Z
L	L	L	L
L	L	H	H

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265
POST OFFICE BOX 1443 • HOUSTON, TEXAS 77251−1443

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} . . . . . −0.5 V to 7 V
Supply voltage range, V_{EE} . . . . . −8 V to 0 V
Input voltage range (TTL) (see Note 1) . . . . . −1.2 V to 7 V
Input voltage range (ECL) . . . . . V_{EE} to 0 V
Voltage applied to any output in the high state . . . . . −0.5 V to V_{CC}
Voltage applied to any output in the disabled or power-off state . . . . . −0.5 V to 5.5 V
Input current range (TTL) . . . . . −30 mA to 5 mA
Current into any output in the low state . . . . . 96 mA
Operating free-air temperature range . . . . . 0°C to 85°C
Storage temperature range . . . . . −65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The TTL input voltage ratings may be exceeded provided the input current ratings are observed.

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{CC}	TTL supply voltage	4.5	5	5.5	V
V_{EE}	ECL supply voltage	−4.2	−4.5	−4.8	V
V_{IH}	TTL high-level input voltage	2			V
V_{IL}	TTL low-level input voltage			0.8	V
V_{IH}	ECL high-level input voltage‡	−1150		−840	mV
V_{IL}	ECL low-level input voltage‡	−1810		−1490	mV
I_{IK}	TTL input clamp current			−18	mA
I_{OH}	High-level output current			−15	mA
I_{OL}	Low-level output current			48	mA
T_A	Operating free-air temperature	0		85	°C

‡ The algebraic convention, in which the least positive (most negative) value is designated minimum, is used in this data sheet for logic levels only.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP†	MAX	UNIT
V_{IK}	$\overline{OE}$2 only	V_{CC} = 4.5 V,	V_{EE} = −4.2 V,	I_I = −18 mA			−1.2	V
I_I	$\overline{OE}$2 only	V_{CC} = 5.5 V,	V_{EE} = −4.8 V,	V_I = 7 V			0.1	mA
I_{IH}	$\overline{OE}$2 only	V_{CC} = 5.5 V,	V_{EE} = −4.8 V,	V_I = 2.7 V			20	µA
I_{IL}	$\overline{OE}$2 only	V_{CC} = 5.5 V,	V_{EE} = −4.8 V,	V_I = 0.5 V			−0.5	mA
I_{IH}	Data inputs and $\overline{OE}$1	V_{CC} = 5.5 V,	V_{EE} = −4.8 V,	V_{IH} = −840 mV			350	µA
I_{IL}	Data inputs and $\overline{OE}$1	V_{CC} = 5.5 V,	V_{EE} = −4.8 V,	V_{IL} = −1810 mV	0.50			µA
V_{OH}		V_{CC} = 4.5 V,	V_{EE} = −4.5 V ± 0.3 V,	I_{OH} = −3 mA	2.4	3.3		V
		V_{CC} = 4.5 V,	V_{EE} = −4.5 V ± 0.3 V,	I_{OH} = −15 mA	2	3.1		
V_{OL}		V_{CC} = 4.5 V,	V_{EE} = −4.5 V ± 0.3 V,	I_{OL} = 48 mA		0.38	0.55	V
I_{OZH}		V_{CC} = 5.5 V,	V_{EE} = −4.8 V,	V_O = 2.7 V			50	µA
I_{OZL}		V_{CC} = 5.5 V,	V_{EE} = −4.8 V,	V_O = 0.5 V			−50	µA
I_{OS}‡		V_{CC} = 5.5 V,	V_{EE} = −4.8 V,	V_O = 0 V	−100		−225	mA
I_{CCH}		V_{CC} = 5.5 V,	V_{EE} = −4.8 V			64	97	mA
I_{CCL}		V_{CC} = 5.5 V,	V_{EE} = −4.8 V			80	120	mA
I_{CCZ}		V_{CC} = 5.5 V,	V_{EE} = −4.8 V			77	116	mA
I_{EE}		V_{CC} = 5.5 V,	V_{EE} = −4.8 V			−22	−33	mA
C_i		V_{CC} = 5 V,	V_{EE} = 4.5 V			5		pF
C_o		V_{CC} = 5 V,	V_{EE} = 4.5 V			7		pF

† All typical values are at V_{CC} = 5 V, V_{EE} = −4.5 V, T_A = 25°C.
‡ Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (see Figure 1)

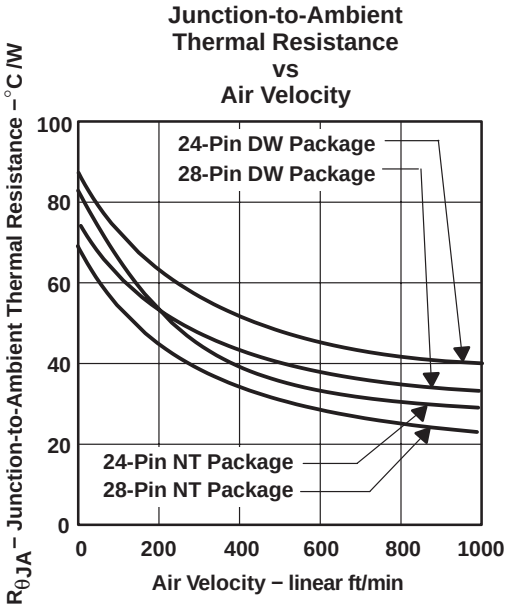
PARAMETER	FROM (INPUT)	TO (OUTPUT)	C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω			UNIT
			MIN	TYP§	MAX	
t_{PLH}	A	Y	1.7	4	6.2	ns
t_{PHL}			1.6	4	6.2	
t_{PZH}	$\overline{OE}$1	Y	2.6	4.7	6.7	ns
t_{PZL}			3.2	5.9	8.5	
t_{PHZ}	$\overline{OE}$1	Y	2.9	5.4	7.8	ns
t_{PLZ}			1.9	4.9	7.8	
t_{PZH}	$\overline{OE}$2	Y	1.7	4	6.2	ns
t_{PZL}			2.5	5.1	7.7	
t_{PHZ}	$\overline{OE}$2	Y	2.1	4.3	6.4	ns
t_{PLZ}			1.1	3.7	6.3	

§ All typical values are at V_{CC} = 5 V, V_{EE} = −4.5 V, T_A = 25°C.

THERMAL INFORMATION

In digital system designs utilizing 100KT' or 10KHT' series logic level translators, good thermal management is an important consideration for proper circuit performance and extended reliability. The size of the "small outline" package makes thermal management even more important due to the increased board and thermal densities.

The thermal resistances in Figure 1 can be used to approximate typical and maximum virtual junction temperatures for the SN100KT' and SN10KHT' translators. The junction temperature of these devices may be estimated using Equation 1.

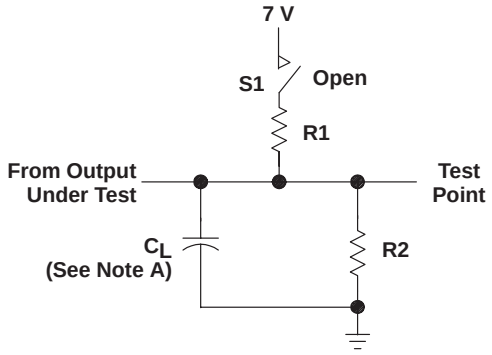


$$T_J = R_{\Theta JA} (V_{CC} \bullet I_{CC} + V_{EE} \bullet I_{EE} + P_{DRIVER}) + T_A \quad (1)$$

where

T_J = virtual junction temperature
T_A = ambient air temperature
$R_{\Theta JA}$ = thermal resistance, junction to ambient air
I_{CC} = TTL level supply current (from the databook)
I_{EE} = ECL supply current
V_{CC} = TTL level suply voltage (5 V for typical, 5.5 V for maximum)
V_{EE} = ECL level supply voltage:
SN10KHT' − (−5.2 V Typ, −5.46 V Max)
SN100KHT' − (−54.5 V Typ, −4.80 V Max)
P_{DRIVER} = total power consumed by the output driver

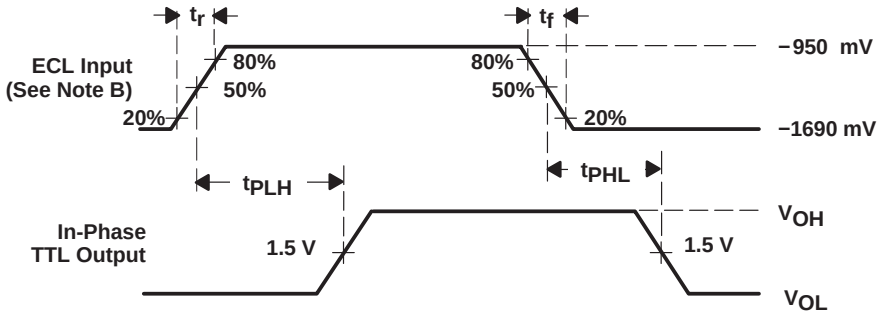
PARAMETER MEASUREMENT INFORMATION



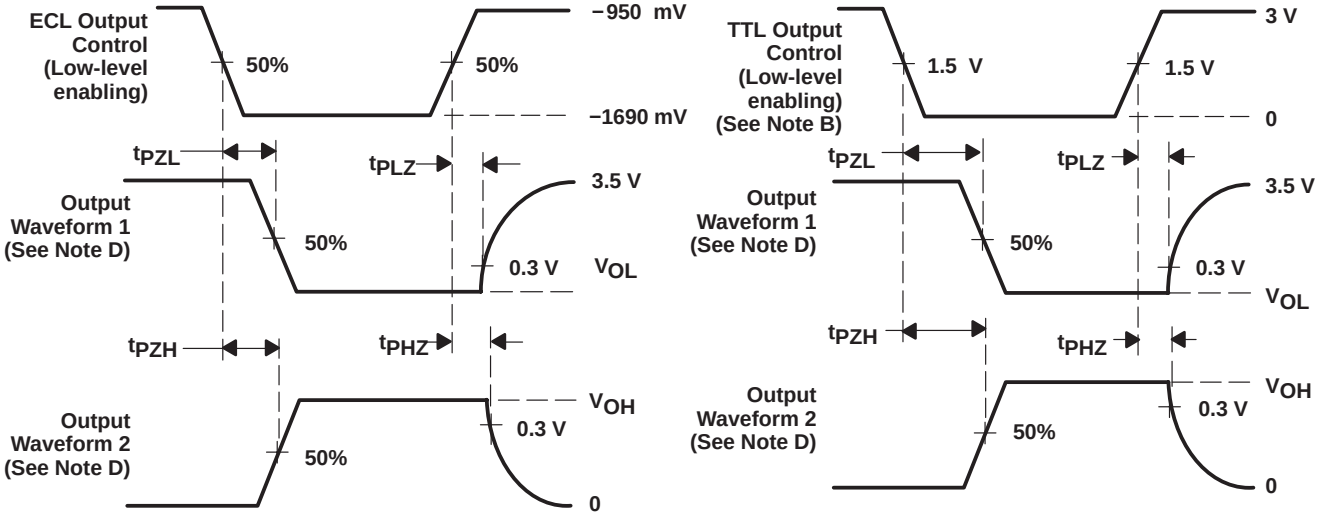
LOAD CIRCUIT

SWITCH POSITION TABLE

TEST	S1
t_{PLH}	Open
t_{PHL}	Open
t_{PZH}	Open
t_{PZL}	Closed
t_{PHZ}	Open
t_{PLZ}	Closed



ECL- INPUT PROPAGATION DELAY TIMES



ECL ENABLE AND DISABLE TIMES

TTL ENABLE AND DISABLE TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. For TTL inputs, input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
C. For ECL inputs, input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 1.5 ns, t_f ≤ 1.5 ns.
D. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
E. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
SN100KT5541DW	OBSOLETE	SOIC	DW	24		TBD	Call TI	Call TI
SN100KT5541NT	OBSOLETE	PDIP	NT	24		TBD	Call TI	Call TI
SN100KT5541NT	OBSOLETE	PDIP	NT	24		TBD	Call TI	Call TI

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS) or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
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(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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