

High Speed CMOS Logic 3-to-8 Line Decoder/ Demultiplexer Inverting and Non-Inverting

October 1997 - Revised July 2002

Features

- Select One Of Eight Data Outputs
Active Low for 138, Active High for 238
- I/O Port or Memory Selector
- Three Enable Inputs to Simplify Cascading
- Typical Propagation Delay of 13ns at $V_{CC} = 5V$,
 $C_L = 15pF$, $T_A = 25^{\circ}C$
- Fanout (Over Temperature Range)
 - Standard Outputs 10 LSTTL Loads
 - Bus Driver Outputs 15 LSTTL Loads
- Wide Operating Temperature Range . . . $-55^{\circ}C$ to $125^{\circ}C$
- Balanced Propagation Delay and Transition Times
- Significant Power Reduction Compared to LSTTL
Logic ICs
- HC Types
 - 2V to 6V Operation
 - High Noise Immunity: $N_{IL} = 30\%$, $N_{IH} = 30\%$ of V_{CC}
at $V_{CC} = 5V$
- HCT Types
 - 4.5V to 5.5V Operation
 - Direct LSTTL Input Logic Compatibility,
 $V_{IL} = 0.8V$ (Max), $V_{IH} = 2V$ (Min)
 - CMOS Input Compatibility, $I_I \leq 1\mu A$ at V_{OL} , V_{OH}

Description

The 'HC138, 'HC238, 'HCT138, and 'HCT238 are high speed silicon gate CMOS decoders well suited to memory address decoding or data routing applications. Both circuits feature low power consumption usually associated with CMOS circuitry, yet have speeds comparable to low power Schottky TTL logic. Both circuits have three binary select inputs (A0, A1 and A2). If the device is enabled, these inputs determine which one of the eight normally high outputs of the HC/HCT138 series will go low or which of the normally low outputs of the HC/HCT238 series will go high.

Two active low and one active high enables ($\overline{E1}$, $\overline{E2}$, and E3) are provided to ease the cascading of decoders. The decoder's 8 outputs can drive 10 low power Schottky TTL equivalent loads.

Ordering Information

PART NUMBER	TEMP. RANGE ($^{\circ}C$)	PACKAGE
CD54HC138F	-55 to 125	16 Ld CERDIP
CD54HC138F3A	-55 to 125	16 Ld CERDIP
CD74HC138E	-55 to 125	16 Ld PDIP
CD74HC138M	-55 to 125	16 Ld SOIC
CD74HC138M96	-55 to 125	16 Ld SOIC
CD54HCT138F	-55 to 125	16 Ld CERDIP
CD54HCT138F3A	-55 to 125	16 Ld CERDIP
CD74HCT138E	-55 to 125	16 Ld PDIP
CD74HCT138M	-55 to 125	16 Ld SOIC
CD74HCT138M96	-55 to 125	16 Ld SOIC
CD54HC238F3A	-55 to 125	16 Ld CERDIP
CD74HC238E	-55 to 125	16 Ld PDIP
CD74HC238M	-55 to 125	16 Ld SOIC
CD74HC238M96	-55 to 125	16 Ld SOIC
CD74HC238NSR	-55 to 125	16 Ld SOP
CD74HC238PWR	-55 to 125	16 Ld TSSOP
CD54HCT238F3A	-55 to 125	16 Ld CERDIP
CD74HCT238E	-55 to 125	16 Ld PDIP
CD74HCT238M	-55 to 125	16 Ld SOIC

NOTES:

1. When ordering, use the entire part number. Add the suffix 96 to obtain the variant in the tape and reel.
2. Wafer and die for this part number is available which meets all electrical specifications. Please contact your local TI sales office or customer service for ordering information.

CD54/74HC138, CD54/74HCT138, CD54/74HC238, CD54/74HCT238

Pinout

CD54HC138, CD54HCT138, CD54HC238, CD54HCT238
(CERDIP)

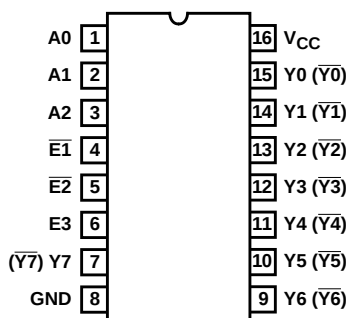
CD74HC138, CD74HCT138, CD74HCT238

(PDIP, SOIC)

CD74HC238

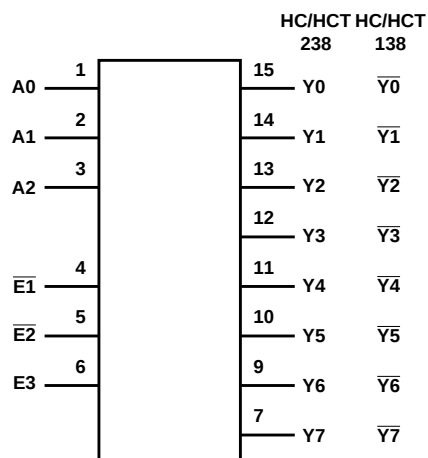
(PDIP, SOIC, SOP, TSSOP)

TOP VIEW



Signal names in parentheses are for 'HC138 and 'HCT138.

Functional Diagram



TRUTH TABLE 'HC138, 'HCT138

INPUTS						OUTPUTS							
ENABLE			ADDRESS										
E3	E2	E1	A2	A1	A0	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
X	X	H	X	X	X	H	H	H	H	H	H	H	H
L	X	X	X	X	X	H	H	H	H	H	H	H	H
X	H	X	X	X	X	H	H	H	H	H	H	H	H
H	L	L	L	L	L	L	H	H	H	H	H	H	H
H	L	L	L	L	H	H	L	H	H	H	H	H	H
H	L	L	L	H	L	H	H	L	H	H	H	H	H
H	L	L	L	H	H	H	H	H	L	H	H	H	H
H	L	L	H	L	L	H	H	H	H	L	H	H	H
H	L	L	H	L	H	H	H	H	H	H	L	H	H
H	L	L	H	H	L	H	H	H	H	H	H	L	H
H	L	L	H	H	H	H	H	H	H	H	H	H	L

NOTE: H = High Voltage Level, L = Low Voltage Level, X = Don't Care

CD54/74HC138, CD54/74HCT138, CD54/74HC238, CD54/74HCT238

TRUTH TABLE 'HC238, 'HCT238

INPUTS						OUTPUTS							
ENABLE			ADDRESS										
E3	E2	E1	A2	A1	A0	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
X	X	H	X	X	X	L	L	L	L	L	L	L	L
L	X	X	X	X	X	L	L	L	L	L	L	L	L
X	H	X	X	X	X	L	L	L	L	L	L	L	L
H	L	L	L	L	L	H	L	L	L	L	L	L	L
H	L	L	L	L	H	L	H	L	L	L	L	L	L
H	L	L	L	H	L	L	L	H	L	L	L	L	L
H	L	L	L	H	H	L	L	L	H	L	L	L	L
H	L	L	H	L	L	L	L	L	L	H	L	L	L
H	L	L	H	L	H	L	L	L	L	L	H	L	L
H	L	L	H	H	L	L	L	L	L	L	L	H	L
H	L	L	H	H	H	L	L	L	L	L	L	L	H

NOTE: H = High Voltage Level, L = Low Voltage Level, X = Don't Care

CD54/74HC138, CD54/74HCT138, CD54/74HC238, CD54/74HCT238

Absolute Maximum Ratings

DC Supply Voltage, V_{CC} -0.5V to 7V
 DC Input Diode Current, I_{IK}
 For $V_I < -0.5V$ or $V_I > V_{CC} + 0.5V$ $\pm 20mA$
 DC Output Diode Current, I_{OK}
 For $V_O < -0.5V$ or $V_O > V_{CC} + 0.5V$ $\pm 20mA$
 DC Output Source or Sink Current per Output Pin, I_O
 For $V_O > -0.5V$ or $V_O < V_{CC} + 0.5V$ $\pm 25mA$
 DC V_{CC} or Ground Current, I_{CC} or I_{GND} $\pm 50mA$

Thermal Information

Package Thermal Impedance, θ_{JA} (see Note 3):
 PDIP Package $67^{\circ}C/W$
 SOIC Package $73^{\circ}C/W$
 SOP Package $64^{\circ}C/W$
 TSSOP Package $108^{\circ}C/W$
 Maximum Junction Temperature $150^{\circ}C$
 Maximum Storage Temperature Range $-65^{\circ}C$ to $150^{\circ}C$
 Maximum Lead Temperature (Soldering 10s) $300^{\circ}C$
 (SOIC - Lead Tips Only)

Operating Conditions

Temperature Range (T_A) $-55^{\circ}C$ to $125^{\circ}C$
 Supply Voltage Range, V_{CC}
 HC Types 2V to 6V
 HCT Types 4.5V to 5.5V
 DC Input or Output Voltage, V_I , V_O 0V to V_{CC}
 Input Rise and Fall Time
 2V 1000ns (Max)
 4.5V 500ns (Max)
 6V 400ns (Max)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

- The package thermal impedance is calculated in accordance with JESD 51-7.

DC Electrical Specifications

PARAMETER	SYMBOL	TEST CONDITIONS		V _{CC} (V)	25°C			-40°C TO 85°C		-55°C TO 125°C		UNITS		
		V _I (V)	I _O (mA)		MIN	TYP	MAX	MIN	MAX	MIN	MAX			
HC TYPES														
High Level Input Voltage	V _{IH}	-	-	2	1.5	-	-	1.5	-	1.5	-	V		
				4.5	3.15	-	-	3.15	-	3.15	-	V		
				6	4.2	-	-	4.2	-	4.2	-	V		
Low Level Input Voltage	V _{IL}	-	-	2	-	-	0.5	-	0.5	-	0.5	V		
				4.5	-	-	1.35	-	1.35	-	1.35	V		
				6	-	-	1.8	-	1.8	-	1.8	V		
High Level Output Voltage CMOS Loads	V _{OH}	V _{IH} or V _{IL}	-0.02	2	1.9	-	-	1.9	-	1.9	-	V		
			-0.02	4.5	4.4	-	-	4.4	-	4.4	-	V		
			-0.02	6	5.9	-	-	5.9	-	5.9	-	V		
-			-	-	-	-	-	-	-	-	V			
-4			4.5	3.98	-	-	3.84	-	3.7	-	V			
-5.2			6	5.48	-	-	5.34	-	5.2	-	V			
Low Level Output Voltage CMOS Loads	V _{OL}	V _{IH} or V _{IL}	0.02	2	-	-	0.1	-	0.1	-	0.1	V		
			0.02	4.5	-	-	0.1	-	0.1	-	0.1	V		
			0.02	6	-	-	0.1	-	0.1	-	0.1	V		
-			-	-	-	-	-	-	-	-	V			
4			4.5	-	-	0.26	-	0.33	-	0.4	V			
5.2			6	-	-	0.26	-	0.33	-	0.4	V			
Low Level Output Voltage TTL Loads	V _{OL}	V _{IH} or V _{IL}	-	-	-	-	-	-	-	-	-	V		
			4	4.5	-	-	0.26	-	0.33	-	0.4	V		
			5.2	6	-	-	0.26	-	0.33	-	0.4	V		
Input Leakage Current			I _I	V _{CC} or GND	-	6	-	-	±0.1	-	±1	-	±1	μA
Quiescent Device Current			I _{CC}	V _{CC} or GND	0	6	-	-	8	-	80	-	160	μA

CD54/74HC138, CD54/74HCT138, CD54/74HC238, CD54/74HCT238

DC Electrical Specifications (Continued)

PARAMETER	SYMBOL	TEST CONDITIONS		V _{CC} (V)	25°C			-40°C TO 85°C		-55°C TO 125°C		UNITS
		V _I (V)	I _O (mA)		MIN	TYP	MAX	MIN	MAX	MIN	MAX	
HCT TYPES												
High Level Input Voltage	V _{IH}	-	-	4.5 to 5.5	2	-	-	2	-	2	-	V
Low Level Input Voltage	V _{IL}	-	-	4.5 to 5.5	-	-	0.8	-	0.8	-	0.8	V
High Level Output Voltage CMOS Loads	V _{OH}	V _{IH} or V _{IL}	-0.02	4.5	4.4	-	-	4.4	-	4.4	-	V
High Level Output Voltage TTL Loads			-4	4.5	3.98	-	-	3.84	-	3.7	-	V
Low Level Output Voltage CMOS Loads	V _{OL}	V _{IH} or V _{IL}	0.02	4.5	-	-	0.1	-	0.1	-	0.1	V
Low Level Output Voltage TTL Loads			4	4.5	-	-	0.26	-	0.33	-	0.4	V
Input Leakage Current	I _I	V _{CC} and GND	0	5.5	-		±0.1	-	±1	-	±1	μA
Quiescent Device Current	I _{CC}	V _{CC} or GND	0	5.5	-	-	8	-	80	-	160	μA
Additional Quiescent Device Current Per Input Pin: 1 Unit Load (Note 4)	ΔI _{CC}	V _{CC} -2.1	-	4.5 to 5.5	-	100	360	-	450	-	490	μA

NOTE:

4. For dual-supply systems theoretical worst case (V_I = 2.4V, V_{CC} = 5.5V) specification is 1.8mA.

HCT Input Loading Table

INPUT	UNIT LOADS
A0-A2	1.5
E1, E2	1.25
E3	1

NOTE: Unit Load is ΔI_{CC} limit specified in DC Electrical Table, e.g., 360μA max at 25°C.

Switching Specifications Input t_r, t_f = 6ns

PARAMETER	SYMBOL	TEST CONDITIONS	V _{CC} (V)	25°C			-40°C TO 85°C		-55°C TO 125°C		UNITS
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
HC TYPES											
Propagation Delay	t _{PLH} , t _{PHL}	C _L = 50pF	2	-	-	150	-	190	-	225	ns
Address to Output			4.5	-	-	30	-	38	-	45	ns
		C _L = 15pF	5	-	13	-	-	-	-	ns	
		C _L = 50pF	6	-	-	26	-	33	-	38	ns

CD54/74HC138, CD54/74HCT138, CD54/74HC238, CD54/74HCT238

Switching Specifications Input $t_r, t_f = 6\text{ns}$ (Continued)

PARAMETER	SYMBOL	TEST CONDITIONS	V_{CC} (V)	25°C			-40°C TO 85°C		-55°C TO 125°C		UNITS
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
Enable to Output HC/HCT138	t_{PLH}, t_{PHL}	$C_L = 50\text{pF}$	2	-	-	150	-	190	-	265	ns
			4.5	-	-	30	-	38	-	53	ns
			6	-	-	26	-	33	-	45	ns
Output Transition Time (Figure 1)	t_{TLH}, t_{THL}	$C_L = 50\text{pF}$	2	-	-	75	-	95	-	110	ns
			4.5	-	-	15	-	19	-	22	ns
			6	-	-	13	-	16	-	19	ns
Power Dissipation Capacitance, (Notes 5, 6)	C_{PD}	$C_L = 15\text{pF}$	5	-	67	-	-	-	-	-	pF
Input Capacitance	C_{IN}	-	-	-	-	10	-	10	-	10	pF

HCT TYPES

Propagation Delay Address to Output	t_{PLH}, t_{PHL}	$C_L = 50\text{pF}$	4.5	-	-	35	-	44	-	53	ns
		$C_L = 15\text{pF}$	5	-	14	-	-	-	-	-	ns
Enable to Output HC/HCT138	t_{PLH}, t_{PHL}	$C_L = 50\text{pF}$	4.5	-	-	35	-	44	-	53	ns
Enable to Output HC/HCT238	t_{PLH}, t_{PHL}	$C_L = 15\text{pF}$	4.5	-	-	40	-	50	-	60	ns
Output Transition Time (Figure 2)	t_{TLH}, t_{THL}	$C_L = 50\text{pF}$	4.5	-	-	15	-	19	-	22	ns
Power Dissipation Capacitance, (Notes 5, 6)	C_{PD}	$C_L = 15\text{pF}$	5	-	67	-	-	-	-	-	pF
Input Capacitance	C_{IN}	-	-	-	-	10	-	10	-	10	pF

NOTES:

- C_{PD} is used to determine the dynamic power consumption, per gate.
- $P_D = V_{CC}^2 f_i (C_{PD} + C_L)$ where: f_i = Input Frequency, C_L = Output Load Capacitance, V_{CC} = Supply Voltage.

Test Circuits and Waveforms

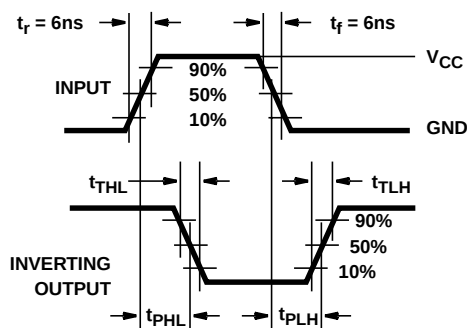


FIGURE 7. HC AND HCU TRANSITION TIMES AND PROPAGATION DELAY TIMES, COMBINATION LOGIC

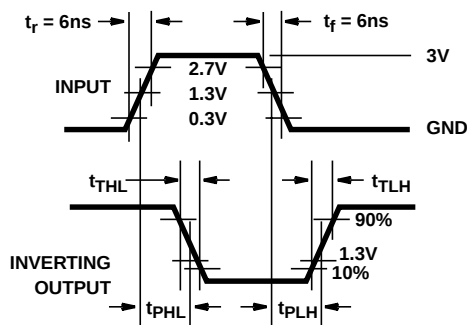


FIGURE 8. HCT TRANSITION TIMES AND PROPAGATION DELAY TIMES, COMBINATION LOGIC

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PRODUCT SUPPORT: [TRAINING](#)

CD74HC238, High Speed CMOS Logic 3-to-8 Line Decoder Demultiplexer Inverting and Non-Inverting

DEVICE STATUS: ACTIVE

PARAMETER NAME	CD54HC238
Voltage Nodes (V)	6, 5, 2

FEATURES [▲Back to Top](#)

- Select One Of Eight Data Outputs Active Low for 138, Active High for 238
- I/O Port or Memory Selector
- Three Enable Inputs to Simplify Cascading
- Typical Propagation Delay of 13ns at V_{CC} = 5V, C_L = 15pF, T_A = 25°C
- Fanout (Over Temperature Range)
 - Standard Outputs 10 LSTTL Loads
 - Bus Driver Outputs 15 LSTTL Loads
- Wide Operating Temperature Range . . . –55°C to 125°C
- Balanced Propagation Delay and Transition Times
- Significant Power Reduction Compared to LSTTL Logic ICs
- HC Types
 - 2V to 6V Operation
 - High Noise Immunity: N_{IL} = 30%, N_{IH} = 30% of V_{CC} at V_{CC} = 5V
- HCT Types
 - 4.5V to 5.5V Operation
 - Direct LSTTL Input Logic Compatibility, V_{IL} = 0.8V (Max), V_{IH} = 2V (Min)
 - CMOS Input Compatibility, I_I ≤ 1uA at V_{OL}, V_{OH}

Data sheet acquired from Harris Semiconductor

DESCRIPTION [▲Back to Top](#)

The 'HC138, 'HC238, 'HCT138, and 'HCT238 are high speed silicon gate CMOS decoders well suited to memory address decoding or data routing applications. Both circuits feature low power consumption usually associated with CMOS circuitry, yet have speeds comparable to low power Schottky TTL logic. Both circuits have three binary select inputs (A0, A1 and A2). If the device is enabled, these inputs determine which one of the eight normally high outputs of the HC/HCT138 series will go low or which of the normally low outputs of the HC/HCT238 series will go high.

Two active low and one active high enables (E1\, E2\, and E3) are provided to ease the cascading of decoders. The decoder's 8 outputs can drive 10 low power Schottky TTL equivalent loads.

TECHNICAL DOCUMENTS [▲Back to Top](#)

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To download a document to your hard drive, right-click on the link and choose 'Save'.

DATASHEET [▲Back to Top](#)

Full datasheet in Acrobat PDF: [cd74hc238.pdf](#) (31 KB,Rev.E) (Updated: 07/18/2002)

APPLICATION NOTES [▲Back to Top](#)

View Application Notes for [Digital Logic](#)

- [CMOS Power Consumption and CPD Calculation \(Rev. B\)](#) (SCAA035B - Updated: 06/01/1997)

- [Designing With Logic \(Rev. C\)](#) (SDYA009C - Updated: 06/01/1997)
- [Evaluation of Nickel/Palladium/Gold-Finished Surface-Mount Integrated Circuits](#) (SZZA026 - Updated: 06/20/2001)
- [Implications of Slow or Floating CMOS Inputs \(Rev. C\)](#) (SCBA004C - Updated: 02/01/1998)
- [Input and Output Characteristics of Digital Integrated Circuits](#) (SDYA010 - Updated: 10/01/1996)
- [Live Insertion](#) (SDYA012 - Updated: 10/01/1996)
- [SN54/74HCT CMOS Logic Family Applications and Restrictions](#) (SCLA011 - Updated: 05/01/1996)
- [Selecting the Right Texas Instruments Signal Switch](#) (SZZA030 - Updated: 09/07/2001)
- [TI IBIS File Creation, Validation, and Distribution Processes](#) (SZZA034 - Updated: 08/29/2002)
- [Understanding and Interpreting Texas Instruments Standard-Logic Products Data Sh \(Rev. A\)](#) (SZZA036A - Updated: 02/27/2003)
- [Using High Speed CMOS and Advanced CMOS in Systems With Multiple Vcc](#) (SCLA008 - Updated: 04/01/1996)

MORE LITERATURE

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- [Enhanced Plastic Portfolio Brochure](#) (SGZB004, 387 KB - Updated: 08/19/2002)
- [Logic Reference Guide](#) (SCYB004, 1032 KB - Updated: 10/23/2001)
- [MicroStar Junior BGA Design Summary](#) (SCET004, 167 KB - Updated: 07/28/2000)
- [Military Brief](#) (SGYN138, 803 KB - Updated: 10/10/2000)
- [Overview of IEEE Std 91-1984, Explanation of Logic Symbols Training Booklet \(Rev. A\)](#) (SDYZ001A, 138 KB - Updated: 07/01/1996)
- [Palladium Lead Finish User's Manual](#) (SDYV001, 2041 KB - Updated: 11/01/1996)
- [QML Class V Space Products Military Brief \(Rev. A\)](#) (SGZN001A, 257 KB - Updated: 10/07/2002)

USER GUIDES

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- [LOGIC Pocket Data Book](#) (SCYD013, 4837 KB - Updated: 12/05/2002)
- [Signal Switch Data Book](#) (SCDD003, 10259 KB - Updated: 03/19/2001)

SAMPLES

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ORDERABLE DEVICE	PACKAGE INDUSTRY (TI)	PINS	TEMP (°C)	STATUS	PRODUCT CONTENT	SAMPLES
CD74HC238M	SOIC (D)	16	-55 TO 125	ACTIVE	View Product Content	Request Samples
CD74HC238PWR	TSSOP (PW)	16	-55 TO 125	ACTIVE	View Product Content	Request Samples

PRICING/AVAILABILITY/PKG

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DEVICE INFORMATION

Updated Daily

ORDERABLE DEVICE	STATUS	PACKAGE TYPE PINS	TEMP (°C)	PRODUCT CONTENT	BUDGETARY PRICING QTY \$US	STD PACK QTY
CD74HC238E	ACTIVE	PDIP (N) 16	-55 TO 125	View Contents	1KU 0.26	25
CD74HC238M	ACTIVE	SOIC (D) 16	-55 TO 125	View Contents	1KU 0.26	40

TI INVENTORY STATUS

As Of 08:00 AM GMT, 17 Apr 2003

IN STOCK	IN PROGRESS QTY DATE	LEAD TIME
<u>0</u> *	> 10k 10 Jun	6 WKS
<u>1040</u> *	560 09 May	5 WKS
	> 10k 13 May	

REPORTED DISTRIBUTOR INVENTORY

As Of 08:00 AM GMT, 17 Apr 2003

DISTRIBUTOR COMPANY REGION	IN STOCK	PURCHASE
Avnet-SILICA Europe	> 1k	BUY NOW
EBV Electronik Europe	> 1k	BUY NOW
Avnet Americas	275	BUY NOW
Newark Electronics Americas	119	BUY NOW
EBV Electronik Europe	> 1k	BUY NOW
DigiKey Americas	> 1k	BUY NOW
Avnet-SILICA Europe	> 1k	BUY NOW

										Newark Electronics Americas	318	BUY NOW
CD74HC238M96	ACTIVE	SOIC (D) 16	-55 TO 125	View Contents	1KU 0.26	2500	Q*	>10k 13 May	5 WKS	Insight Americas	47	BUY NOW
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CD54HC238, High Speed CMOS Logic 3-to-8 Line Decoder Demultiplexer Inverting and Non-Inverting

DEVICE STATUS: ACTIVE

PARAMETER NAME	CD54HC238
Voltage Nodes (V)	6, 5, 2

FEATURES [▲Back to Top](#)

- Select One Of Eight Data Outputs Active Low for 138, Active High for 238
- I/O Port or Memory Selector
- Three Enable Inputs to Simplify Cascading
- Typical Propagation Delay of 13ns at V_{CC} = 5V, C_L = 15pF, T_A = 25°C
- Fanout (Over Temperature Range)
 - Standard Outputs 10 LSTTL Loads
 - Bus Driver Outputs 15 LSTTL Loads
- Wide Operating Temperature Range . . . –55°C to 125°C
- Balanced Propagation Delay and Transition Times
- Significant Power Reduction Compared to LSTTL Logic ICs
- HC Types
 - 2V to 6V Operation
 - High Noise Immunity: N_{IL} = 30%, N_{IH} = 30% of V_{CC} at V_{CC} = 5V
- HCT Types
 - 4.5V to 5.5V Operation
 - Direct LSTTL Input Logic Compatibility, V_{IL} = 0.8V (Max), V_{IH} = 2V (Min)
 - CMOS Input Compatibility, I_I ≤ 1uA at V_{OL}, V_{OH}

Data sheet acquired from Harris Semiconductor

DESCRIPTION [▲Back to Top](#)

The 'HC138, 'HC238, 'HCT138, and 'HCT238 are high speed silicon gate CMOS decoders well suited to memory address decoding or data routing applications. Both circuits feature low power consumption usually associated with CMOS circuitry, yet have speeds comparable to low power Schottky TTL logic. Both circuits have three binary select inputs (A0, A1 and A2). If the device is enabled, these inputs determine which one of the eight normally high outputs of the HC/HCT138 series will go low or which of the normally low outputs of the HC/HCT238 series will go high.

Two active low and one active high enables (E1\, E2\, and E3) are provided to ease the cascading of decoders. The decoder's 8 outputs can drive 10 low power Schottky TTL equivalent loads.

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- [Input and Output Characteristics of Digital Integrated Circuits](#) (SDYA010 - Updated: 10/01/1996)
- [Live Insertion](#) (SDYA012 - Updated: 10/01/1996)
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- [Understanding and Interpreting Texas Instruments Standard-Logic Products Data Sh \(Rev. A\)](#) (SZZA036A - Updated: 02/27/2003)
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- [Enhanced Plastic Portfolio Brochure](#) (SGZB004, 387 KB - Updated: 08/19/2002)
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- [MicroStar Junior BGA Design Summary](#) (SCET004, 167 KB - Updated: 07/28/2000)
- [Military Brief](#) (SGYN138, 803 KB - Updated: 10/10/2000)
- [Overview of IEEE Std 91-1984, Explanation of Logic Symbols Training Booklet \(Rev. A\)](#) (SDYZ001A, 138 KB - Updated: 07/01/1996)
- [Palladium Lead Finish User's Manual](#) (SDYV001, 2041 KB - Updated: 11/01/1996)
- [QML Class V Space Products Military Brief \(Rev. A\)](#) (SGZN001A, 257 KB - Updated: 10/07/2002)

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- [LOGIC Pocket Data Book](#) (SCYD013, 4837 KB - Updated: 12/05/2002)
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5962- 8688401EA	ACTIVE	CDIP (J)	16	-55 TO 125		View Contents	1KU 3.32	1	86 *	>10k 27 May	8 WKS	Avnet Americas	78	BUY NOW
CD54HC238F3A	ACTIVE	CDIP (J)	16	-55 TO 125	5962- 8688401EA	View Contents	1KU 3.30	1	0 *	>10k 27 May	8 WKS	EBV Electronik Europe	25	BUY NOW

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PRODUCT SUPPORT: [TRAINING](#)

CD54HCT238, High Speed CMOS Logic 3-to-8 Line Decoder Demultiplexer Inverting and Non-Inverting

DEVICE STATUS: ACTIVE

PARAMETER NAME	CD54HCT238
Voltage Nodes (V)	5

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- Select One Of Eight Data Outputs Active Low for 138, Active High for 238
- I/O Port or Memory Selector
- Three Enable Inputs to Simplify Cascading
- Typical Propagation Delay of 13ns at V_{CC} = 5V, C_L = 15pF, T_A = 25°C
- Fanout (Over Temperature Range)
 - Standard Outputs 10 LSTTL Loads
 - Bus Driver Outputs 15 LSTTL Loads
- Wide Operating Temperature Range . . . -55°C to 125°C
- Balanced Propagation Delay and Transition Times
- Significant Power Reduction Compared to LSTTL Logic ICs
- HC Types
 - 2V to 6V Operation
 - High Noise Immunity: N_{IL} = 30%, N_{IH} = 30% of V_{CC} at V_{CC} = 5V
- HCT Types
 - 4.5V to 5.5V Operation
 - Direct LSTTL Input Logic Compatibility, V_{IL} = 0.8V (Max), V_{IH} = 2V (Min)
 - CMOS Input Compatibility, I_I ≤ 1uA at V_{OL}, V_{OH}

Data sheet acquired from Harris Semiconductor

DESCRIPTION [▲Back to Top](#)

The 'HC138, 'HC238, 'HCT138, and 'HCT238 are high speed silicon gate CMOS decoders well suited to memory address decoding or data routing applications. Both circuits feature low power consumption usually associated with CMOS circuitry, yet have speeds comparable to low power Schottky TTL logic. Both circuits have three binary select inputs (A0, A1 and A2). If the device is enabled, these inputs determine which one of the eight normally high outputs of the HC/HCT138 series will go low or which of the normally low outputs of the HC/HCT238 series will go high.

Two active low and one active high enables (E1\, E2\, and E3) are provided to ease the cascading of decoders. The decoder's 8 outputs can drive 10 low power Schottky TTL equivalent loads.

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- [Implications of Slow or Floating CMOS Inputs \(Rev. C\)](#) (SCBA004C - Updated: 02/01/1998)
- [SN54/74HCT CMOS Logic Family Applications and Restrictions](#) (SCLA011 - Updated: 05/01/1996)
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- [MicroStar Junior BGA Design Summary](#) (SCET004, 167 KB - Updated: 07/28/2000)
- [Military Brief](#) (SGYN138, 803 KB - Updated: 10/10/2000)
- [Overview of IEEE Std 91-1984, Explanation of Logic Symbols Training Booklet \(Rev. A\)](#) (SDYZ001A, 138 KB - Updated: 07/01/1996)
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CD54HCT238F3A	ACTIVE	CDIP (J)	16	-55 TO 125	5962-8974501EA	View Contents	1KU 3.25	1	537 *	> 10k 20 May	8 WKS	None Reported View Distributors		

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PRODUCT SUPPORT: [TRAINING](#)

CD54HC138, High Speed CMOS Logic Inverting and Non-Inverting 3-to-8 Line Decoder Demultiplexer
DEVICE STATUS: ACTIVE

PARAMETER NAME	CD54HC138
Voltage Nodes (V)	6, 5, 2

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- Select One Of Eight Data Outputs Active Low for 138, Active High for 238
- I/O Port or Memory Selector
- Three Enable Inputs to Simplify Cascading
- Typical Propagation Delay of 13ns at V_{CC} = 5V, C_L = 15pF, T_A = 25°C
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Data sheet acquired from Harris Semiconductor

DESCRIPTION [▲Back to Top](#)

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- [Live Insertion](#) (SDYA012 - Updated: 10/01/1996)
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