

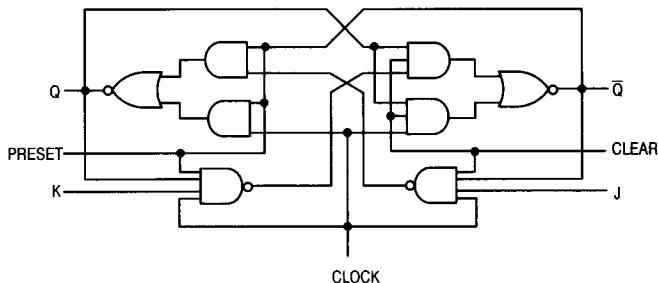


Dual J-K Flip-Flop With Clear and Preset

ELECTRICALLY TESTED PER:
MIL-M-38510/30103

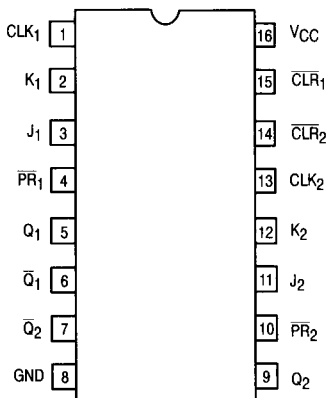
The 54LS112A dual flip-flop features individual J, K, clock, and asynchronous set and clear inputs to each flip-flop. When the clock goes HIGH, the inputs are enabled and data will be accepted. The logic level of the J and K inputs may be allowed to change when the clock pulse is HIGH and the bistable will perform according to the truth table as long as minimum set-up and hold time are observed. Input data is transferred to the outputs on the negative-going edge of the clock pulse.

LOGIC DIAGRAM (one half shown)

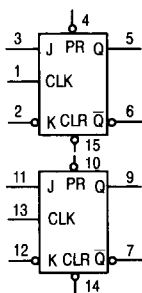


Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

CONNECTION DIAGRAM



LOGIC SYMBOL



Military 54LS112A



AVAILABLE AS:

- 1) JAN: JM38510/30103BXA
- 2) SMD: N/A
- 3) 883: 54LS112A/BXAJC

X = CASE OUTLINE AS FOLLOWS:
PACKAGE: CERDIP: E
CERFLAT: F
LCC: 2

THE LETTER "M" APPEARS
BEFORE THE / ON LCC.

PIN ASSIGNMENTS

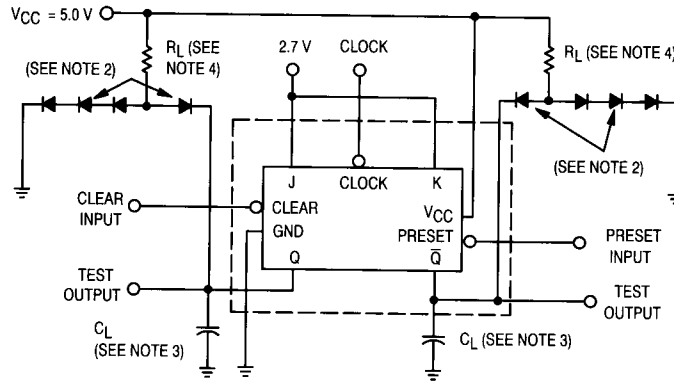
FUNCT.	DIL 620-09	FLATS 650-05	LCC 756A-02	BURN-IN (COND. A)
CLK ₁	1	1	2	VCC
K ₁	2	2	3	VCC
J ₁	3	3	4	VCC
PR ₁	4	4	5	GND
Q ₁	5	5	7	VCC
Q ₁	6	6	8	VCC
Q ₂	7	7	9	VCC
GND	8	8	10	GND
Q ₂	9	9	12	VCC
PR ₂	10	10	13	GND
J ₂	11	11	14	VCC
K ₂	12	12	15	VCC
CLK ₂	13	13	17	VCC
CLR ₂	14	14	18	GND
CLR ₁	15	15	19	GND
VCC	16	16	20	VCC

BURN-IN CONDITIONS:

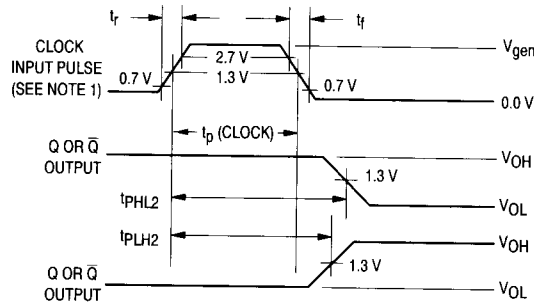
VCC = 5.0 V MIN/6.0 V MAX

54LS112A

AC TEST CIRCUIT



WAVEFORMS



NOTES:

1. Clock input characteristics for t_{PLH} , t_{PHL} (clock to output):
 $V_{gen} = 3.0\text{ V}$, $t_r \leq 15\text{ ns}$, $t_f = 6.0\text{ ns}$, t_p (clock) = 25 ns and
 $PRR = \leq 1.0\text{ MHz}$. When testing f_{MAX} the clock input
characteristics are: $V_{gen} = 3.0\text{ V}$, $t_r = t_f \leq 10\text{ ns}$,
 t_p (clock) $\leq 25\text{ ns}$ and $PRR =$ (see table).
2. All diodes are 1N3064, or equivalent.
3. $C_L = 50\text{ pF} \pm 10\%$ (including jig and probe capacitance).
4. $R_L = 2.0\text{ k}\Omega \pm 5.0\%$.

MODE SELECT - TRUTH TABLE

Operating Mode	Inputs		Outputs			
	PR	CLR	J	K	Q	$\bar{Q}$
Set	L	H	X	X	H	L
Reset (Clear)	H	L	X	X	L	H
*Undetermined	L	L	X	X	H	H
Toggle	H	H	h	l	$\bar{q}$	q
Load "0" (Reset)	H	H	h	l	L	H
Load "1" (Set)	H	H	l	h	H	L
Hold	H	H	l	h	q	$\bar{q}$

H, h = HIGH Voltage Level

L, l = LOW Voltage Level

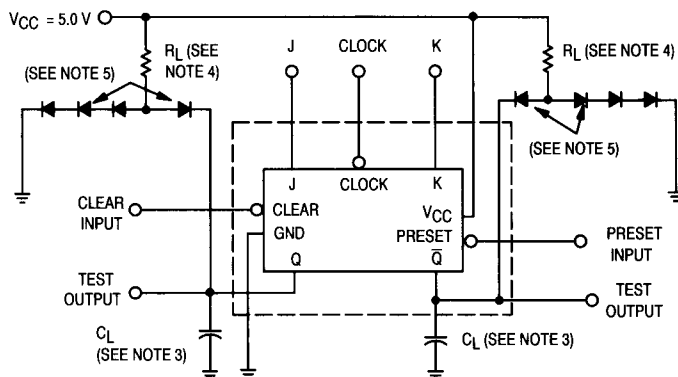
X = Don't Care

l, h (q) = Lower case letters indicate the state of referenced input (or output) one set-up time prior to the HIGH to LOW clock transition.

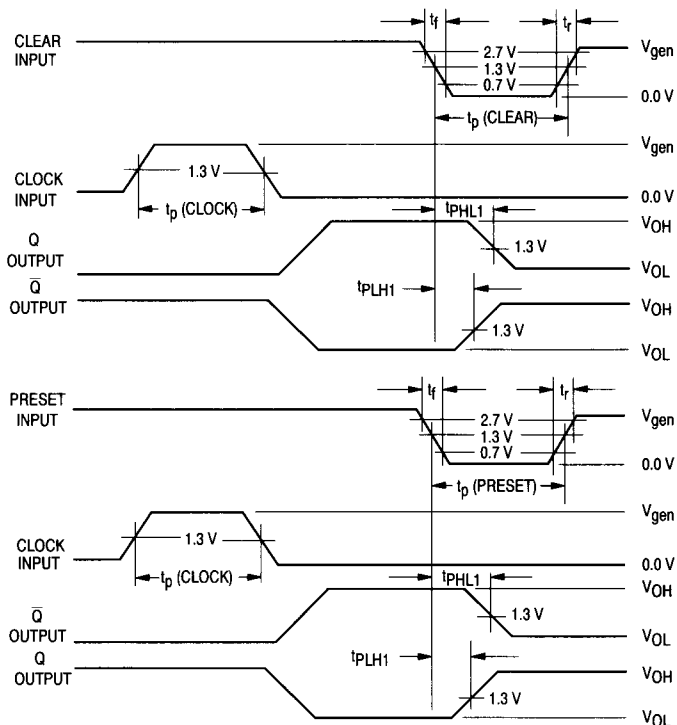
*Both outputs will be HIGH while both $\bar{PR}$ and $\bar{CLR}$ are LOW, but the output states are unpredictable if $\bar{PR}$ and $\bar{CLR}$ go HIGH simultaneously.

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AC TEST CIRCUIT



WAVEFORMS



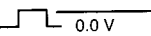
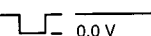
NOTES:

1. Clear or preset inputs dominate regardless of the state of clock J-K inputs.
2. Clear or preset input pulse characteristics: $V_{gen} = 3.0 \text{ V}$, $t_r \leq 15 \text{ ns}$, $t_f \leq 6.0 \text{ ns}$, $PRR \leq 1.0 \text{ MHz}$, $t_p(\text{clear}) = t_p(\text{preset}) = 30 \text{ ns}$, $Z_{OUT} \approx 50 \Omega$.
3. $C_L = 50 \text{ pF} \pm 10\%$ (including jig and probe capacitance).
4. $R_L = 2.0 \text{ k}\Omega \pm 5.0\%$.
5. All diodes are 1N3064, or equivalent.
6. When testing clear to output switching, preset shall have a logical "1" voltage applied. When testing preset to output switching, clear input shall have a logical "1" voltage applied (see table).
7. Clock input pulse characteristics: $t_p(\text{clock}) \geq 25 \text{ ns}$, $V_{gen} = 3.0 \text{ V}$, $PRR \leq 1.0 \text{ MHz}$.

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Symbol	Parameter	Limits						Unit	Test Condition (Unless Otherwise Specified)
		+ 25°C		+ 125°C		– 55°C			
		Subgroup 1		Subgroup 2		Subgroup 3			
		Min	Max	Min	Max	Min	Max		
V _{OH}	Logical “1” Output Voltage	2.5		2.5		2.5		V	V _{CC} = 4.5 V, I _{OH} = – 0.4 mA, V _{IN} = 2.0 V, V _{IL} = 0.7 V.
V _{OL}	Logical “0” Output Voltage		0.4		0.4		0.4	V	V _{CC} = 4.5 V, I _{OL} = 4.0 mA, V _{IH} = 2.0 V, V _{IL} = 0.7 V.
V _{IC}	Input Clamping Voltage		– 1.5					V	V _{CC} = 4.5 V, I _{IN} = – 18 mA, other inputs are open.
I _{IH}	Logical “1” Input Current (J & K inputs)		20		20		20	μA	V _{CC} = 5.5 V, V _{IH} = 2.7 V, other inputs = 4.5 V, CLR & CLK = GND.
I _{IHH}	Logical “1” Input Current (J & K inputs)		100		100		100	μA	V _{CC} = 5.5 V, V _{IHH} = 5.5 V, J & CLR = 4.5 V, PR & CLK = GND.
I _{IH}	Logical “1” Input Current (CLR & PR)		60		60		60	μA	V _{CC} = 5.5 V, V _{IH} = 2.7 V, other inputs = 4.5 V, CLK & J = GND, PR = (see note 2).
I _{IHH}	Logical “1” Input Current (CLR & PR)		300		300		300	μA	V _{CC} = 5.5 V, V _{IHH} = 5.5 V, J = 4.5 V, CLK & K = GND, CLR = (see note 2).
I _{IH}	Logical “1” Input Current (CLK inputs)		80		80		80	μA	V _{CC} = 5.5 V, V _{IH} = 2.7 V, other inputs are GND.
I _{IHH}	Logical “1” Input Current (CLK inputs)		400		400		400	μA	V _{CC} = 5.5 V, V _{IHH} = 5.5 V, other inputs are GND.
I _{IL}	Logical “0” Input Current (J & K inputs)	– 0.12	– 0.36	– 0.12	– 0.36	– 0.12	– 0.36	mA	V _{CC} = 5.5 V, V _{IL} = 0.4 V, other inputs = 4.5 V, PR = (see note 2).
I _{IL}	Logical “0” Input Current (CLK inputs)	– 0.24	– 0.72	– 0.24	– 0.72	– 0.24	– 0.72	mA	V _{CC} = 5.5 V, V _{IL} = 0.4 V, other inputs = 4.5 V, CLR = (see note 2).
I _{IL}	Logical “0” Input Current (CLR & PR)	– 0.12	– 0.72	– 0.12	– 0.72	– 0.12	– 0.72	mA	V _{CC} = 5.5 V, V _{IL} = 0.4 V, other inputs = 4.5 V, PR is open.
I _{OS}	Output Short Circuit Current	– 15	– 100	– 15	– 100	– 15	– 100	mA	V _{CC} = 5.5 V, V _{IN} = 4.5 V, other inputs = GND.
I _{CC}	Power Supply Current		8.0		8.0		8.0	mA	V _{CC} = 5.5 V, other inputs are open.
V _{IH}	Logical “1” Input Voltage	2.0		2.0		2.0		V	V _{CC} = 4.5 V.
V _{IL}	Logical “0” Input Voltage		0.7		0.7		0.7	V	V _{CC} = 4.5 V.
	Functional Tests	Subgroup 7		Subgroup 8A		Subgroup 8B			per Truth Table with V _{CC} = 5.0 V, V _{INL} = 0.V, and V _{INH} = 2.5 V.

NOTES:

1. =  2.5 V min/5.5 V max
2. =  2.5 V min/5.5 V max

54LS112A

Symbol	Parameter	Limits						Unit	Test Condition (Unless Otherwise Specified)
	Switching Parameters:	+ 25°C		+ 125°C		– 55°C			
		Subgroup 9		Subgroup 10		Subgroup 11			
		Min	Max	Min	Max	Min	Max		
t _{PHL1} t _{PHL1}	Propagation Delay /Data-Output Output <u>High-Low</u>	5.0 —	28 20	5.0 —	40 35	5.0 —	40 35	ns	V _{CC} = 5.0 V, C _L = 50 pF, R _L = 2.0 kΩ ± 5.0%. V _{CC} = 5.0 V, C _L = 15 pF R _L = 2.0 kΩ ± 5.0%.
t _{PLH1} t _{PLH1}	Propagation Delay /Data-Output Output <u>Low-High</u>	5.0 —	21 20	5.0 —	32 27	5.0 —	32 27	ns	V _{CC} = 5.0 V, C _L = 50 pF, R _L = 2.0 kΩ ± 5.0%. V _{CC} = 5.0 V, C _L = 15 pF, R _L = 2.0 kΩ ± 5.0%.
t _{PHL2}	Propagation Delay /Data-Output Output <u>High-Low</u>	5.0	30	5.0	42	5.0	42	ns	V _{CC} = 5.0 V, C _L = 50 pF, R _L = 2.0 kΩ ± 5.0%.
t _{PLH2}	Propagation Delay /Data-Output Output <u>Low-High</u>	5.0	22	5.0	32	5.0	32	ns	V _{CC} = 5.0 V, C _L = 50 pF, R _L = 2.0 kΩ ± 5.0%.
f _{MAX}	Maximum Clock Frequency	25		25		25		MHz	V _{CC} = 5.0 V, V _{IN} = 2.7 V, C _L = 50 pF, R _L = 2.0 kΩ ± 5.0%.
f _{MAX}	Maximum Clock Frequency	30						MHz	V _{CC} = 5.0 V, C _L = 15 pF, R _L = 2.0 kΩ ± 5.0%.

NOTES:

1. f_{MAX}, min. limit specified is the frequency of the input pulse. The output frequency shall be one-half of the input frequency.
2. Tests shall be performed in sequence, attributes data only.
3. The limits specified for C_L = 15 pF are guaranteed but not tested.