

FEATURES

14 Ω (maximum) on resistance
1.4 Ω (maximum) on-resistance flatness
2.7 V to 5.5 V single supply
 ± 2.7 V to ± 5.5 V dual supply
Rail-to-rail operation
8-lead SOT-23
Typical power consumption (<0.1 μ W)
TTL-/CMOS-compatible inputs
Supports defense and aerospace applications
(AQEC standard)
Military temperature range: -55°C to $+125^{\circ}\text{C}$
Controlled manufacturing baseline
One assembly and test site
One fabrication site
Enhanced product change notification
Qualification data available on request

APPLICATIONS

Automatic test equipment
Power routing
Communication systems
Data acquisition systems
Sample-and-hold systems
Avionics
Relay replacement
Battery-powered systems

GENERAL DESCRIPTION

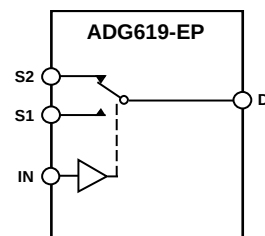
The ADG619-EP is a monolithic, CMOS single-pole double-throw (SPDT) switch.

The ADG619-EP offers a low on resistance of 4 Ω , which is matched to within 0.7 Ω between channels. These switches also provide low power dissipation, yet result in high switching speeds. The ADG619-EP exhibits break-before-make switching action, thus preventing momentary shorting when switching channels.

The ADG619-EP is available in an 8-lead SOT-23 package.

Additional application and technical information can be found in the [ADG619](#) data sheet.

FUNCTIONAL BLOCK DIAGRAM



NOTES
 1. SWITCHES SHOWN FOR
 A LOGIC 1 INPUT.

08844-001

Figure 1.

PRODUCT HIGHLIGHTS

1. Low on resistance (R_{ON}): 4 Ω typical.
2. Dual ± 2.7 V to ± 5.5 V or single 2.7 V to 5.5 V supplies.
3. Low power dissipation.
4. Fast t_{ON}/t_{OFF} .
5. Tiny, 8-lead SOT-23 package.

Rev. 0

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TABLE OF CONTENTS

Features	1	Single Supply.....	4
Applications.....	1	Absolute Maximum Ratings	5
Functional Block Diagram	1	ESD Caution.....	5
General Description	1	Pin Configurations and Function Descriptions	6
Product Highlights	1	Typical Performance Characteristics	7
Revision History	2	Test Circuits.....	8
Specifications.....	3	Outline Dimensions	10
Dual Supply	3	Ordering Guide	10

REVISION HISTORY

11/10—Revision 0: Initial Version

SPECIFICATIONS

DUAL SUPPLY

$V_{DD} = +5\text{ V} \pm 10\%$, $V_{SS} = -5\text{ V} \pm 10\%$, GND = 0 V. All specifications -55°C to $+125^{\circ}\text{C}$, unless otherwise noted.

Table 1.

Parameter	+25°C	−55°C to +125°C	Unit	Test Conditions/Comments
ANALOG SWITCH				
Analog Signal Range		V_{SS} to V_{DD}	V	$V_{DD} = +4.5\text{ V}$, $V_{SS} = -4.5\text{ V}$
On Resistance (R_{ON})	4		Ω typ	$V_S = \pm 4.5\text{ V}$, $I_{DS} = -10\text{ mA}$; see Figure 9
	6.5	10	Ω max	
R_{ON} Match Between Channels (ΔR_{ON})	0.7		Ω typ	$V_S = \pm 4.5\text{ V}$, $I_{DS} = -10\text{ mA}$
	1.1	1.45	Ω max	
On-Resistance Flatness ($R_{FLAT(ON)}$)	0.7		Ω typ	$V_S = \pm 3.3\text{ V}$, $I_{DS} = -10\text{ mA}$
	1.35	1.6	Ω max	
LEAKAGE CURRENTS				
Source Off Leakage, I_S (Off)	± 0.01		nA typ	$V_{DD} = +5.5\text{ V}$, $V_{SS} = -5.5\text{ V}$
	± 0.25	± 3	nA max	$V_S = \pm 4.5\text{ V}$, $V_D = \mp 4.5\text{ V}$; see Figure 10
Channel On Leakage, I_D , I_S (On)	± 0.01		nA typ	$V_S = V_D = \pm 4.5\text{ V}$; see Figure 11
	± 0.25	± 25	nA max	
DIGITAL INPUTS				
Input High Voltage, V_{INH}		2.4	V min	$V_{IN} = V_{INL}$ or V_{INH}
Input Low Voltage, V_{INL}		0.8	V max	
Input Current, I_{INL} or I_{INH}	0.005		μA typ	
		± 0.1	μA max	
Digital Input Capacitance, C_{IN}	2		pF typ	
DYNAMIC CHARACTERISTICS¹				
t_{ON}	80		ns typ	$R_L = 300\ \Omega$, $C_L = 35\text{ pF}$
	120	215	ns max	$V_S = 3.3\text{ V}$; see Figure 12
t_{OFF}	45		ns typ	$R_L = 300\ \Omega$, $C_L = 35\text{ pF}$
	75	105	ns max	$V_S = 3.3\text{ V}$; see Figure 12
Break-Before-Make Time Delay, t_{BBM}	40		ns typ	$R_L = 300\ \Omega$, $C_L = 35\text{ pF}$
		10	ns min	$V_{S1} = V_{S2} = 3.3\text{ V}$; see Figure 13
Charge Injection	110		pC typ	$V_S = 0\text{ V}$, $R_S = 0\ \Omega$, $C_L = 1\text{ nF}$; see Figure 14
Off Isolation	−67		dB typ	$R_L = 50\ \Omega$, $C_L = 5\text{ pF}$, $f = 1\text{ MHz}$; see Figure 15
Channel-to-Channel Crosstalk	−67		dB typ	$R_L = 50\ \Omega$, $C_L = 5\text{ pF}$, $f = 1\text{ MHz}$; see Figure 16
Bandwidth −3 dB	190		MHz typ	$R_L = 50\ \Omega$, $C_L = 5\text{ pF}$; see Figure 17
C_S (Off)	25		pF typ	$f = 1\text{ MHz}$
C_D , C_S (On)	95		pF typ	$f = 1\text{ MHz}$
POWER REQUIREMENTS				
I_{DD}	0.001		μA typ	$V_{DD} = +5.5\text{ V}$, $V_{SS} = -5.5\text{ V}$
		1.0	μA max	Digital inputs = 0 V or 5.5 V
I_{SS}	0.001		μA typ	Digital inputs = 0 V or 5.5 V
		1.0	μA max	

¹ Guaranteed by design, not subject to production test.

ADG619-EP

SINGLE SUPPLY

$V_{DD} = 5\text{ V} \pm 10\%$, $V_{SS} = 0\text{ V}$, $GND = 0\text{ V}$. All specifications -55°C to $+125^{\circ}\text{C}$, unless otherwise noted.

Table 2.

Parameter	+25°C	−55°C to +125°C	Unit	Test Conditions/Comments
ANALOG SWITCH				
Analog Signal Range		0 V to V_{DD}	V	$V_{DD} = 4.5\text{ V}$, $V_{SS} = 0\text{ V}$
On Resistance (R_{ON})	7	14	Ω typ Ω max	$V_S = 0\text{ V}$ to 4.5 V , $I_{DS} = -10\text{ mA}$; see Figure 9
R_{ON} Match Between Channels (ΔR_{ON})	0.8	1.4	Ω typ Ω max	$V_S = 0\text{ V}$ to 4.5 V , $I_{DS} = -10\text{ mA}$
On-Resistance Flatness ($R_{FLAT(ON)}$)	0.5	1.4	Ω typ Ω max	$V_S = 1.5\text{ V}$ to 3.3 V , $I_{DS} = -10\text{ mA}$
LEAKAGE CURRENTS				
Source Off Leakage, I_S (Off)	± 0.01	± 3	nA typ nA max	$V_{DD} = 5.5\text{ V}$ $V_S = 1\text{ V}/4.5\text{ V}$, $V_D = 4.5\text{ V}/1\text{ V}$; see Figure 10
Channel On Leakage, I_{D1} , I_S (On)	± 0.01 ± 0.25	± 25	nA typ nA max	$V_S = V_D = 1\text{ V}/4.5\text{ V}$; see Figure 11
DIGITAL INPUTS				
Input High Voltage, V_{INH}		2.4	V min	$V_{IN} = V_{INL}$ or V_{INH}
Input Low Voltage, V_{INL}		0.8	V max	
Input Current, I_{INL} or I_{INH}	0.005	± 0.1	μA typ μA max	
Digital Input Capacitance, C_{IN}	2		pF typ	
DYNAMIC CHARACTERISTICS¹				
t_{ON}	120	390	ns typ	$R_L = 300\ \Omega$, $C_L = 35\text{ pF}$
	220		ns max	$V_S = 3.3\text{ V}$; see Figure 12
t_{OFF}	50	135	ns typ	$R_L = 300\ \Omega$, $C_L = 35\text{ pF}$
	75		ns max	$V_S = 3.3\text{ V}$; see Figure 12
Break-Before-Make Time Delay, t_{BBM}	70	10	ns typ	$R_L = 300\ \Omega$, $C_L = 35\text{ pF}$
			ns min	$V_{S1} = V_{S2} = 3.3\text{ V}$; see Figure 13
Charge Injection	6		pC typ	$V_S = 0\text{ V}$, $R_S = 0\ \Omega$, $C_L = 1\text{ nF}$; see Figure 14
Off Isolation	−67		dB typ	$R_L = 50\ \Omega$, $C_L = 5\text{ pF}$, $f = 1\text{ MHz}$; see Figure 15
Channel-to-Channel Crosstalk	−67		dB typ	$R_L = 50\ \Omega$, $C_L = 5\text{ pF}$, $f = 1\text{ MHz}$; see Figure 16
Bandwidth −3 dB	190		MHz typ	$R_L = 50\ \Omega$, $C_L = 5\text{ pF}$; see Figure 17
C_S (OFF)	25		pF typ	$f = 1\text{ MHz}$
C_{D1} , C_S (ON)	95		pF typ	$f = 1\text{ MHz}$
POWER REQUIREMENTS				
I_{DD}	0.001	1.0	μA typ μA max	$V_{DD} = 5.5\text{ V}$ Digital inputs = 0 V or 5.5 V

¹ Guaranteed by design, not subject to production test.

ABSOLUTE MAXIMUM RATINGS

$T_A = 25^\circ\text{C}$, unless otherwise noted.

Table 3.

Parameter	Rating
V_{DD} to V_{SS}	13 V
V_{DD} to GND	$-0.3\text{ V to }+6.5\text{ V}$
V_{SS} to GND	$+0.3\text{ V to }-6.5\text{ V}$
Analog Inputs ¹	$V_{SS} - 0.3\text{ V to }V_{DD} + 0.3\text{ V}$
Digital Inputs ¹	$-0.3\text{ V to }V_{DD} + 0.3\text{ V}$ or 30 mA (whichever occurs first)
Peak Current, S or D	100 mA (pulsed at 1 ms, 10% duty cycle maximum)
Continuous Current, S or D	50 mA
Operating Temperature Range	$-55^\circ\text{C to }+125^\circ\text{C}$
Storage Temperature Range	$-65^\circ\text{C to }+150^\circ\text{C}$
Junction Temperature	150°C
Thermal impedance	
θ_{JA}	229.6°C/W
θ_{JC}	91.99°C/W
Lead Soldering	
Reflow, Peak Temperature	$260(+0/-5)^\circ\text{C}$
Time at Peak Temperature	20 sec to 40 sec

¹ Overvoltages at IN, S, or D are clamped by internal diodes. Current should be limited to the maximum ratings given.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Only one absolute maximum rating may be applied at a time.

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

ADG619-EP

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

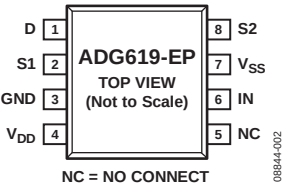


Figure 2. 8-Lead SOT-23 (RJ-8)

Table 4. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	D	Drain Terminal. Can be an input or output.
2	S1	Source Terminal. Can be an input or output.
3	GND	Ground (0 V) Reference.
4	V _{DD}	Most Positive Power Supply.
5	NC	No Connect. Not internally connected.
6	IN	Logic Control Input.
7	V _{SS}	Most Negative Power Supply. This pin is only used in dual-supply applications and should be tied to ground in single-supply applications.
8	S2	Source Terminal. Can be an input or output.

Table 5. Truth Table for the ADG619-EP

IN	Switch S1	Switch S2
0	On	Off
1	Off	On

TYPICAL PERFORMANCE CHARACTERISTICS

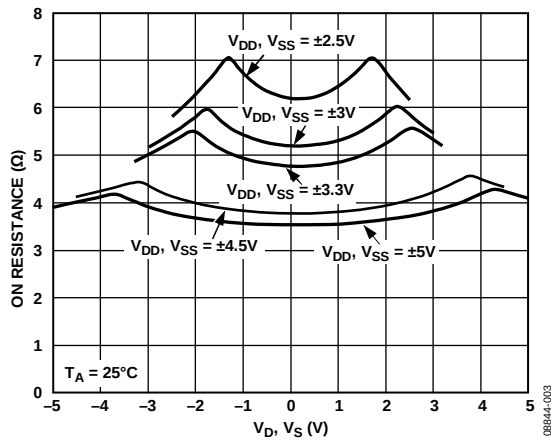


Figure 3. On Resistance vs. V_D , V_S (Dual Supply)

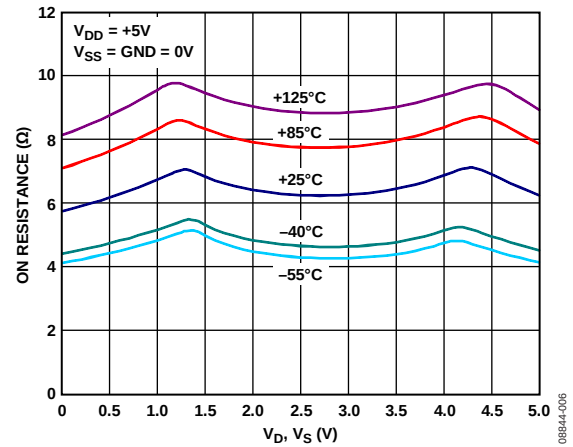


Figure 6. On Resistance vs. V_D , V_S for Different Temperatures (Single Supply)

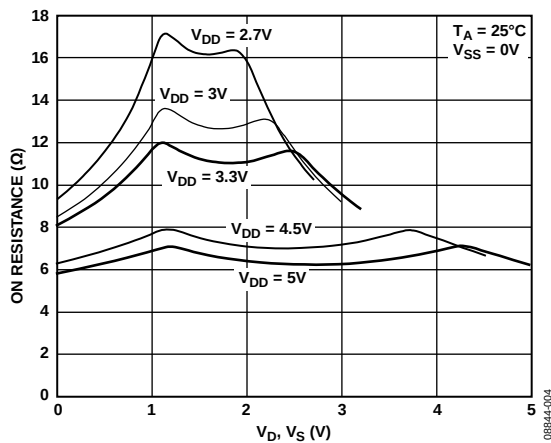


Figure 4. On Resistance vs. V_D , V_S (Single Supply)

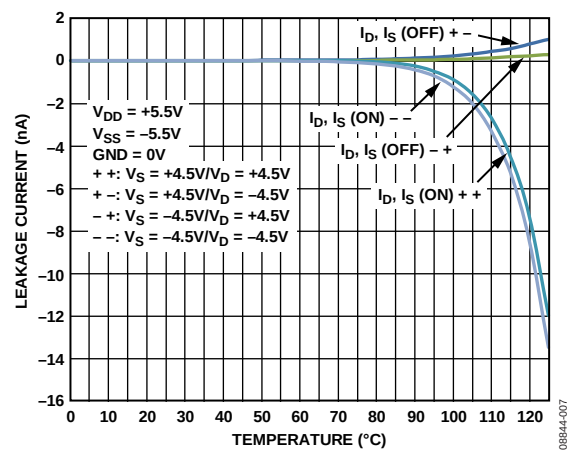


Figure 7. Leakage Currents vs. Temperature (Dual Supply)

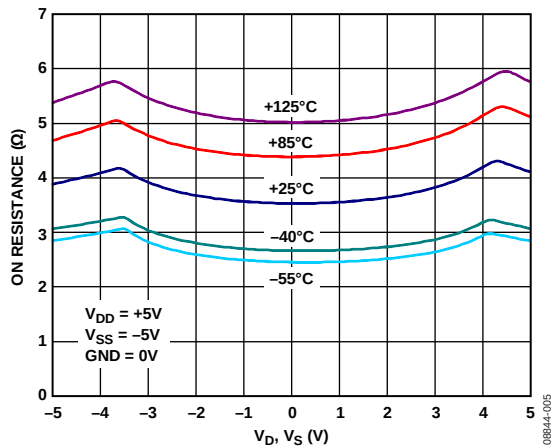


Figure 5. On Resistance vs. V_D , V_S for Different Temperatures (Dual Supply)

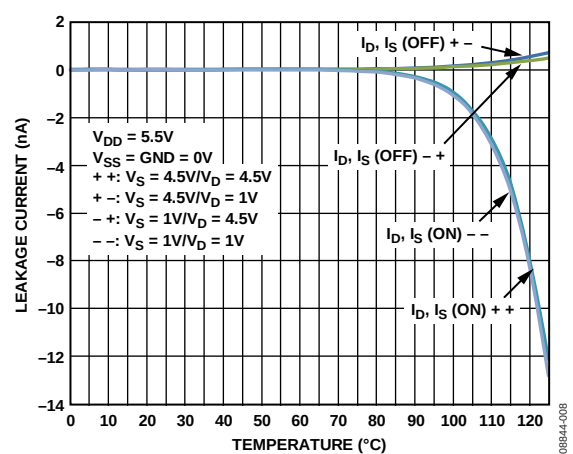


Figure 8. Leakage Currents vs. Temperature (Single Supply)

TEST CIRCUITS

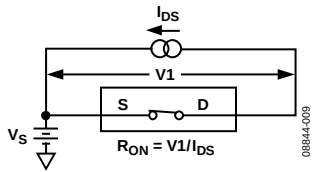


Figure 9. On Resistance

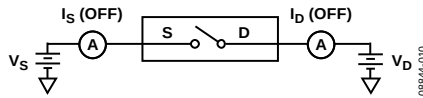


Figure 10. Off Leakage

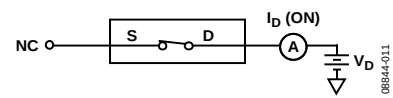


Figure 11. On Leakage

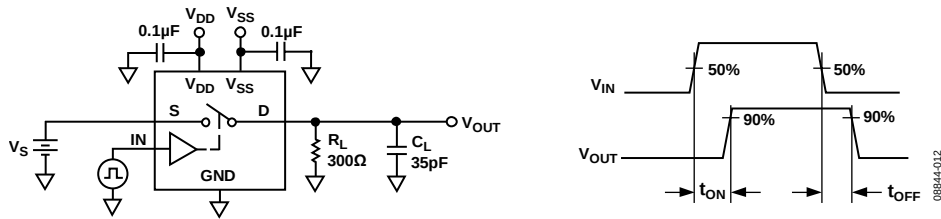


Figure 12. Switching Times

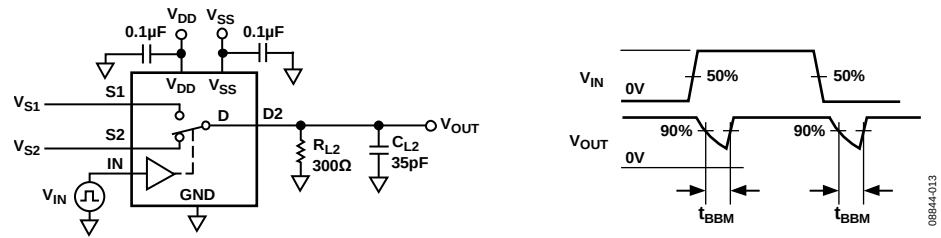


Figure 13. Break-Before-Make Time Delay, t_{BBM}

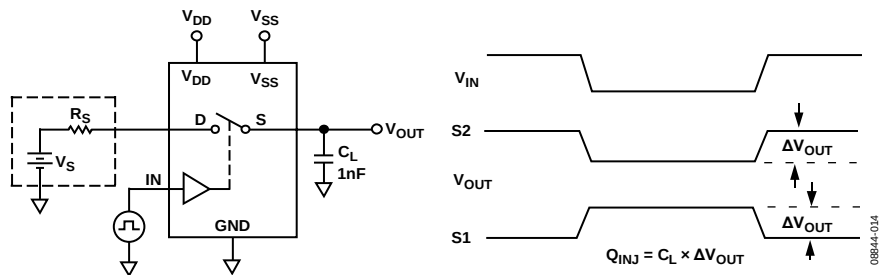


Figure 14. Charge Injection

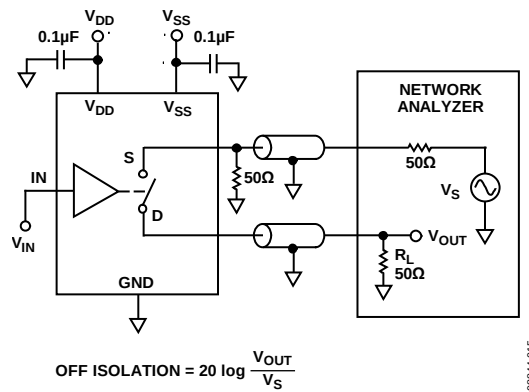
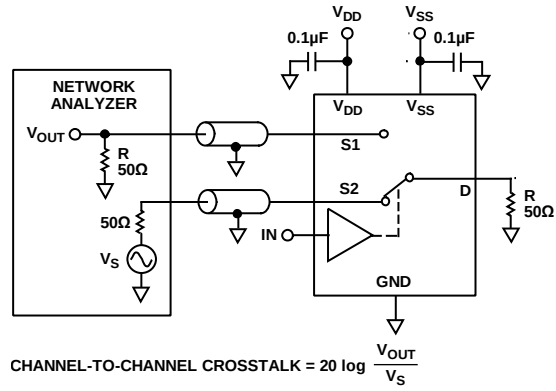
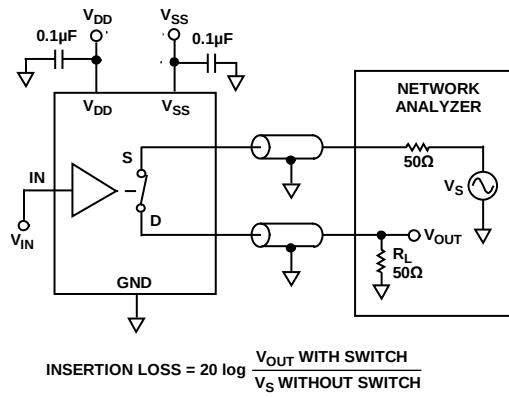


Figure 15. Off Isolation



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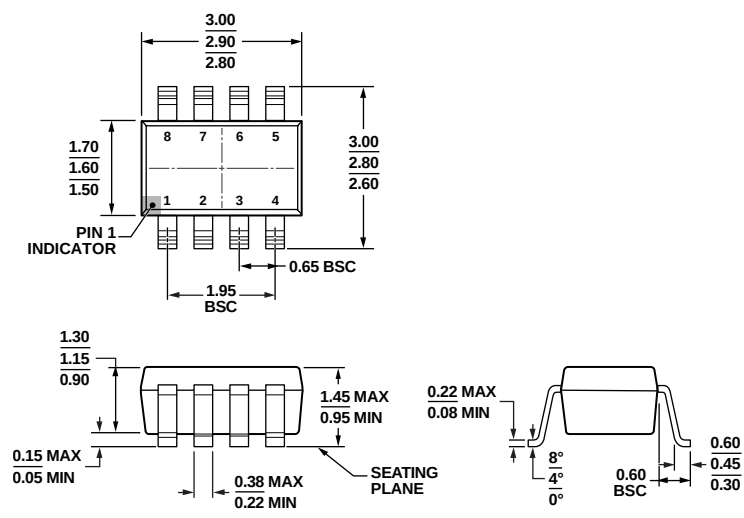
Figure 16. Channel-to-Channel Crosstalk



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Figure 17. Bandwidth

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-178-BA
Figure 18. 8-Lead Small Outline Transistor Package [SOT-23]
(RJ-8)
Dimensions shown in millimeters

ORDERING GUIDE

Model ¹	Temperature Range	Package Description	Package Option	Branding ²
ADG619SRJZ-EP-RL7	–55°C to +125°C	8-Lead Small Outline Transistor Package [SOT-23]	RJ-8	S3V

¹ Z =RoHS Compliant Part.
² Branding on SOT-23 packages is limited to three characters due to space constraints

NOTES

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