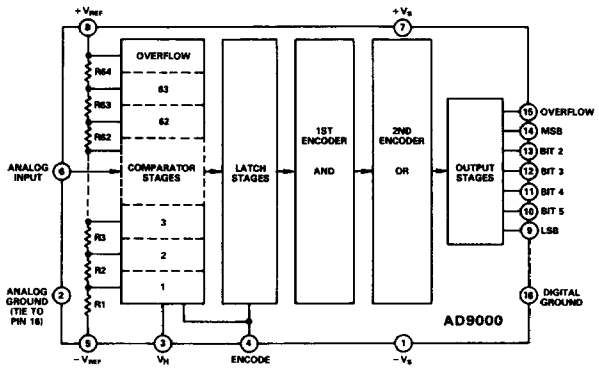
High Speed 6-Bit A/D Converter

AD9000

FEATURES
77MSPS Encode Rate
Bipolar Input Range
Low Error Rate
Overflow Bit
MIL-STD-883 Compliant Versions Available

APPLICATIONS
QAM Telecommunications
Electronic Warfare (ECM, ECCM, ESM)
Radar Guidance Digitizers

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD9000 is a 6-bit, high speed, analog-to-digital converter with ECL compatible outputs and a bipolar input stage. The AD9000 is fabricated in a high-performance bipolar process which allows encode rates up to 77MSPS.

The AD9000 employs the standard flash converter architecture based on 64 individual comparators which simultaneously determine the precise analog signal level. The comparators are followed by two stages of decoding logic, allowing the AD9000 to operate with a very low error rate. The low 35pF input capacitance of the AD9000 greatly simplifies the analog driver stage. Also incorporated into the AD9000 design is an overflow output bit as well as a hysteresis control pin to modify comparator sensitivity.

The AD9000 is offered as both an commercial temperature range device 0 to +70°C, and as an extended temperature range device −55°C to +125°C. Both versions are available packaged in a 16-pin ceramic DIP. The extended temperature range device is also available in a 28-pin ceramic LCC package. The extended temperature range versions are offered as fully compliant MIL-STD-883 Class B devices.

AD9000 – SPECIFICATIONS

ELECTRICAL CHARACTERISTICS (Supply Voltages = −5.2V and +5.0V; Differential Reference Voltage = 2.0V unless otherwise stated)

Parameter	Temp	Commercial 0 to +70°C AD9000JD Min	Typ	Max	Military −55°C to +125°C AD9000SD/SE Min	Typ	Max	Units
RESOLUTION		6			6			Bits
DC ACCURACY								
Differential Linearity	+25°C		0.25	0.5		0.25	0.5	LSB
	Full			1.0			1.0	LSB
Integral Linearity	+25°C		0.25	0.5		0.25	0.5	LSB
	Full			1.0			1.0	LSB
No Missing Codes	Full		GUARANTEED			GUARANTEED		
INITIAL OFFSET ERROR								
Top of Reference Ladder	+25°C		0.3	7/8		0.3	7/8	LSB
	Full			1.5			1.5	LSB
Bottom of Reference Ladder	+25°C		0.25	7/8		0.25	7/8	LSB
	Full			1.5			1.5	LSB
Offset Drift Coefficient	Full		145			145		µV/°C
ANALOG INPUT								
Input Voltage Range	Full		±2.0V			±2.0V		V
Input Bias Current (Sampling)[1]	Full			800			800	µA
Input Bias Current (Latched)[1]	Full			20			20	µA
Input Resistance	+25°C		3.0			3.0		kΩ
Input Capacitance	+25°C		35	50		35	50	pF
Full Power Bandwidth[2]	+25°C		20			20		MHz
REFERENCE INPUT[3,4]								
Reference Ladder Resistance	+25°C	80		200	80		200	Ω
Ladder Temperature Coefficient			0.275			0.275		Ω/°C
Reference Input Bandwidth	+25°C		20			20		MHz
DYNAMIC PERFORMANCE[5]								
Conversion Rate	+25°C	50	70		75	77		MHz
Conversion Time (+1 Clock)	+25°C			20			13.3	ns
Aperture Delay (t_D)	+25°C		2			2		ns
Aperture Uncertainty (Jitter)	+25°C		25			25		ps
Output Propagation Delay (t_{PD})[6]	+25°C	8		12	8		12	ns
Output Hold Time (t_{OH})[7]	+25°C	8		14	8		14	ns
Transient Response[8]	+25°C		13			13		ns
Overvoltage Recovery Time[9]	+25°C		11			11		ns
Output Rise Time[10]	+25°C			5.0			4.5	ns
Output Fall Time[10]	+25°C			5.0			4.5	ns
Output Time Skew	+25°C		0.4			0.4		ns
ENCODE INPUT								
Logic "1" Voltage	Full	−1.1			−1.1			V
Logic "0" Voltage	Full			−1.5			−1.5	V
Logic "1" Current	Full			100			100	µA
Logic "0" Current	Full			100			100	µA
Input Capacitance	+25°C		2.5	5.0		2.5	5.0	pF
ENCODE Pulse Width High (t_{PWH})	+25°C	6.6			6.6			ns
ENCODE Pulse Width Low (t_{PWL})	+25°C	6.6			6.6			ns

ELECTRICAL CHARACTERISTICS (Continued)

Parameter	Temp	Commercial 0 to +70°C AD9000JD Min	Typ	Max	Military −55°C to +125°C AD9000SD/SE Min	Typ	Max	Units
AC LINEARITY[11]								
Dynamic Linearity[12]	+25°C		0.5			0.5		LSB
In-Band Harmonics								
(DC to 1MHz)	+25°C		44			44		dBc
(1MHz to 5MHz)	+25°C		42			42		dBc
(5MHz to 8MHz)	+25°C		38			38		dBc
Signal to Noise Ratio[13]	+25°C	31	33		31	33		dB
Signal to Noise Ratio[14]	+25°C	40	42		40	42		dB
Two Tone Intermodulation Rejection[15]	+25°C		46			46		dBc
Noise Power Ratio (NPR)[16]	+25°C		30			30		dBc
DIGITAL OUTPUTS[5]								
Logic "1" Voltage	Full	−1.1			−1.1			V
Logic "0" Voltage	Full			−1.5			−1.5	V
POWER SUPPLY[17]								
Positive Supply Current (+5.0V)	+25°C		60	70		60	70	mA
	Full			75			75	mA
Negative Supply Current (−5.2V)	+25°C		68	80		68	80	mA
	Full			85			85	mA
Nominal Power Dissipation	+25°C		675			675		mW
Reference Ladder Dissipation	+25°C		20			20		mW

NOTES
[1] $A_{IN} = +V_{REF}$.
[2] Determined by 3dB reduction in reconstructed output at 75MSPS.
[3] Under normal operating conditions, the analog input voltages should not exceed nominal ±2V operating range, nor the supply voltages ($+V_S$ and $-V_S$), whichever is smaller.
[4] Under normal operating conditions the differential reference voltage may range from ±0.5V to ±2V; $+V_{REF} \geq -V_{REF}$.
[5] Output terminated with 100Ω resistors to −2.0V.
[6] Measured from the leading edge of ENCODE to data out on Bit 1 (MSB).
[7] Measured from the trailing edge of ENCODE to data out on Bit 1 (MSB).
[8] For full-scale step input, 6-bit accuracy is attained in specified time.
[9] Recovers to 6-bit accuracy in specified time, after 150% full-scale input overvoltage.
[10] Measured on Bit 1 (MSB) only.
[11] Measured at 50MSPS encode rate.
[12] Analog input frequency = 15MHz.
[13] RMS signal to RMS noise, with 540kHz analog input signal.
[14] Peak-to-peak signal to rms noise, with 540kHz analog input signal.
[15] $f_1 = 9.3$MHz; $f_2 = 7.6$MHz; Encode = 42MHz.
[16] DC to 8.2MHz noise bandwidth with 3.886MHz slot.
[17] Supply voltage should remain stable within ±5% for normal operation.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS[1]

Positive Supply Voltage . . . . . −0.3V to +6V
Negative Supply Voltage . . . . . −6.0V to +0.3V
Analog-to-Digital Ground Voltage Differential 0.5
Analog Input Voltages (A_{IN}, $+V_{REF}$, $-V_{REF}$)[2] . . . . . ±3V
Differential Reference Voltage ($+V_{REF}$ to $-V_{REF}$)[3] 6V
ENCODE Input Voltage . . . . . $-V_S$ to 0V
HYSTERESIS Control Voltage . . . . . 0V to +3.0V
Digital Output Current 20mA
Power Dissipation (+25°C Free Air)[4] 745mW
Operating Temperature Range
AD9000JD . . . . . 0 to +70°C
AD9000SD/SE . . . . . −55°C to +125°C
Storage Temperature Range . . . . . −65°C to +150°C
Junction Temperature . . . . . +175°C
Lead Soldering Temperature (10sec) . . . . . +300°C

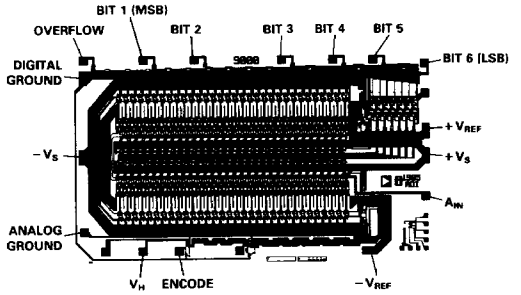
NOTES
[1] Absolute maximum ratings are limiting values, to be applied individually, and beyond which serviceability of the circuit may be impaired. Functional operability under any of these conditions is not necessarily implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
[2] Under normal operating conditions, the analog input voltages should not exceed nominal ±2V operating range, nor the supply voltages ($+V_S$ and $-V_S$), whichever is smaller.
[3] Under normal operating conditions the differential reference voltage may range from ±0.5V to ±2V; $+V_{REF} \geq -V_{REF}$.
[4] Typical thermal impedances . . .
16-Pin Ceramic $\theta_{ja} = 67°C/W$; $\theta_{jc} = 7°C/W$
28-Pin LCC $\theta_{ja} = 62°C/W$; $\theta_{jc} = 14°C/W$

ORDERING GUIDE

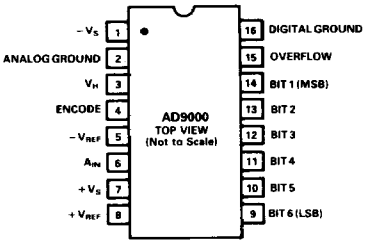
Model[1]	Temperature Range	Description	Package Option[2]
AD9000JD	0 to +70°C	16-Pin DIP, Industrial	D-16
AD9000SD	−55°C to +125°C	16-Pin DIP	D-16
AD9000SE	−55°C to +125°C	28-Pin LCC	E-28A

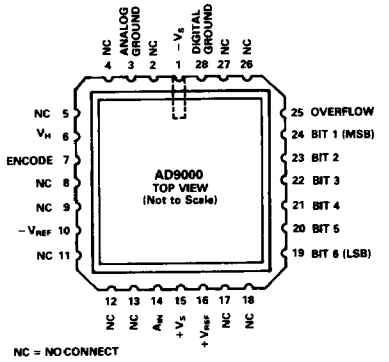
NOTES
[1]MIL-STD-883 versions available, contact factory.
[2]D = Ceramic DIP; E = Leadless Ceramic Chip Carrier. For outline information see Package Information section.

DIE LAYOUT



PIN DESIGNATIONS



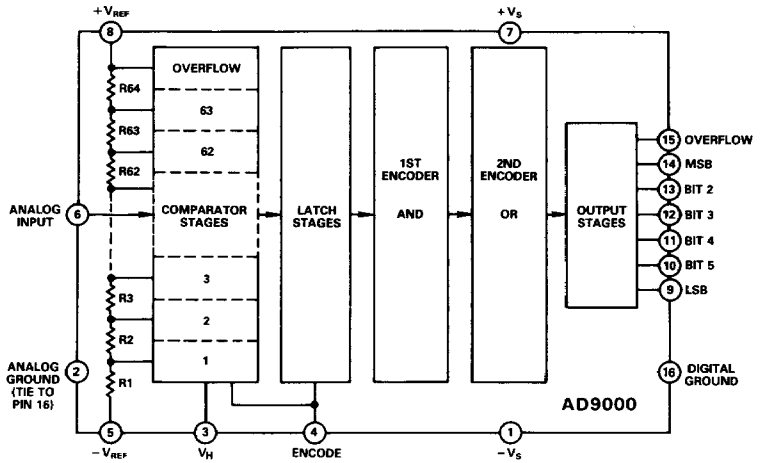


MECHANICAL INFORMATION

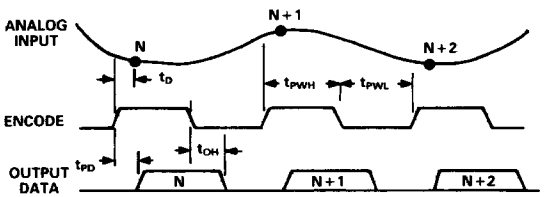
Die Dimensions	129×217×15 (±2) mils
Pad Dimensions	4×4 mils
Metalization	10,000Å Aluminum
Backing	None
Substrate Potential	$-V_S$
Passivation	10,000Å Oxynitride
Die Attach	Gold Eutectic
Bond Wire	1.25 mil Aluminum; Ultrasonic Bonding or 1mil Gold; Gold Ball Bonding

FUNCTIONAL DESCRIPTION

PIN NAME	DESCRIPTION
$-V_S$	Negative supply terminal, nominally −5.2V.
ANALOG GROUND	Analog ground return. All grounds should be connected together near the the AD9000.
$V_{HYSTERESIS}$	The hysteresis control voltage varies the comparator hysteresis from 15mV to 50mV, for a change of 0V to +3V at the hysteresis control pin.
ENCODE	The ENCODE pin controls the conversion cycle. Encode is rising edge sensitive and should be driven with a 50% duty-cycle waveform under normal conditions.
$-V_{REF}$	The most negative reference voltage for the internal resistor ladder.
ANALOG INPUT	Analog input pin.
$+V_S$	Positive supply terminal, nominally +5.0V.
$+V_{REF}$	Most positive reference voltage of the internal resistor ladder.
BIT 6 (LSB)	One of six digital outputs. BIT 6 (LSB) is the least-significant-bit of the digital output.
BIT 5 – BIT 2	One of six digital outputs.
BIT 1 (MSB)	One of six digital outputs. BIT1 (MSB) is the most-significant-bit of the digital output.
OVERFLOW	Overflow data output. Logic high indicates an input overvoltage ($A_{IN} \geq +V_{REF}$).
DIGITAL GROUND	Digital ground return. All grounds should be connected together near the AD9000.

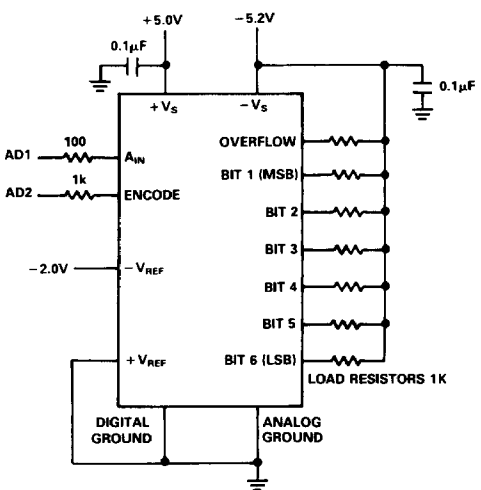


AD9000 Functional Block Diagram

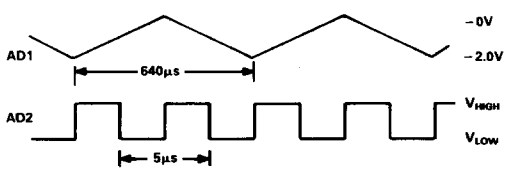


t_D	APERTURE DELAY
t_{PD}	OUTPUT PROPAGATION DELAY
t_{OH}	MINIMUM OUTPUT HOLD TIME
t_{PWH}	MINIMUM ENCODE PULSE WIDTH HIGH
t_{PWL}	MINIMUM ENCODE PULSE WIDTH LOW

System Timing Diagram



ALL RESISTORS ±5%
ALL CAPACITORS ±20%
ALL SUPPLY VOLTAGES ±5%
OPTION #1: (STATIC) AD1 = 0.0V, AD2 = LOGIC HIGH
OPTION #2: (DYNAMIC) SEE WAVEFORMS



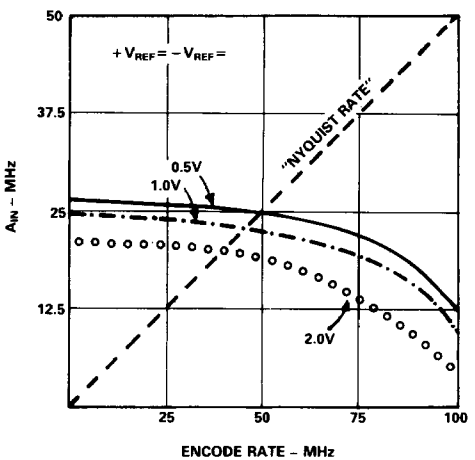
Burn-In Test Circuit

ABOUT THE AD9000

Analog Bandwidth

Quantifying the high-frequency analog performance of the AD9000 is somewhat difficult because of the various criteria that can be applied. At one extreme there is the analog input bandwidth of a single input comparator (which tends to be extremely high). At the other end of the performance criteria is the "no missing codes" restriction, which tends to be the most conservative measure of analog bandwidth.

The "no missing codes" criteria simply means that the converter is capable of generating all 64 output codes for an analog and ENCODE frequency. At higher ENCODE rates to analog frequencies, the converter continues to function, but with reduced resolution. The graph below details the "no missing codes" region of operation for the AD9000 at several reference levels. Note that nearly all analog-to-digital converter applications operate in the oversampled region to avoid generation of indeterminate data (aliasing).

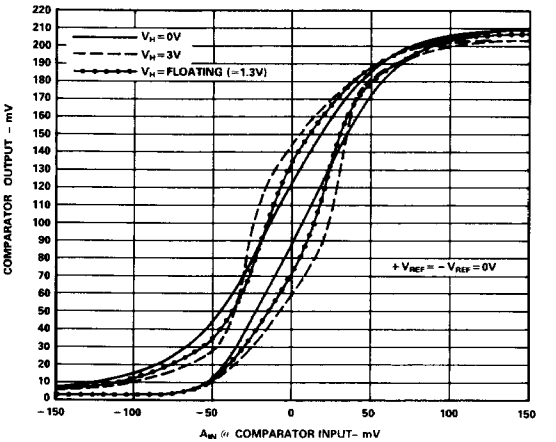


Analog Input vs. Encode Rate "No Missing Codes"

High-Speed Performance Enhancements

The AD9000 employs a hysteresis control pin which affects comparator sensitivity. The error rate (number of full-scale errors in a given period) is directly affected by the comparator sensitivity. By varying the voltage on the hysteresis control pin, the error rate can be reduced. The AD9000 is capable of extremely low error rate operation, which makes it ideal for error sensitive applications like QAM demodulation. If the hysteresis control pin is used, it should be decoupled to ground through a 0.1μF capacitor, otherwise it may be left floating.

At the highest encode rates, overall accuracy can be improved by skewing the ENCODE signal duty-cycle to allow more time in the "latch" mode. Specifically, extending the logic HIGH portion of the ENCODE signal allows the comparators more time to achieve an appropriate logic level prior to the decoding cycle that begins on the rising edge of the ENCODE pulse.



Comparator Switching vs. Hysteresis Voltage

Layout Considerations

The AD9000, like all high-speed circuits, requires certain precautions be taken to insure optimum performance. The foremost of these is the use of a substantial low impedance ground plane around and under the AD9000. Just as important are high quality ground connections to the AD9000 itself. It is probably more effective to keep the analog and digital grounds separate, except at the AD9000 where they should be connected together. Sockets should generally be avoided due to the increased interlead capacitance they induce. If socketing must be used, pin sockets are preferred.

Decoupling is especially important to high-speed analog circuits. Each supply should be decoupled to ground with 0.1μF ceramic and 0.001μF mica capacitors. The ladder reference pins should be treated in a similar manner. In addition to decoupling the reference ladder, the reference ladder should be driven from a low output impedance source for the best noise rejection. In all cases, chip capacitors are recommended, where practical, to reduce the effects of lead inductance associated with standard discrete capacitors.

MIL-STD-883 Compliance Information

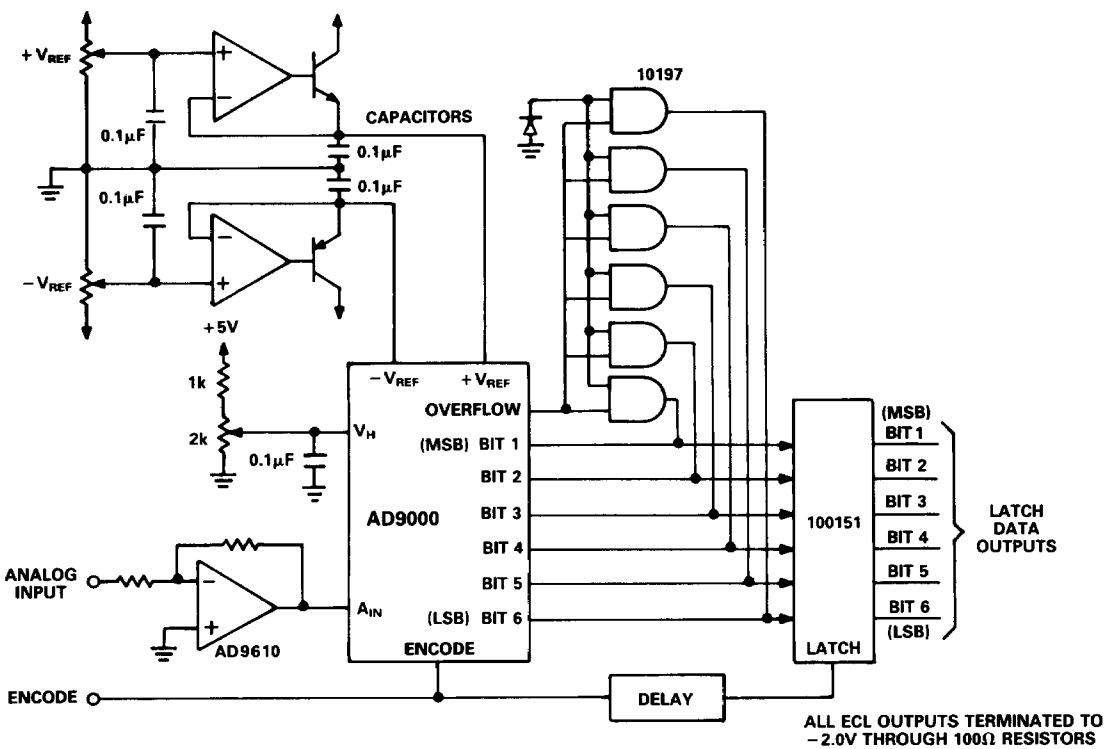
The AD9000SE/SD/883C are classified within microcircuits group 57-technology group D (bipolar A/D converters), and are constructed in accordance with the latest revision of MIL-STD-883. The AD9000 is electrostatic sensitive and falls within electrostatic sensitivity classification Category A. PDA (Percent Defective Allowance) is computed based of Subgroups 1 of the specified Group A test list. QA screening is in accordance with "Alternate Method A" of method 5005. The following apply: Burn-In per 1015, Life Test per 1005, Electrical Testing per 5004. (Note: Group A electrical Testing assumes $T_A = T_C = T_J$.)

TYPICAL APPLICATION

The AD9000 is a relatively flexible device which can be configured in a number of ways. One very useful feature of the AD9000 is the open emitter outputs. The open emitters allow the outputs of several AD9000s to be OR-WIRED in stacking applications for increased resolution. This kind of application depends on the return-to-zero nature of the output bits when $A_{IN} \geq +V_{REF}$ (overflow). In circuits which employ only one AD9000, this is not always an advantage. The circuit below illustrates one method of converting the outputs to nonreturn-to-zero.

The 10197 (standard 10K ECL logic) hex-AND group senses the active OVERFLOW output and forces all other bits to logic HIGH. The 10151 latch is not required for AD9000 applications, but it may ease data transfer sensitivities in asnychronous data collection systems.

The reference driver circuits should provide a low source impedance to prevent noise on the reference inputs from affecting the AD9000's accuracy. This is accomplished to a large extent by adequately decoupling the reference pins to ground. An improved method is employed below. The reference voltages ($+V_{REF}$, $-V_{REF}$) are buffered by a transistor/amplifier combination. This has the advantages of wide bandwidth (hence low impedance over a wide frequency range to eliminate high frequency noise components), and improved temperature stability.

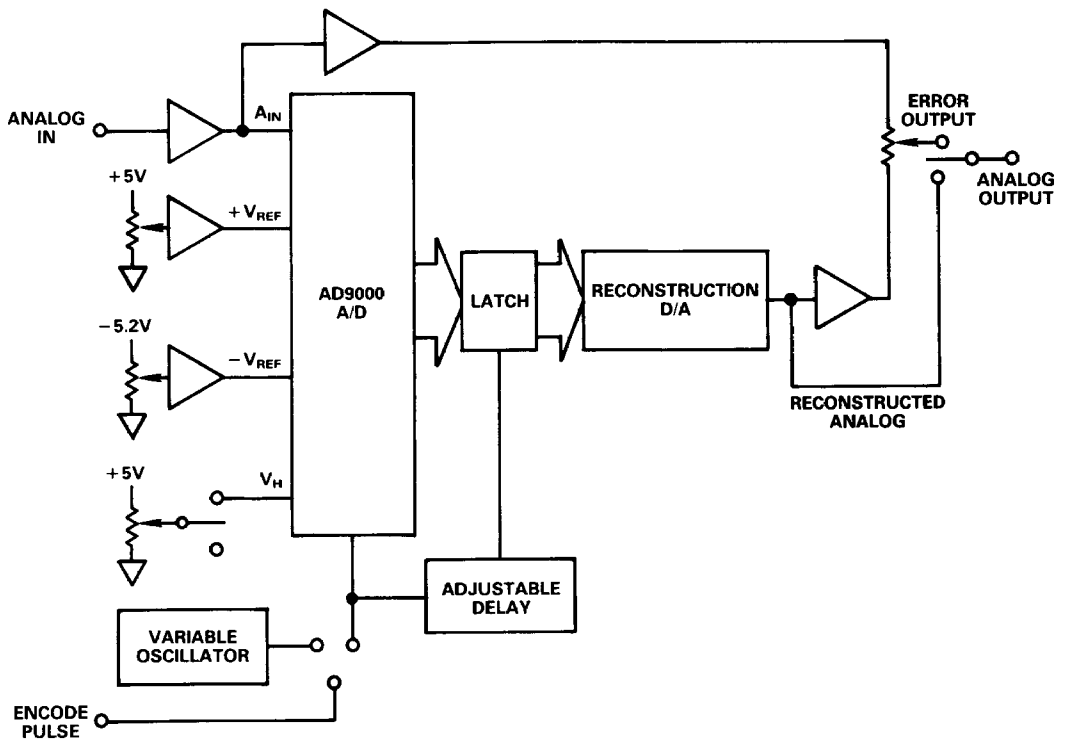


AD9000/PCB EVALUATION AND TEST BOARD

Evaluating and testing the AD9000 is greatly simplified with the AD9000/PCB evaluation board. The printed circuit board contains all of the driver and buffering circuits needed to test and evaluate the AD9000. The board outputs include both a high quality reconstructed representation of the input waveform, and a dc error waveform output which can be used to determine device linearities.

Inputs to the AD9000/PCB evaluation board include the analog signal to be digitized, as well as an optional ENCODE input for high stability measurements. All components, except the AD9000, are soldered onto the 8.5" × 6.3" board. The AD9000 is socketed to facilitate moderate volume testing. The evaluation board is offered with either a commercial temperature range AD9000, or an extended temperature range device installed.

The respective ordering numbers are AD9000JD/PCB and AD9000SD/PCB.



AD9000/PCB Block Diagram