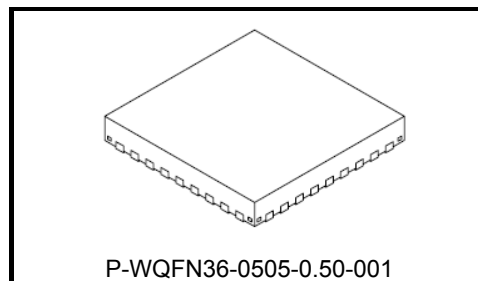


# TC78B015AFTG

## 3-phase Driver for Brushless DC Motors

The TC78B015AFTG is for three-phase full-wave brushless DC motor with 150-degree trapezoid PWM chopper system. They control motor rotational speed by changing the PWM duty, based on the speed control input. Hall signal is supported to one sensor for the TC78B015AFTG.



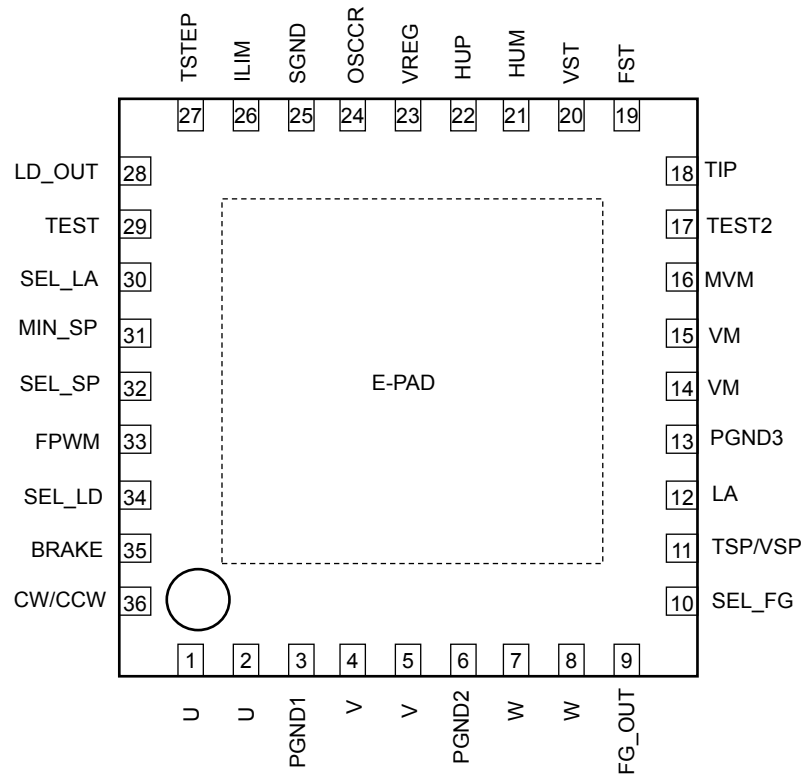
Weight: 0.06 g (typ.)

## Features

- Three-phase full wave drive
- 150-degree trapezoid PWM chopper system
- Soft switching
- Hall amplifier (hall element / hall IC):
  - 1-sensor drive
- Power supply: absolute maximum voltage: 36 V
- Output current: absolute maximum current: 3 A
- Selectable rotational speed command input signal:
  - Pulse duty signal input/analog voltage input/PWM signal input
- Selectable PWM frequency
- Adjustable minimum duty in PWM control
- Adjustable speed ratio in PWM control
- Selectable lead angle control function: Auto lead angle function/External lead angle control (32 steps correspond to 0 to 58°)
- Selectable rotation direction
- Brake function terminal
- Selectable lock detection function
- Restart function
- Rotation frequency signal (FG\_OUT):
  - 1 pulse/ electrical angle 360°, 2/3 pulse/ electrical angle 360°, 1/2 pulse/ electrical angle 360°, 1/3 pulse/ electrical angle 360°
- Lock detection signal (LD\_OUT)
- Power supply voltage monitoring function
- Overcurrent detection circuit (ISD)
- Thermal shutdown circuit (TSD)
- Under voltage lockout circuit (UVLO)
- Current limit circuit
- Adjustable start conditions
- Selectable control function of forced commutation frequency (1-sensor drive).

Pin assignment

<Top view>



- Note 1: Design the pattern in consideration of the heat design because the back side (E-PAD) has the role of heat radiation. The back side (E-PAD) should be connected to GND because it is connected to the back of the chip electrically.
- Note 2: There are four pairs of terminals named U, V, W, and VM. Connect two each of the terminals which has the same pin symbol via external patterns. Regarding GND, connect PGND1, PGND2, PGND3, and SGND via external patterns. PGND1 and PGND2 are short-circuited in the IC.

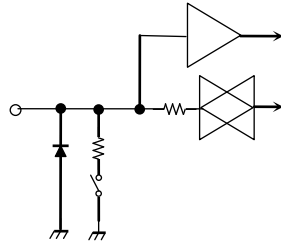
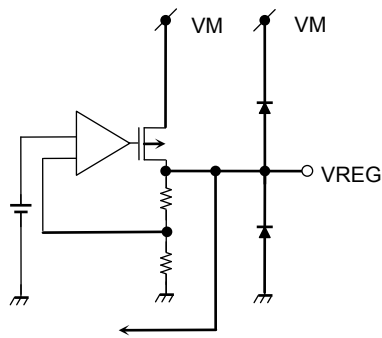
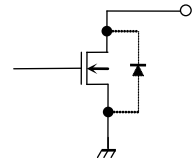
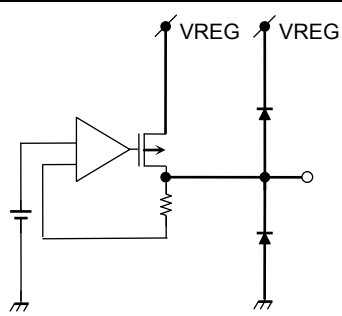
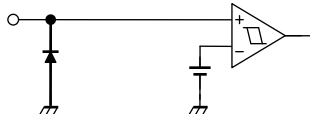
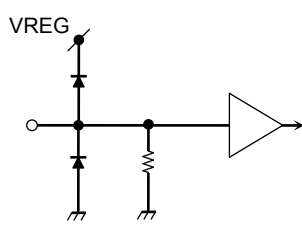
**Pin description**

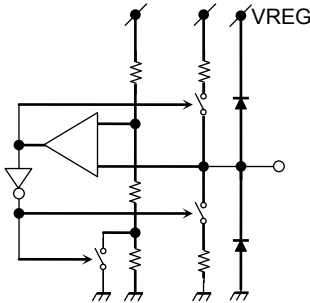
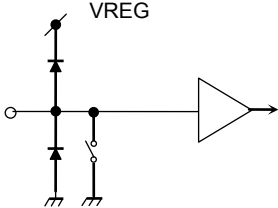
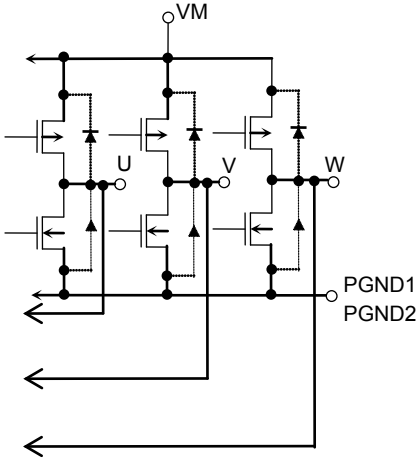
| Pin No. | Symbol  | I/O | Description                                                                   |
|---------|---------|-----|-------------------------------------------------------------------------------|
| 1       | U       | O   | Output terminal for U phase                                                   |
| 2       | U       | O   | Output terminal for U phase                                                   |
| 3       | PGND1   | —   | Power ground terminal (source of output Nch MOS transistor)                   |
| 4       | V       | O   | Output terminal for V phase                                                   |
| 5       | V       | O   | Output terminal for V phase                                                   |
| 6       | PGND2   | —   | Power ground terminal (source of output Nch MOS transistor)                   |
| 7       | W       | O   | Output terminal for W phase                                                   |
| 8       | W       | O   | Output terminal for W phase                                                   |
| 9       | FG_OUT  | O   | Output terminal for rotation frequency                                        |
| 10      | SEL_FG  | I   | Selectable terminal for FG frequency division ratio                           |
| 11      | TSP/VSP | I   | Input terminal for rotational speed command                                   |
| 12      | LA      | I   | Input terminal for setting lead angle                                         |
| 13      | PGND3   | —   | Power ground terminal (GND for pre-driver block)                              |
| 14      | VM      | —   | Power supply terminal for motor                                               |
| 15      | VM      | —   | Power supply terminal for motor                                               |
| 16      | MVM     | I   | Terminal for monitoring power supply                                          |
| 17      | TEST2   | —   | Terminal for test                                                             |
| 18      | TIP     | I   | Capacitor connecting terminal for setting DC excitation time                  |
| 19      | FST     | I   | Selectable terminal for forced commutation frequency                          |
| 20      | VST     | I   | Terminal for setting PWM ON duty of DC excitation and forced commutation mode |
| 21      | HUM     | I   | U-phase Hall-signal input (-)                                                 |
| 22      | HUP     | I   | U-phase Hall-signal input (+)                                                 |
| 23      | VREG    | —   | Output terminal for reference voltage (5 V)                                   |
| 24      | OSCCR   | —   | Terminal for setting internal oscillator circuit                              |
| 25      | SGND    | —   | Signal ground terminal                                                        |
| 26      | ILIM    | I   | Terminal for setting current limit                                            |
| 27      | TSTEP   | —   | Terminal for setting acceleration and deceleration time of PWM duty           |
| 28      | LD_OUT  | O   | Output terminal for lock detection                                            |
| 29      | TEST    | I   | Terminal for test                                                             |
| 30      | SEL_LA  | I   | Input terminal for selecting a method of lead angle or external input         |
| 31      | MIN_SP  | I   | Input terminal for setting minimum output on duty                             |
| 32      | SEL_SP  | I   | Input terminal for selecting a method of rotational speed command             |
| 33      | FPWM    | I   | Input terminal for selecting PWM frequency                                    |
| 34      | SEL_LD  | I   | Selectable terminal for motor lock detection function                         |
| 35      | BRAKE   | I   | Brake on/off terminal                                                         |
| 36      | CW/CCW  | I   | Input terminal for selecting rotation direction                               |

I/O Equivalent circuits

The equivalent circuit diagrams may be simplified or some parts of them may be omitted for explanatory purposes.

| Pin symbol                               | I/O Signal                                                                                                                                                                             | I/O Internal Circuit |
|------------------------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------------|
| HUP<br>HUM                               | Input terminal<br><br>Hysteresis $\pm 8\text{ mV}$ (typ.)                                                                                                                              |                      |
| CW/CCW<br>BRAKE                          | Input terminal<br><br>H: 2 V (min)<br><br>L: 0.8 V (max)                                                                                                                               |                      |
| FST<br>SEL_SP<br>SEL_LA                  | Input terminal<br><br>When leaving the terminal open, it is set to Middle level. When leaving the terminal open, plenty of evaluations using actual systems are required before using. |                      |
| SEL_FG<br>MIN_SP<br>LA<br>FPWM<br>SEL_LD | Input terminal<br><br>Applying a voltage to the terminals is required.                                                                                                                 |                      |
| VST                                      | Terminal for setting ON duty from DC excitation mode to forced commutation mode                                                                                                        |                      |

| Pin symbol       | I/O Signal                                                                                                                                            | I/O Internal Circuit                                                                 |
|------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------|--------------------------------------------------------------------------------------|
| TSP/VSP          | Input terminal for rotational speed command                                                                                                           |    |
| VREG             | Output terminal for reference voltage<br>VREG = 5 V (typ.)<br><br>Connect a capacitor (Recommended value: 0.1 μF) for voltage stability between SGND. |    |
| FG_OUT<br>LD_OUT | Open drain output<br><br>Pull-up the terminals externally to output high level.                                                                       |   |
| ILIM             | Terminal for setting current limit<br><br>Connect the resistance between SGND                                                                         |  |
| MVM              | Input terminal for monitoring power supply voltage<br><br>Applying a voltage to the terminals is required.                                            |  |
| TEST             | Test terminal                                                                                                                                         |  |

| Pin symbol        | I/O Signal                                                                                           | I/O Internal Circuit                                                                |
|-------------------|------------------------------------------------------------------------------------------------------|-------------------------------------------------------------------------------------|
| TIP<br>TSTEP      | Terminal for setting time<br><br>Connect a capacitor to SGND.                                        |   |
| OSCCR             | Terminal for setting internal oscillation frequency<br><br>Connect 27 kΩ to VREG and 360 pF to SGND. |   |
| VM<br>U<br>V<br>W | Output terminals for U, V, and W phases<br><br>VM: Power supply terminal for motor                   |  |

**Absolute Maximum Ratings (Ta = 25°C)**

| Characteristics       | Symbol                     | Rating                         | Unit |
|-----------------------|----------------------------|--------------------------------|------|
| Power supply voltage  | VM                         | 36                             | V    |
| Input voltage         | V <sub>IN1</sub> (Note 1)  | -0.3 to 6                      | V    |
|                       | V <sub>IN2</sub> (Note 2)  | -0.3 to V <sub>REG</sub> + 0.3 | V    |
| Output voltage        | V <sub>OUT1</sub> (Note 3) | 36                             | V    |
|                       | V <sub>OUT2</sub> (Note 4) | 36                             |      |
| Output current        | I <sub>OUT1</sub> (Note 5) | 3 (Note 8)                     | A    |
|                       | I <sub>OUT2</sub> (Note 6) | 10                             | mA   |
|                       | I <sub>OUT3</sub> (Note 7) | 40                             | mA   |
| Power dissipation     | P <sub>D</sub>             | 4.1 (Note 9)                   | W    |
| Operating temperature | T <sub>opr</sub>           | -40 to 85                      | °C   |
| Storage temperature   | T <sub>stg</sub>           | -55 to 150                     | °C   |

Note: The absolute maximum ratings of a semiconductor device are a set of ratings that must not be exceeded, even for a moment. Do not exceed any of these ratings. Exceeding the ratings may cause the device breakdown, damage or deterioration, and may result injury by explosion or combustion. Please use within the specified operating ranges.

Note 1: Terminal for V<sub>IN1</sub>: TSP/VSP, CW/CCW, and BRAKE

Note 2: Terminal for V<sub>IN2</sub>: HUP, HUM, SEL\_LD, SEL\_FG, CW/CCW, BRAKE, ILIM, MIN\_SP, MVM, SEL\_SP, LA, FPWM, SEL\_LA, and TEST

Note 3: Terminal for V<sub>OUT1</sub>: U, V, and W

Note 4: Terminal for V<sub>OUT2</sub>: FG\_OUT and LD\_OUT

Note 5: Terminal for I<sub>OUT1</sub>: U, V, and W

Note 6: Terminal for I<sub>OUT2</sub>: FG\_OUT and LD\_OUT

Note 7: Terminal for I<sub>OUT3</sub>: VREG

Note 8: Output current may be limited by the ambient temperature or the device implementation. The maximum junction temperature should not exceed T<sub>j</sub> (max) = 150°C.

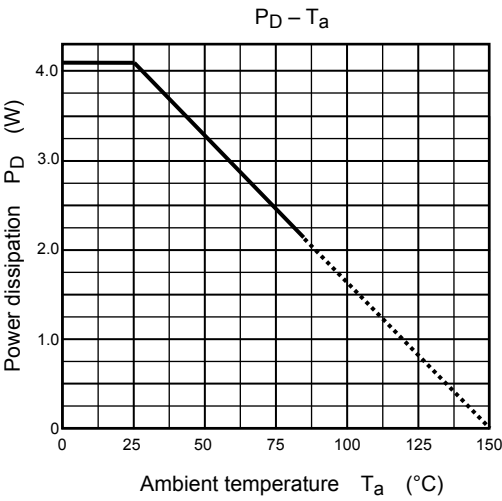
Note 9: When mounted on a board (4 layers, FR4, 76.2 mm × 114.3 mm × 1.6 mm), R<sub>th</sub> (j-a) = 30.5°C/W

Operating ranges

| Characteristics      | Symbol            | Operating range | Unit |
|----------------------|-------------------|-----------------|------|
| Power supply voltage | VM <sub>opr</sub> | 6 to 30 V       | V    |

Power dissipation (reference data)

When mounted on a board (4 layers, FR4, 76.2 mm × 114.3 mm × 1.6 mm), Rth (j-a) = 30.5°C/W





**Electrical Characteristics (Ta = 25°C)**

| Characteristics                           |                        | Symbol    | Test Conditions                                             | Min        | Typ. | Max  | Unit |
|-------------------------------------------|------------------------|-----------|-------------------------------------------------------------|------------|------|------|------|
| Power supply current                      |                        | IM        | IVreg = 0 mA                                                | —          | 6.0  | 8.5  | mA   |
| Input current                             |                        | IIN1A     | TSP/VSP<br>(SEL_SP = VREG)                                  | -1         | —    | 1    | μA   |
|                                           |                        | IIN1D(H)  | TSP/VSP = 5 V<br>(SEL_SP = Open, GND)                       | —          | 100  | 150  |      |
|                                           |                        | IIN1D(L)  | TSP/VSP = 0 V<br>(SEL_SP = Open, GND)                       | -1         | —    | 1    |      |
|                                           |                        | IIN2      | SEL_FG, MIN_SP, LA, FPWM, SEL_LD                            | -1         | —    | 1    |      |
|                                           |                        | IN3(H)    | VIN = 5 V<br>FST, SEL_SP, LA, SEL_LA                        | —          | 100  | 150  |      |
|                                           |                        | IN3(L)    | VIN = 0 V<br>FST, SEL_SP, LA, SEL_LA                        | -150       | -100 | —    |      |
|                                           |                        | IN4(H)    | VIN = 5 V<br>CW/CCW, BRAKE                                  | —          | 100  | 150  |      |
|                                           |                        | IN4(L)    | VIN = 0 V<br>CW/CCW, BRAKE                                  | -1         | 0    | —    |      |
|                                           |                        | IN5       | MVM                                                         | -1         | —    | 1    |      |
| Hall element input                        | Input sensitivity      | VS        | Differential input                                          | 40         | —    | —    | mVpp |
|                                           | In-phase voltage range | VW        | —                                                           | 0.5        | —    | 3.5  | V    |
|                                           | Input hysteresis       | VH        | (Reference data)                                            | ±4         | ±8   | ±12  | mV   |
| Hall IC input                             |                        | VIN4      | H                                                           | VREG<br>-1 | —    | VREG | V    |
|                                           |                        |           | L                                                           | 0          | —    | 0.8  |      |
| Input voltage                             |                        | VIN1 (H)  | TSP/VSP                                                     | 2.0        | —    | 5.5  | V    |
|                                           |                        | VIN1 (L)  | SEL_SP = Open, GND                                          | GND        | —    | 0.8  |      |
|                                           |                        | VIN2 (H)  | CW/CCW, BRAKE                                               | 2.0        | —    | 5.5  |      |
|                                           |                        | VIN2 (L)  | CW/CCW, BRAKE                                               | GND        | —    | 0.8  |      |
|                                           |                        | VIN3 (H)  | MVM<br>L→H: 150-degree commutation → 120-degree commutation | 1.9        | 2.0  | 2.1  |      |
|                                           |                        | VIN3 (L)  | MVM<br>H→L: 120-degree commutation → 150-degree commutation | 1.7        | 1.8  | 1.9  |      |
| Input hysteresis range                    |                        | V1hys     | (Reference data) TSP/VSP SEL_SP = GND                       | 0.3        | 0.4  | 0.5  | V    |
|                                           |                        | V2hys     | (Reference data) CW/CCW, BRAKE                              | 0.3        | 0.4  | 0.5  |      |
| Output low voltage of FG_OUT/LD_OUT       |                        | VOOUT     | IOOUT = 5 mA                                                | GND        | —    | 0.5  | V    |
| Leakage current of FG_OUT/LD_OUT          |                        | ILOUT     | VOOUT = 30 V                                                | —          | 0    | 2    | μA   |
| Output on resistance of U, V, W           |                        | RON (H+L) | IOOUT = 1 A                                                 | —          | 0.24 | 0.33 | Ω    |
| Output leakage current of U, V, W         |                        | IL (H)    | VOOUT = 0 V                                                 | -10        | 0    | —    | μA   |
|                                           |                        | IL (L)    | VOOUT = 30 V                                                | —          | 0    | 10   |      |
| ON resistance of VST terminal in starting |                        | RVST      | —                                                           | —          | 600  | 1000 | Ω    |

| Characteristics                                 | Symbol  | Test Conditions                                                                                                                                            | Min  | Typ.  | Max  | Unit |
|-------------------------------------------------|---------|------------------------------------------------------------------------------------------------------------------------------------------------------------|------|-------|------|------|
| Masking time for detecting current limit        | TRS     | (Reference data)                                                                                                                                           | —    | 1.2   | —    | μs   |
| Detection error of current limit                | ΔIOUT   | I <sub>out</sub> (U/V/W) = 1 A, ILIM: 39 kΩ                                                                                                                | -10  | —     | 10   | %    |
| Relative detection error of current limit       | ΔIOUT_R | (Reference data)<br>I <sub>out</sub> (U/V/W) = 1 A, ILIM: 39 kΩ<br>Measured value of each upper-and-lower phase for average value of upper-and-lower phase | -8.5 | —     | 8.5  | %    |
| PWM oscillation frequency                       | FPWM3   | (Reference data)FPWM = "3"                                                                                                                                 | 22.5 | 25    | 27.5 | kHz  |
|                                                 | FPWM2   | (Reference data)FPWM = "2"                                                                                                                                 | 180  | 200   | 220  |      |
|                                                 | FPWM1   | (Reference data)FPWM = "1"                                                                                                                                 | 90   | 100   | 110  |      |
|                                                 | FPWM0   | (Reference data)FPWM = "0"                                                                                                                                 | 45   | 50    | 55   |      |
| OSC frequency                                   | OSC     | (Reference data)OSCCR: 27 kΩ, 360 pF                                                                                                                       | 11.7 | 13    | 14.3 | MHz  |
| Setting time of TSTEP terminal                  | Tsoft   | (Reference data)TSTEP = 0.01 μF                                                                                                                            | —    | 0.100 | —    | s    |
| Setting time of TIP terminal                    | Tip     | (Reference data)TIP = 0.01 μF                                                                                                                              | —    | 0.100 | —    | s    |
| Lock detection time                             | Tlock1  | (Reference data)SEL_LD = "0"                                                                                                                               | —    | 0.5   | —    | s    |
| Restart time after lock                         | Tlock2  | (Reference data)SEL_LD = "0"                                                                                                                               | —    | 5     | —    | s    |
| Masking time for detecting overcurrent          | TISD    | (Reference data)                                                                                                                                           | —    | 1.9   | —    | μs   |
| Current when overcurrent detection operates     | ISD     | (Reference data)                                                                                                                                           | 3    | 4.5   | 6    | A    |
| Thermal shutdown circuit                        | TSD     | (Reference data)                                                                                                                                           | 150  | 165   | 180  | °C   |
|                                                 | TSDhys  | (Reference data) Hysteresis for restart                                                                                                                    | —    | 15    | —    |      |
| Under lockout voltage of VM terminal            | VMUVLO  | —                                                                                                                                                          | 5.0  | 5.3   | 5.6  | V    |
| Under lockout restarting voltage of VM terminal | VMUVLOR | —                                                                                                                                                          | 5.3  | 5.6   | 5.9  | V    |
| VREG output voltage                             | VREG    | IVREG = -40 mA (Note 1)                                                                                                                                    | 4.7  | 5     | 5.3  | V    |

(Reference data): No shipping inspection

Note 1: There is a possibility that VREG output voltage does not reach the minimum value in the above Electrical Characteristics when the power supply voltage is less than the operating ranges. Moreover, it depends on VM and the conditions of IVREG. Therefore, confirm there are not any problems by evaluating actual systems at about VMUVLO.

## The relation of setting steps and terminal voltage

| SEL_SP<br>FST<br>SEL_LA | SEL_FG<br>FPWM<br>SEL_LD | MIN_SP | LA (Auto lead<br>angle:<br>SEL_LA = "1") | LA (External<br>input:<br>SEL_LA = "0") | Input voltage (V)<br>(Written by VREG) |              | Input voltage (V)<br>(When VREG = 5 V) |       |
|-------------------------|--------------------------|--------|------------------------------------------|-----------------------------------------|----------------------------------------|--------------|----------------------------------------|-------|
|                         |                          |        |                                          |                                         | Min                                    | Max          | Min                                    | Max   |
| 2                       | 3                        | 8      | 7                                        | 31                                      | Vreg/256*160                           | Vreg         | 3.125                                  | 5     |
|                         |                          |        |                                          | 30                                      | Vreg/256*155                           | Vreg/256*159 | 3.027                                  | 3.105 |
|                         |                          |        |                                          | 29                                      | Vreg/256*150                           | Vreg/256*154 | 2.93                                   | 3.008 |
| 1                       | 2                        | 7      | 7                                        | 28                                      | Vreg/256*145                           | Vreg/256*149 | 2.832                                  | 2.910 |
|                         |                          |        |                                          | 27                                      | Vreg/256*140                           | Vreg/256*144 | 2.734                                  | 2.813 |
|                         |                          |        |                                          | 26                                      | Vreg/256*135                           | Vreg/256*139 | 2.637                                  | 2.715 |
|                         |                          | 6      | 6                                        | 25                                      | Vreg/256*130                           | Vreg/256*134 | 2.539                                  | 2.617 |
|                         |                          |        |                                          | 24                                      | Vreg/256*125                           | Vreg/256*129 | 2.441                                  | 2.520 |
|                         |                          |        |                                          | 23                                      | Vreg/256*120                           | Vreg/256*124 | 2.344                                  | 2.422 |
|                         |                          | 5      | 5                                        | 22                                      | Vreg/256*115                           | Vreg/256*119 | 2.246                                  | 2.324 |
|                         |                          |        |                                          | 21                                      | Vreg/256*110                           | Vreg/256*114 | 2.148                                  | 2.227 |
|                         |                          |        |                                          | 20                                      | Vreg/256*105                           | Vreg/256*109 | 2.051                                  | 2.129 |
|                         |                          | 4      | 4                                        | 19                                      | Vreg/256*100                           | Vreg/256*104 | 1.953                                  | 2.031 |
|                         |                          |        |                                          | 18                                      | Vreg/256*95                            | Vreg/256*99  | 1.855                                  | 1.934 |
|                         |                          |        |                                          | 17                                      | Vreg/256*90                            | Vreg/256*94  | 1.758                                  | 1.836 |
|                         | 1                        | 4      | 4                                        | 16                                      | Vreg/256*85                            | Vreg/256*89  | 1.66                                   | 1.738 |
|                         |                          |        |                                          | 15                                      | Vreg/256*80                            | Vreg/256*84  | 1.563                                  | 1.641 |
|                         |                          |        |                                          | 14                                      | Vreg/256*75                            | Vreg/256*79  | 1.465                                  | 1.543 |
|                         |                          | 3      | 3                                        | 13                                      | Vreg/256*70                            | Vreg/256*74  | 1.367                                  | 1.445 |
|                         |                          |        |                                          | 12                                      | Vreg/256*65                            | Vreg/256*69  | 1.27                                   | 1.348 |
|                         |                          | 3      | 2                                        | 11                                      | Vreg/256*60                            | Vreg/256*64  | 1.172                                  | 1.250 |
|                         |                          |        |                                          | 10                                      | Vreg/256*55                            | Vreg/256*59  | 1.074                                  | 1.152 |
|                         |                          |        |                                          | 9                                       | Vreg/256*50                            | Vreg/256*54  | 0.977                                  | 1.055 |
| 0                       | 0                        | 2      | 2                                        | 8                                       | Vreg/256*45                            | Vreg/256*49  | 0.879                                  | 0.957 |
|                         |                          |        |                                          | 7                                       | Vreg/256*40                            | Vreg/256*44  | 0.781                                  | 0.859 |
|                         |                          | 1      | 1                                        | 6                                       | Vreg/256*35                            | Vreg/256*39  | 0.684                                  | 0.762 |
|                         |                          |        |                                          | 5                                       | Vreg/256*30                            | Vreg/256*34  | 0.586                                  | 0.664 |
|                         |                          |        |                                          | 4                                       | Vreg/256*25                            | Vreg/256*29  | 0.488                                  | 0.566 |
|                         |                          | 1      | 0                                        | 3                                       | Vreg/256*20                            | Vreg/256*24  | 0.391                                  | 0.469 |
|                         |                          |        |                                          | 2                                       | Vreg/256*15                            | Vreg/256*19  | 0.293                                  | 0.371 |
|                         |                          |        |                                          | 1                                       | Vreg/256*10                            | Vreg/256*14  | 0.195                                  | 0.273 |
|                         |                          | 0      | 0                                        | 0                                       | 0                                      | Vreg/256*9   | 0                                      | 0.176 |

## Functional Description

The equivalent circuit diagrams may be simplified or some parts of them may be omitted for explanatory purposes. Timing charts may be simplified for explanatory purposes.

### 1. Basic operation

In receiving the start command, rotational speed and rotation direction are detected and the motor operates by the sequence of the following table.

| Detection of rotation direction | State                                   | Sequence of operation                                                   |
|---------------------------------|-----------------------------------------|-------------------------------------------------------------------------|
| Enable                          | Rotation direction agrees               | 150-degree PWM drive                                                    |
|                                 | Rotation direction disagrees            | Reverse brake → Forced commutation → 150-degree PWM drive               |
| Disenable                       | Position signal frequency ≤ 40 Hz       | DC excitation → Forced commutation → 150-degree PWM drive               |
|                                 | Position signal frequency: 40 to 200 Hz | Short brake → DC excitation → Forced commutation → 150-degree PWM drive |
|                                 | Position signal frequency > 200 Hz      | Detecting rotation direction is retried.                                |

### 2. Startup operation

Term of the DC excitation is configured by the TIP terminal. Forced commutation frequency is configured by the FST terminal. When the frequency of a position signal exceeds the frequency configured by the FST terminal, the operation moves from the forced commutation mode to the 150-degree PWM drive. In outputting, the on-duty in the DC excitation mode and the forced commutation mode correspond to the duty according to VST terminal voltage. The on-duty in the 150-degree PWM drive is determined by the input of TSP/VSP terminals. And startup, speed variable, and stop of the motor are controlled.

Time configuration and starting torque (output duty) of DC excitation and forced commutation are changed depending on motors and loads. So, adjustment is needed by experiment.

#### 1) DC excitation mode

Term of the DC excitation is configured by the TIP terminal. The motor operates in the DC excitation mode for  $2 \times T2[s]$ . The operation shifts to the DC excitation (2) after  $T2$  term of the DC excitation (1). And it shifts to the forced commutation after  $T2$  term of the DC excitation (2).

In the term of the DC excitation (1) and (2), when  $C_2$  is 0.01  $\mu F$ ,  $T2$  is calculated as follows;

$$32 \times 0.313 \times C_2 \times 10^6 = \text{approximately } 0.100 \text{ s}$$

States of the excitation phase of the DC excitation (1) and (2) according to the state of CW/CCW and the signals of HUP and HUM terminals are shown in the following table.

When CW/CCW = L, HU (HUP-HUM) = H

| Mode             | DC excitation (1)                                                          | DC excitation (2)                                                          |
|------------------|----------------------------------------------------------------------------|----------------------------------------------------------------------------|
| Term[s]          | T2                                                                         | T2                                                                         |
| Conduction phase | U phase: Full ON (Lower side)<br>V phase: OFF<br>W phase: PWM (Upper side) | U phase: OFF<br>V phase: PWM (Lower side)<br>W phase: Full ON (Upper side) |

When CW/CCW = L, HU (HUP-HUM) = L

| Mode             | DC excitation (1)                                                          | DC excitation (2)                                                          |
|------------------|----------------------------------------------------------------------------|----------------------------------------------------------------------------|
| Term[s]          | T2                                                                         | T2                                                                         |
| Conduction phase | U phase: Full ON (Upper side)<br>V phase: OFF<br>W phase: PWM (Lower side) | U phase: OFF<br>V phase: PWM (Upper side)<br>W phase: Full ON (Lower side) |

When CW/CCW=H, HU (HUP-HUM) = H

| Mode             | DC excitation (1)                                                          | DC excitation (2)                                                          |
|------------------|----------------------------------------------------------------------------|----------------------------------------------------------------------------|
| Term[s]          | T2                                                                         | T2                                                                         |
| Conduction phase | U phase: PWM (Upper side)<br>V phase: OFF<br>W phase: Full ON (Lower side) | U phase: Full ON (Upper side)<br>V phase: PWM (Lower side)<br>W phase: OFF |

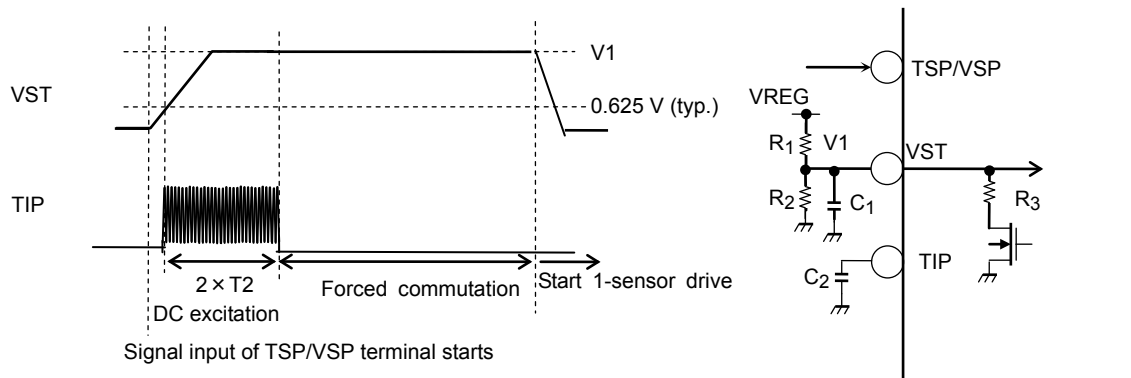
When CW/CCW = H, HU (HUP-HUM) = L

| Mode             | DC excitation (1)                                                          | DC excitation (2)                                                          |
|------------------|----------------------------------------------------------------------------|----------------------------------------------------------------------------|
| Term[s]          | T2                                                                         | T2                                                                         |
| Conduction phase | U phase: PWM (Lower side)<br>V phase: OFF<br>W phase: Full ON (Upper side) | U phase: Full ON (Lower side)<br>V phase: PWM (Upper side)<br>W phase: OFF |

## 2) Forced commutation mode

Forced commutation frequency is determined by the FST terminal.

| Number of steps set of FST terminal | Forced commutation frequency                                    |
|-------------------------------------|-----------------------------------------------------------------|
| 2                                   | Forced commutation frequency<br>$f_{ST} \approx 1.6 \text{ Hz}$ |
| 1                                   | Forced commutation frequency<br>$f_{ST} \approx 6.4 \text{ Hz}$ |
| 0                                   | Forced commutation frequency<br>$f_{ST} \approx 3.2 \text{ Hz}$ |



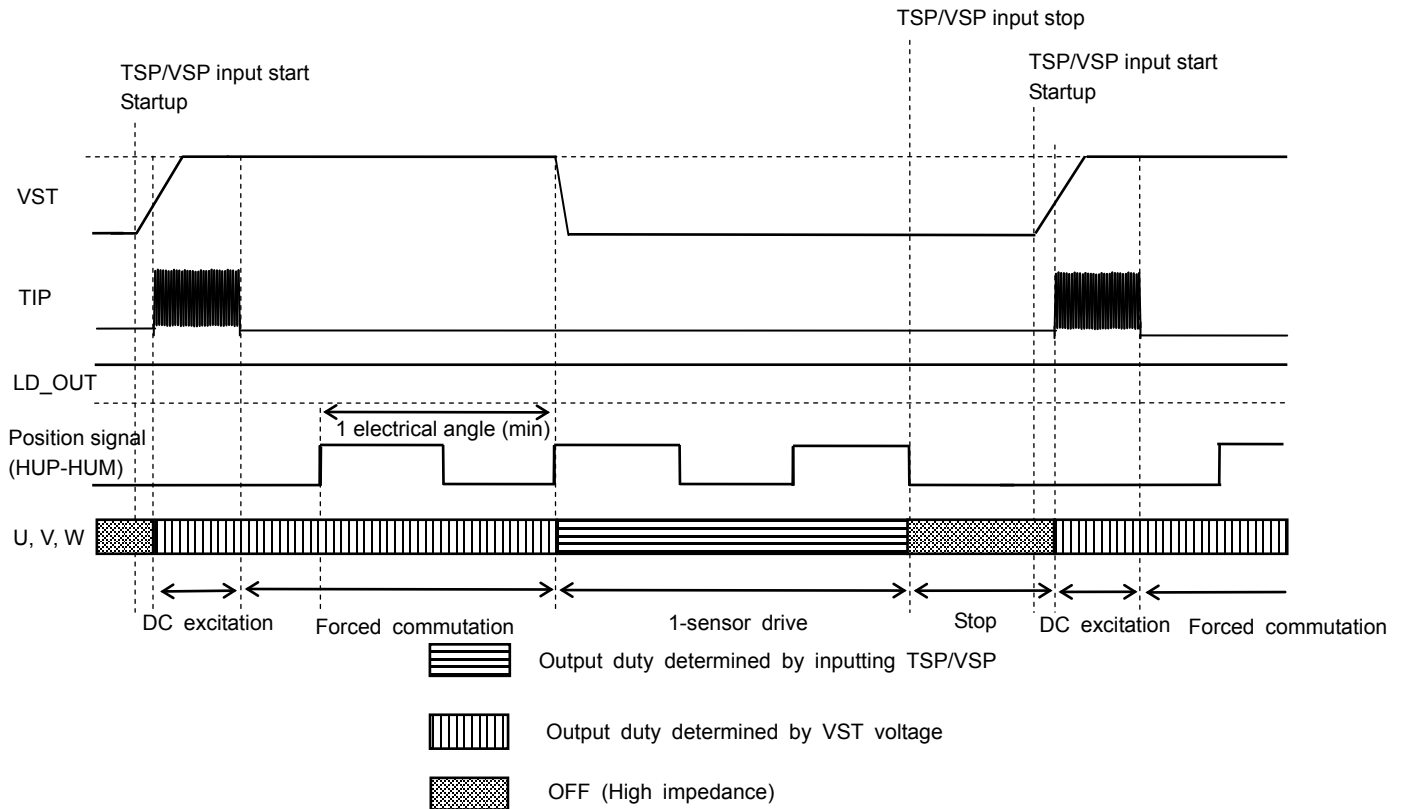
VST voltage is calculated from the following formula. ( $t = 0 \text{ s}$  in startup)

$$VST(t) = V1 \times (1 - e^{-t/\tau})$$

$$V1 = R_2 / (R_1 + R_2) \times VREG \quad (VREG = 5 \text{ V (typ.)})$$

$$\tau = (R_1 \times R_2) / (R_1 + R_2) \times C_1$$

### 3) Timing chart in starting

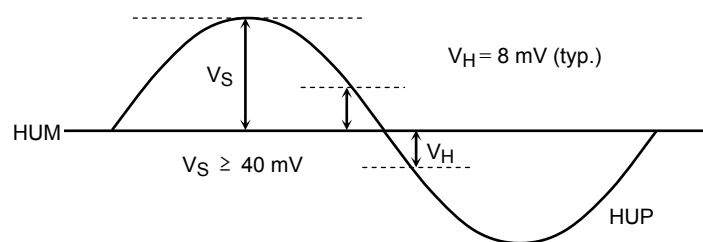


### 3. Position detection terminal

#### <Hall element input>

In-phase voltage range:  $V_W = 0.5$  to  $3.5$  V

Input hysteresis:  $V_H = 8$  mV (typ.)



#### <Hall IC input>

Conditions: HUP = GND to VREG

HUM = VREG/2

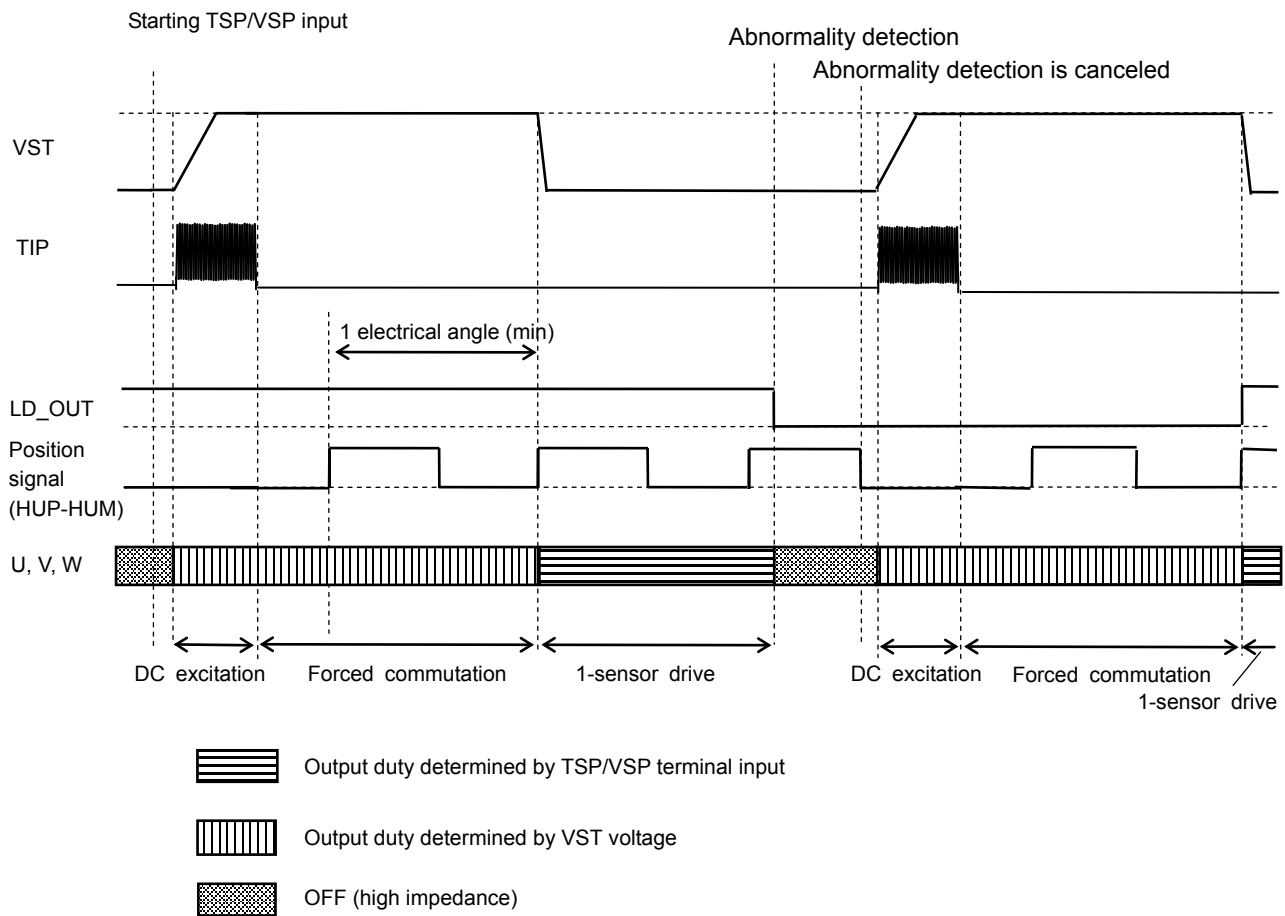
#### 4. Operation in abnormality detection

The following states are detected as abnormalities:

1. The ISD circuit is activated.
2. The TSD circuit is activated.
3. The motor lockout detection is activated.
4. Overvoltage detection is activated.
5. Frequency of position signal is abnormal ( $\geq 3$  kHz per electrical angle)

If either of the above abnormality of 1, 2, 3 or 5 is detected, the LD\_OUT terminal outputs low level until 150-degree PWM drive starts.

<Output operation of U, V, W, and LD\_OUT terminals in abnormality detection>



## 5. Motor lockout detection

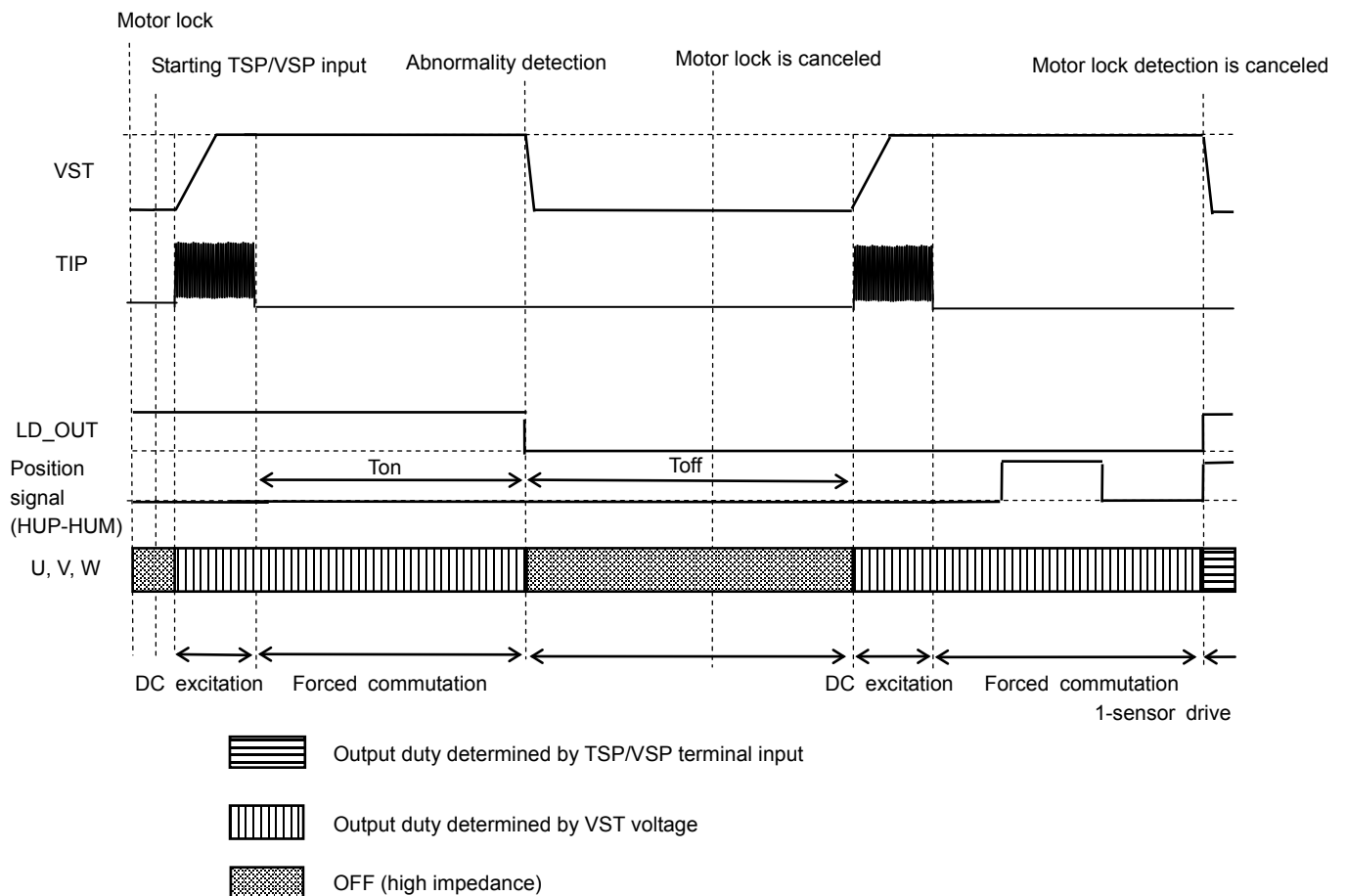
If the position signal does not change within the term of  $T_{on}$ , which is configured by SEL\_LD terminal, during the forced commutation mode or 150-degree PWM drive, the operation turns off, and re-starts after the term of  $T_{off}$ . After abnormality is detected, LD\_OUT terminal outputs low. It outputs high when the operation moves to the 150-degree PWM drive. When on duty = 0 % as a rotational speed command is input into TSP/VSP terminal, the term of  $T_{off}$  is released. After a start command signal is input into TSP/VSP terminal, the drive will restart.

To release the abnormality detection, input a rotational speed command of 'on duty = 0 %' for 2 ms period or more.

$T_{on}$  and  $T_{off}$  are set by SEL\_LD terminal as follows.

| Number of steps set of SEL_LD terminal | Functional description                                                                                                                                              |
|----------------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 3                                      | Motor lockout detection does not work.<br>Also disable for abnormality detection when the frequency of position signal is abnormal ( $\geq 3$ kHz/electrical angle) |
| 2                                      | $T_{on} = 1$ s (typ.), $T_{off} = 10$ s (typ.)                                                                                                                      |
| 1                                      | $T_{on} = 0.5$ s (typ.), $T_{off} = 10$ s (typ.)                                                                                                                    |
| 0                                      | $T_{on} = 0.5$ s (typ.), $T_{off} = 5$ s (typ.)                                                                                                                     |

<Output operation of U, V, W, and LD\_OUT terminals in lockout detection>





## 6. Forward /Reverse rotation direction switching

CW/CCW = Low: Forward direction, CW/CCW = High: Reverse direction.

When input level (H or L) of CW/CCW terminal is switched during 150-degree PWM drive, reverse brake operates until the position signal frequency decreases to 40 Hz or less. And then, it operates by the sequence of DC excitation, forced commutation, and 150-degree PWM drive.

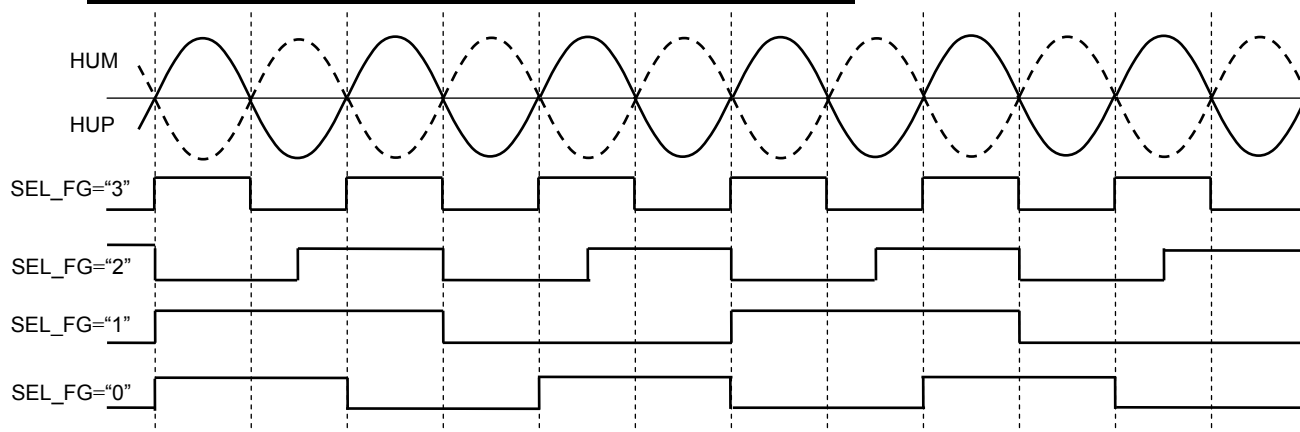
| CW/CCW | Order of conduction phase of output      |
|--------|------------------------------------------|
| L      | Forward rotation direction: U→V→W→U→ ... |
| H      | Reverse rotation direction: W→V→U→W→ ... |

## 7. Rotation speed output

A rotation pulse based upon hall signals is output.

Either of 1 pulse, 2/3, 1/3, or 1/2 pulses per electrical angle can be selected by SEL\_FG terminal. In selecting 2/3, 1/2, or 1/3 pulses per electrical angle, FG\_OUT terminal outputs low when the frequency of the position signal is 1 Hz or less.

| Number of steps set by SEL_FG terminal | FG_OUT                        |
|----------------------------------------|-------------------------------|
| 3                                      | 1 pulse / electrical angle    |
| 2                                      | 2/3 pulses / electrical angle |
| 1                                      | 1/3 pulses / electrical angle |
| 0                                      | 1/2 pulses / electrical angle |



## 8. Rotational speed command

Startup, stop and motor rotational speed which is set by output PWM duty are able to be controlled by an input signal into TSP/VSP terminal.

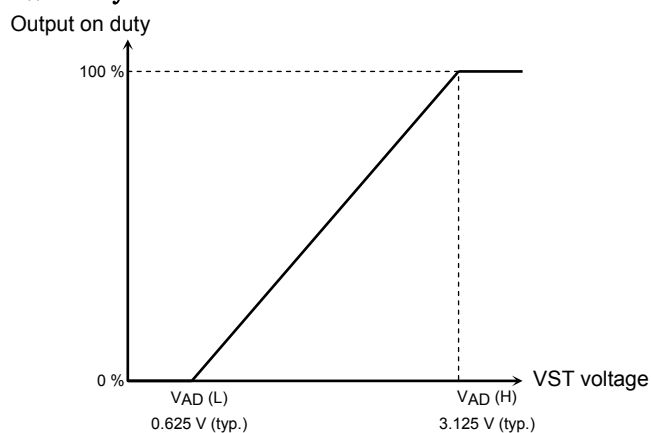
Pulse duty control, analog voltage control, or direct PWM control can be selected as a mode of TSP/VSP terminal by the number of steps set by SEL\_SP terminal.

Output PWM duty in DC excitation mode and forced commutation mode is according to VST voltage.

| Number of steps set by SEL_SP terminal | Input control at TSP/VSP terminal |
|----------------------------------------|-----------------------------------|
| 2                                      | Analog voltage control            |
| 1                                      | Pulse duty control                |
| 0                                      | Direct PWM control                |

### 1) Relation of VST terminal voltage and output PWM duty

- $0 \leq \text{VST voltage} \leq 0.625 \text{ V (typ.)}$   
 → Duty = 0 %  
 $0.625 \text{ V (typ.)} \leq \text{VST voltage} \leq 3.125 \text{ V (typ.)}$   
 → See the right figure (1/128 to 128/128)  
 $3.125 \text{ V (typ.)} \leq \text{VST voltage} \leq \text{VREG}$   
 → Duty = 100 % (128/128)

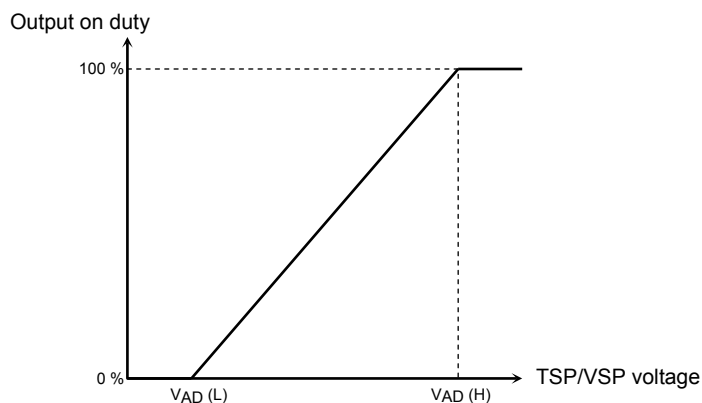


### 2) Relation of TSP/VSP terminal voltage and output PWM duty in controlling analog voltage (SEL\_SP="2")

When the voltage of TSP/VSP terminal  $\geq 0.625 \text{ V}$ , startup sequence starts.

When the voltage of TSP/VSP terminal  $< 0.625 \text{ V}$ , the sequence is reset.

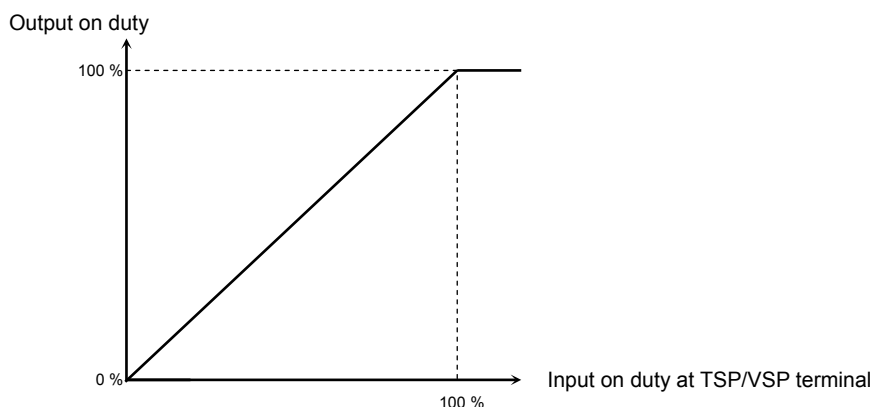
- $0 \leq \text{VSP/TSP (when analog voltage control)} \leq \text{VAD (L): } 0.625 \text{ V (typ.)}$   
 → Duty = 0 %  
 $\text{VAD (L): } 0.625 \text{ V (typ.)} \leq \text{VSP/TSP (when analog voltage control)} \leq \text{VAD (H): } 3.125 \text{ V (typ.)}$   
 → See the below figure. (1/128 to 128/128)  
 $\text{VAD (H) } 3.125 \text{ V (typ.)} \leq \text{VSP/TSP (when analog voltage control)} \leq \text{VREG}$   
 → Duty = 100 % (128/128)



### 3) Relation of TSP/VSP terminal voltage and output PWM duty in controlling pulse duty (SEL\_SP="1")

When a PWM signal is input into TSP/VSP terminal, startup sequence starts.

The pulse frequency input into TSP/VSP terminal should be set from 1 kHz to 100 kHz. Because input signal may be ineffective when on duty is for 0.2  $\mu$ s or less. Because the operation may be judged off state when output off duty is for 1 ms or more.



### 4) Relation of TSP/VSP terminal voltage and output PWM duty in controlling direct PWM (SEL\_SP = "0")

When a PWM signal is input into TSP/VSP terminal, startup sequence starts.

The pulse frequency of input into TSP/VSP terminal should be set from 23 kHz to 100 kHz.

The PWM frequency in DC excitation mode and forced commutation mode is determined by configuration of FPWM terminal and the output PWM duty is determined by the input voltage of VST terminal. The PWM frequency of 150-degree PWM drive is determined by the input signal of TSP/VSP terminal.

When SEL\_SP is "0", configurations of TSTEP terminal and MIN\_SP terminal become invalid, and the functions of control configuration of acceleration and deceleration and configuration of minimum output on-duty become invalid.

## 9. Setting minimum output on duty

Minimum output on duty is determined by the input voltage into MIN\_SP terminal.

However, minimum output on-duty becomes invalid for MIN\_SP terminal in DC excitation mode, forced commutation mode, and setting SEL\_SP = "0".

| Number of steps set by MIN_SP terminal | Minimum output duty [%] |
|----------------------------------------|-------------------------|
| 8                                      | 20.3                    |
| 7                                      |                         |
| 6                                      | 18.8                    |
| 5                                      | 17.2                    |
| 4                                      | 15.6                    |
| 3                                      | 14.1                    |
| 2                                      | 12.5                    |
| 1                                      | 10.9                    |
| 0                                      | 0                       |

**10. PWM frequency**

Output PWM frequency either in analog voltage control or in pulse duty control is determined by input voltage at FPWM terminal.

Output PWM frequency should be much higher than the electrical frequency of the motor. Please determine the value within switching performance of the drive circuits.

| Number of steps set by FPWM terminal | PWM frequency |
|--------------------------------------|---------------|
| 3                                    | 25 kHz        |
| 2                                    | 200 kHz       |
| 1                                    | 100 kHz       |
| 0                                    | 50 kHz        |

## 11. Lead angle control

Lead angle control mode is determined by setting both SEL\_LA and LA terminal.

| Number of steps set by SEL_LA terminal | Functional description                                                            |
|----------------------------------------|-----------------------------------------------------------------------------------|
| 2                                      | Test mode                                                                         |
| 1                                      | Auto lead angle: Auto lead angle mode is selected by input voltage of LA terminal |
| 0                                      | External input: Lead angle value is configured by input voltage of LA terminal    |

### 1) Auto lead angle (SEL\_LA = "1")

The threshold of the frequency has hysteresis +0 Hz/-50 Hz.

Lead angle value [deg]

| Number of steps set by LA terminal | Electrical frequency [Hz] |            |            |            |            |            |            |            |            |             |
|------------------------------------|---------------------------|------------|------------|------------|------------|------------|------------|------------|------------|-------------|
|                                    | 0 to 100                  | 100 to 200 | 200 to 300 | 300 to 400 | 400 to 500 | 500 to 600 | 600 to 700 | 700 to 800 | 800 to 900 | 900 to 1000 |
| 7                                  | 0                         | 1.875      | 1.875      | 1.875      | 1.875      | 3.750      | 3.750      | 3.750      | 3.750      | 5.625       |
| 6                                  | 0                         | 1.875      | 1.875      | 3.750      | 3.750      | 5.625      | 5.625      | 7.500      | 7.500      | 9.325       |
| 5                                  | 0                         | 1.875      | 1.875      | 3.750      | 5.625      | 7.500      | 7.500      | 9.325      | 11.250     | 13.125      |
| 4                                  | 0                         | 1.875      | 3.750      | 5.625      | 9.325      | 11.250     | 13.125     | 15.000     | 18.750     | 20.625      |
| 3                                  | 0                         | 1.875      | 5.625      | 7.500      | 11.250     | 13.125     | 16.875     | 18.750     | 22.500     | 24.375      |
| 2                                  | 0                         | 3.750      | 5.625      | 9.325      | 13.125     | 16.875     | 18.750     | 22.500     | 26.250     | 30.000      |
| 1                                  | 0                         | 3.750      | 7.500      | 11.250     | 15.000     | 18.750     | 22.500     | 26.250     | 30.000     | 33.750      |
| 0                                  | 0                         | 1.875      | 3.750      | 5.625      | 7.500      | 9.325      | 11.250     | 13.125     | 15.000     | 16.875      |

Lead angle value [deg]

| Number of steps set by LA terminal | Electrical frequency [Hz] |              |              |              |              |              |              |              |              |              |                |
|------------------------------------|---------------------------|--------------|--------------|--------------|--------------|--------------|--------------|--------------|--------------|--------------|----------------|
|                                    | 1000 to 1100              | 1100 to 1200 | 1200 to 1300 | 1300 to 1400 | 1400 to 1500 | 1500 to 1600 | 1600 to 1700 | 1700 to 1800 | 1800 to 1900 | 1900 to 2000 | More than 2000 |
| 7                                  | 5.625                     | 5.625        | 5.625        | 7.500        | 7.500        | 7.500        | 7.500        | 9.375        | 9.375        | 9.375        | 9.375          |
| 6                                  | 9.325                     | 11.250       | 11.250       | 13.125       | 13.125       | 15.000       | 15.000       | 16.875       | 16.875       | 18.750       | 18.750         |
| 5                                  | 13.125                    | 15.000       | 16.875       | 18.750       | 18.750       | 20.625       | 22.500       | 24.375       | 24.375       | 26.250       | 28.125         |
| 4                                  | 22.500                    | 24.375       | 28.125       | 30.000       | 31.875       | 33.750       | 37.500       | 39.375       | 41.250       | 43.125       | 46.875         |
| 3                                  | 28.125                    | 30.000       | 33.750       | 35.625       | 39.375       | 41.250       | 45.000       | 46.875       | 50.625       | 52.500       | 56.250         |
| 2                                  | 31.875                    | 35.625       | 39.375       | 43.125       | 45.000       | 48.750       | 52.500       | 56.250       | 58.125       | 58.125       | 58.125         |
| 1                                  | 37.500                    | 41.250       | 45.000       | 48.750       | 52.500       | 56.250       | 56.250       | 56.250       | 56.250       | 56.250       | 56.250         |
| 0                                  | 18.750                    | 20.625       | 22.500       | 24.375       | 26.250       | 28.125       | 30.000       | 31.875       | 33.750       | 35.625       | 37.500         |

## 2) External input (SEL\_LA = "0")

Lead angle in the range of 0° to 58.125° as commutation signals which correspond to the induced voltage can be adjusted.

The range from 0 V to 3.125 V as analog input voltage into LA terminal is divided into 32 parts.

Input voltage into LA terminal = 0 V: lead angle = 0°.

Input voltage into LA terminal = 3.125 V: lead angle = 58.125°.

Input voltage  $\geq 3.125$  V, input voltage: lead angle = 58.125°.

(Design value)

| Number of steps | LA [V] | Lead angle [deg] | Number of steps | LA [V] | Lead angle [deg] |
|-----------------|--------|------------------|-----------------|--------|------------------|
| 31              | 3.125  | 58.125           | 15              | 1.563  | 28.125           |
| 30              | 3.027  | 56.250           | 14              | 1.465  | 26.250           |
| 29              | 2.930  | 54.375           | 13              | 1.367  | 24.375           |
| 28              | 2.832  | 52.500           | 12              | 1.270  | 22.500           |
| 27              | 2.734  | 50.625           | 11              | 1.172  | 20.625           |
| 26              | 2.637  | 48.750           | 10              | 1.074  | 18.750           |
| 25              | 2.539  | 46.875           | 9               | 0.977  | 16.875           |
| 24              | 2.441  | 45.000           | 8               | 0.879  | 15.000           |
| 23              | 2.344  | 43.125           | 7               | 0.781  | 13.125           |
| 22              | 2.246  | 41.250           | 6               | 0.684  | 11.250           |
| 21              | 2.148  | 39.375           | 5               | 0.586  | 9.375            |
| 20              | 2.051  | 37.500           | 4               | 0.488  | 7.500            |
| 19              | 1.953  | 35.625           | 3               | 0.391  | 5.625            |
| 18              | 1.855  | 33.750           | 2               | 0.293  | 3.750            |
| 17              | 1.758  | 31.875           | 1               | 0.195  | 1.875            |
| 16              | 1.660  | 30.000           | 0               | 0.000  | 0.000            |

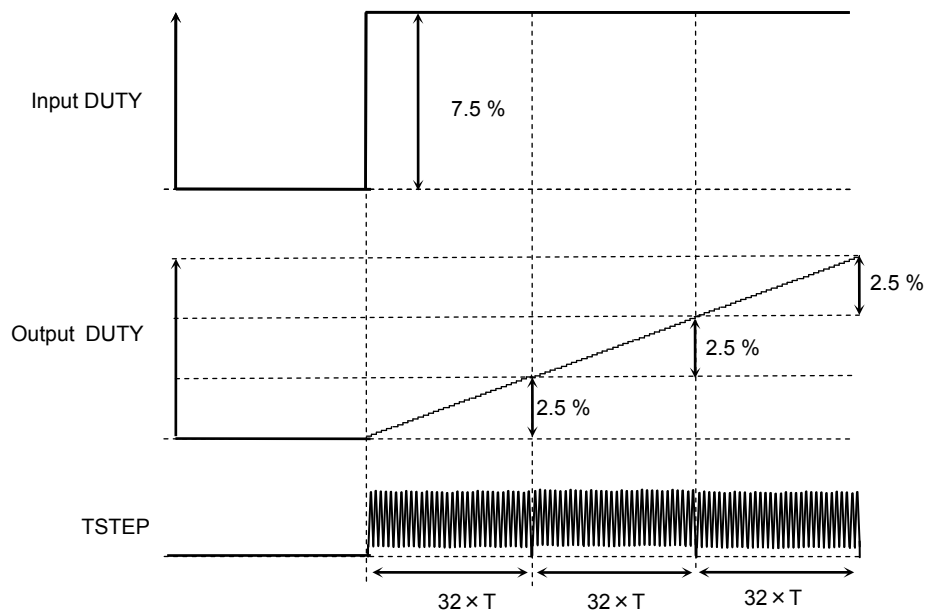
## 12. Acceleration and deceleration control setting

Time to reflect the duty of the input control signal of TSP/VSP terminal in the output duty during acceleration and deceleration can be set by connecting the capacitor to TSTEP terminal. (About  $0.078 \%/\text{T}$ ) Therefore, the rotation speed can accelerate and slow down gradually in startup. However, when change of the duty of an input control signal is 2.5 % or less, it is reflected in output duty for every PWM cycle. Acceleration and deceleration time: (For example) When  $C = 0.01 \mu\text{F}$ ,  $32 \times T = 32 \times 0.313 \times C \times 10^6 = \text{about } 0.100 \text{ s}$ .

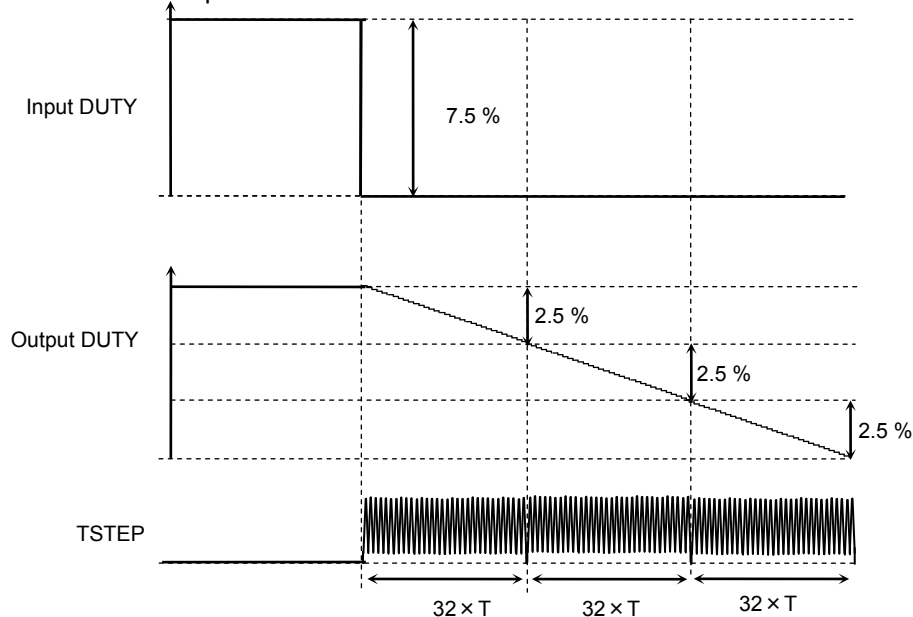
When the speed command that the output on duty is 0 % is inputted during operation, the deceleration function becomes invalid, and the output is turned off.

At this time, an output duty is reset to 0 %. When restarting, please input a start command signal to TSP/VSP pin after inputting a speed control command that the output on duty is 0 % for 2 ms or more.

In case of 7.5 % increase in input DUTY



In case of 7.5 % decrease in input DUTY



### 13. Brake function

If high level is input into BRAKE terminal, the reverse brake works to stop the motor operation.

After the input signal into BRAKE terminal is changed from L level to H level during the motor rotation, the reverse brake works until the position signal frequency becomes 40 Hz. When the position signal frequency is less than 40 Hz, the motor will stop.

However, when the input signal into BRAKE terminal is changed from L level to H level under the condition that the output duty command of TSP/VSP terminal is 0 %, the operation sequence is shown as the below table.

| BRAKE       | Functional description |
|-------------|------------------------|
| High        | Brake                  |
| Low or open | Normal operation       |

In case the input signal into BRAKE terminal is changed from L level to H level under the condition that the output duty command of TSP/VSP terminal is 0 %

| Detection of rotation direction | Status                                     | Brake sequence                             |
|---------------------------------|--------------------------------------------|--------------------------------------------|
| Enable                          | Position signal frequency ≤ 40 Hz          | Short brake                                |
|                                 | Position signal frequency > 40 Hz          | Reverse brake → Short brake                |
| Disenable                       | Position signal frequency ≤ 200 Hz or less | Short brake                                |
|                                 | Position signal frequency > 200 Hz or more | Detection of rotation direction is retried |

### 14. Overvoltage monitoring function

When MVM = 2.0 V (typ.) or more, drive mode is 120-degree conduction.

MVM has 0.2 V (typ.) of hysteresis. If MVM < 1.8 V (typ.), drive restarts.

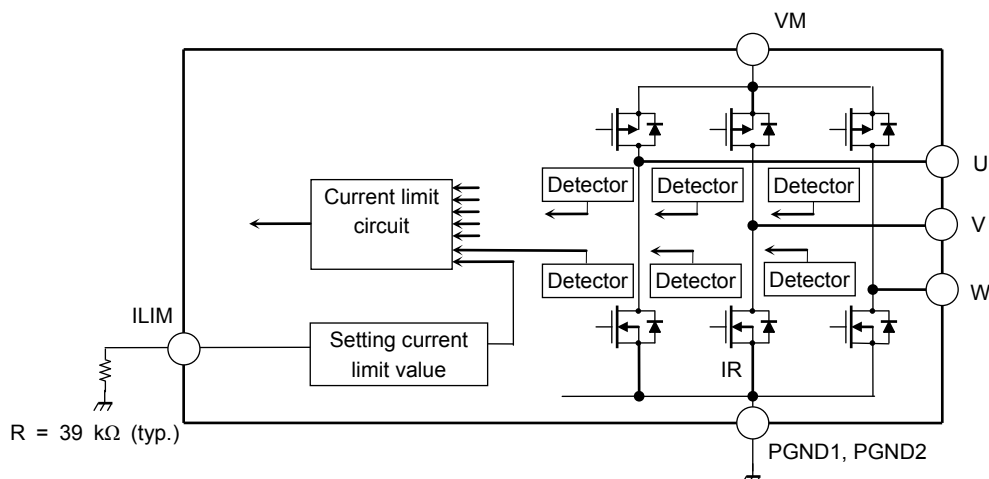
| MVM                | Functional description |
|--------------------|------------------------|
| MVM ≥ 2.0 V (typ.) | 120-degree commutation |
| MVM < 1.8 V (typ.) | 150-degree commutation |

### 15. Current limit circuit

Current limit circuit turns off upper side of the output transistors and limits the current. Driver restarts just when PWM turns on.

Value of current limit is configured by the external resistance.

(Example) When 39 kΩ is set as the resistor (R),  $I_{OUT} (typ.) = 39000/R = 39000/39000 \approx 1.0 \text{ A}$





**16. Overcurrent detection circuit (ISD)**

Six overcurrent detectors are built in each output transistor. If detected value exceeds the absolute maximum rating, all of outputs are turned off (high impedance: Hi-Z).

If output on duty of rotational speed command is set 0 %, abnormality detection is released.

Please input a rotational speed command (0 % for 2 ms or more) to release the abnormality detection.

**17. Thermal shutdown circuit (TSD)**

It turns off output (high impedance: Hi-Z), when the junction temperature ( $T_j$ ) exceeds 165°C (typ.). There is 15°C (typ.) of hysteresis.

Temperature for restart is  $T_{SD} - T_{SDhys}$  after thermal shutdown circuit operates.

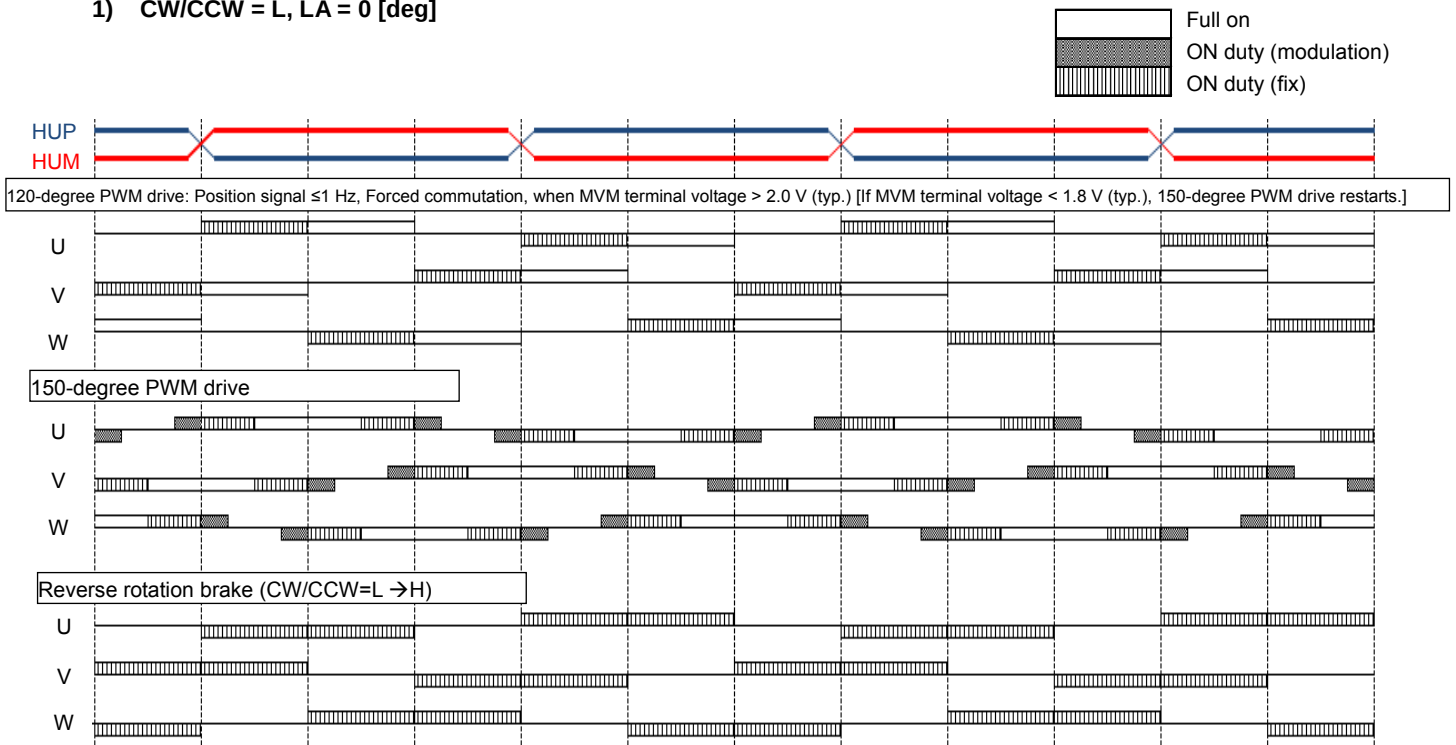
$T_{SD} = 165^{\circ}\text{C}$  (typ.),  $T_{SDhys} = 15^{\circ}\text{C}$  (typ.)

**18. Under voltage lockout (UVLO)**

It turns off each output of U, V, W, FG\_OUT and LD\_OUT (high impedance: Hi-Z), when VM is 5.3 V (typ.) or less. There is 0.3 V (typ.) of hysteresis. Voltage for restart is 5.6 V (typ.).

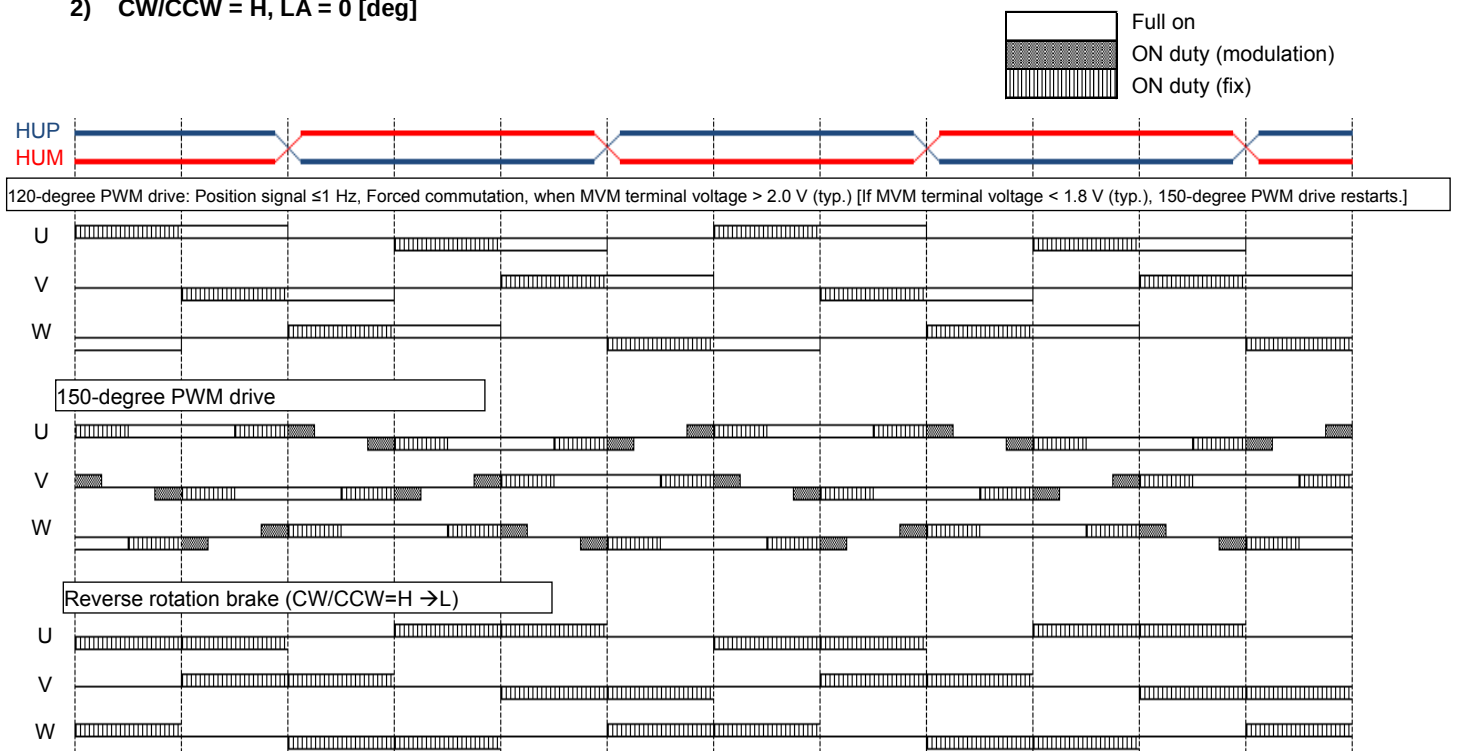
## Timing chart

### 1) CW/CCW = L, LA = 0 [deg]



In this timing chart, the reverse rotation brake is indicated without current limit.

### 2) CW/CCW = H, LA = 0 [deg]

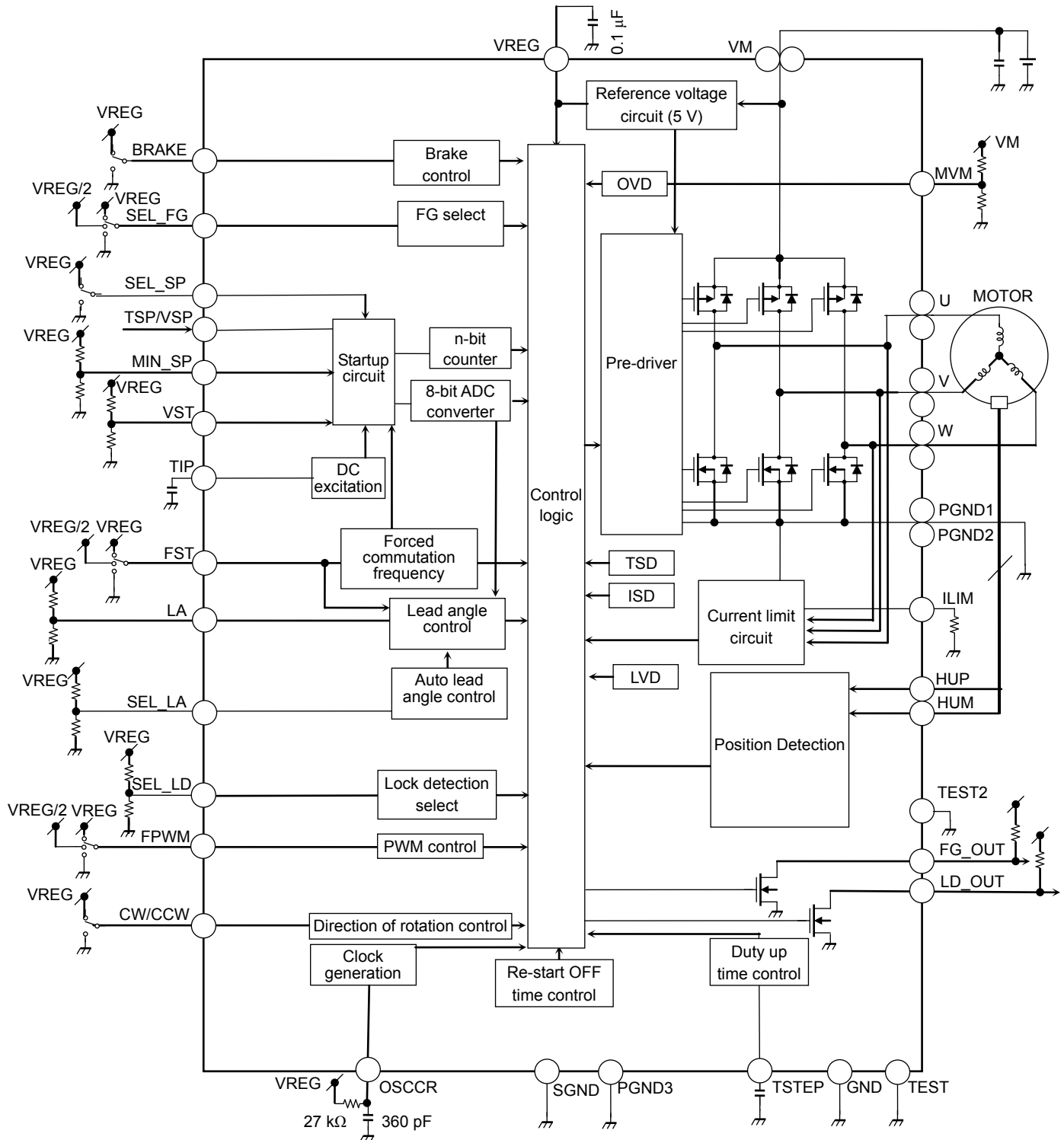


In this timing chart, the reverse rotation brake is indicated without current limit.

## Application circuit example

Some of the functional blocks, circuits, or constants in the block diagram may be omitted or simplified for explanatory purposes. The application circuits shown in this document are provided for reference purposes only.

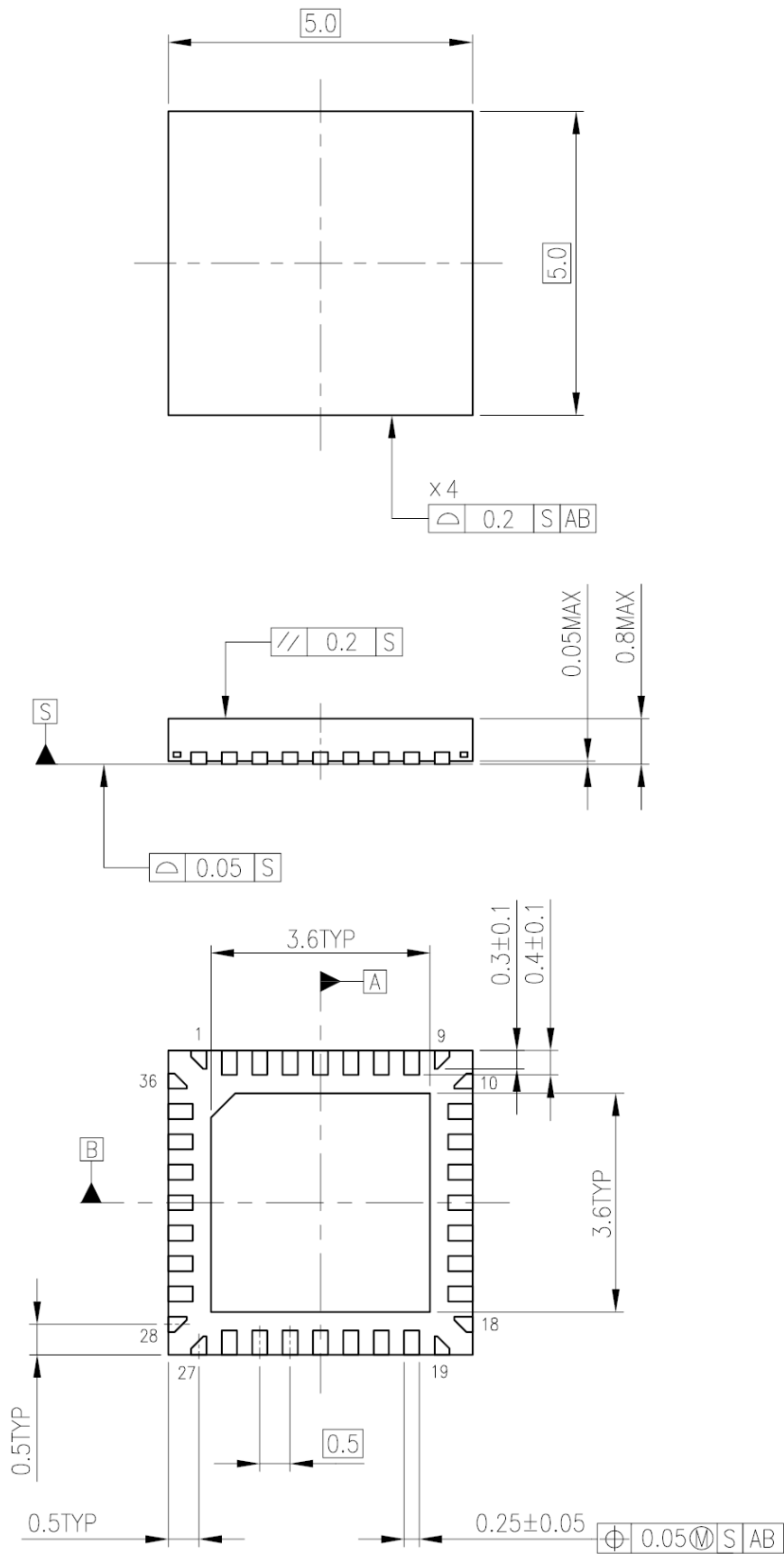
Thorough evaluation is required, especially at the mass production design stage.



Package Dimensions

P-WQFN36-0505-0.50-001

Unit: mm



Weight: 0.06 g (typ.)

**Notes on Contents****1. Block Diagrams**

Some of the functional blocks, circuits, or constants in the block diagram may be omitted or simplified for explanatory purposes.

**2. Equivalent Circuits**

The equivalent circuit diagrams may be simplified or some parts of them may be omitted for explanatory purposes.

**3. Timing Charts**

Timing charts may be simplified for explanatory purposes.

**4. Application Circuits**

The application circuits shown in this document are provided for reference purposes only. Thorough evaluation is required, especially at the mass production design stage. Toshiba does not grant any license to any industrial property rights by providing these examples of application circuits.

**5. Test Circuits**

Components in the test circuits are used only to obtain and confirm the device characteristics. These components and circuits are not guaranteed to prevent malfunction or failure from occurring in the application equipment.

**IC Usage Considerations****Notes on handling of ICs**

- (1) The absolute maximum ratings of a semiconductor device are a set of ratings that must not be exceeded, even for a moment. Do not exceed any of these ratings.  
Exceeding the rating(s) may cause the device breakdown, damage or deterioration, and may result injury by explosion or combustion.
- (2) Use an appropriate power supply fuse to ensure that a large current does not continuously flow in case of over current and/or IC failure. The IC will fully break down when used under conditions that exceed its absolute maximum ratings, when the wiring is routed improperly or when an abnormal pulse noise occurs from the wiring or load, causing a large current to continuously flow and the breakdown can lead smoke or ignition. To minimize the effects of the flow of a large current in case of breakdown, appropriate settings, such as fuse capacity, fusing time and insertion circuit location, are required.
- (3) If your design includes an inductive load such as a motor coil, incorporate a protection circuit into the design to prevent device malfunction or breakdown caused by the current resulting from the inrush current at power ON or the negative current resulting from the back electromotive force at power OFF. IC breakdown may cause injury, smoke or ignition. Use a stable power supply with ICs with built-in protection functions. If the power supply is unstable, the protection function may not operate, causing IC breakdown. IC breakdown may cause injury, smoke or ignition.
- (4) Do not insert devices in the wrong orientation or incorrectly. Make sure that the positive and negative terminals of power supplies are connected properly. Otherwise, the current or power consumption may exceed the absolute maximum rating, and exceeding the rating(s) may cause the device breakdown, damage or deterioration, and may result injury by explosion or combustion. In addition, do not use any device that is applied the current with inserting in the wrong orientation or incorrectly even just one time.

### Points to remember on handling of ICs

(1) Over current Protection Circuit

Over current protection circuits (referred to as current limiter circuits) do not necessarily protect ICs under all circumstances. If the Over current protection circuits operate against the over current, clear the over current status immediately. Depending on the method of use and usage conditions, such as exceeding absolute maximum ratings can cause the over current protection circuit to not operate properly or IC breakdown before operation. In addition, depending on the method of use and usage conditions, if over current continues to flow for a long time after operation, the IC may generate heat resulting in breakdown.

(2) Thermal Shutdown Circuit

Thermal shutdown circuits do not necessarily protect ICs under all circumstances. If the thermal shutdown circuits operate against the over temperature, clear the heat generation status immediately. Depending on the method of use and usage conditions, such as exceeding absolute maximum ratings can cause the thermal shutdown circuit to not operate properly or IC breakdown before operation.

(3) Heat Radiation Design

In using an IC with large current flow such as power amp, regulator or driver, please design the device so that heat is appropriately radiated, not to exceed the specified junction temperature ( $T_j$ ) at any time and condition. These ICs generate heat even during normal use. An inadequate IC heat radiation design can lead to decrease in IC life, deterioration of IC characteristics or IC breakdown. In addition, please design the device taking into consideration the effect of IC heat radiation with peripheral components.

(4) Back-EMF

When a motor rotates in the reverse direction, stops or slows down abruptly, a current flow back to the motor's power supply due to the effect of back-EMF. If the current sink capability of the power supply is small, the device's motor power supply and output pins might be exposed to conditions beyond absolute maximum ratings. To avoid this problem, take the effect of back-EMF into consideration in system design.

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