

RL78/L12

RENESAS MCU

R01DS0157EJ0210

Rev.2.10

Sep 30, 2016

Integrated LCD controller/driver, True Low Power Platform (as low as 62.5 μ A/MHz, and 0.64 μ A for RTC + LVD), 1.6 V to 5.5 V operation, 8 to 32 Kbyte Flash, 31 DMIPS at 24 MHz, for All LCD Based Applications

1. OUTLINE

1.1 Features

Ultra-Low Power Technology

- 1.6 V to 5.5 V operation from a single supply
- Stop (RAM retained): 0.23 μ A, (LVD enabled): 0.31 μ A
- Halt (RTC + LVD): 0.64 μ A
- Supports snooze
- Operating: 62.5 μ A/MHz
- LCD operating current (Capacitor split method): 0.12 μ A
- LCD operating current (Internal voltage boost method): 0.63 μ A ($V_{DD} = 3.0$ V)

16-bit RL78 CPU Core

- Delivers 31 DMIPS at maximum operating frequency of 24 MHz
- Instruction Execution: 86% of instructions can be executed in 1 to 2 clock cycles
- CISC Architecture (Harvard) with 3-stage pipeline
- Multiply Signed & Unsigned: 16 x 16 to 32-bit result in 1 clock cycle
- MAC: 16 x 16 to 32-bit result in 2 clock cycles
- 16-bit barrel shifter for shift & rotate in 1 clock cycle
- 1-wire on-chip debug function

Code Flash Memory

- Density: 8 KB to 32 KB
- Block size: 1 KB
- On-chip single voltage flash memory with protection from block erase/writing
- Self-programming with flash shield window function

Data Flash Memory

- Data flash with background operation
- Data flash size: 2 KB size
- Erase cycles: 1 Million (typ.)
- Erase/programming voltage: 1.8 V to 5.5 V

RAM

- 1 KB and 1.5 KB size options
- Supports operands or instructions
- Back-up retention in all modes

High-speed On-chip Oscillator

- 24 MHz with $\pm 1\%$ accuracy over voltage (1.8 V to 5.5 V) and temperature (-20°C to 85°C)
- Pre-configured settings: 24 MHz, 16 MHz, 12 MHz, 8 MHz, 6 MHz, 4 MHz, 3 MHz, 2 MHz & 1 MHz

Reset and Supply Management

- Power-on reset (POR) monitor/generator
- Low voltage detection (LVD) with 14 setting options (Interrupt and/or reset function)

LCD Controller/Driver

- Up to 35 seg x 8 com or 39 seg x 4 com
- Supports capacitor split method, internal voltage boost method and resistance division method
- Supports waveform types A and B
- Supports LCD contrast adjustment (16 steps)
- Supports LCD blinking

Direct Memory Access (DMA) Controller

- Up to 2 fully programmable channels
- Transfer unit: 8- or 16-bit

Multiple Communication Interfaces

- Up to 1 $\times$ I²C multi-master
- Up to 2 $\times$ CSI/SPI (7-, 8-bit)
- Up to 1 $\times$ UART (7-, 8-, 9-bit)
- Up to 1 $\times$ LIN

Extended-Function Timers

- Multi-function 16-bit timers: Up to 8 channels
- Real-time clock (RTC): 1 channel (full calendar and alarm function with watch correction function)
- Interval Timer: 12-bit, 1 channel
- 15 kHz watchdog timer: 1 channel (window function)

Rich Analog

- ADC: Up to 10 channels, 10-bit resolution, 2.1 μ s conversion time
- Supports 1.6 V
- Internal reference voltage (1.45 V)
- On-chip temperature sensor

Safety Features (IEC or UL 60730 compliance)

- Flash memory CRC calculation
- RAM parity error check
- RAM write protection
- SFR write protection
- Illegal memory access detection
- Clock frequency detection
- ADC self-test

General Purpose I/O

- 5V tolerant, high-current (up to 20 mA per pin)
- Open-Drain, Internal Pull-up support

Operating Ambient Temperature

- T_A: -40°C to $+85^{\circ}\text{C}$ (A: Consumer applications)
- T_A: -40°C to $+105^{\circ}\text{C}$ (G: Industrial applications)

Package Type and Pin Count

From 7mm x 7mm to 12mm x 12mm
QFP: 32, 44, 48, 52, 64

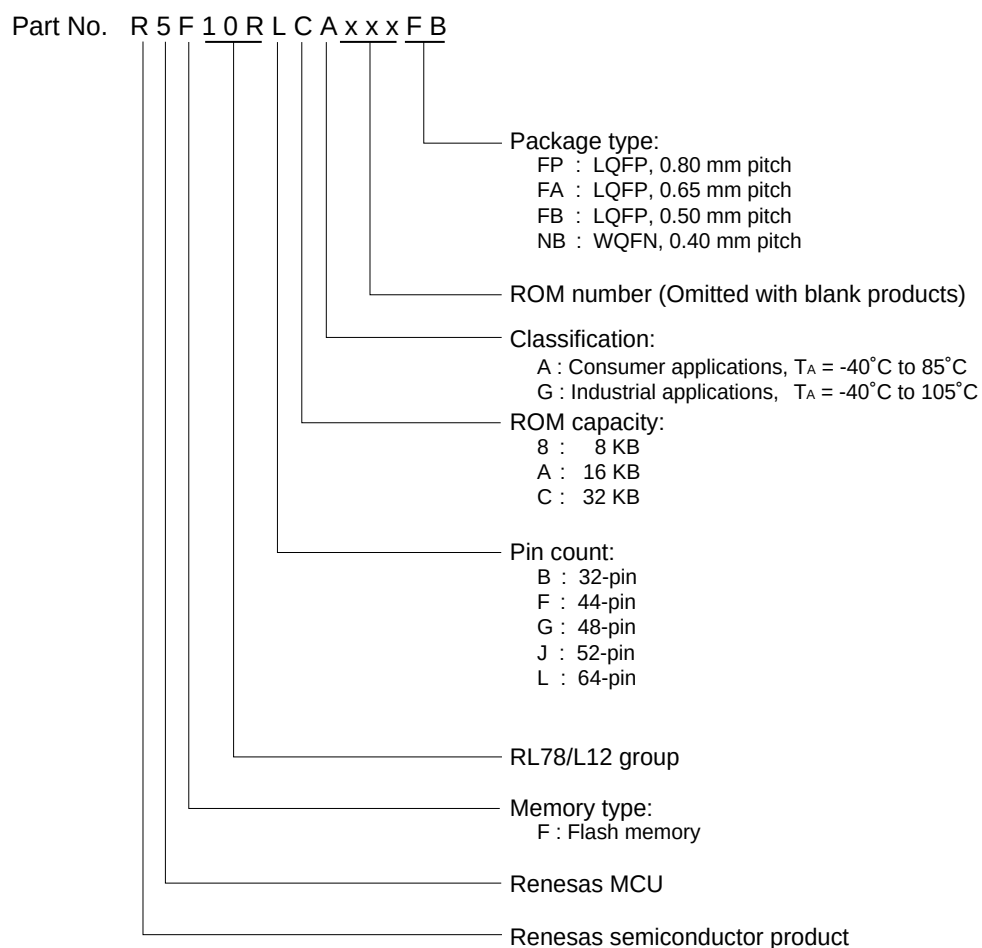
○ ROM, RAM capacities

Flash ROM	Data flash	RAM	RL78/L12				
			32 pins	44 pins	48 pins	52 pins	64 pins
32 KB	2 KB	1.5 KB ^{Note}	R5F10RBC	R5F10RFC	R5F10RGC	R5F10RJC	R5F10RLC
16 KB	2 KB	1 KB ^{Note}	R5F10RBA	R5F10RFA	R5F10RGA	R5F10RJA	R5F10RLA
8KB	2 KB	1 KB ^{Note}	R5F10RB8	R5F10RF8	R5F10RG8	R5F10RJ8	—

Note In the case of the 1 KB, and 1.5 KB, this is 630 bytes when the self-programming function and data flash function is used.

Remark The functions mounted depend on the product. See **1.6 Outline of Functions**.

1.2 List of Part Numbers

Figure 1-1 Part Number, Memory Size, and Package of RL78/L12

Pin count	Package	Fields of Application ^{Note}	Part Number
32 pins	32-pin plastic LQFP (7 × 7)	A G	R5F10RB8AFP, R5F10RBAAFP, R5F10RBCAFP R5F10RB8GFP, R5F10RBAGFP, R5F10RBCGFP
44 pins	44-pin plastic LQFP (10 × 10)	A G	R5F10RF8AFP, R5F10RFAAFP, R5F10RFCAFP R5F10RF8GFP, R5F10RFAGFP, R5F10RFCGFP
48 pins	48-pin plastic LQFP (fine pitch) (7 × 7)	A G	R5F10RG8AFB, R5F10RGAAFB, R5F10RGCAFB R5F10RG8GFB, R5F10RGAGFB, R5F10RGCGFB
52 pins	52-pin plastic LQFP (10 × 10)	A G	R5F10RJ8AFA, R5F10RJAAFA, R5F10RJCAFA R5F10RJ8GFA, R5F10RJAGFA, R5F10RJCGFA
64 pins	64-pin plastic WQFN (8 × 8)	A G	R5F10RLAANB, R5F10RLCANB R5F10RLAGNB, R5F10RLCGNB
	64-pin plastic LQFP (fine pitch) (10 × 10)	A G	R5F10RLAAFB, R5F10RLCAFB R5F10RLAGFB, R5F10RLCGFB
	64-pin plastic LQFP (12 × 12)	A G	R5F10RLAAFA, R5F10RLCAFA R5F10RLAGFA, R5F10RLCGFA

Note For the fields of application, refer to **Figure 1-1 Part Number, Memory Size, and Package of RL78/L12**.

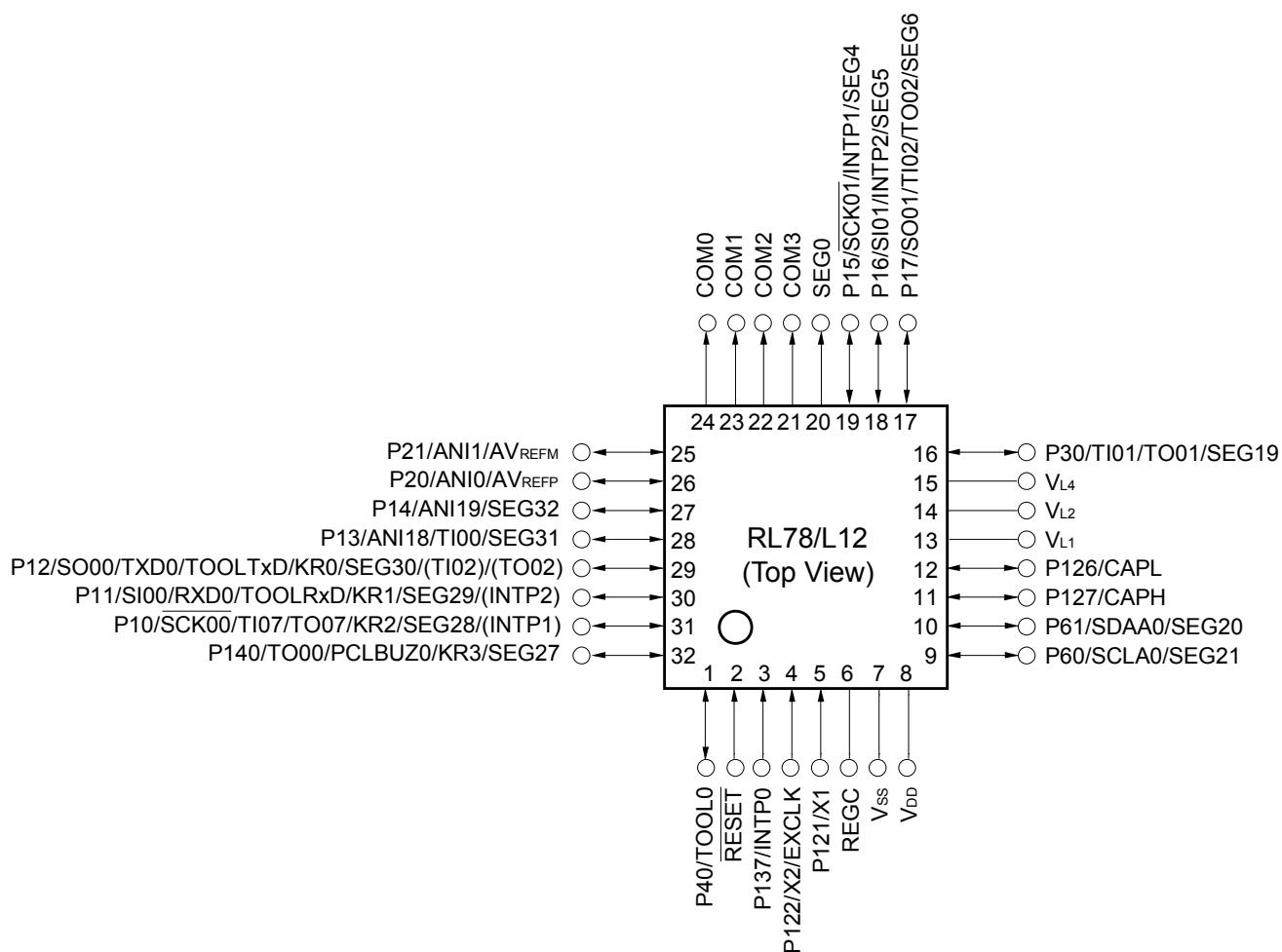
Caution The ordering part numbers represent the numbers at the time of publication. For the latest ordering part numbers, refer to the target product page of the Renesas Electronics website.

1.3 Pin Configuration (Top View)

1.3.1 32-pin products

- 32-pin plastic LQFP (7 × 7)

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Caution Connect the REGC pin to V_{SS} via a capacitor (0.47 to 1 μ F).

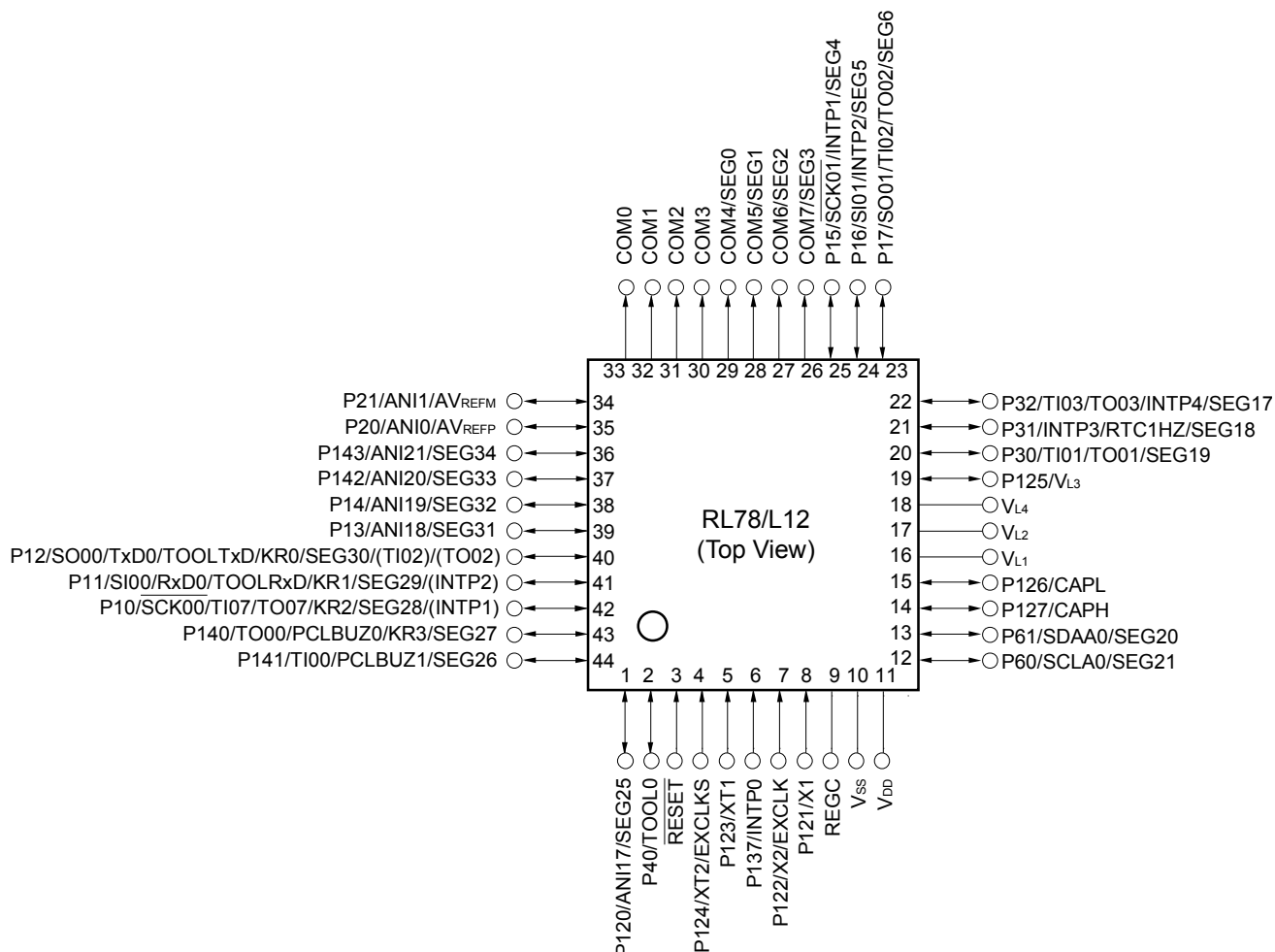
Remarks 1. For pin identification, see 1.4 Pin Identification.

2. Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR).

1.3.2 44-pin products

- 44-pin plastic LQFP (10 × 10)

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Caution Connect the REGC pin to Vss via a capacitor (0.47 to 1 μ F).

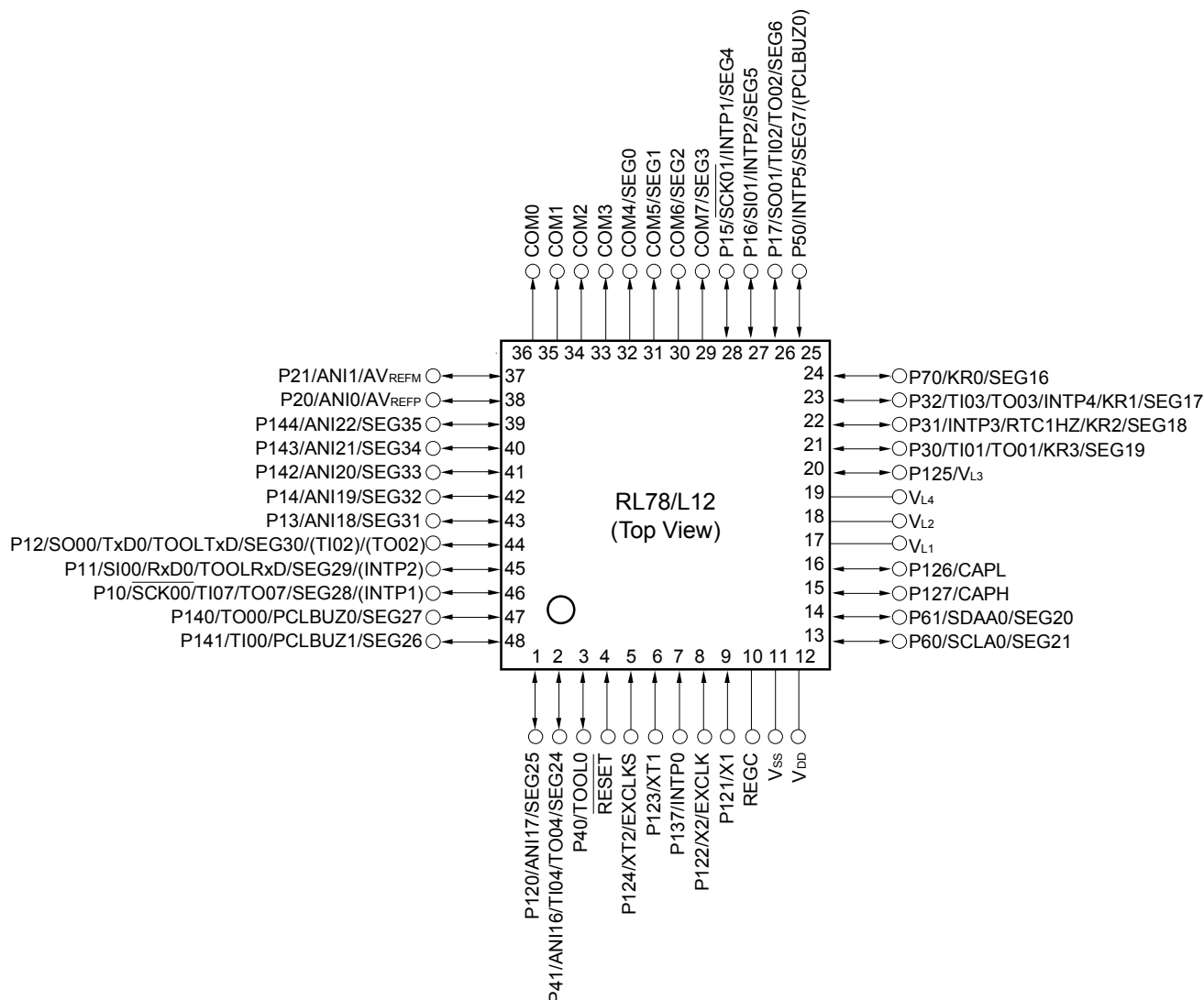
Remarks 1. For pin identification, see 1.4 Pin Identification.

2. Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR).

1.3.3 48-pin products

- 48-pin plastic LQFP (fine pitch) (7 × 7)

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Caution Connect the REGC pin to V_{SS} via a capacitor (0.47 to 1 μ F).

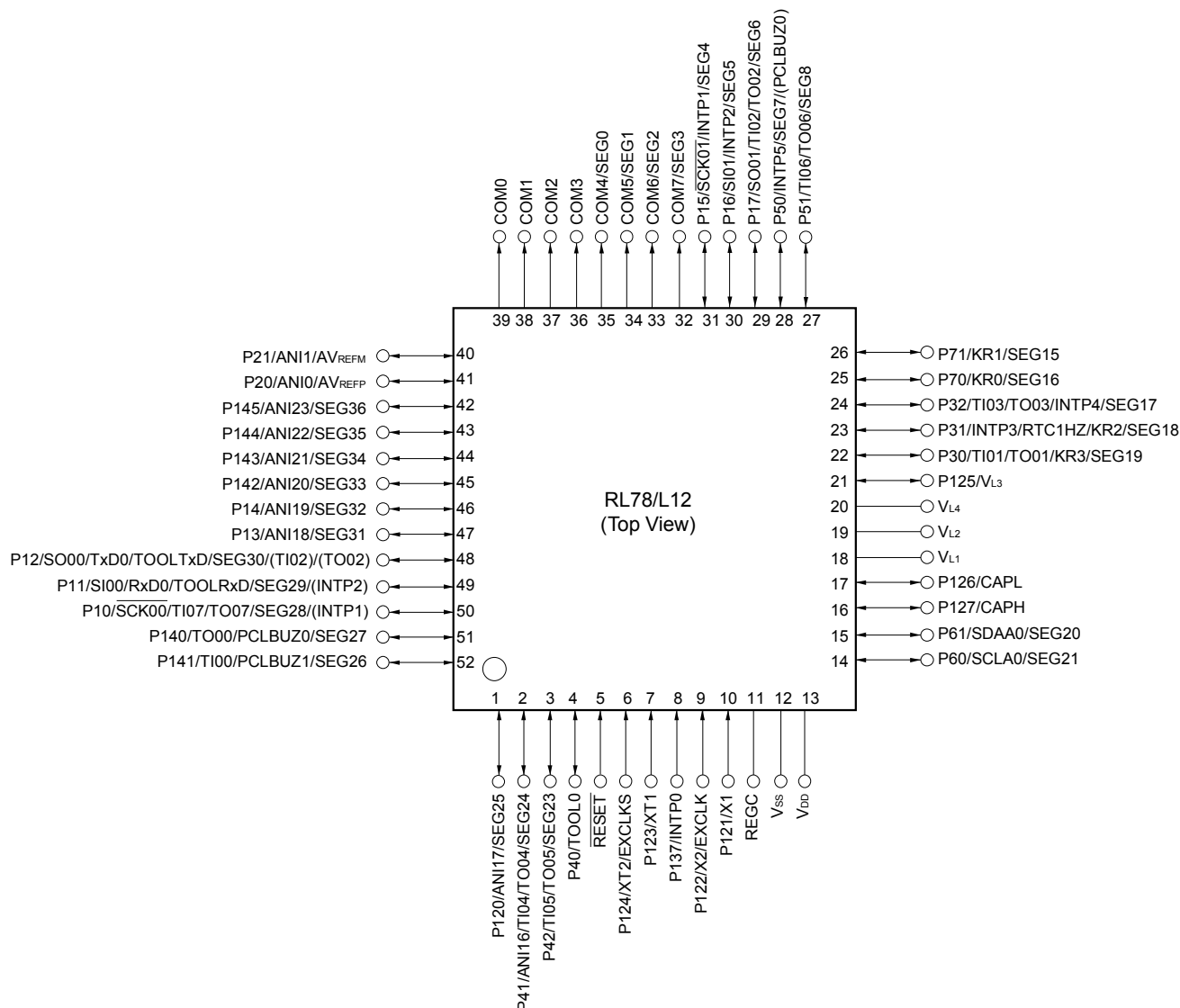
Remarks 1. For pin identification, see 1.4 Pin Identification.

2. Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR).

1.3.4 52-pin products

- 52-pin plastic LQFP (10 × 10)

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Caution Connect the REGC pin to Vss via a capacitor (0.47 to 1 μ F).

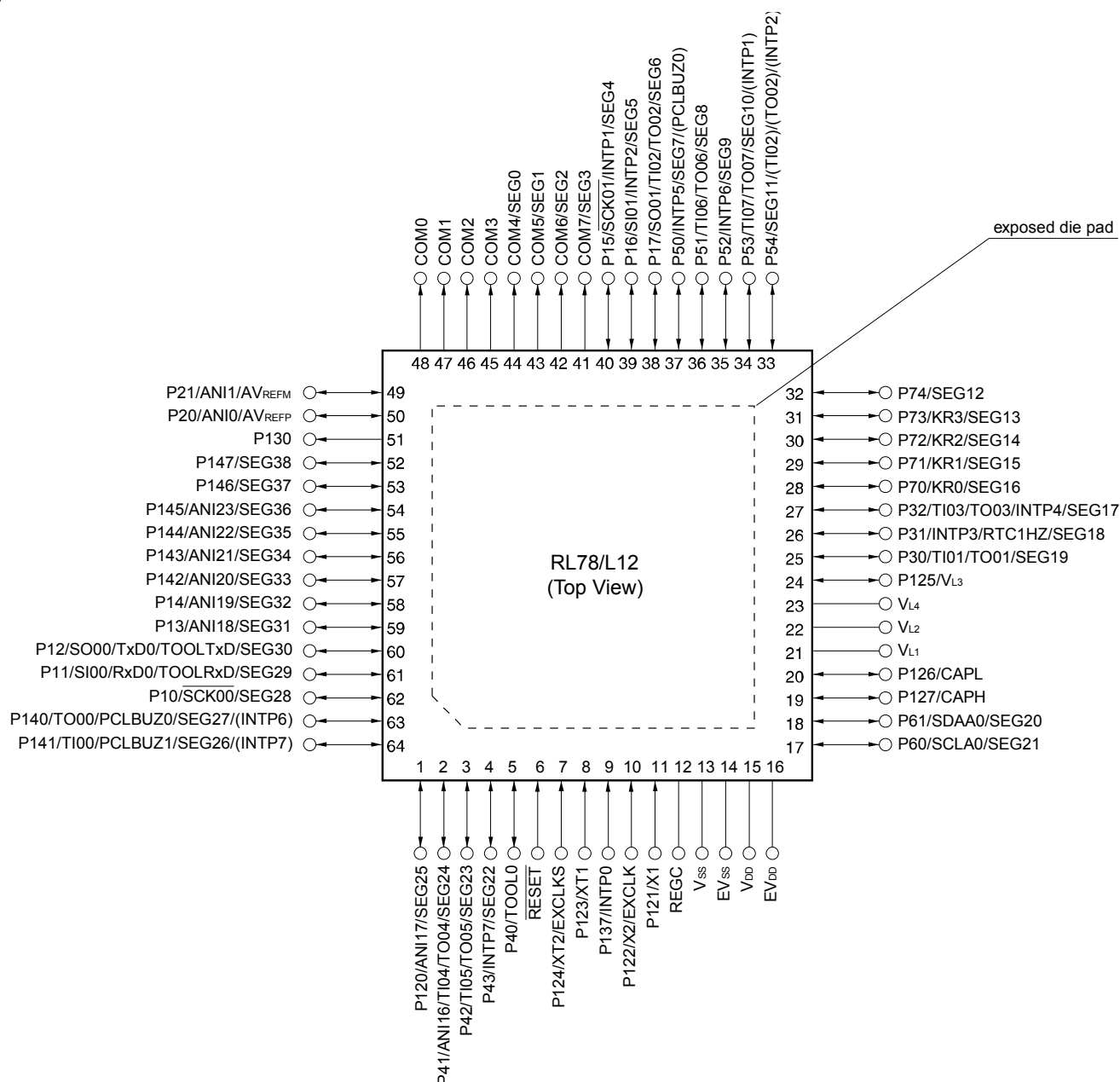
Remarks 1. For pin identification, see 1.4 Pin Identification.

- 2.** Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR).

1.3.5 64-pin products

- 64-pin plastic WQFN (8 × 8)

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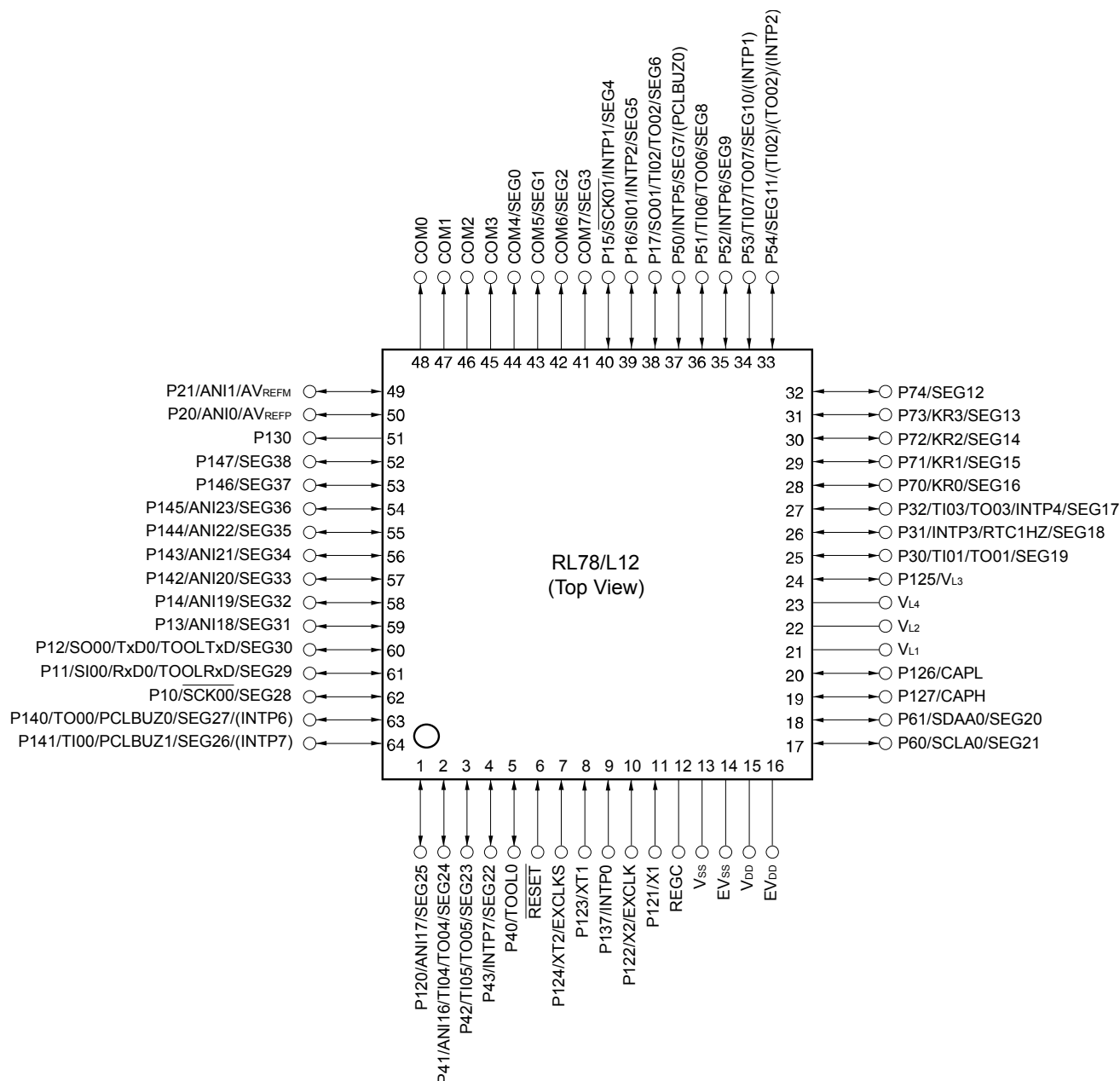


- Cautions**
1. Make EV_{ss} pin the same potential as V_{ss} pin.
 2. Make V_{DD} pin the same potential as EV_{DD} pin.
 3. Connect the REGC pin to V_{ss} via a capacitor (0.47 to 1 μ F).

- Remarks**
1. For pin identification, see 1.4 Pin Identification.
 2. When using the microcontroller for an application where the noise generated inside the microcontroller must be reduced, it is recommended to supply separate powers to the V_{DD} and EV_{DD} pins and connect the V_{ss} and EV_{ss} pins to separate ground lines.
 3. Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR).

- 64-pin plastic LQFP (fine pitch) (10 × 10)
- 64-pin plastic LQFP (12 × 12)

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- Cautions**
1. Make EV_{SS} pin the same potential as V_{SS} pin.
 2. Make V_{DD} pin the same potential as EV_{DD} pin.
 3. Connect the REGC pin to V_{SS} via a capacitor (0.47 to 1 μ F).

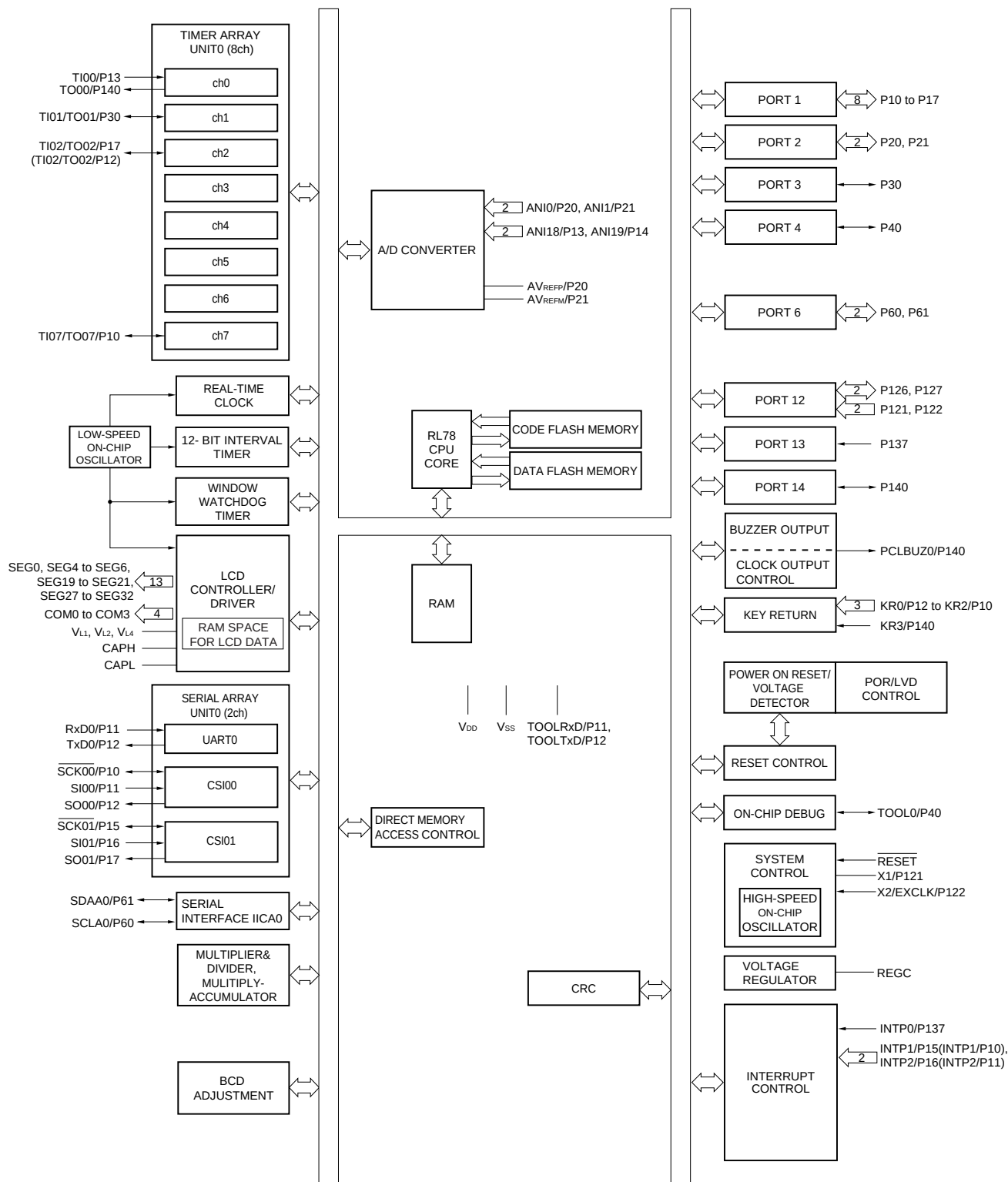
- Remarks**
1. For pin identification, see **1.4 Pin Identification**.
 2. When using the microcontroller for an application where the noise generated inside the microcontroller must be reduced, it is recommended to supply separate powers to the V_{DD} and EV_{DD} pins and connect the V_{SS} and EV_{SS} pins to separate ground lines.
 3. Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR).

1.4 Pin Identification

ANI0, ANI1,		P130, P137:	Port 13
ANI16 to ANI23:	Analog Input	P140 to P147:	Port 14
AVREFM:	Analog Reference Voltage Minus	PCLBUZ0, PCLBUZ1:	Programmable Clock Output/Buzzer Output
AVREFP:	Analog Reference Voltage Plus	REGC:	Regulator Capacitance
CAPH, CAPL:	Capacitor for LCD	<u>RESET</u> :	Reset
COM0 to COM7,		RTC1HZ:	Real-time Clock Correction Clock (1 Hz) Output
EVDD:	Power Supply for Port	RxD0:	Receive Data
EVSS:	Ground for Port	<u>SCK00</u> , <u>SCK01</u> :	Serial Clock Input/Output
EXCLK:	External Clock Input (Main System Clock)	SCLA0:	Serial Clock Input/Output
EXCLKS:	External Clock Input (Subsystem Clock)	SDAA0:	Serial Data Input/Output
INTP0 to INTP7:	Interrupt Request From Peripheral	SEG0 to SEG38:	LCD Segment Output
KR0 to KR3:	Key Return	SI00, SI01:	Serial Data Input
P10 to P17:	Port 1	SO00, SO01:	Serial Data Output
P20, P21:	Port 2	TI00 to TI07:	Timer Input
P30 to P32:	Port 3	TO00 to TO07:	Timer Output
P40 to P43:	Port 4	TOOL0:	Data Input/Output for Tool
P50 to P54:	Port 5	TOOLRxD, TOOLTxD:	Data Input/Output for External Device
P60, P61:	Port 6	TxD0:	Transmit Data
P70 to P74:	Port 7	VDD:	Power Supply
P120 to P127:	Port 12	VL1 to VL4:	LCD Power Supply
		VSS:	Ground
		X1, X2:	Crystal Oscillator (Main System Clock)
		XT1, XT2:	Crystal Oscillator (Subsystem Clock)

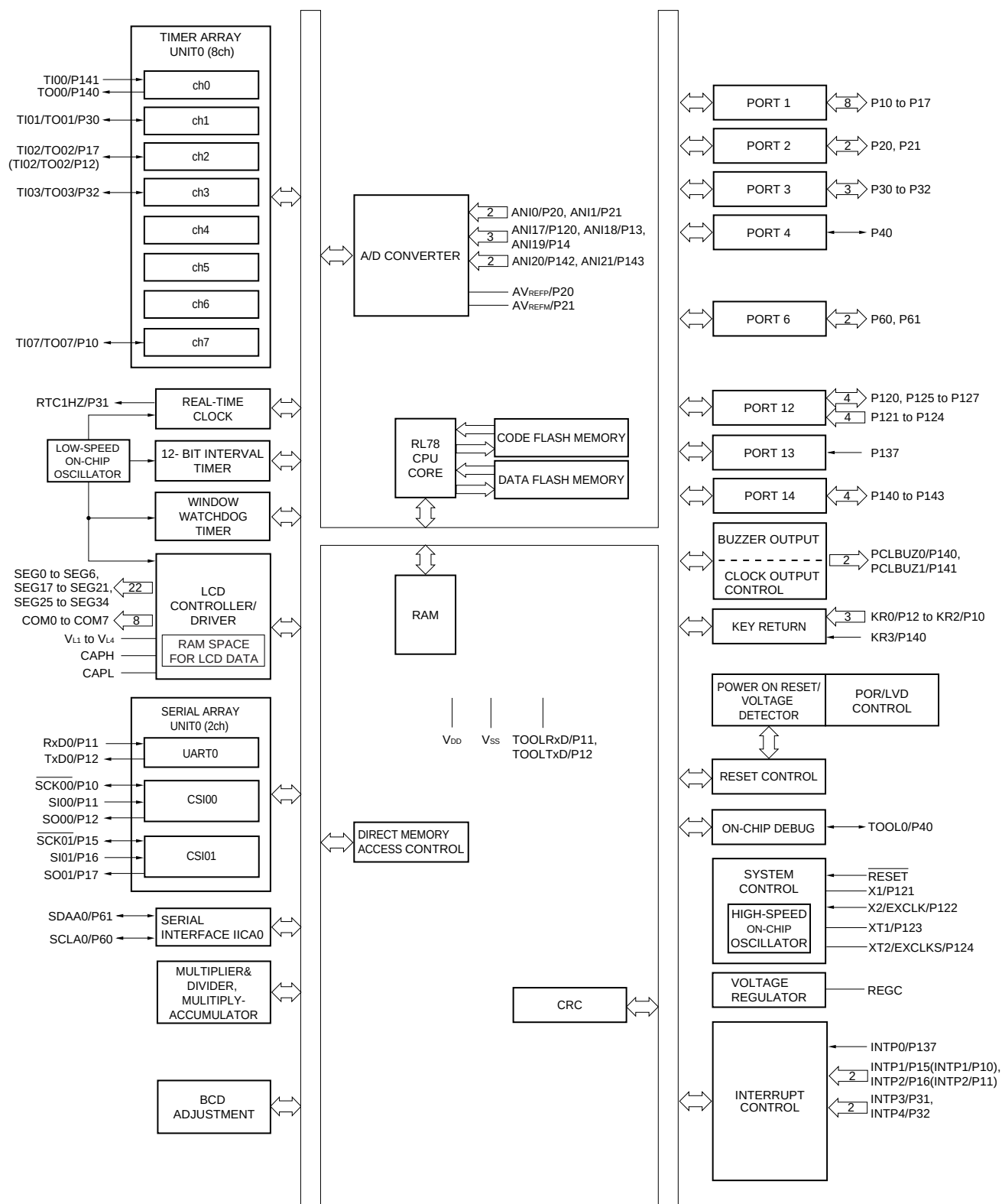
1.5 Block Diagram

1.5.1 32-pin products



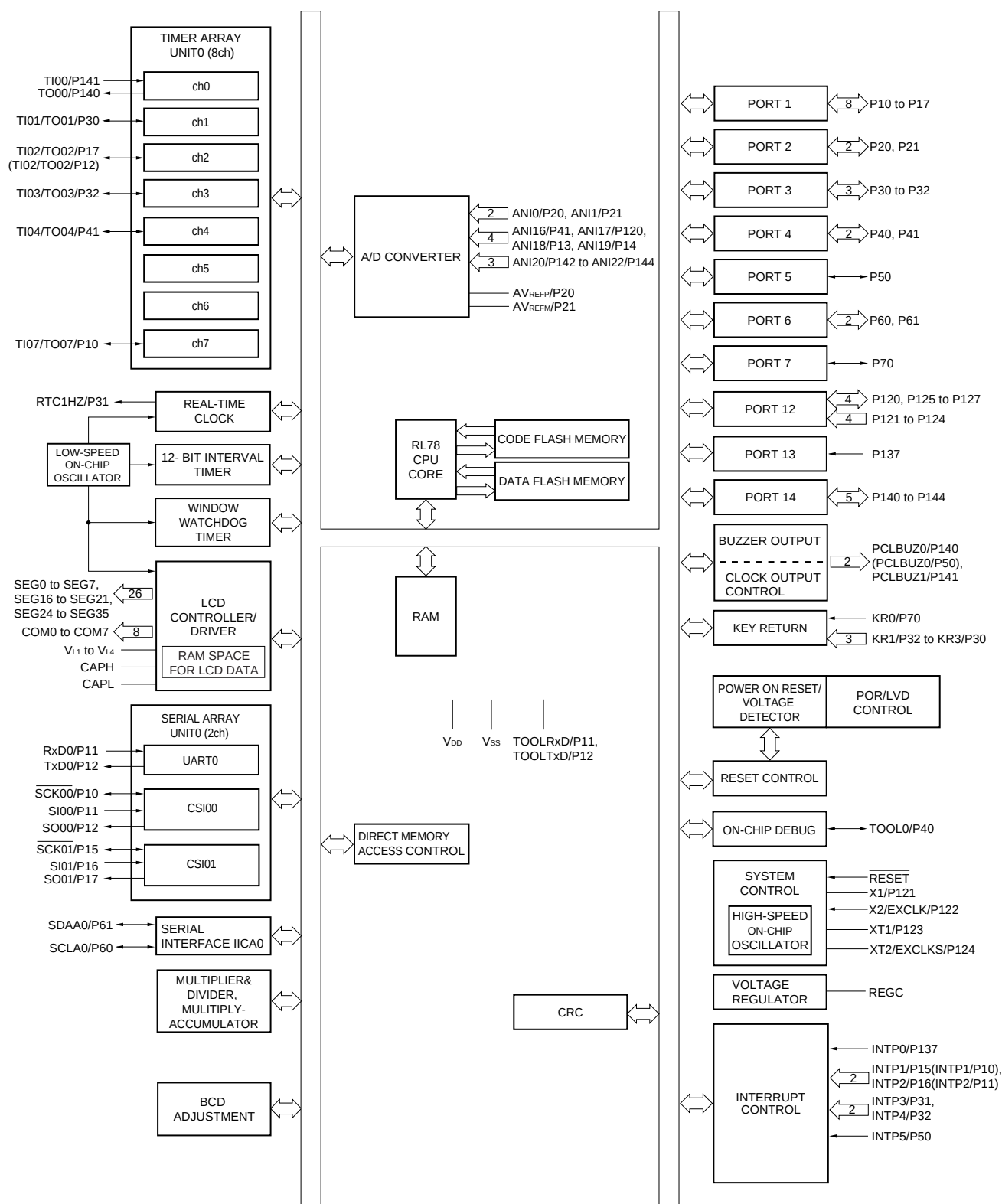
Remark Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR)

1.5.2 44-pin products



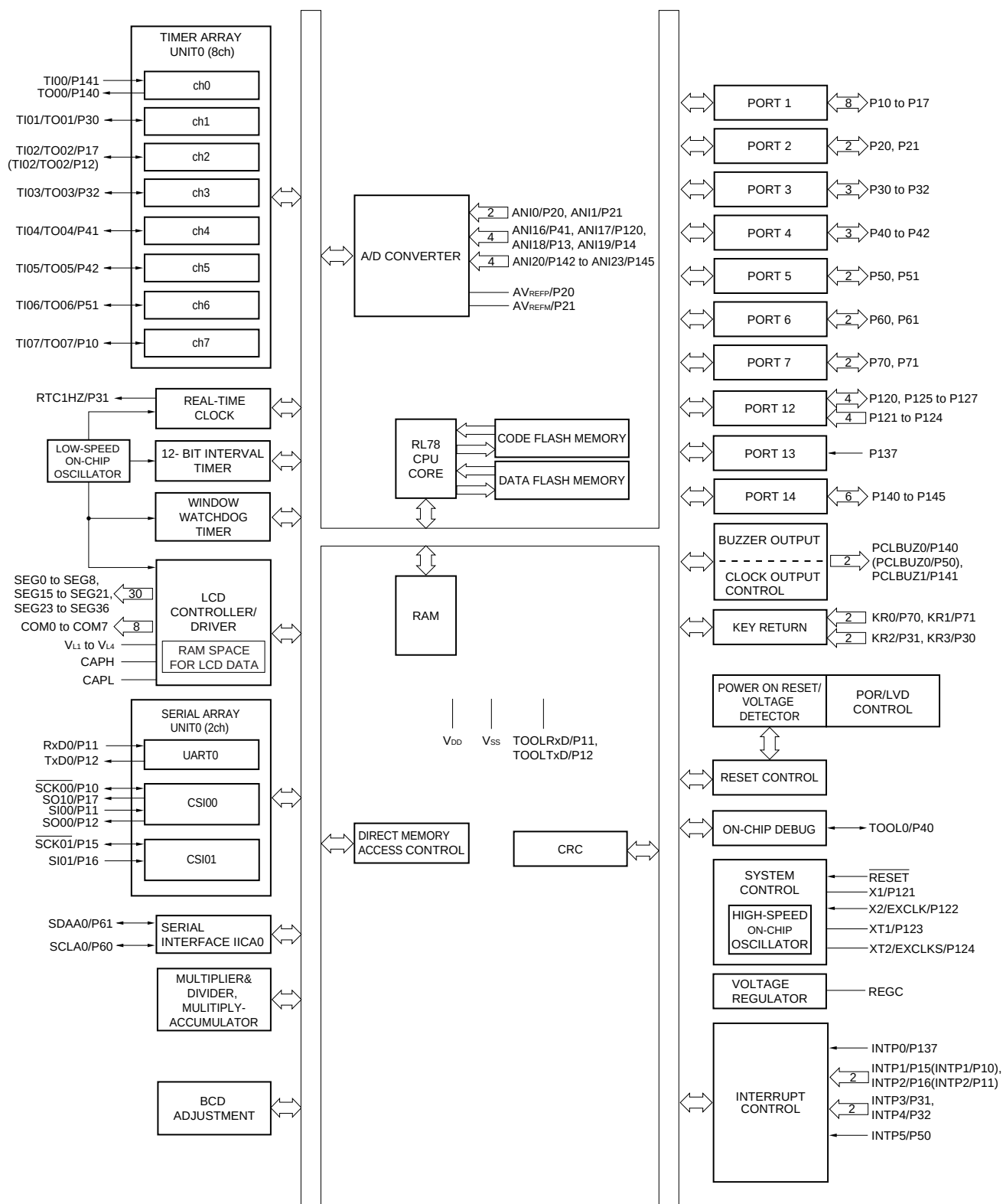
Remark Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR)

1.5.3 48-pin products



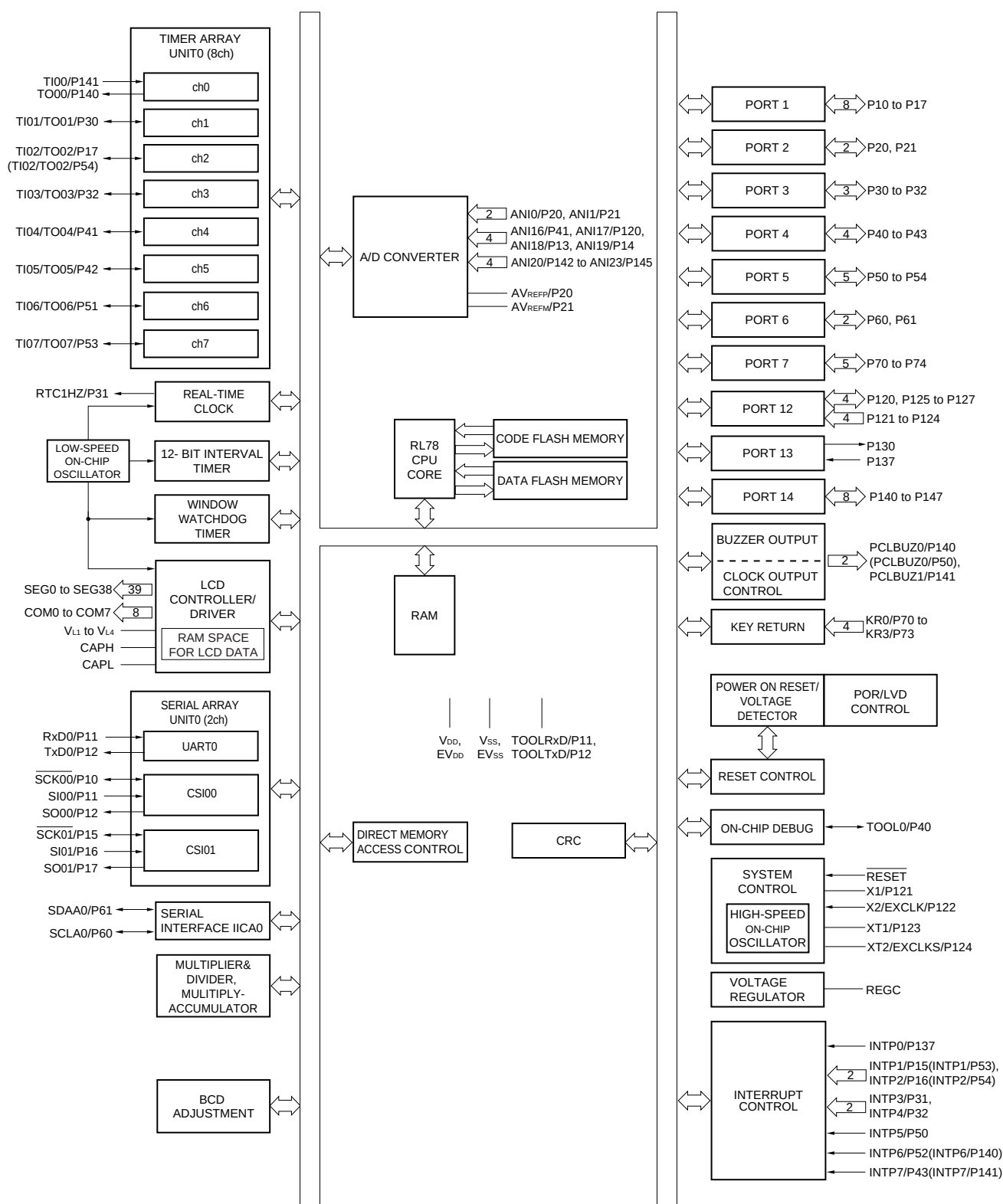
Remark Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR)

1.5.4 52-pin products



Remark Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR)

1.5.5 64-pin products



Remark Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR)

1.6 Outline of Functions

Caution This outline describes the functions at the time when Peripheral I/O redirection register (PIOR) is set to 00H.

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Item		32-pin	44-pin	48-pin	52-pin	64-pin
		R5F10RBx	R5F10RFx	R5F10RGx	R5F10RJx	R5F10RLx
Code flash memory (KB)		8 to 32	8 to 32	8 to 32	8 to 32	16, 32
Data flash memory (KB)		2	2	2	2	2
RAM (KB)		1, 1.5 ^{Note 1}	1, 1.5 ^{Note 1}	1, 1.5 ^{Note 1}	1, 1.5 ^{Note 1}	1, 1.5 ^{Note 1}
Memory space		1 MB				
Main system clock	High-speed system clock	X1 (crystal/ceramic) oscillation, external main system clock input (EXCLK) HS (high-speed main) operation: 1 to 20 MHz (V _{DD} = 2.7 to 5.5 V), HS (high-speed main) operation: 1 to 16 MHz (V _{DD} = 2.4 to 5.5 V), LS (low-speed main) operation: 1 to 8 MHz (V _{DD} = 1.8 to 5.5 V), LV (low-voltage main) operation: 1 to 4 MHz (V _{DD} = 1.6 to 5.5 V)				
	High-speed on-chip oscillator clock	HS (high-speed main) operation: 1 to 24 MHz (V _{DD} = 2.7 to 5.5 V), HS (high-speed main) operation: 1 to 16 MHz (V _{DD} = 2.4 to 5.5 V), LS (low-speed main) operation: 1 to 8 MHz (V _{DD} = 1.8 to 5.5 V), LV (low-voltage main) operation: 1 to 4 MHz (V _{DD} = 1.6 to 5.5 V)				
Subsystem clock		–	XT1 (crystal) oscillation , external subsystem clock input (EXCLKS) 32.768 kHz (TYP.): V _{DD} = 1.6 to 5.5 V			
Low-speed on-chip oscillator clock		Internal oscillation 15 kHz (TYP.): V _{DD} = 1.6 to 5.5 V				
General-purpose register		8 bits × 32 registers (8 bits × 8 registers × 4 banks)				
Minimum instruction execution time		0.04167 μs (High-speed on-chip oscillator clock: f _{IH} = 24 MHz operation)				
		0.05 μs (High-speed system clock: f _{MX} = 20 MHz operation)				
		30.5 μs (Subsystem clock: f _{SUB} = 32.768 kHz operation)				
Instruction set		• Data transfer (8/16 bits) • Adder and subtractor/logical operation (8/16 bits) • Multiplication (8 bits × 8 bits) • Rotate, barrel shift, and bit manipulation (Set, reset, test, and Boolean operation), etc.				
Total number of I/O port pins and pins dedicated to drive an LCD		28	40	44	48	58
I/O port	Total	20	29	33	37	47
	CMOS I/O	15	22	26	30	39
	CMOS input	3	5	5	5	5
	CMOS output	–	–	–	–	1
	N-ch open-drain I/O (EV _{DD} tolerance)	2	2	2	2	2
Pins dedicated to drive an LCD		8	11	11	11	11
LCD controller/driver		Internal voltage boosting method, capacitor split method, and external resistance division method are switchable.				
Segment signal output		13	22 (18) ^{Note 2}	26 (22) ^{Note 2}	30 (26) ^{Note 2}	39 (35) ^{Note 2}
Common signal output		4	4 (8) ^{Note 2}			

Notes 1. In the case of the 1 KB, and 1.5 KB, this is 630 bytes when the self-programming function and data flash function is used.

2. The values in parentheses are the number of signal outputs when 8 com is used.

(2/2)

Item		32-pin	44-pin	48-pin	52-pin	64-pin
		R5F10RBx	R5F10RFx	R5F10RGx	R5F10RJx	R5F10RLx
Timer	16-bit timer	8 channels	8 channels (with 1 channel remote control output function)			
	Watchdog timer	1 channel				
	Real-time clock (RTC)	1 channel				
	12-bit interval timer (IT)	1 channel				
	Timer output	4 channels (PWM outputs: 3 ^{Note 1})	5 channels (PWM outputs: 4 ^{Note 1})	6 channels (PWM outputs: 5 ^{Note 1})	8 channels (PWM outputs: 7 ^{Note 1})	
	RTC output	–	1 • 1 Hz (subsystem clock: f _{SUB} = 32.768 kHz or)			
Clock output/buzzer output		1	2			
		• 2.44 kHz, 4.88 kHz, 9.76 kHz, 1.25 MHz, 2.5 MHz, 5 MHz, 10 MHz (Main system clock: f _{MAIN} = 20 MHz operation) • 256 Hz, 512 Hz, 1.024 kHz, 2.048 kHz, 4.096 kHz, 8.192 kHz, 16.384 kHz, 32.768 kHz (Subsystem clock: f _{SUB} = 32.768 kHz operation)				
8/10-bit resolution A/D converter		4 channels	7 channels	9 channels	10 channels	10 channels
Serial interface		• CSI: 2 channel/UART (LIN-bus supported): 1 channel				
	I ² C bus	1 channel	1 channel	1 channel	1 channel	1 channel
Multiplier and divider/multiply-accumulator		• 16 bits × 16 bits = 32 bits (Unsigned or signed) • 32 bits ÷ 32 bits = 32 bits (Unsigned) • 16 bits × 16 bits + 32 bits = 32 bits (Unsigned or signed)				
DMA controller		2 channels				
Vectored interrupt sources	Internal	23	23	23	23	23
	External	4	6	7	7	9
Key interrupt		4				
Reset		• Reset by $\overline{\text{RESET}}$ pin • Internal reset by watchdog timer • Internal reset by power-on-reset • Internal reset by voltage detector • Internal reset by illegal instruction execution ^{Note 2} • Internal reset by RAM parity error • Internal reset by illegal-memory access				
Power-on-reset circuit		• Power-on-reset: 1.51 ±0.04 V • Power-down-reset: 1.50 ±0.04 V				
Voltage detector		• Rising edge : 1.67 V to 4.06 V (14 stages) • Falling edge : 1.63 V to 3.98 V (14 stages)				
On-chip debug function		Provided				
Power supply voltage		V _{DD} = 1.6 to 5.5 V				
Operating ambient temperature		T _A = –40 to +85 °C				

Notes 1. The number of PWM outputs varies depending on the setting of channels in use (the number of masters and slaves).

2. The illegal instruction is generated when instruction code FFH is executed.

Reset by the illegal instruction execution not issued by emulation with the in-circuit emulator or on-chip debug emulator.

2. ELECTRICAL SPECIFICATIONS (A, G: T_A = -40 to +85°C)

This chapter describes the electrical specifications for the products "A: Consumer applications (T_A = -40 to +85°C)" and "G: Industrial applications (with T_A = -40 to +85°C)".

- Cautions**
1. The RL78 microcontrollers have an on-chip debug function, which is provided for development and evaluation. Do not use the on-chip debug function in products designated for mass production, because the guaranteed number of rewritable times of the flash memory may be exceeded when this function is used, and product reliability therefore cannot be guaranteed. Renesas Electronics is not liable for problems occurring when the on-chip debug function is used.
 2. With products not provided with an EV_{DD}, or EV_{SS} pin, replace EV_{DD} with V_{DD}, or replace EV_{SS} with V_{SS}.

2.1 Absolute Maximum Ratings

Absolute Maximum Ratings (T_A = 25°C)

(1/3)

Parameter	Symbols	Conditions	Ratings	Unit
Supply voltage	V _{DD}	V _{DD} = EV _{DD}	-0.5 to +6.5	V
	EV _{DD}	V _{DD} = EV _{DD}	-0.5 to +6.5	V
	EV _{SS}		-0.5 to +0.3	V
REGC pin input voltage	V _{IREGC}	REGC	-0.3 to +2.8 and -0.3 to V _{DD} + 0.3 ^{Note 1}	V
Input voltage	V _{I1}	P10 to P17, P30 to P32, P40 to P43, P50 to P54, P70 to P74, P120, P125 to P127, P140 to P147	-0.3 to EV _{DD} + 0.3 and -0.3 to V _{DD} + 0.3 ^{Note 2}	V
	V _{I2}	P60, P61 (N-ch open-drain)	-0.3 to EV _{DD} + 0.3 and -0.3 to V _{DD} + 0.3 ^{Note 2}	V
	V _{I3}	P20, P21, P121 to P124, P137, EXCLK, EXCLKS, RESET	-0.3 to V _{DD} + 0.3 ^{Note 2}	V
Output voltage	V _{O1}	P10 to P17, P30 to P32, P40 to P43, P50 to P54, P60, P61, P70 to P74, P120, P125 to P127, P130, P140 to P147	-0.3 to EV _{DD} + 0.3 and -0.3 to V _{DD} + 0.3 ^{Note 2}	V
	V _{O2}	P20, P21	-0.3 to V _{DD} + 0.3 ^{Note 2}	V
Analog input voltage	V _{AI1}	ANI16 to ANI23	-0.3 to EV _{DD} + 0.3 and -0.3 to AV _{REF(+)} + 0.3 Notes 2, 3	V
	V _{AI2}	ANI0, ANI1	-0.3 to V _{DD} + 0.3 and -0.3 to AV _{REF(+)} + 0.3 Notes 2, 3	V

- Notes**
1. Connect the REGC pin to V_{SS} via a capacitor (0.47 to 1 μF). This value regulates the absolute maximum rating of the REGC pin. Do not use this pin with voltage applied to it.
 2. Must be 6.5 V or lower.
 3. Do not exceed AV_{REF(+)} + 0.3 V in case of A/D conversion target pin.

Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

- Remarks**
1. Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.
 2. AV_{REF(+)} : + side reference voltage of the A/D converter.
 3. V_{SS} : Reference voltage

Absolute Maximum Ratings (T_A = 25°C)**(2/3)**

Parameter	Symbols	Conditions	Ratings	Unit
LCD voltage	V _{L1}	V _{L1} voltage ^{Note 1}	-0.3 to +2.8 and -0.3 to V _{L4} + 0.3	V
	V _{L2}	V _{L2} voltage ^{Note 1}	-0.3 to V _{L4} + 0.3 ^{Note 2}	V
	V _{L3}	V _{L3} voltage ^{Note 1}	-0.3 to V _{L4} + 0.3 ^{Note 2}	V
	V _{L4}	V _{L4} voltage ^{Note 1}	-0.3 to +6.5	V
	V _{LCAP}	CAPL, CAPH voltage ^{Note 1}	-0.3 to V _{L4} + 0.3 ^{Note 2}	V
	V _{LOUT}	COM0 to COM7, SEG0 to SEG38, output voltage	External resistance division method Capacitor split method Internal voltage boosting method	-0.3 to V _{DD} + 0.3 ^{Note 2} -0.3 to V _{DD} + 0.3 ^{Note 2} -0.3 to V _{L4} + 0.3 ^{Note 2}

Notes 1. This value only indicates the absolute maximum ratings when applying voltage to the V_{L1}, V_{L2}, V_{L3}, and V_{L4} pins; it does not mean that applying voltage to these pins is recommended. When using the internal voltage boosting method or capacitance split method, connect these pins to V_{SS} via a capacitor (0.47 μ F $\pm$ 30%) and connect a capacitor (0.47 μ F $\pm$ 30%) between the CAPL and CAPH pins.

2. Must be 6.5 V or lower.

Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

Remark V_{SS} : Reference voltage

Absolute Maximum Ratings (T_A = 25°C)**(3/3)**

Parameter	Symbols	Conditions		Ratings	Unit
Output current, high	I _{OH1}	Per pin	P10 to P17, P30 to P32, P40 to P43, P50 to P54, P70 to P74, P120, P125 to P127, P130, P140 to P147	−40	mA
		Total of all pins −170 mA	P10 to P14, P40 to P43, P120, P130, P140 to P147	−70	mA
			P15 to P17, P30 to P32, P50 to P54, P70 to P74, P125 to P127	−100	mA
	I _{OH2}	Per pin	P20, P21	−0.5	mA
		Total of all pins		−1	mA
Output current, low	I _{OL1}	Per pin	P10 to P17, P30 to P32, P40 to P43, P50 to P54, P60, P61, P70 to P74, P120, P125 to P127, P130, P140 to P147	40	mA
		Total of all pins 170 mA	P10 to P14, P40 to P43, P120, P130, P140 to P147	70	mA
			P15 to P17, P30 to P32, P50 to P54, P60, P61, P70 to P74, P125 to P127	100	mA
	I _{OL2}	Per pin	P20, P21	1	mA
		Total of all pins		2	mA
Operating ambient temperature	T _A	In normal operation mode		−40 to +85	°C
		In flash memory programming mode			
Storage temperature	T _{stg}			−65 to +150	°C

Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

2.2 Oscillator Characteristics

2.2.1 X1, XT1 oscillator characteristics

(T_A = -40 to +85°C, 1.6 V ≤ E_{VDD} = V_{DD} ≤ 5.5 V, V_{SS} = E_{VSS} = 0 V)

Parameter	Resonator	Conditions	MIN.	TYP.	MAX.	Unit
X1 clock oscillation frequency (f _X) ^{Note}	Ceramic resonator/ crystal resonator	2.7 V ≤ V _{DD} ≤ 5.5 V	1.0		20.0	MHz
		2.4 V ≤ V _{DD} ≤ 2.7 V	1.0		16.0	MHz
		1.8 V ≤ V _{DD} < 2.7 V	1.0		8.0	MHz
		1.6 V ≤ V _{DD} < 1.8 V	1.0		4.0	MHz
XT1 clock oscillation frequency (f _{XT}) ^{Note}	Crystal resonator		32	32.768	35	kHz

Note Indicates only permissible oscillator frequency ranges. Refer to **2.4 AC Characteristics** for instruction execution time. Request evaluation by the manufacturer of the oscillator circuit mounted on a board to check the oscillator characteristics.

Caution Since the CPU is started by the high-speed on-chip oscillator clock after a reset release, check the X1 clock oscillation stabilization time using the oscillation stabilization time counter status register (OSTC) by the user. Determine the oscillation stabilization time of the OSTC register and the oscillation stabilization time select register (OSTS) after sufficiently evaluating the oscillation stabilization time with the resonator to be used.

2.2.2 On-chip oscillator characteristics

(T_A = -40 to +85°C, 1.6 V ≤ E_{VDD} = V_{DD} ≤ 5.5 V, V_{SS} = E_{VSS} = 0 V)

Oscillators	Parameters	Conditions		MIN.	TYP.	MAX.	Unit
High-speed on-chip oscillator clock frequency ^{Notes 1, 2}	f _{IH}			1		24	MHz
High-speed on-chip oscillator clock frequency accuracy		-20 to +85°C	1.8 V ≤ V _{DD} ≤ 5.5 V	-1		+1	%
			1.6 V ≤ V _{DD} < 1.8 V	-5		+5	%
		-40 to -20°C	1.8 V ≤ V _{DD} ≤ 5.5 V	-1.5		+1.5	%
			1.6 V ≤ V _{DD} < 1.8 V	-5.5		+5.5	%
Low-speed on-chip oscillator clock frequency	f _{IL}				15		kHz
Low-speed on-chip oscillator clock frequency accuracy				-15		+15	%

Notes 1. High-speed on-chip oscillator frequency is selected by bits 0 to 3 of option byte (000C2H) and bits 0 to 2 of HOCODIV register.

2. This indicates the oscillator characteristics only. Refer to **2.4 AC Characteristics** for instruction execution time.

2.3 DC Characteristics

2.3.1 Pin characteristics

(T_A = -40 to +85°C, 1.6 V ≤ EV_{DD} = V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS} = 0 V)

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Items	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Output current, high ^{Note 1}	I _{OH1}	Per pin for P10 to P17, P30 to P32, P40 to P43, P50 to P54, P70 to P74, P120, P125 to P127, P130, P140 to P147				-10.0 Note 2	mA
		Total of P10 to P14, P40 to P43, P120, P130, P140 to P147 (When duty = 70% ^{Note 3})	4.0 V ≤ EV _{DD} ≤ 5.5 V			-40.0	mA
			2.7 V ≤ EV _{DD} < 4.0 V			-8.0	mA
			1.8 V ≤ EV _{DD} < 2.7 V			-4.0	mA
			1.6 V ≤ EV _{DD} < 1.8 V			-2.0	mA
		Total of P15 to P17, P30 to P32, P50 to P54, P70 to P74, P125 to P127 (When duty = 70% ^{Note 3})	4.0 V ≤ EV _{DD} ≤ 5.5 V			-60.0	mA
			2.7 V ≤ EV _{DD} < 4.0 V			-15.0	mA
			1.8 V ≤ EV _{DD} < 2.7 V			-8.0	mA
			1.6 V ≤ EV _{DD} < 1.8 V			-4.0	mA
		Total of all pins (When duty = 70% ^{Note 3})				-100.0	mA
	I _{OH2}	P20, P21	Per pin			-0.1	mA
			Total of all pins	1.6 V ≤ V _{DD} ≤ 5.5 V		-0.2	mA

- Notes**
1. Value of current at which the device operation is guaranteed even if the current flows from the V_{DD} and EV_{DD} pins to an output pin.
 2. Do not exceed the total current value.
 3. Specification under conditions where the duty factor ≤ 70%.

The output current value that has changed to the duty factor > 70% the duty ratio can be calculated with the following expression (when changing the duty factor from 70% to n%).

- Total output current of pins = (I_{OH} × 0.7)/(n × 0.01)

<Example> Where n = 80% and I_{OH} = -40.0 mA

$$\text{Total output current of pins} = (-40.0 \times 0.7)/(80 \times 0.01) \cong -35.0 \text{ mA}$$

However, the current that is allowed to flow into one pin does not vary depending on the duty factor. A current higher than the absolute maximum rating must not flow into one pin.

Caution P10, P12, P15, and P17 do not output high level in N-ch open-drain mode.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

(T_A = -40 to +85°C, 1.6 V ≤ E_{VDD} = V_{DD} ≤ 5.5 V, V_{SS} = E_{VSS} = 0 V)

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Items	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Output current, low ^{Note 1}	I _{OL1}	Per pin for P10 to P17, P30 to P32, P40 to P43, P50 to P54, P70 to P74, P120, P125 to P127, P130, P140 to P147				20.0 ^{Note 2}	mA
		Per pin for P60, P61				15.0 ^{Note 2}	mA
		Total of P10 to P14, P40 to P43, P120, P130, P140 to P147 (When duty = 70% ^{Note 3})	4.0 V ≤ E _{VDD} ≤ 5.5 V			70.0	mA
			2.7 V ≤ E _{VDD} < 4.0 V			15.0	mA
			1.8 V ≤ E _{VDD} < 2.7 V			9.0	mA
			1.6 V ≤ E _{VDD} < 1.8 V			4.5	mA
		Total of P15 to P17, P30 to P32, P50 to P54, P60, P61, P70 to P74, P125 to P127 (When duty = 70% ^{Note 3})	4.0 V ≤ E _{VDD} ≤ 5.5 V			80.0	mA
			2.7 V ≤ E _{VDD} < 4.0 V			35.0	mA
			1.8 V ≤ E _{VDD} < 2.7 V			20.0	mA
			1.6 V ≤ E _{VDD} < 1.8 V			10.0	mA
		Total of all pins (When duty = 70% ^{Note 3})				150.0	mA
	I _{OL2}	P20, P21	Per pin			0.4	mA
		Total of all pins		1.6 V ≤ V _{DD} ≤ 5.5 V		0.8	mA

Notes 1. Value of current at which the device operation is guaranteed even if the current flows from the V_{DD} and E_{VDD} pins to an output pin.

2. Do not exceed the total current value.

3. Specification under conditions where the duty factor ≤ 70%.

The output current value that has changed to the duty factor > 70% the duty ratio can be calculated with the following expression (when changing the duty factor from 70% to n%).

- Total output current of pins = (I_{OH} × 0.7)/(n × 0.01)

<Example> Where n = 80% and I_{OL} = 70.0 mA

$$\text{Total output current of pins} = (70.0 \times 0.7)/(80 \times 0.01) \cong 61.25 \text{ mA}$$

However, the current that is allowed to flow into one pin does not vary depending on the duty factor. A current higher than the absolute maximum rating must not flow into one pin.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

(T_A = -40 to +85°C, 1.6 V ≤ EV_{DD} = V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS} = 0 V)

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Items	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Input voltage, high	V _{IH1}	P10 to P17, P30 to P32, P40 to P43, P50 to P54, P70 to P74, P120, P125 to P127, P140 to P147	Normal input buffer	0.8EV _{DD}		EV _{DD}	V
	V _{IH2}	P10, P11, P15, P16	TTL input buffer 4.0 V ≤ EV _{DD} ≤ 5.5 V	2.2		EV _{DD}	V
			TTL input buffer 3.3 V ≤ EV _{DD} < 4.0 V	2.0		EV _{DD}	V
			TTL input buffer 1.6 V ≤ EV _{DD} < 3.3 V	1.50		EV _{DD}	V
	V _{IH3}	P20, P21		0.7V _{DD}		V _{DD}	V
	V _{IH4}	P60, P61		0.7EV _{DD}		EV _{DD}	V
	V _{IH5}	P121 to P124, P137, EXCLK, EXCLKS, RESET		0.8V _{DD}		V _{DD}	V
Input voltage, low	V _{IL1}	P10 to P17, P30 to P32, P40 to P43, P50 to P54, P70 to P74, P120, P125 to P127, P140 to P147	Normal input buffer	0		0.2EV _{DD}	V
	V _{IL2}	P10, P11, P15, P16	TTL input buffer 4.0 V ≤ EV _{DD} ≤ 5.5 V	0		0.8	V
			TTL input buffer 3.3 V ≤ EV _{DD} < 4.0 V	0		0.5	V
			TTL input buffer 1.6 V ≤ EV _{DD} < 3.3 V	0		0.32	V
	V _{IL3}	P20, P21		0		0.3V _{DD}	V
	V _{IL4}	P60, P61		0		0.3EV _{DD}	V
	V _{IL5}	P121 to P124, P137, EXCLK, EXCLKS, RESET		0		0.2V _{DD}	V

Caution The maximum value of V_{IH} of P10, P12, P15, P17 is EV_{DD}, even in the N-ch open-drain mode.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

(T_A = -40 to +85°C, 1.6 V ≤ E_{VDD} = V_{DD} ≤ 5.5 V, V_{SS} = E_{VSS} = 0 V)

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Items	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Output voltage, high	V _{OH1}	P10 to P17, P30 to P32, P40 to P43, P50 to P54, P70 to P74, P120, P125 to P127, P130, P140 to P147	4.0 V ≤ E _{VDD} ≤ 5.5 V, I _{OH1} = -10 mA	E _{VDD} -1.5		V
			4.0 V ≤ E _{VDD} ≤ 5.5 V, I _{OH1} = -3.0 mA	E _{VDD} -0.7		V
			2.7 V ≤ E _{VDD} ≤ 5.5 V, I _{OH1} = -2.0 mA	E _{VDD} -0.6		V
			1.8 V ≤ E _{VDD} ≤ 5.5 V, I _{OH1} = -1.5 mA	E _{VDD} -0.5		V
			1.6 V ≤ E _{VDD} ≤ 5.5 V, I _{OH1} = -1.0 mA	E _{VDD} -0.5		V
	V _{OH2}	P20, P21	1.6 V ≤ V _{DD} ≤ 5.5 V, I _{OH2} = -100 μA	V _{DD} -0.5		V
Output voltage, low	V _{OL1}	P10 to P17, P30 to P32, P40 to P43, P50 to P54, P70 to P74, P120, P125 to P127, P130, P140 to P147	4.0 V ≤ E _{VDD} ≤ 5.5 V, I _{OL1} = 20 mA		1.3	V
			4.0 V ≤ E _{VDD} ≤ 5.5 V, I _{OL1} = 8.5 mA		0.7	V
			2.7 V ≤ E _{VDD} ≤ 5.5 V, I _{OL1} = 3.0 mA		0.6	V
			2.7 V ≤ E _{VDD} ≤ 5.5 V, I _{OL1} = 1.5 mA		0.4	V
			1.8 V ≤ E _{VDD} ≤ 5.5 V, I _{OL1} = 0.6 mA		0.4	V
			1.6 V ≤ E _{VDD} < 5.5 V, I _{OL1} = 0.3 mA		0.4	V
	V _{OL2}	P20, P21	1.6 V ≤ V _{DD} ≤ 5.5 V, I _{OL2} = 400 μA		0.4	V
	V _{OL3}	P60, P61	4.0 V ≤ E _{VDD} ≤ 5.5 V, I _{OL3} = 15.0 mA		2.0	V
			4.0 V ≤ E _{VDD} ≤ 5.5 V, I _{OL3} = 5.0 mA		0.4	V
			2.7 V ≤ E _{VDD} ≤ 5.5 V, I _{OL3} = 3.0 mA		0.4	V
			1.8 V ≤ E _{VDD} ≤ 5.5 V, I _{OL3} = 2.0 mA		0.4	V
			1.6 V ≤ E _{VDD} < 5.5 V, I _{OL3} = 1.0 mA		0.4	V

Caution P10, P12, P15, P17 do not output high level in N-ch open-drain mode.**Remark** Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

(T_A = -40 to +85°C, 1.6 V ≤ E_{VDD} = V_{DD} ≤ 5.5 V, V_{SS} = E_{VSS} = 0 V)

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Items	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Input leakage current, high	I _{LIH1}	P10 to P17, P30 to P32, P40 to P43, P50 to P54, P60, P61, P70 to P74, P120, P125 to P127, P140 to P147	V _I = E _{VDD}			1	μA
	I _{LIH2}	P20, P21, P137, RESET	V _I = V _{DD}			1	μA
	I _{LIH3}	P121 to P124 (X1, X2, XT1, XT2, EXCLK, EXCLKS)	V _I = V _{DD}	In input port or external clock input		1	μA
				In resonator connection		10	μA
Input leakage current, low	I _{LIL1}	P10 to P17, P30 to P32, P40 to P43, P50 to P54, P60, P61, P70 to P74, P120, P125 to P127, P140 to P147	V _I = E _{VSS}			-1	μA
	I _{LIL2}	P20, P21, P137, RESET	V _I = V _{SS}			-1	μA
	I _{LIL3}	P121 to P124 (X1, X2, XT1, XT2, EXCLK, EXCLKS)	V _I = V _{SS}	In input port or external clock input		-1	μA
				In resonator connection		-10	μA
On-chip pll-up resistance	R _{U1}	V _I = E _{VSS}	SEGxx port				
			2.4 V ≤ E _{VDD} = V _{DD} ≤ 5.5 V		10	20	100
			1.6 V ≤ E _{VDD} = V _{DD} < 2.4 V		10	30	100
	R _{U2}		Ports other than above (Except for P60, P61, and P130)		10	20	100

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

2.3.2 Supply current characteristics

(T_A = -40 to +85°C, 1.6 V ≤ E_{VDD} = V_{DD} ≤ 5.5 V, V_{SS} = E_{VSS} = 0 V)

(1/3)

Parameter	Symbol	Conditions					MIN.	TYP.	MAX.	Unit
Supply current Note 1	I _{DD1}	Operating mode	HS (high-speed main) mode ^{Note 5}	f _{IH} = 24 MHz ^{Note 3}	Basic operation	V _{DD} = 5.0 V		1.5		mA
						V _{DD} = 3.0 V		1.5		mA
				f _{IH} = 16 MHz ^{Note 3}	Normal operation	V _{DD} = 5.0 V		3.3	5.0	mA
						V _{DD} = 3.0 V		3.3	5.0	mA
			LS (low-speed main) mode ^{Note 5}	f _{IH} = 8 MHz ^{Note 3}	Normal operation	V _{DD} = 5.0 V		2.5	3.7	mA
						V _{DD} = 3.0 V		2.5	3.7	mA
			LV (low-voltage main) mode ^{Note 5}	f _{IH} = 4 MHz ^{Note 3}	Normal operation	V _{DD} = 3.0 V		1.2	1.8	mA
						V _{DD} = 2.0 V		1.2	1.8	mA
			HS (high-speed main) mode ^{Note 5}	f _{MX} = 20 MHz ^{Note 2} , V _{DD} = 5.0 V	Normal operation	Square wave input		2.8	4.4	mA
						Resonator connection		3.0	4.6	mA
				f _{MX} = 20 MHz ^{Note 2} , V _{DD} = 3.0 V	Normal operation	Square wave input		2.8	4.4	mA
						Resonator connection		3.0	4.6	mA
				f _{MX} = 10 MHz ^{Note 2} , V _{DD} = 5.0 V	Normal operation	Square wave input		1.8	2.6	mA
						Resonator connection		1.8	2.6	mA
				f _{MX} = 10 MHz ^{Note 2} , V _{DD} = 3.0 V	Normal operation	Square wave input		1.8	2.6	mA
						Resonator connection		1.8	2.6	mA
			LS (low-speed main) mode ^{Note 5}	f _{MX} = 8 MHz ^{Note 2} , V _{DD} = 3.0 V	Normal operation	Square wave input		1.1	1.7	mA
						Resonator connection		1.1	1.7	mA
				f _{MX} = 8 MHz ^{Note 2} , V _{DD} = 2.0 V	Normal operation	Square wave input		1.1	1.7	mA
						Resonator connection		1.1	1.7	mA
			Subsystem clock operation	f _{SUB} = 32.768 kHz ^{Note 4} , T _A = -40°C	Normal operation	Square wave input		3.5	4.9	μA
						Resonator connection		3.6	5.0	μA
				f _{SUB} = 32.768 kHz ^{Note 4} , T _A = +25°C	Normal operation	Square wave input		3.6	4.9	μA
						Resonator connection		3.7	5.0	μA
				f _{SUB} = 32.768 kHz ^{Note 4} , T _A = +50°C	Normal operation	Square wave input		3.7	5.5	μA
						Resonator connection		3.8	5.6	μA
				f _{SUB} = 32.768 kHz ^{Note 4} , T _A = +70°C	Normal operation	Square wave input		3.8	6.3	μA
						Resonator connection		3.9	6.4	μA
				f _{SUB} = 32.768 kHz ^{Note 4} , T _A = +85°C	Normal operation	Square wave input		4.1	7.7	μA
						Resonator connection		4.2	7.8	μA

(Notes and Remarks are listed on the next page.)

- Notes**
1. Total current flowing into V_{DD} and EV_{DD}, including the input leakage current flowing when the level of the input pin is fixed to V_{DD}, EV_{DD} or V_{SS}, EV_{SS}. The values below the MAX. column include the peripheral operation current. However, not including the current flowing into the A/D converter, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors and the current flowing during data flash rewrite.
 2. When high-speed on-chip oscillator and subsystem clock are stopped.
 3. When high-speed system clock and subsystem clock are stopped.
 4. When high-speed on-chip oscillator and high-speed system clock are stopped. When AMPHS1 = 1 (Ultra-low power consumption oscillation). However, not including the current flowing into the RTC, 12-bit interval timer, watchdog timer, and LCD controller/driver.
 5. Relationship between operation voltage width, operation frequency of CPU and operation mode is as below.
 - HS (high-speed main) mode: $2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ @1 MHz to 24 MHz
 - $2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ @1 MHz to 16 MHz
 - LS (low-speed main) mode: $1.8\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ @1 MHz to 8 MHz
 - LV (low-voltage main) mode: $1.6\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ @1 MHz to 4 MHz

- Remarks**
1. f_{MX}: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)
 2. f_{IH}: High-speed on-chip oscillator clock frequency
 3. f_{SUB}: Subsystem clock frequency (XT1 clock oscillation frequency)
 4. Except subsystem clock operation, temperature condition of the TYP. value is T_A = 25°C

(T_A = -40 to +85°C, 1.6 V ≤ EV_{DD} = V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS} = 0 V)

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Parameter	Symbol	Conditions				MIN.	TYP.	MAX.	Unit	
Supply current Note 1	I _{DD2} Note 2	HALT mode	HS (high-speed main) mode Note 7	f _{IH} = 24 MHz Note 4	V _{DD} = 5.0 V		0.44	1.28	mA	
					V _{DD} = 3.0 V		0.44	1.28	mA	
				f _{IH} = 16 MHz Note 4	V _{DD} = 5.0 V		0.40	1.00	mA	
					V _{DD} = 3.0 V		0.40	1.00	mA	
			LS (low-speed main) mode Note 7	f _{IH} = 8 MHz Note 4	V _{DD} = 3.0 V		260	530	μA	
					V _{DD} = 2.0 V		260	530	μA	
			LV (low-voltage main) mode Note 7	f _{IH} = 4 MHz Note 4	V _{DD} = 3.0 V		420	640	μA	
					V _{DD} = 2.0 V		420	640	μA	
			HS (high-speed main) mode Note 7	f _{MX} = 20 MHz Note 3, V _{DD} = 5.0 V	Square wave input		0.28	1.00	mA	
					Resonator connection		0.45	1.17	mA	
				f _{MX} = 20 MHz Note 3, V _{DD} = 3.0 V	Square wave input		0.28	1.00	mA	
					Resonator connection		0.45	1.17	mA	
				f _{MX} = 10 MHz Note 3, V _{DD} = 5.0 V	Square wave input		0.19	0.60	mA	
					Resonator connection		0.26	0.67	mA	
				f _{MX} = 10 MHz Note 3, V _{DD} = 3.0 V	Square wave input		0.19	0.60	mA	
					Resonator connection		0.26	0.67	mA	
			LS (low-speed main) mode Note 7	f _{MX} = 8 MHz Note 3, V _{DD} = 3.0 V	Square wave input		95	330	μA	
					Resonator connection		145	380	μA	
				f _{MX} = 8 MHz Note 3, V _{DD} = 2.0 V	Square wave input		95	330	μA	
					Resonator connection		145	380	μA	
			Subsystem clock operation	f _{SUB} = 32.768 kHz Note 5, T _A = −40°C	Square wave input		0.31	0.57	μA	
					Resonator connection		0.50	0.76	μA	
				f _{SUB} = 32.768 kHz Note 5, T _A = +25°C	Square wave input		0.37	0.57	μA	
					Resonator connection		0.56	0.76	μA	
				f _{SUB} = 32.768 kHz Note 5, T _A = +50°C	Square wave input		0.46	1.17	μA	
					Resonator connection		0.65	1.36	μA	
				f _{SUB} = 32.768 kHz Note 5, T _A = +70°C	Square wave input		0.57	1.97	μA	
					Resonator connection		0.76	2.16	μA	
				f _{SUB} = 32.768 kHz Note 5, T _A = +85°C	Square wave input		0.85	3.37	μA	
					Resonator connection		1.04	3.56	μA	
	I _{DD3} Note 6	STOP mode Note 8	T _A = −40°C					0.17	0.50	μA
			T _A = +25°C					0.23	0.50	μA
			T _A = +50°C					0.32	1.10	μA
			T _A = +70°C					0.43	1.90	μA
			T _A = +85°C					0.71	3.30	μA

(Notes and Remarks are listed on the next page.)

- Notes**
1. Total current flowing into V_{DD} and EV_{DD} , including the input leakage current flowing when the level of the input pin is fixed to V_{DD} , EV_{DD} or V_{SS} , EV_{SS} . The values below the MAX. column include the peripheral operation current. However, not including the current flowing into the A/D converter, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors and the current flowing during data flash rewrite.
 2. During HALT instruction execution by flash memory.
 3. When high-speed on-chip oscillator and subsystem clock are stopped.
 4. When high-speed system clock and subsystem clock are stopped.
 5. When high-speed on-chip oscillator and high-speed system clock are stopped. When $RTCLPC = 1$ and setting ultra-low current consumption ($AMPHS1 = 1$). The current flowing into the RTC is included. However, not including the current flowing into the 12-bit interval timer, watchdog timer, and LCD controller/driver.
 6. Not including the current flowing into the RTC, 12-bit interval timer, and watchdog timer.
 7. Relationship between operation voltage width, operation frequency of CPU and operation mode is as below.
HS (high-speed main) mode: $2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}@1\text{ MHz to }24\text{ MHz}$
 $2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}@1\text{ MHz to }16\text{ MHz}$
LS (low-speed main) mode: $1.8\text{ V} \leq V_{DD} \leq 5.5\text{ V}@1\text{ MHz to }8\text{ MHz}$
LV (low-voltage main) mode: $1.6\text{ V} \leq V_{DD} \leq 5.5\text{ V}@1\text{ MHz to }4\text{ MHz}$
 8. Regarding the value for current to operate the subsystem clock in STOP mode, refer to that in HALT mode.

- Remarks 1.** f_{MX} : High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)
2. f_{IH} : High-speed on-chip oscillator clock frequency
3. f_{SUB} : Subsystem clock frequency (XT1 clock oscillation frequency)
4. Except subsystem clock operation and STOP mode, temperature condition of the TYP. value is $T_A = 25^{\circ}\text{C}$

(T_A = -40 to +85°C, 1.6 V ≤ E_{VDD} = V_{DD} ≤ 5.5 V, V_{SS} = E_{VSS} = 0 V)

(3/3)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Low-speed on-chip oscillator operating current	I _{FIL} ^{Note 1}				0.20		μA
RTC operating current	I _{RTC} ^{Notes 1, 2, 3}	f _{MAIN} is stopped			0.08		μA
12-bit interval timer current	I _{IT} ^{Notes 1, 2, 4}				0.08		μA
Watchdog timer operating current	I _{WDT} ^{Notes 1, 2, 5}	f _{IL} = 15 kHz			0.24		μA
A/D converter operating current	I _{ADC} ^{Notes 1, 6}	When conversion at maximum speed	Normal mode, AV _{REFP} = V _{DD} = 5.0 V		1.3	1.7	mA
			Low voltage mode, AV _{REFP} = V _{DD} = 3.0 V		0.5	0.7	mA
A/D converter reference voltage current	I _{ADREF} ^{Note 1}				75.0		μA
Temperature sensor operating current	I _{TMPS} ^{Note 1}				75.0		μA
LVD operating current	I _{LVD} ^{Notes 1, 7}				0.08		μA
Self-programming operating current	I _{FSP} ^{Notes 1, 9}				2.50	12.20	mA
BGO operating current	I _{BGO} ^{Notes 1, 8}				2.00	12.20	mA
LCD operating current	I _{LCD1} ^{Notes 11, 12}	External resistance division method	V _{DD} = E _{VDD} = 5.0 V V _{L4} = 5.0 V		0.04	0.20	μA
	I _{LCD2} ^{Note 11}	Internal voltage boosting method	V _{DD} = E _{VDD} = 5.0 V V _{L4} = 5.1 V (VLCD = 12H)		1.12	3.70	μA
			V _{DD} = E _{VDD} = 3.0 V V _{L4} = 3.0 V (VLCD = 04H)		0.63	2.20	μA
	I _{LCD3} ^{Note 11}	Capacitor split method	V _{DD} = E _{VDD} = 3.0 V V _{L4} = 3.0 V		0.12	0.50	μA
SNOOZE operating current	I _{SNOZ} ^{Note 1}	ADC operation	The mode is performed ^{Note 10}		0.50	0.60	mA
			The A/D conversion operations are performed, Low voltage mode, AV _{REFP} = V _{DD} = 3.0 V		1.20	1.44	mA
		CSI/UART operation			0.70	0.84	mA

(Notes and Remarks are listed on the next page.)

Notes 1. Current flowing to V_{DD}.

2. When high speed on-chip oscillator and high-speed system clock are stopped.
3. Current flowing only to the real-time clock (RTC) (excluding the operating current of the low-speed on-chip oscillator and the XT1 oscillator). The supply current of the RL78 microcontrollers is the sum of the values of either I_{DD1} or I_{DD2}, and I_{RTC}, when the real-time clock operates in operation mode or HALT mode. When the low-speed on-chip oscillator is selected, I_{FIL} should be added. I_{DD2} subsystem clock operation includes the operational current of the real-time clock.
4. Current flowing only to the 12-bit interval timer (excluding the operating current of the low-speed on-chip oscillator and the XT1 oscillator). The supply current of the RL78 microcontrollers is the sum of the values of either I_{DD1} or I_{DD2}, and I_{IT}, when the 12-bit interval timer operates in operation mode or HALT mode. When the low-speed on-chip oscillator is selected, I_{FIL} should be added.
5. Current flowing only to the watchdog timer (including the operating current of the low-speed on-chip oscillator). The supply current of the RL78 microcontrollers is the sum of I_{DD1}, I_{DD2} or I_{DD3} and I_{WDT} when the watchdog timer is in operation.
6. Current flowing only to the A/D converter. The supply current of the RL78 microcontrollers is the sum of I_{DD1} or I_{DD2} and I_{ADC} when the A/D converter operates in an operation mode or the HALT mode.
7. Current flowing only to the LVD circuit. The supply current of the RL78 microcontrollers is the sum of I_{DD1}, I_{DD2} or I_{DD3} and I_{LVD} when the LVD circuit is in operation.
8. Current flowing only during data flash rewrite.
9. Current flowing only during self programming.
10. For shift time to the SNOOZE mod.
11. Current flowing only to the LCD controller/driver. The supply current value of the RL78 microcontrollers is the sum of the LCD operating current (I_{LCD1}, I_{LCD2} or I_{LCD3}) to the supply current (I_{DD1} or I_{DD2}) when the LCD controller/driver operates in an operation mode or HALT mode. Not including the current that flows through the LCD panel.
The TYP. value and MAX. value are following conditions.
 - When f_{SUB} is selected for system clock, LCD clock = 128 Hz (LCDC0 = 07H)
 - 4-Time-Slice, 1/3 Bias Method
12. Not including the current that flows through the external divider resistor when the external resistance division method is used.

Remarks 1. f_{IL}: Low-speed on-chip oscillator clock frequency

2. f_{SUB}: Subsystem clock frequency (XT1 clock oscillation frequency)
3. f_{CLK}: CPU/peripheral hardware clock frequency
4. Temperature condition of the TYP. value is T_A = 25°C

2.4 AC Characteristics

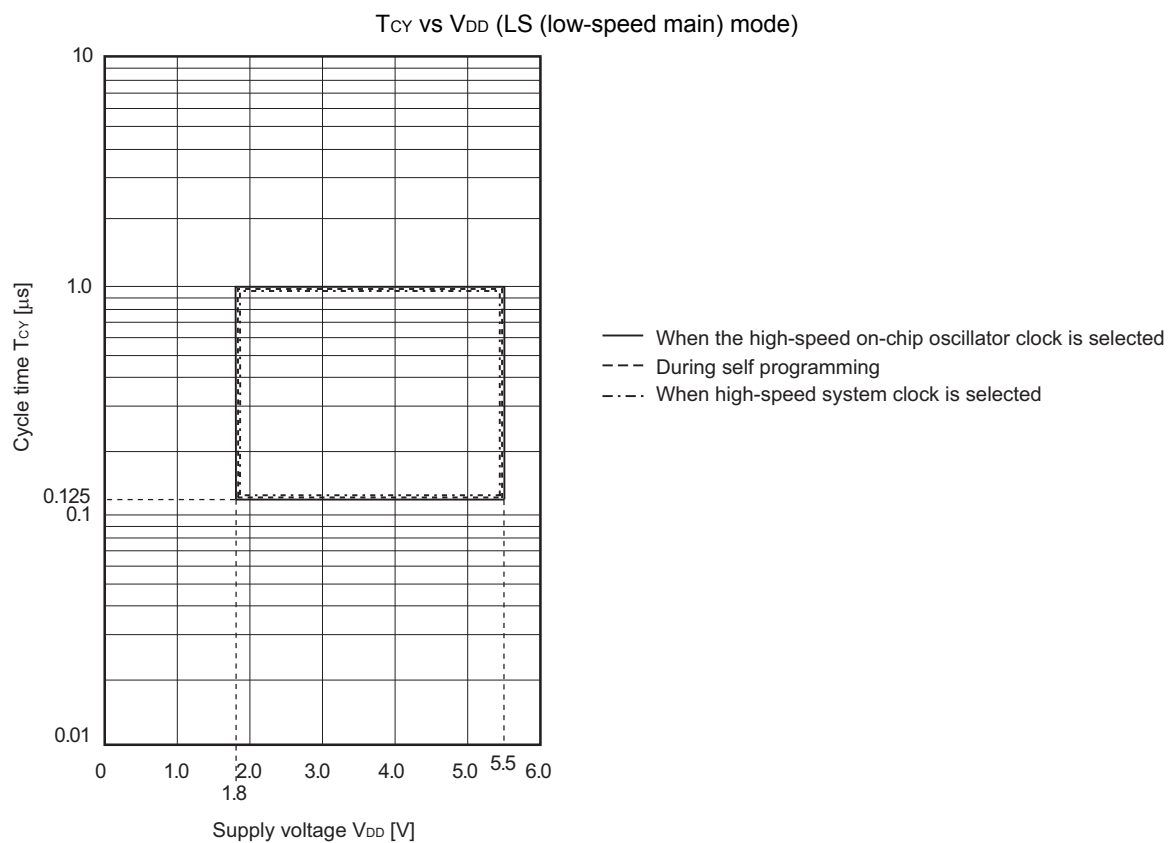
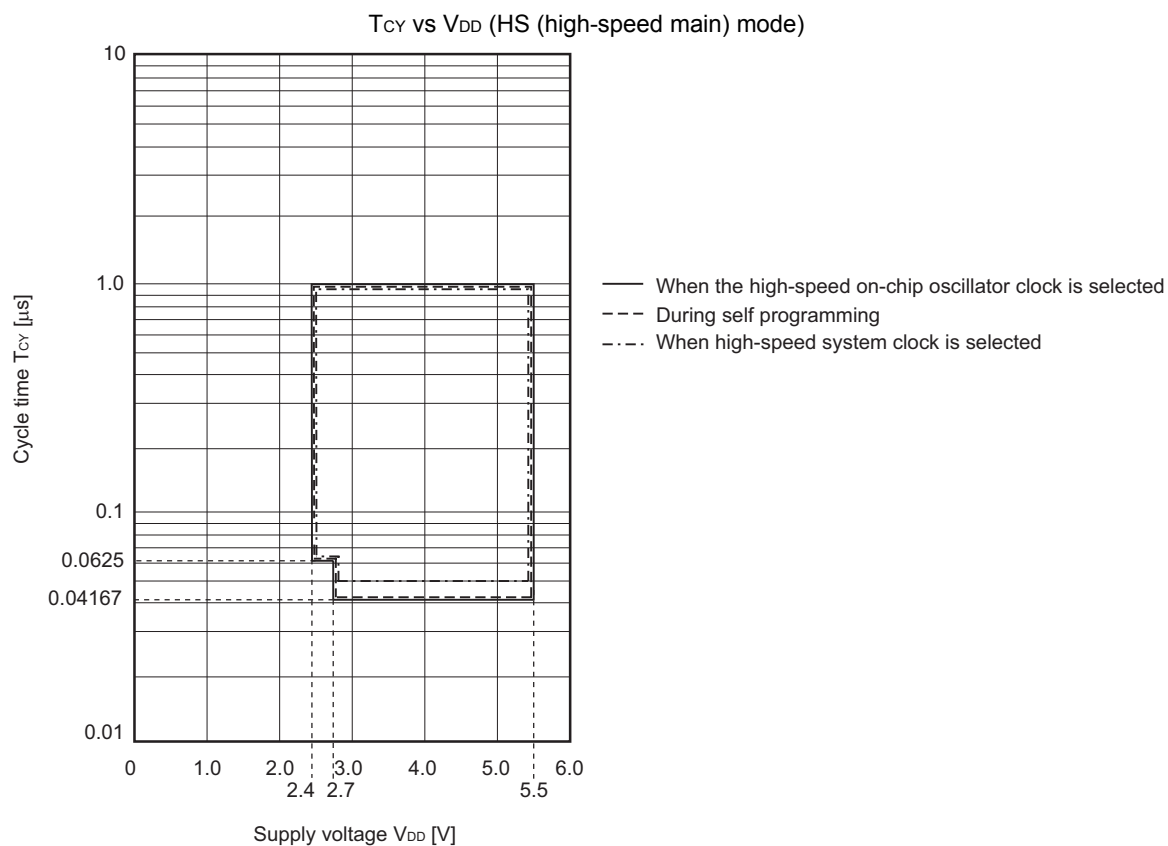
2.4.1 Basic operation

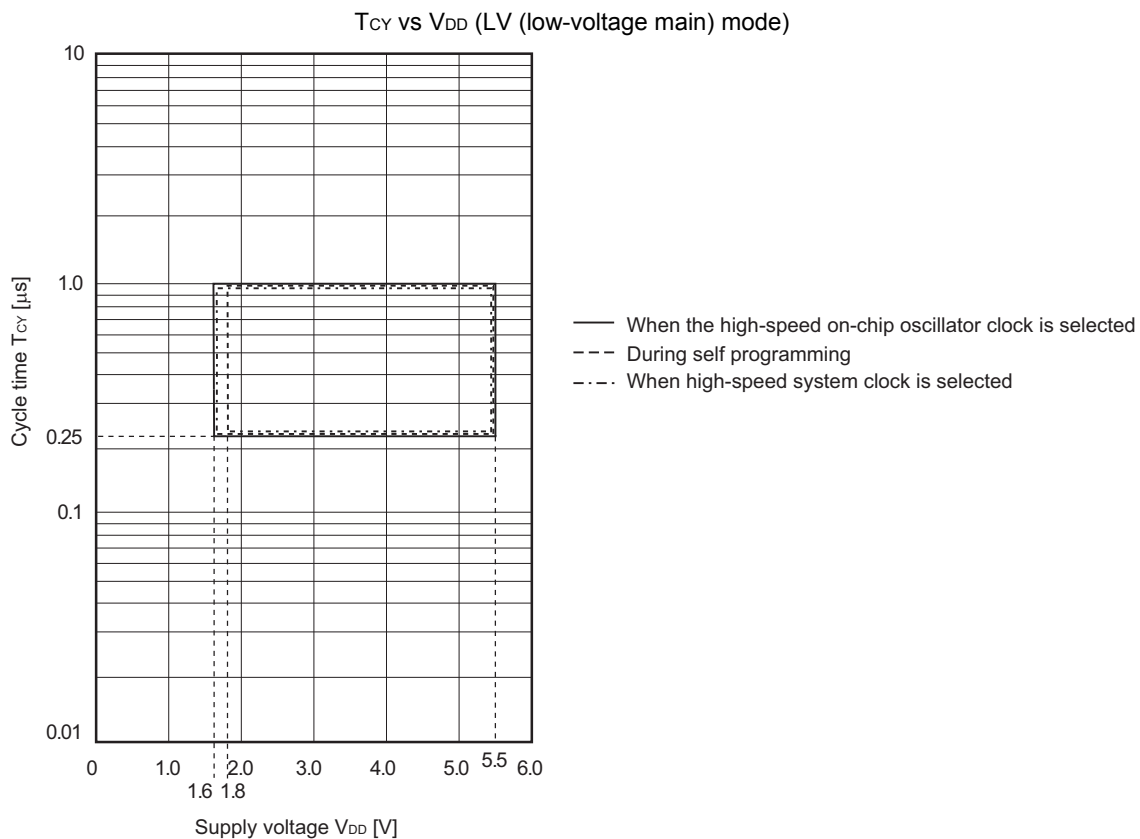
(T_A = -40 to +85°C, 1.6 V ≤ E_{VDD} = V_{DD} ≤ 5.5 V, V_{SS} = E_{VSS} = 0 V)

Items	Symbol	Conditions		MIN.	TYP.	MAX.	Unit	
Instruction cycle (minimum instruction execution time)	T _{cy}	Main system clock (f _{MAIN}) operation	HS (high-speed main) mode	2.7 V ≤ V _{DD} ≤ 5.5 V	0.04167		1	μs
				2.4 V ≤ V _{DD} < 2.7 V	0.0625		1	μs
			LV (low voltage main) mode	1.6 V ≤ V _{DD} ≤ 5.5 V	0.25		1	μs
			LS (low-speed main) mode	1.8 V ≤ V _{DD} ≤ 5.5 V	0.125		1	μs
		Subsystem clock (f _{SUB}) operation		1.8 V ≤ V _{DD} ≤ 5.5 V	28.5	30.5	31.3	μs
		In the self programming mode	HS (high-speed main) mode	2.7 V ≤ V _{DD} ≤ 5.5 V	0.04167		1	μs
				2.4 V ≤ V _{DD} < 2.7 V	0.0625		1	μs
			LV (low voltage main) mode	1.8 V ≤ V _{DD} ≤ 5.5 V	0.25		1	μs
			LS (low-speed main) mode	1.8 V ≤ V _{DD} ≤ 5.5 V	0.125		1	μs
External main system clock frequency	f _{EX}	2.7 V ≤ V _{DD} ≤ 5.5 V		1.0		20.0	MHz	
		2.4 V ≤ V _{DD} < 2.7 V		1.0		16.0	MHz	
		1.8 V ≤ V _{DD} < 2.4 V		1.0		8.0	MHz	
		1.6 V ≤ V _{DD} < 1.8 V		1.0		4.0	MHz	
	f _{EXS}			32		35	kHz	
External main system clock input high-level width, low-level width	t _{EXH} , t _{EXL}	2.7 V ≤ V _{DD} ≤ 5.5 V		24			ns	
		2.4 V ≤ V _{DD} < 2.7 V		30			ns	
		1.8 V ≤ V _{DD} < 2.4 V		60			ns	
		1.6 V ≤ V _{DD} < 1.8 V		120			ns	
	t _{EXHS} , t _{EXLS}			13.7			μs	
TI00 to TI07 input high-level width, low-level width	t _{TIH} , t _{TIL}			1/f _{MCK} +10			ns	
TO00 to TO07 output frequency	f _{TO}	HS (high-speed main) mode	4.0 V ≤ EV _{DD} ≤ 5.5 V			16	MHz	
			2.7 V ≤ EV _{DD} < 4.0 V			8	MHz	
			2.4 V ≤ EV _{DD} < 2.7 V			4	MHz	
		LS (low-speed main) mode	1.8 V ≤ EV _{DD} ≤ 5.5 V			4	MHz	
		LV (low voltage main) mode	1.6 V ≤ EV _{DD} ≤ 5.5 V			2	MHz	
PCLBUZ0, PCLBUZ1 output frequency	f _{PCL}	HS (high-speed main) mode	4.0 V ≤ EV _{DD} ≤ 5.5 V			16	MHz	
			2.7 V ≤ EV _{DD} < 4.0 V			8	MHz	
			2.4 V ≤ EV _{DD} < 2.7 V			4	MHz	
		LS (low-speed main) mode	1.8 V ≤ EV _{DD} ≤ 5.5 V			4	MHz	
		LV (low-voltage main) mode	1.8 V ≤ EV _{DD} ≤ 5.5 V			4	MHz	
			1.6 V ≤ EV _{DD} < 1.8 V			2	MHz	
Interrupt input high-level width, low-level width	t _{INTH} , t _{INTL}	INTP0	1.6 V ≤ V _{DD} ≤ 5.5 V	1			μs	
		INTP1 to INTP7	1.6 V ≤ EV _{DD} ≤ 5.5 V	1			μs	
Key interrupt input low-level width	t _{KR}	KR0 to KR3	1.8 V ≤ EV _{DD} ≤ 5.5 V	250			ns	
			1.6 V ≤ EV _{DD} < 1.8 V	1			μs	
RESET low-level width	t _{RSL}			10			μs	

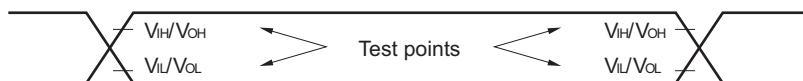
Remark f_{MCK}: Timer array unit operation clock frequency

(Operation clock to be set by the CKS0n bit of timer mode register 0n (TMR0n). n: Channel number (n = 0 to 7))

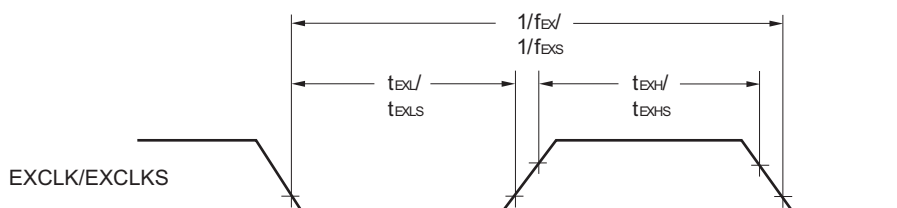
Minimum Instruction Execution Time during Main System Clock Operation

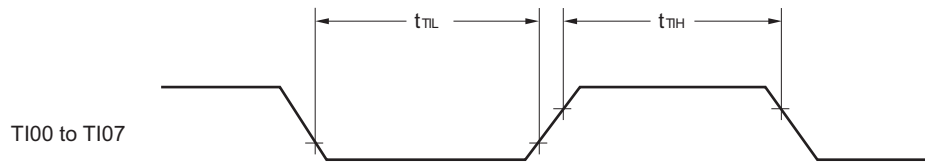
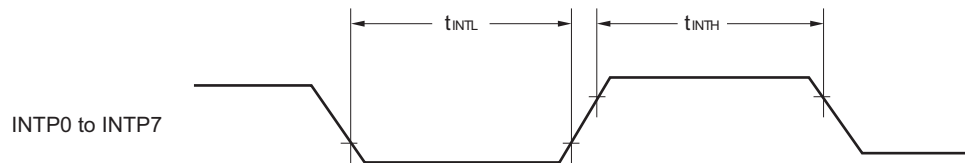
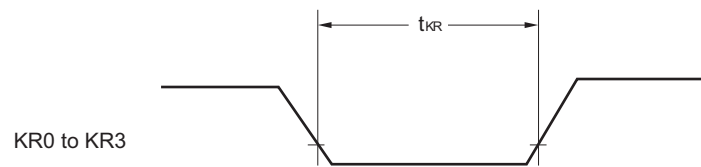
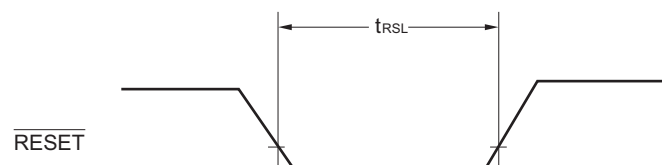


AC Timing Test Points



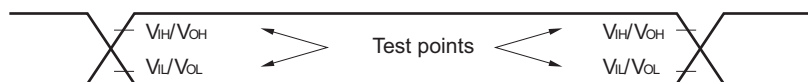
External System Clock Timing



TI/TO Timing**Interrupt Request Input Timing****Key Interrupt Input Timing****RESET Input Timing**

2.5 Peripheral Functions Characteristics

AC Timing Test Points



2.5.1 Serial array unit

(1) During communication at same potential (UART mode)

(T_A = -40 to +85°C, 1.6 V ≤ EV_{DD} = V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS} = 0 V)

Parameter	Symbol	Conditions	HS (high-speed main) Mode		LS (low-speed main) Mode		LV (low-voltage main) Mode		Unit
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Transfer rate ^{Note 1}		2.4 V ≤ EV _{DD} = V _{DD} ≤ 5.5 V		f _{MCK} /6		f _{MCK} /6		f _{MCK} /6	bps
		Theoretical value of the maximum transfer rate f _{MCK} = f _{CLK} ^{Note 2}		4.0		1.3		0.6	Mbps
		1.8 V ≤ EV _{DD} = V _{DD} ≤ 5.5 V				f _{MCK} /6		f _{MCK} /6	bps
		Theoretical value of the maximum transfer rate f _{MCK} = f _{CLK} ^{Note 2}				1.3		0.6	Mbps
		1.6 V ≤ EV _{DD} = V _{DD} ≤ 5.5 V						f _{MCK} /6	bps
		Theoretical value of the maximum transfer rate f _{MCK} = f _{CLK} ^{Note 2}						0.6	Mbps

Notes 1. Transfer rate in the SNOOZE mode is 4800 bps only.

2. The maximum operating frequencies of the CPU/peripheral hardware clock (f_{CLK}) are:

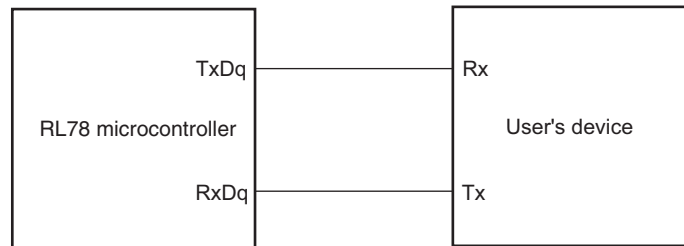
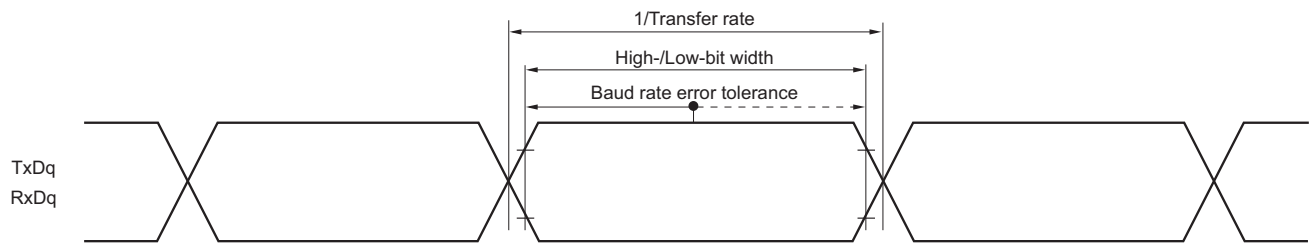
HS (high-speed main) mode: 24 MHz (2.7 V ≤ V_{DD} ≤ 5.5 V)

16 MHz (2.4 V ≤ V_{DD} ≤ 5.5 V)

LS (low-speed main) mode: 8 MHz (1.8 V ≤ V_{DD} ≤ 5.5 V)

LV (low-voltage main) mode: 4 MHz (1.6 V ≤ V_{DD} ≤ 5.5 V)

Caution Select the normal input buffer for the Rx_{DQ} pin and the normal output mode for the Tx_{DQ} pin by using port input mode register g (PIMg) and port output mode register g (POMg).

UART mode connection diagram (during communication at same potential)**UART mode bit width (during communication at same potential) (reference)**

- Remarks**
1. q: UART number (q = 0), g: PIM and POM number (g = 1)
 2. f_{MCK}: Serial array unit operation clock frequency
(Operation clock to be set by the serial clock select register m (SPSm) and the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00, 01))

(2) During communication at same potential (CSI mode) (master mode, SCKp... internal clock output)

(T_A = -40 to +85°C, 1.6 V ≤ EV_{DD} = V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS} = 0 V)

Parameter	Symbol	Conditions	HS (high-speed main) Mode		LS (low-speed main) Mode		LV (low-voltage main) Mode		Unit
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
SCKp cycle time	t _{KCY1}	2.7 V ≤ EV _{DD} ≤ 5.5 V	167 Note 1		500 Note 1		1000 Note 1		ns
		2.4 V ≤ EV _{DD} ≤ 5.5 V	250 Note 1		500 Note 1		1000 Note 1		ns
		1.8 V ≤ EV _{DD} ≤ 5.5 V			500 Note 1		1000 Note 1		ns
		1.6 V ≤ EV _{DD} ≤ 5.5 V					1000 Note 1		ns
SCKp high-/low-level width	t _{KH1} , t _{KL1}	4.0 V ≤ EV _{DD} ≤ 5.5 V	t _{KCY1} /2 - 12		t _{KCY1} /2 - 50		t _{KCY1} /2 - 50		ns
		2.7 V ≤ EV _{DD} ≤ 5.5 V	t _{KCY1} /2 - 18		t _{KCY1} /2 - 50		t _{KCY1} /2 - 50		ns
		2.4 V ≤ EV _{DD} ≤ 5.5 V	t _{KCY1} /2 - 38		t _{KCY1} /2 - 50		t _{KCY1} /2 - 50		ns
		1.8 V ≤ EV _{DD} ≤ 5.5 V			t _{KCY1} /2 - 50		t _{KCY1} /2 - 50		ns
		1.6 V ≤ EV _{DD} ≤ 5.5 V					t _{KCY1} /2 - 100		ns
Slp setup time (to SCKp↑) Note 2	t _{SIK1}	2.7 V ≤ EV _{DD} ≤ 5.5 V	44		110		110		ns
		2.4 V ≤ EV _{DD} ≤ 5.5 V	75		110		110		ns
		1.8 V ≤ EV _{DD} ≤ 5.5 V			110		110		ns
		1.6 V ≤ EV _{DD} ≤ 5.5 V					220		ns
Slp hold time (from SCKp↑) Note 3	t _{KSH1}	2.4 V ≤ EV _{DD} ≤ 5.5 V	19		19		19		ns
		1.8 V ≤ EV _{DD} ≤ 5.5 V			19		19		
		1.6 V ≤ EV _{DD} ≤ 5.5 V					19		
Delay time from SCKp↓ to SOp output Note 4	t _{KSO1}	C = 30 pF Note 5	2.4 V ≤ EV _{DD} ≤ 5.5 V	25		25		25	ns
			1.8 V ≤ EV _{DD} ≤ 5.5 V			25		25	
			1.6 V ≤ EV _{DD} ≤ 5.5 V					25	

Notes 1. For CSI00, set a cycle of 2/f_{MCK} or longer. For CSI01, set a cycle of 4/f_{MCK} or longer.2. When DAP_{mn} = 0 and CKP_{mn} = 0, or DAP_{mn} = 1 and CKP_{mn} = 1. The Slp setup time becomes “to SCKp↓” when DAP_{mn} = 0 and CKP_{mn} = 1, or DAP_{mn} = 1 and CKP_{mn} = 0.3. When DAP_{mn} = 0 and CKP_{mn} = 0, or DAP_{mn} = 1 and CKP_{mn} = 1. The Slp hold time becomes “from SCKp↓” when DAP_{mn} = 0 and CKP_{mn} = 1, or DAP_{mn} = 1 and CKP_{mn} = 0.4. When DAP_{mn} = 0 and CKP_{mn} = 0, or DAP_{mn} = 1 and CKP_{mn} = 1. The delay time to SOp output becomes “from SCKp↑” when DAP_{mn} = 0 and CKP_{mn} = 1, or DAP_{mn} = 1 and CKP_{mn} = 0.

5. C is the load capacitance of the SCKp and SOp output lines.

Caution Select the normal input buffer for the Slp pin and the normal output mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg).

(Remarks are listed on the next page.)

- Remarks 1.** p: CSI number (p = 00, 01), m: Unit number (m = 0), n: Channel number (n = 0, 1),
g: PIM and POM numbers (g = 1)
- 2.** f_{MCK}: Serial array unit operation clock frequency
(Operation clock to be set by the serial clock select register m (SPSM) and the CKSMn bit of serial mode register mn (SMRmn).
m: Unit number, n: Channel number (mn = 00, 01))

(3) During communication at same potential (CSI mode) (slave mode, SCKp... external clock input) (1/2)
(T_A = -40 to +85°C, 1.6 V ≤ EV_{DD} = V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS} = 0 V)

Parameter	Symbol	Conditions		HS (high-speed main) Mode		LS (low-speed main) Mode		LV (low-voltage main) Mode		Unit
				MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
SCKp cycle time ^{Note 5}	t _{KCY2}	4.0 V ≤ EV _{DD} ≤ 5.5 V	20 MHz < f _{MCK}	8/f _{MCK}						ns
			f _{MCK} ≤ 20 MHz	6/f _{MCK}		6/f _{MCK}		6/f _{MCK}		ns
		2.7 V ≤ EV _{DD} < 4.0 V	16 MHz < f _{MCK}	8/f _{MCK}						ns
			f _{MCK} ≤ 16 MHz	6/f _{MCK}		6/f _{MCK}		6/f _{MCK}		ns
		2.4 V ≤ EV _{DD} ≤ 5.5 V		6/f _{MCK} and 500		6/f _{MCK}		6/f _{MCK}		ns
		1.8 V ≤ EV _{DD} < 2.4 V				6/f _{MCK}		6/f _{MCK}		ns
		1.6 V ≤ EV _{DD} < 1.8 V						6/f _{MCK}		ns
SCKp high-/low-level width	t _{KH2} , t _{KL2}	4.0 V ≤ EV _{DD} ≤ 5.5 V		t _{KCY2} /2 – 7		t _{KCY2} /2 – 7		t _{KCY2} /2 – 7		ns
		2.7 V ≤ EV _{DD} < 4.0 V		t _{KCY2} /2 – 8		t _{KCY2} /2 – 8		t _{KCY2} /2 – 8		ns
		2.4 V ≤ EV _{DD} < 2.7 V		t _{KCY2} /2 – 18		t _{KCY2} /2 – 18		t _{KCY2} /2 – 18		ns
		1.8 V ≤ EV _{DD} < 2.4 V				t _{KCY2} /2 – 18		t _{KCY2} /2 – 18		ns
		1.6 V ≤ EV _{DD} < 1.8 V						t _{KCY2} /2 – 66		ns
Slp setup time (to SCKp↑) ^{Note 1}	t _{SIK2}	2.7 V ≤ EV _{DD} ≤ 5.5 V		1/f _{MCK} + 20		1/f _{MCK} + 30		1/f _{MCK} + 30		ns
		2.4 V ≤ EV _{DD} < 2.7 V		1/f _{MCK} + 30		1/f _{MCK} + 30		1/f _{MCK} + 30		
		1.8 V ≤ EV _{DD} < 2.4 V				1/f _{MCK} + 30		1/f _{MCK} + 30		ns
		1.6 V ≤ EV _{DD} < 1.8 V						1/f _{MCK} + 40		ns
Slp hold time (from SCKp↑) ^{Note 2}	t _{SIK2}	2.4 V ≤ EV _{DD} ≤ 5.5 V		1/f _{MCK} + 31		1/f _{MCK} + 31		1/f _{MCK} + 31		ns
		1.8 V ≤ EV _{DD} < 2.4 V				1/f _{MCK} + 31		1/f _{MCK} + 31		ns
		1.6 V ≤ EV _{DD} < 1.8 V						1/f _{MCK} + 250		ns

(Notes, Caution, and Remarks are listed on the next page.)

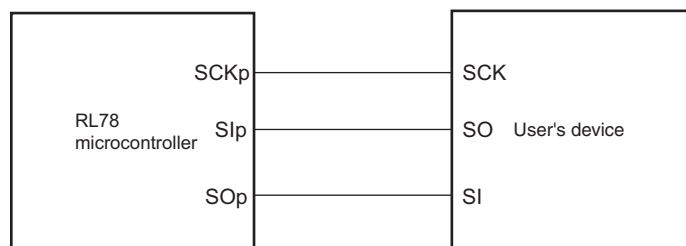
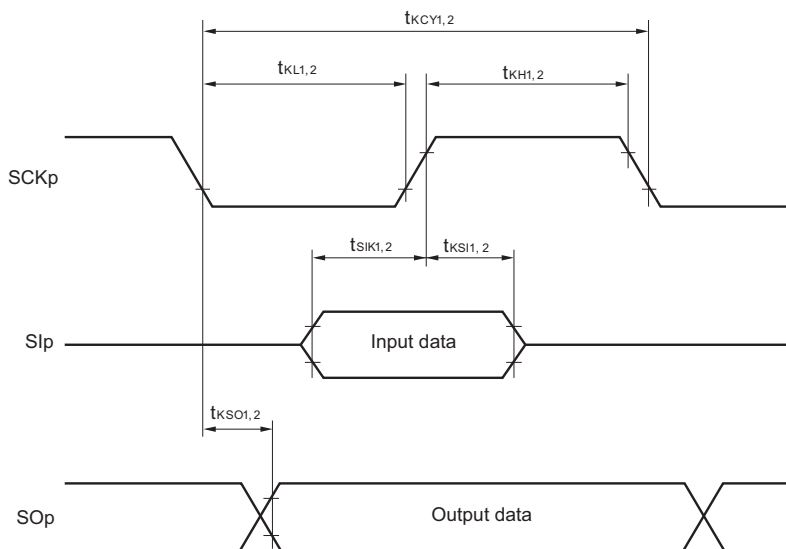
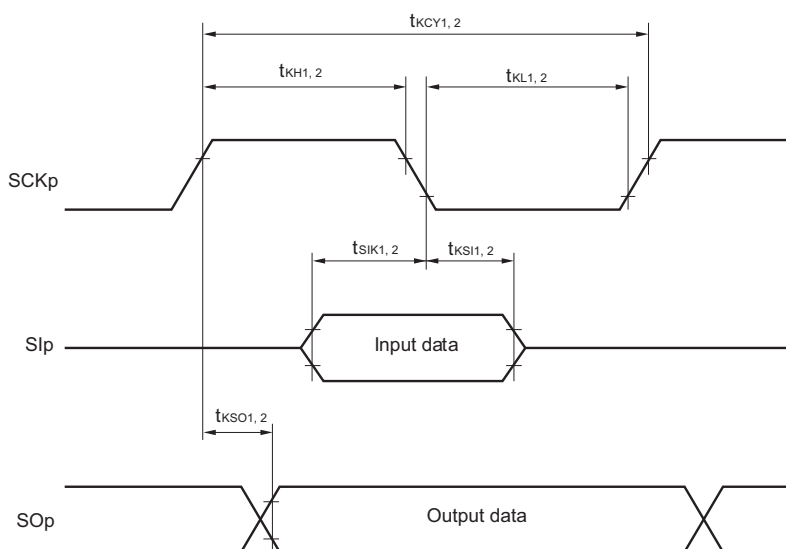
(3) During communication at same potential (CSI mode) (slave mode, SCKp... external clock input) (2/2)
 (T_A = -40 to +85°C, 1.6 V ≤ EV_{DD} = V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS} = 0 V)

Parameter	Symbol	Conditions	HS (high-speed main) Mode	LS (low- speed main) Mode	LV (low- voltage main) Mode	Unit	Para meter	Symbol	Conditions
Delay time from SCKp↓ to SOp output ^{Note 3}	t _{KSO2}	C = 30 pF ^{Note 4}	4.0 V ≤ EV _{DD} ≤ 5.5 V			2/f _{MCK} + 44		2/f _{MCK} + 110	ns
			2.7 V ≤ EV _{DD} < 4.0 V			2/f _{MCK} + 44		2/f _{MCK} + 110	ns
			2.4 V ≤ EV _{DD} < 2.7 V			2/f _{MCK} + 75		2/f _{MCK} + 110	ns
			1.8 V ≤ EV _{DD} < 2.4 V			2/f _{MCK} + 110		2/f _{MCK} + 110	ns
			1.6 V ≤ EV _{DD} < 1.8 V					2/f _{MCK} + 220	ns

- Notes**
1. When DAP_{mn} = 0 and CKP_{mn} = 0, or DAP_{mn} = 1 and CKP_{mn} = 1. The SIp setup time becomes “to SCKp↓” when DAP_{mn} = 0 and CKP_{mn} = 1, or DAP_{mn} = 1 and CKP_{mn} = 0.
 2. When DAP_{mn} = 0 and CKP_{mn} = 0, or DAP_{mn} = 1 and CKP_{mn} = 1. The SIp hold time becomes “from SCKp↓” when DAP_{mn} = 0 and CKP_{mn} = 1, or DAP_{mn} = 1 and CKP_{mn} = 0.
 3. When DAP_{mn} = 0 and CKP_{mn} = 0, or DAP_{mn} = 1 and CKP_{mn} = 1. The delay time to SOp output becomes “from SCKp↑” when DAP_{mn} = 0 and CKP_{mn} = 1, or DAP_{mn} = 1 and CKP_{mn} = 0.
 4. C is the load capacitance of the SCKp and SOp output lines.
 5. Transfer rate in the SNOOZE mode: MAX. 1 Mbps

Caution Select the normal input buffer for the SIp pin and SCKp pin and the normal output mode for the SOp pin by using port input mode register g (PIMg) and port output mode register g (POMg).

- Remarks**
1. p: CSI number (p = 00, 01), m: Unit number (m = 0),
n: Channel number (n = 0, 1), g: PIM number (g = 1)
 2. f_{MCK}: Serial array unit operation clock frequency
(Operation clock to be set by the serial clock select register m (SPSm) and the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00, 01))

CSI mode connection diagram (during communication at same potential)
CSI mode serial transfer timing (during communication at same potential)
 (When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.)

CSI mode serial transfer timing (during communication at same potential)
 (When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.)


- Remarks**
1. p: CSI number (p = 00, 01)
 2. m: Unit number, n: Channel number (mn = 00, 01)

(4) Communication at different potential (1.8 V, 2.5 V, 3 V) (UART mode)

(1/2)

(T_A = -40 to +85°C, 1.8 V ≤ EV_{DD} = V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS} = 0 V)

Parameter	Symbol	Conditions	HS (high-speed main) Mode		LS (low-speed main) Mode		LV (low-voltage main) Mode		Unit
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Transfer rate		Reception	4.0 V ≤ EV _{DD} ≤ 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V	f _{MCK} /6 Note 1		f _{MCK} /6 Note 1		f _{MCK} /6 Note 1	bps
				4.0		1.3		0.6	Mbps
			Theoretical value of the maximum transfer rate f _{MCK} = f _{CLK} Note 3						
			2.7 V ≤ EV _{DD} < 4.0 V, 2.3 V ≤ V _b ≤ 2.7 V	f _{MCK} /6 Note 1		f _{MCK} /6 Note 1		f _{MCK} /6 Note 1	bps
				4.0		1.3		0.6	Mbps
			Theoretical value of the maximum transfer rate f _{MCK} = f _{CLK} Note 3						
			2.4 V ≤ EV _{DD} < 3.3 V, 1.6 V ≤ V _b ≤ 2.0 V	f _{MCK} /6 Note 1		f _{MCK} /6 Note 1		f _{MCK} /6 Note 1	bps
				4.0		1.3		0.6	Mbps
			Theoretical value of the maximum transfer rate f _{MCK} = f _{CLK} Note 3						
			1.8 V ≤ EV _{DD} < 3.3 V, 1.6 V ≤ V _b ≤ 2.0 V			f _{MCK} /6 Notes 1, 2		f _{MCK} /6 Notes 1, 2	bps
						1.3		0.6	Mbps
			Theoretical value of the maximum transfer rate f _{MCK} = f _{CLK} Note 3						

Notes 1. Transfer rate in the SNOOZE mode is 4800 bps only.**2.** Use it with EV_{DD} ≥ V_b.**3.** The maximum operating frequencies of the CPU/peripheral hardware clock (f_{CLK}) are:HS (high-speed main) mode: 24 MHz (2.7 V ≤ V_{DD} ≤ 5.5 V)16 MHz (2.4 V ≤ V_{DD} ≤ 5.5 V)LS (low-speed main) mode: 8 MHz (1.8 V ≤ V_{DD} ≤ 5.5 V)LV (low-voltage main) mode: 4 MHz (1.6 V ≤ V_{DD} ≤ 5.5 V)

Caution Select the TTL input buffer for the Rx_{Dq} pin and the N-ch open drain output (V_{DD} tolerance (32-pin to 52-pin products)/EV_{DD} tolerance (64-pin products)) mode for the Tx_{Dq} pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V_{IH} and V_{IL}, see the DC characteristics with TTL input buffer selected.

Remarks 1. V_b[V]: Communication line voltage**2.** q: UART number (q = 0), g: PIM and POM number (g = 1)**3.** f_{MCK}: Serial array unit operation clock frequency(Operation clock to be set by the serial clock select register m (SPS_m) and the CKS_{mn} bit of serial mode register mn (SMR_{mn}). m: Unit number, n: Channel number (mn = 00, 01))

(4) Communication at different potential (1.8 V, 2.5 V, 3 V) (UART mode)

(2/2)

(T_A = -40 to +85°C, 1.8 V ≤ EV_{DD} = V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS} = 0 V)

Parameter	Symbol	Conditions	HS (high-speed main) Mode		LS (low-speed main) Mode		LV (low-voltage main) Mode		Unit
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Transfer rate		Transmission	4.0 V ≤ EV _{DD} ≤ 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V			Note 1		Note 1	bps
			Theoretical value of the maximum transfer rate C _b = 50 pF, R _b = 1.4 kΩ, V _b = 2.7 V			2.8 ^{Note 2}		2.8 ^{Note 2}	Mbps
			2.7 V ≤ EV _{DD} < 4.0 V, 2.3 V ≤ V _b ≤ 2.7 V			Note 3		Note 3	bps
			Theoretical value of the maximum transfer rate C _b = 50 pF, R _b = 2.7 kΩ, V _b = 2.3 V			1.2 ^{Note 4}		1.2 ^{Note 4}	Mbps
			2.4 V ≤ EV _{DD} < 3.3 V, 1.6 V ≤ V _b ≤ 2.0 V			Note 6		Note 6	bps
			Theoretical value of the maximum transfer rate C _b = 50 pF, R _b = 5.5 kΩ, V _b = 1.6 V			0.43 ^{Note 7}		0.43 ^{Note 7}	Mbps
			1.8 V ≤ EV _{DD} < 3.3 V, 1.6 V ≤ V _b ≤ 2.0 V				Notes 5, 6	Notes 5, 6	bps
			Theoretical value of the maximum transfer rate C _b = 50 pF, R _b = 5.5 kΩ, V _b = 1.6 V				0.43 ^{Note 7}	0.43 ^{Note 7}	Mbps

Notes 1. The smaller maximum transfer rate derived by using f_{MCK}/6 or the following expression is the valid maximum transfer rate.

Expression for calculating the transfer rate when 4.0 V ≤ EV_{DD} ≤ 5.5 V and 2.7 V ≤ V_b ≤ 4.0 V

$$\text{Maximum transfer rate} = \frac{1}{\{-C_b \times R_b \times \ln(1 - \frac{2.2}{V_b})\} \times 3} \text{ [bps]}$$

$$\text{Baud rate error (theoretical value)} = \frac{\frac{1}{\text{Transfer rate} \times 2} - \{-C_b \times R_b \times \ln(1 - \frac{2.2}{V_b})\}}{(\frac{1}{\text{Transfer rate}}) \times \text{Number of transferred bits}} \times 100 \text{ [%]}$$

* This value is the theoretical value of the relative difference between the transmission and reception sides.

- 2.** This value as an example is calculated when the conditions described in the “Conditions” column are met. Refer to Note 1 above to calculate the maximum transfer rate under conditions of the customer.

3. The smaller maximum transfer rate derived by using $f_{MCK}/6$ or the following expression is the valid maximum transfer rate.

Expression for calculating the transfer rate when $2.7\text{ V} \leq E_{VDD} < 4.0\text{ V}$ and $2.3\text{ V} \leq V_b \leq 2.7\text{ V}$

$$\text{Maximum transfer rate} = \frac{1}{\{-C_b \times R_b \times \ln(1 - \frac{2.0}{V_b})\} \times 3} \text{ [bps]}$$

$$\text{Baud rate error (theoretical value)} = \frac{\frac{1}{\text{Transfer rate} \times 2} - \{-C_b \times R_b \times \ln(1 - \frac{2.0}{V_b})\}}{(\frac{1}{\text{Transfer rate}}) \times \text{Number of transferred bits}} \times 100 \text{ [%]}$$

* This value is the theoretical value of the relative difference between the transmission and reception sides.

4. This value as an example is calculated when the conditions described in the “Conditions” column are met. Refer to Note 3 above to calculate the maximum transfer rate under conditions of the customer.
5. Use it with $E_{VDD} \geq V_b$.

6. The smaller maximum transfer rate derived by using $f_{MCK}/6$ or the following expression is the valid maximum transfer rate.

Expression for calculating the transfer rate when $1.8\text{ V} \leq E_{VDD} < 3.3\text{ V}$ and $1.6\text{ V} \leq V_b \leq 2.0\text{ V}$

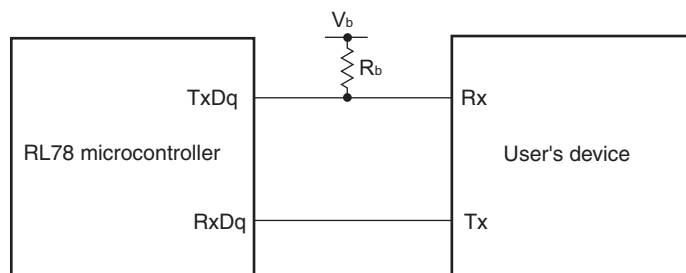
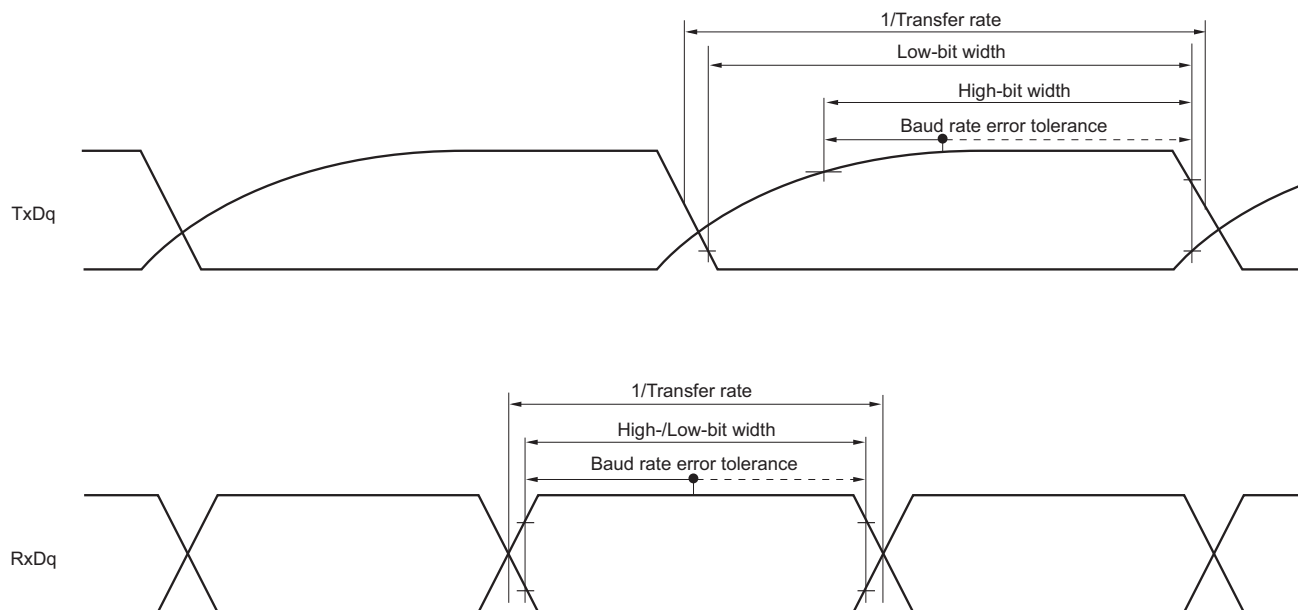
$$\text{Maximum transfer rate} = \frac{1}{\{-C_b \times R_b \times \ln(1 - \frac{1.5}{V_b})\} \times 3} \text{ [bps]}$$

$$\text{Baud rate error (theoretical value)} = \frac{\frac{1}{\text{Transfer rate} \times 2} - \{-C_b \times R_b \times \ln(1 - \frac{1.5}{V_b})\}}{(\frac{1}{\text{Transfer rate}}) \times \text{Number of transferred bits}} \times 100 \text{ [%]}$$

* This value is the theoretical value of the relative difference between the transmission and reception sides.

7. This value as an example is calculated when the conditions described in the “Conditions” column are met. Refer to Note 6 above to calculate the maximum transfer rate under conditions of the customer.

Caution Select the TTL input buffer for the RxDq pin and the N-ch open drain output (V_{DD} tolerance (32-pin to 52-pin products)/ E_{VDD} tolerance (64-pin products)) mode for the TxDq pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V_{IH} and V_{IL} , see the DC characteristics with TTL input buffer selected.

UART mode connection diagram (during communication at different potential)**UART mode bit width (during communication at different potential) (reference)**

- Remarks**
1. $R_b[\Omega]$: Communication line (TxDq) pull-up resistance,
 $C_b[\text{F}]$: Communication line (TxDq) load capacitance, $V_b[\text{V}]$: Communication line voltage
 2. q: UART number (q = 0, 1), g: PIM and POM number (g = 1)
 3. f_{MCK} : Serial array unit operation clock frequency
 (Operation clock to be set by the serial clock select register m (SPS_m) and the CKS_{mn} bit of serial mode register mn (SMR_{mn}). m: Unit number, n: Channel number (mn = 00, 01))

(5) Communication at different potential (2.5 V, 3 V) (CSI mode) (master mode, SCKp... internal clock output, corresponding CSI00 only)**(T_A = -40 to +85°C, 2.7 V ≤ EV_{DD} = V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS} = 0 V)**

Parameter	Symbol	Conditions		HS (high-speed main) Mode		LS (low-speed main) Mode		LV (low-voltage main) Mode		Unit
				MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
SCKp cycle time	t _{KCY1}	t _{KCY1} ≥ 2/f _{CLK} 4.0 V ≤ EV _{DD} ≤ 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V, C _b = 20 pF, R _b = 1.4 kΩ		200 Note 1		1150 Note 1		1150 Note 1		ns
				300 Note 1		1150 Note 1		1150 Note 1		ns
SCKp high-level width	t _{KH1}	4.0 V ≤ EV _{DD} ≤ 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V, C _b = 20 pF, R _b = 1.4 kΩ		t _{KCY1} /2 – 50		t _{KCY1} /2 – 50		t _{KCY1} /2 – 50		ns
		2.7 V ≤ EV _{DD} < 4.0 V, 2.3 V ≤ V _b ≤ 2.7 V, C _b = 20 pF, R _b = 2.7 kΩ		t _{KCY1} /2 – 120		t _{KCY1} /2 – 120		t _{KCY1} /2 – 120		ns
SCKp low-level width	t _{KL1}	4.0 V ≤ EV _{DD} ≤ 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V, C _b = 20 pF, R _b = 1.4 kΩ		t _{KCY1} /2 – 7		t _{KCY1} /2 – 50		t _{KCY1} /2 – 50		ns
		2.7 V ≤ EV _{DD} < 4.0 V, 2.3 V ≤ V _b ≤ 2.7 V, C _b = 20 pF, R _b = 2.7 kΩ		t _{KCY1} /2 – 10		t _{KCY1} /2 – 50		t _{KCY1} /2 – 50		ns
Slp setup time (to SCKp↑) ^{Note 2}	t _{SIK1}	4.0 V ≤ EV _{DD} ≤ 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V, C _b = 20 pF, R _b = 1.4 kΩ		58		479		479		ns
		2.7 V ≤ EV _{DD} < 4.0 V, 2.3 V ≤ V _b ≤ 2.7 V, C _b = 20 pF, R _b = 2.7 kΩ		121		479		479		ns
Slp hold time (from SCKp↑) ^{Note 2}	t _{KSI1}	4.0 V ≤ EV _{DD} ≤ 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V, C _b = 20 pF, R _b = 1.4 kΩ		10		10		10		ns
		2.7 V ≤ EV _{DD} < 4.0 V, 2.3 V ≤ V _b ≤ 2.7 V, C _b = 20 pF, R _b = 2.7 kΩ		10		10		10		ns
Delay time from SCKp↓ to SOp output ^{Note 2}	t _{KSO1}	4.0 V ≤ EV _{DD} ≤ 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V, C _b = 20 pF, R _b = 1.4 kΩ			60		60		60	ns
		2.7 V ≤ EV _{DD} < 4.0 V, 2.3 V ≤ V _b ≤ 2.7 V, C _b = 20 pF, R _b = 2.7 kΩ			130		130		130	ns
Slp setup time (to SCKp↓) ^{Note 3}	t _{SIK1}	4.0 V ≤ EV _{DD} ≤ 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V, C _b = 20 pF, R _b = 1.4 kΩ		23		110		110		ns
		2.7 V ≤ EV _{DD} < 4.0 V, 2.3 V ≤ V _b ≤ 2.7 V, C _b = 20 pF, R _b = 2.7 kΩ		33		110		110		ns
Slp hold time (from SCKp↓) ^{Note 3}	t _{KSI1}	4.0 V ≤ EV _{DD} ≤ 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V, C _b = 20 pF, R _b = 1.4 kΩ		10		10		10		ns
		2.7 V ≤ EV _{DD} < 4.0 V, 2.3 V ≤ V _b ≤ 2.7 V, C _b = 20 pF, R _b = 2.7 kΩ		10		10		10		ns
Delay time from SCKp↑ to SOp output ^{Note 3}	t _{KSO1}	4.0 V ≤ EV _{DD} ≤ 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V, C _b = 20 pF, R _b = 1.4 kΩ			10		10		10	ns
		2.7 V ≤ EV _{DD} < 4.0 V, 2.3 V ≤ V _b ≤ 2.7 V, C _b = 20 pF, R _b = 2.7 kΩ			10		10		10	ns

(Notes, Caution and Remarks are listed on the next page.)

- Notes**
1. For CSI00, set a cycle of $2/f_{MCK}$ or longer. For CSI01, set a cycle of $4/f_{MCK}$ or longer.
 2. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.
 3. When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

Caution Select the TTL input buffer for the SIp pin and the N-ch open drain output (V_{DD} tolerance (32-pin to 52-pin products)/EV_{DD} tolerance (64-pin products)) mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V_{IH} and V_{IL}, see the DC characteristics with TTL input buffer selected.

- Remarks**
1. R_b[Ω]: Communication line (SCKp, SOp) pull-up resistance, C_b[F]: Communication line (SCKp, SOp) load capacitance, V_b[V]: Communication line voltage
 2. p: CSI number (p = 00, 01), m: Unit number (m = 0), n: Channel number (n = 0, 1),
g: PIM and POM number (g = 1)
 3. f_{MCK}: Serial array unit operation clock frequency
(Operation clock to be set by the serial clock select register m (SPSm) and the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00, 01))

(6) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (master mode, SCKp... internal clock output) (1/3)
(T_A = -40 to +85°C, 1.8 V ≤ EV_{DD} = V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS} = 0 V)

Parameter	Symbol	Conditions		HS (high-speed main) Mode		LS (low-speed main) Mode		LV (low-voltage main) Mode		Unit
				MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
SCKp cycle time	t _{KCY1}	t _{KCY1} ≥ 4/f _{CLK} 4.0 V ≤ EV _{DD} ≤ 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V, C _b = 30 pF, R _b = 1.4 kΩ		300		1150		1150		ns
SCKp high-level width	t _{KH1}	4.0 V ≤ EV _{DD} ≤ 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V, C _b = 30 pF, R _b = 1.4 kΩ		t _{KCY1} /2 – 75		t _{KCY1} /2 – 75		t _{KCY1} /2 – 75		ns
		2.7 V ≤ EV _{DD} < 4.0 V, 2.3 V ≤ V _b ≤ 2.7 V, C _b = 30 pF, R _b = 2.7 kΩ		t _{KCY1} /2 – 170		t _{KCY1} /2 – 170		t _{KCY1} /2 – 170		ns
		2.4 V ≤ EV _{DD} < 3.3 V, 1.6 V ≤ V _b ≤ 2.0 V, C _b = 30 pF, R _b = 5.5 kΩ		t _{KCY1} /2 – 458		t _{KCY1} /2 – 458		t _{KCY1} /2 – 458		ns
		1.8 V ≤ EV _{DD} < 3.3 V, 1.6 V ≤ V _b ≤ 2.0 V ^{Note} , C _b = 30 pF, R _b = 5.5 kΩ				t _{KCY1} /2 – 458		t _{KCY1} /2 – 458		ns
SCKp low-level width	t _{KL1}	4.0 V ≤ EV _{DD} ≤ 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V, C _b = 30 pF, R _b = 1.4 kΩ		t _{KCY1} /2 – 12		t _{KCY1} /2 – 50		t _{KCY1} /2 – 50		ns
		2.7 V ≤ EV _{DD} < 4.0 V, 2.3 V ≤ V _b ≤ 2.7 V, C _b = 30 pF, R _b = 2.7 kΩ		t _{KCY1} /2 – 18		t _{KCY1} /2 – 50		t _{KCY1} /2 – 50		ns
		2.4 V ≤ EV _{DD} < 3.3 V, 1.6 V ≤ V _b ≤ 2.0 V, C _b = 30 pF, R _b = 5.5 kΩ		t _{KCY1} /2 – 50		t _{KCY1} /2 – 50		t _{KCY1} /2 – 50		ns
		1.8 V ≤ EV _{DD} < 3.3 V, 1.6 V ≤ V _b ≤ 2.0 V ^{Note} , C _b = 30 pF, R _b = 5.5 kΩ				t _{KCY1} /2 – 50		t _{KCY1} /2 – 50		ns

Note Use it with EV_{DD} ≥ V_b.

Caution Select the TTL input buffer for the SIp pin and the N-ch open drain output (V_{DD} tolerance (32-pin to 52-pin products)/EV_{DD} tolerance (64-pin products)) mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V_{IH} and V_{IL}, see the DC characteristics with TTL input buffer selected.

(6) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (master mode, SCKp... internal clock output) (2/3)
(T_A = -40 to +85°C, 1.8 V ≤ EV_{DD} = V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS} = 0 V)

Parameter	Symbol	Conditions	HS (high-speed main) Mode		LS (low-speed main) Mode		LV (low-voltage main) Mode		Unit
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Slp setup time (to SCKp↑) ^{Note 1}	t _{SIK1}	4.0 V ≤ EV _{DD} ≤ 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V, C _b = 30 pF, R _b = 1.4 kΩ	81		479		479		ns
		2.7 V ≤ EV _{DD} < 4.0 V, 2.3 V ≤ V _b ≤ 2.7 V, C _b = 30 pF, R _b = 2.7 kΩ	177		479		479		ns
		2.4 V ≤ EV _{DD} < 3.3 V, 1.6 V ≤ V _b ≤ 2.0 V, C _b = 30 pF, R _b = 5.5 kΩ	479		479		479		ns
		1.8 V ≤ EV _{DD} < 3.3 V, 1.6 V ≤ V _b ≤ 2.0 V ^{Note 3} , C _b = 30 pF, R _b = 5.5 kΩ			479		479		ns
Slp hold time (from SCKp↑) ^{Note 1}	t _{KSI1}	4.0 V ≤ EV _{DD} ≤ 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V, C _b = 30 pF, R _b = 1.4 kΩ	19		19		19		ns
		2.7 V ≤ EV _{DD} < 4.0 V, 2.3 V ≤ V _b ≤ 2.7 V, C _b = 30 pF, R _b = 2.7 kΩ	19		19		19		ns
		2.4 V ≤ EV _{DD} < 3.3 V, 1.6 V ≤ V _b ≤ 2.0 V, C _b = 30 pF, R _b = 5.5 kΩ	19		19		19		ns
		1.8 V ≤ EV _{DD} < 3.3 V, 1.6 V ≤ V _b ≤ 2.0 V ^{Note 3} , C _b = 30 pF, R _b = 5.5 kΩ			19		19		ns
Delay time from SCKp↓ to SOp output ^{Note 1}	t _{KSO1}	4.0 V ≤ EV _{DD} ≤ 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V, C _b = 30 pF, R _b = 1.4 kΩ		100		100		100	ns
		2.7 V ≤ EV _{DD} < 4.0 V, 2.3 V ≤ V _b ≤ 2.7 V, C _b = 30 pF, R _b = 2.7 kΩ		195		195		195	ns
		2.4 V ≤ EV _{DD} < 4.0 V, 2.3 V ≤ V _b ≤ 2.7 V, C _b = 30 pF, R _b = 2.7 kΩ		483		483		483	ns
		1.8 V ≤ EV _{DD} < 3.3 V, 1.6 V ≤ V _b ≤ 2.0 V ^{Note 3} , C _b = 30 pF, R _b = 5.5 kΩ				483		483	ns
Slp setup time (to SCKp↓) ^{Note 2}	t _{SIK1}	4.0 V ≤ EV _{DD} ≤ 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V, C _b = 30 pF, R _b = 1.4 kΩ	44		110		110		ns
		2.7 V ≤ EV _{DD} < 4.0 V, 2.3 V ≤ V _b ≤ 2.7 V, C _b = 30 pF, R _b = 2.7 kΩ	44		110		110		ns
		2.4 V ≤ EV _{DD} < 4.0 V, 2.3 V ≤ V _b ≤ 2.7 V, C _b = 30 pF, R _b = 2.7 kΩ	110		110		110		ns
		1.8 V ≤ EV _{DD} < 3.3 V, 1.6 V ≤ V _b ≤ 2.0 V ^{Note 3} , C _b = 30 pF, R _b = 5.5 kΩ			110		110		ns

- Notes**
1. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.
 2. When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.
 3. Use it with EV_{DD} ≥ V_b.

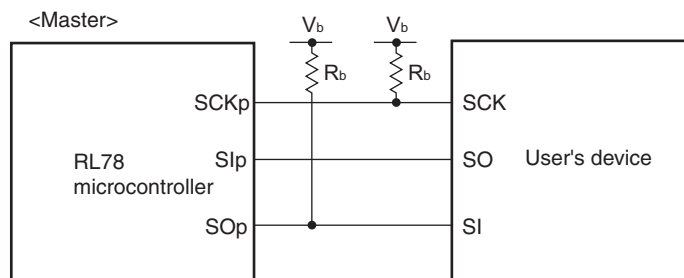
Caution Select the TTL input buffer for the Slp pin and the N-ch open drain output (V_{DD} tolerance (32-pin to 52-pin products)/EV_{DD} tolerance (64-pin products)) mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V_{IH} and V_{IL}, see the DC characteristics with TTL input buffer selected.

(6) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (master mode, SCKp... internal clock output) (3/3)
(T_A = -40 to +85°C, 1.8 V ≤ EV_{DD} = V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS} = 0 V)

Parameter	Symbol	Conditions	HS (high-speed main) Mode		LS (low-speed main) Mode		LV (low-voltage main) Mode		Unit
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Slp hold time (from SCKp↓) ^{Note 2}	t _{KSI1}	4.0 V ≤ EV _{DD} ≤ 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V, C _b = 30 pF, R _b = 1.4 kΩ	19		19		19		ns
		2.7 V ≤ EV _{DD} < 4.0 V, 2.3 V ≤ V _b ≤ 2.7 V, C _b = 30 pF, R _b = 2.7 kΩ	19		19		19		ns
		2.4 V ≤ EV _{DD} < 3.3 V, 1.6 V ≤ V _b ≤ 2.0 V, C _b = 30 pF, R _b = 5.5 kΩ	19		19		19		ns
		1.8 V ≤ EV _{DD} < 3.3 V, 1.6 V ≤ V _b ≤ 2.0 V ^{Note 3} , C _b = 30 pF, R _b = 5.5 kΩ			19		19		ns
Delay time from SCKp↑ to SOp output ^{Note 2}	t _{KSO1}	4.0 V ≤ EV _{DD} ≤ 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V, C _b = 30 pF, R _b = 1.4 kΩ		25		25		25	ns
		2.7 V ≤ EV _{DD} < 4.0 V, 2.3 V ≤ V _b ≤ 2.7 V, C _b = 30 pF, R _b = 2.7 kΩ		25		25		25	ns
		2.4 V ≤ EV _{DD} < 3.3 V, 1.6 V ≤ V _b ≤ 2.0 V, C _b = 30 pF, R _b = 5.5 kΩ		25		25		25	ns
		1.8 V ≤ EV _{DD} < 3.3 V, 1.6 V ≤ V _b ≤ 2.0 V ^{Note 3} , C _b = 30 pF, R _b = 5.5 kΩ				25		25	ns

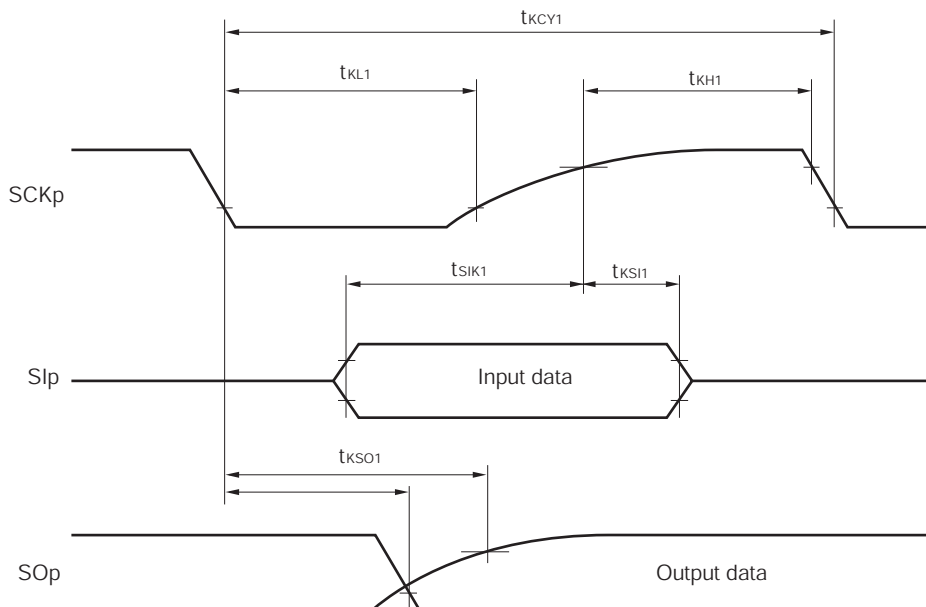
- Notes**
1. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.
 2. When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.
 3. Use it with EV_{DD} ≥ V_b.

Caution Select the TTL input buffer for the Slp pin and the N-ch open drain output (V_{DD} tolerance (32-pin to 52-pin products)/EV_{DD} tolerance (64-pin products)) mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V_{IH} and V_{IL}, see the DC characteristics with TTL input buffer selected.

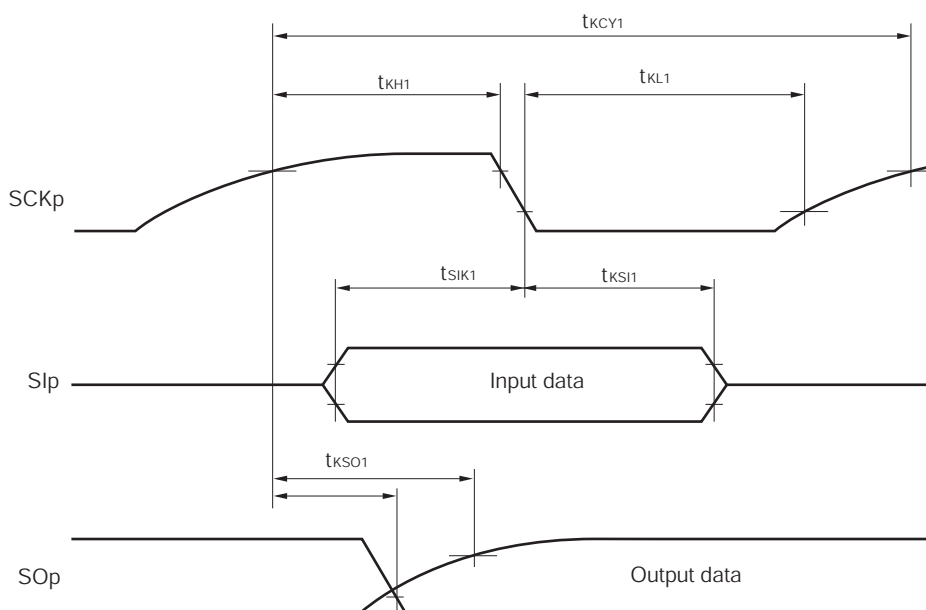
CSI mode connection diagram (during communication at different potential)

- Remarks**
1. $R_b[\Omega]$: Communication line (SCKp, SOp) pull-up resistance, $C_b[\text{F}]$: Communication line (SCKp, SOp) load capacitance, $V_b[\text{V}]$: Communication line voltage
 2. p: CSI number ($p = 00, 01$), m: Unit number ($m = 0$), n: Channel number ($n = 0, 1$), g: PIM and POM number ($g = 1$)
 3. f_{MCK} : Serial array unit operation clock frequency
(Operation clock to be set by the serial clock select register m (SPSm) and the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number ($mn = 00, 01$))

CSI mode serial transfer timing (master mode) (during communication at different potential)
(When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.)



CSI mode serial transfer timing (master mode) (during communication at different potential)
(When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.)



Remark p: CSI number (p = 00, 01), m: Unit number (m = 0), n: Channel number (n = 0, 1),
g: PIM and POM number (g = 1)

(7) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (slave mode, SCKp... external clock input)
(T_A = -40 to +85°C, 1.8 V ≤ EV_{DD} = V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS} = 0 V) (1/2)

Parameter	Symbol	Conditions		HS (high-speed main) mode		LS (low-speed main) mode		LV (low-voltage main) mode		Unit
				MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
SCKp cycle time ^{Note 1}	t _{KCY2}	4.0 V ≤ EV _{DD} ≤ 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V	20 MHz < f _{MCK} ≤ 24 MHz	12/f _{MCK}						ns
			8 MHz < f _{MCK} ≤ 20 MHz	10/f _{MCK}						ns
			4 MHz < f _{MCK} ≤ 8 MHz	8/f _{MCK}		16/f _{MCK}				ns
			f _{MCK} ≤ 4 MHz	6/f _{MCK}		10/f _{MCK}		10/f _{MCK}		ns
		2.7 V ≤ EV _{DD} < 4.0 V, 2.3 V ≤ V _b ≤ 2.7 V	20 MHz < f _{MCK} ≤ 24 MHz	16/f _{MCK}						ns
			16 MHz < f _{MCK} ≤ 20 MHz	14/f _{MCK}						ns
			8 MHz < f _{MCK} ≤ 16 MHz	12/f _{MCK}						ns
			4 MHz < f _{MCK} ≤ 8 MHz	8/f _{MCK}		16/f _{MCK}				ns
			f _{MCK} ≤ 4 MHz	6/f _{MCK}		10/f _{MCK}		10/f _{MCK}		ns
		2.4 V ≤ EV _{DD} < 3.3 V, 1.6 V ≤ V _b ≤ 2.0 V	20 MHz < f _{MCK} ≤ 24 MHz	36/f _{MCK}						ns
			16 MHz < f _{MCK} ≤ 20 MHz	32/f _{MCK}						ns
			8 MHz < f _{MCK} ≤ 16 MHz	26/f _{MCK}						ns
			4 MHz < f _{MCK} ≤ 8 MHz	16/f _{MCK}		16/f _{MCK}				ns
SCKp high-/low-level width	t _{KH2} , t _{KL2}	4.0 V ≤ EV _{DD} ≤ 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V	4 MHz < f _{MCK} ≤ 8 MHz			16/f _{MCK}				ns
			f _{MCK} ≤ 4 MHz			10/f _{MCK}		10/f _{MCK}		ns
		2.7 V ≤ EV _{DD} < 4.0 V, 2.3 V ≤ V _b ≤ 2.7 V	4 MHz < f _{MCK} ≤ 8 MHz			16/f _{MCK}				ns
			f _{MCK} ≤ 4 MHz			10/f _{MCK}		10/f _{MCK}		ns
Slp setup time (to SCKp↑) ^{Note 3}	t _{SIK2}	4.0 V ≤ EV _{DD} < 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V	4 MHz < f _{MCK} ≤ 8 MHz			16/f _{MCK}				ns
			f _{MCK} ≤ 4 MHz			10/f _{MCK}		10/f _{MCK}		ns
		2.7 V ≤ EV _{DD} < 4.0 V, 2.3 V ≤ V _b ≤ 2.7 V	4 MHz < f _{MCK} ≤ 8 MHz			16/f _{MCK}				ns
			f _{MCK} ≤ 4 MHz			10/f _{MCK}		10/f _{MCK}		ns
Slp hold time (from SCKp↑) ^{Note 4}	t _{SIK2}	4.0 V ≤ EV _{DD} < 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V	4 MHz < f _{MCK} ≤ 8 MHz			16/f _{MCK}				ns
			f _{MCK} ≤ 4 MHz			10/f _{MCK}		10/f _{MCK}		ns
		2.7 V ≤ EV _{DD} < 4.0 V, 2.3 V ≤ V _b ≤ 2.7 V	4 MHz < f _{MCK} ≤ 8 MHz			16/f _{MCK}				ns
			f _{MCK} ≤ 4 MHz			10/f _{MCK}		10/f _{MCK}		ns

(Notes, Caution and Remarks are listed on the next page.)

(7) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (slave mode, SCKp... external clock input)
(T_A = -40 to +85°C, 1.8 V ≤ EV_{DD} = V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS} = 0 V) **(2/2)**

Parameter	Symbol	Conditions	HS (high-speed main) mode		LS (low-speed main) mode		LV (low-voltage main) mode		Unit
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Delay time from SCKp↓ to SOp output ^{Note 5}	t _{KS02}	4.0 V ≤ EV _{DD} ≤ 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V, C _b = 30 pF, R _b = 1.4 kΩ		2/f _{MCK} + 120		2/f _{MCK} + 573		2/f _{MCK} + 573	ns
		2.7 V ≤ EV _{DD} < 4.0 V, 2.3 V ≤ V _b ≤ 2.7 V, C _b = 30 pF, R _b = 2.7 kΩ		2/f _{MCK} + 214		2/f _{MCK} + 573		2/f _{MCK} + 573	ns
		2.4 V ≤ EV _{DD} < 3.3 V, 1.6 V ≤ V _b ≤ 2.0 V, C _b = 30 pF, R _b = 5.5 kΩ		2/f _{MCK} + 573		2/f _{MCK} + 573		2/f _{MCK} + 573	ns
		1.8 V ≤ EV _{DD} < 3.3 V, 1.6 V ≤ V _b ≤ 2.0 V ^{Note 2} , C _b = 30 pF, R _b = 5.5 kΩ				2/f _{MCK} + 573		2/f _{MCK} + 573	ns

Notes 1. Transfer rate in the SNOOZE mode : MAX. 1 Mbps

2. Use it with EV_{DD} ≥ V_b.

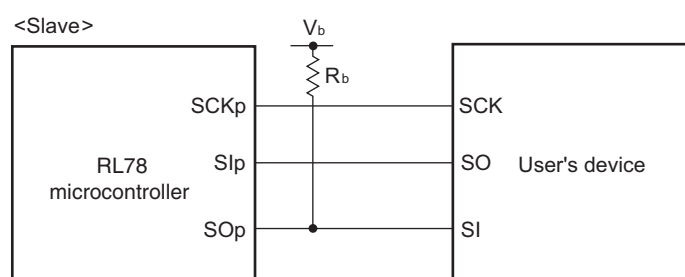
3. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp setup time becomes “to SCKp↓” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

4. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp hold time becomes “from SCKp↓” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

5. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The delay time to SOp output becomes “from SCKp↑” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

Caution Select the TTL input buffer for the SIp pin and SCKp pin and the N-ch open drain output (V_{DD} tolerance (32-pin to 52-pin products)/EV_{DD} tolerance (64-pin products)) mode for the SOp pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V_{IH} and V_{IL}, see the DC characteristics with TTL input buffer selected.

CSI mode connection diagram (during communication at different potential)

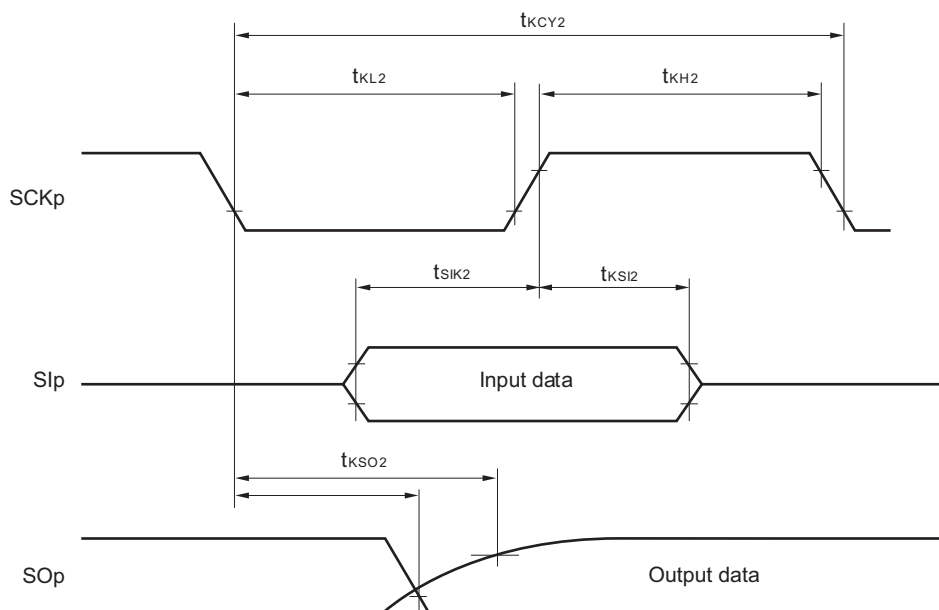


Remarks 1. R_b[Ω]: Communication line (SO_p) pull-up resistance, C_b[F]: Communication line (SO_p) load capacitance, V_b[V]: Communication line voltage

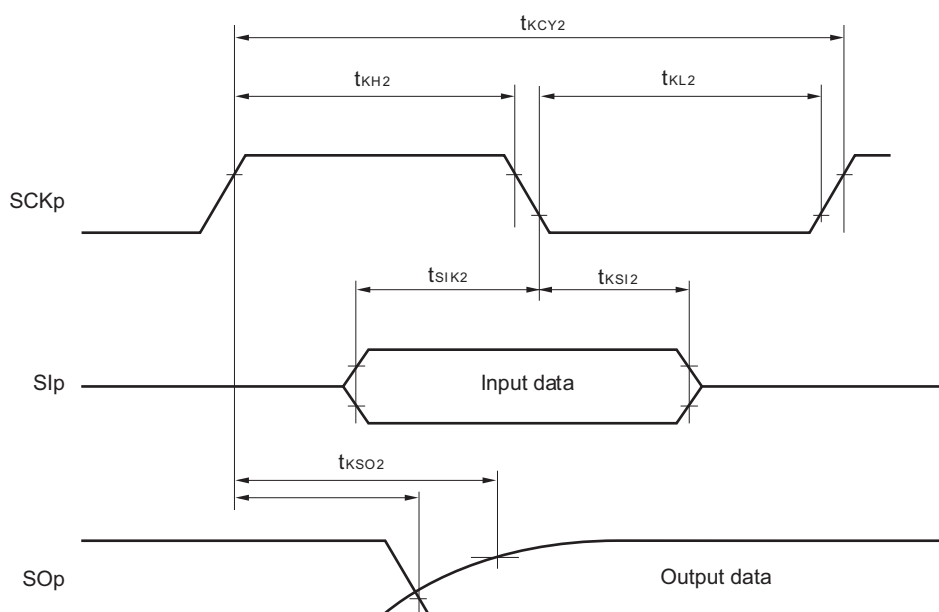
2. p: CSI number (p = 00, 01), m: Unit number (m = 0), n: Channel number (n = 0, 1), g: PIM and POM number (g = 1)

3. f_{MCK}: Serial array unit operation clock frequency
 (Operation clock to be set by the serial clock select register m (SPSm) and the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00, 01))

CSI mode serial transfer timing (slave mode) (during communication at different potential)
(When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.)



CSI mode serial transfer timing (slave mode) (during communication at different potential)
(When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.)



Remark p: CSI number (p = 00, 01), m: Unit number (m = 0), n: Channel number (n = 0, 1),
 g: PIM and POM number (g = 1)

2.5.2 Serial interface IICA

(1) I²C standard mode(T_A = -40 to +85°C, 1.6 V ≤ EV_{DD} = V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS} = 0 V)

Parameter	Symbol	Conditions		HS (high-speed main) Mode		LS (low-speed main) Mode		LV (low-voltage main) Mode		Unit
				MIN.	MAX.	MIN.	MIN.	MAX.	MIN.	
SCLA0 clock frequency	f _{SCL}	Standard mode: f _{CLK} ≥ 1 MHz	2.7 V ≤ EV _{DD} ≤ 5.5 V	0	100	0	100	0	100	kHz
			2.4 V ≤ EV _{DD} ≤ 5.5 V	0	100	0	100	0	100	
			1.8 V ≤ EV _{DD} ≤ 5.5 V			0	100	0	100	
			1.6 V ≤ EV _{DD} ≤ 5.5 V					0	100	
Setup time of restart condition	t _{SU:STA}	2.7 V ≤ EV _{DD} ≤ 5.5 V		4.7		4.7		4.7		μs
		2.4 V ≤ EV _{DD} ≤ 5.5 V		4.7		4.7		4.7		
		1.8 V ≤ EV _{DD} ≤ 5.5 V				4.7		4.7		
		1.6 V ≤ EV _{DD} ≤ 5.5 V						4.7		
Hold time ^{Note 1}	t _{HD:STA}	2.7 V ≤ EV _{DD} ≤ 5.5 V		4.0		4.0		4.0		μs
		2.4 V ≤ EV _{DD} ≤ 5.5 V		4.0		4.0		4.0		
		1.8 V ≤ EV _{DD} ≤ 5.5 V				4.0		4.0		
		1.6 V ≤ EV _{DD} ≤ 5.5 V						4.0		
Hold time when SCLA0 = “L”	t _{LOW}	2.7 V ≤ EV _{DD} ≤ 5.5 V		4.7		4.7		4.7		μs
		2.4 V ≤ EV _{DD} ≤ 5.5 V		4.7		4.7		4.7		
		1.8 V ≤ EV _{DD} ≤ 5.5 V				4.7		4.7		
		1.6 V ≤ EV _{DD} ≤ 5.5 V						4.7		
Hold time when SCLA0 = “H”	t _{HIGH}	2.7 V ≤ EV _{DD} ≤ 5.5 V		4.0		4.0		4.0		μs
		2.4 V ≤ EV _{DD} ≤ 5.5 V		4.0		4.0		4.0		
		1.8 V ≤ EV _{DD} ≤ 5.5 V				4.0		4.0		
		1.6 V ≤ EV _{DD} ≤ 5.5 V						4.0		
Data setup time (reception)	t _{SU:DAT}	2.7 V ≤ EV _{DD} ≤ 5.5 V		250		250		250		ns
		2.4 V ≤ EV _{DD} ≤ 5.5 V		250		250		250		
		1.8 V ≤ EV _{DD} ≤ 5.5 V				250		250		
		1.6 V ≤ EV _{DD} ≤ 5.5 V						250		
Data hold time (transmission) ^{Note 2}	t _{HD:DAT}	2.7 V ≤ EV _{DD} ≤ 5.5 V		0	3.45	0	3.45	0	3.45	μs
		2.4 V ≤ EV _{DD} ≤ 5.5 V		0	3.45	0	3.45	0	3.45	
		1.8 V ≤ EV _{DD} ≤ 5.5 V				0	3.45	0	3.45	
		1.6 V ≤ EV _{DD} ≤ 5.5 V						0	3.45	
Setup time of stop condition	t _{SU:STO}	2.7 V ≤ EV _{DD} ≤ 5.5 V		4.0		4.0		4.0		μs
		2.4 V ≤ EV _{DD} ≤ 5.5 V		4.0		4.0		4.0		
		1.8 V ≤ EV _{DD} ≤ 5.5 V				4.0		4.0		
		1.6 V ≤ EV _{DD} ≤ 5.5 V						4.0		
Bus-free time	t _{BUF}	2.7 V ≤ EV _{DD} ≤ 5.5 V		4.7		4.7		4.7		μs
		2.4 V ≤ EV _{DD} ≤ 5.5 V		4.7		4.7		4.7		
		1.8 V ≤ EV _{DD} ≤ 5.5 V				4.7		4.7		
		1.6 V ≤ EV _{DD} ≤ 5.5 V						4.7		

(Notes and Remark are listed on the next page.)

- Notes**
1. The first clock pulse is generated after this period when the start/restart condition is detected.
 2. The maximum value (MAX.) of t_{HD:DAT} is during normal transfer and a wait state is inserted in the $\overline{\text{ACK}}$ (acknowledge) timing.

Remark The maximum value of C_b (communication line capacitance) and the value of R_b (communication line pull-up resistor) at that time in each mode are as follows.

Standard mode: C_b = 400 pF, R_b = 2.7 kΩ

(2) I²C fast mode(T_A = -40 to +85°C, 1.6 V ≤ EV_{DD} = V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS} = 0 V)

Parameter	Symbol	Conditions		HS (high-speed main) Mode		LS (low-speed main) Mode		LV (low-voltage main) Mode		Unit
				MIN.	MAX.	MIN.	MIN.	MAX.	MIN.	
SCLA0 clock frequency	f _{SCL}	Fast mode: f _{CLK} ≥ 3.5 MHz	2.7 V ≤ EV _{DD} ≤ 5.5 V	0	400	0	400	0	400	kHz
			2.4 V ≤ EV _{DD} ≤ 5.5 V	0	400	0	400	0	400	
			1.8 V ≤ EV _{DD} ≤ 5.5 V			0	400	0	400	
Setup time of restart condition	t _{SU:STA}	2.7 V ≤ EV _{DD} ≤ 5.5 V		0.6		0.6		0.6		μs
		2.4 V ≤ EV _{DD} ≤ 5.5 V		0.6		0.6		0.6		
		1.8 V ≤ EV _{DD} ≤ 5.5 V				0.6		0.6		
Hold time ^{Note 1}	t _{HD:STA}	2.7 V ≤ EV _{DD} ≤ 5.5 V		0.6		0.6		0.6		μs
		2.4 V ≤ EV _{DD} ≤ 5.5 V		0.6		0.6		0.6		
		1.8 V ≤ EV _{DD} ≤ 5.5 V				0.6		0.6		
Hold time when SCLA0 = “L”	t _{LOW}	2.7 V ≤ EV _{DD} ≤ 5.5 V		1.3		1.3		1.3		μs
		2.4 V ≤ EV _{DD} ≤ 5.5 V		1.3		1.3		1.3		
		1.8 V ≤ EV _{DD} ≤ 5.5 V				1.3		1.3		
Hold time when SCLA0 = “H”	t _{HIGH}	2.7 V ≤ EV _{DD} ≤ 5.5 V		0.6		0.6		0.6		μs
		2.4 V ≤ EV _{DD} ≤ 5.5 V		0.6		0.6		0.6		
		1.8 V ≤ EV _{DD} ≤ 5.5 V				0.6		0.6		
Data setup time (reception)	t _{SU:DAT}	2.7 V ≤ EV _{DD} ≤ 5.5 V		100		100		100		ns
		2.4 V ≤ EV _{DD} ≤ 5.5 V		100		100		100		
		1.8 V ≤ EV _{DD} ≤ 5.5 V				100		100		
Data hold time (transmission) ^{Note 2}	t _{HD:DAT}	2.7 V ≤ EV _{DD} ≤ 5.5 V		0	0.9	0	0.9	0	0.9	μs
		2.4 V ≤ EV _{DD} ≤ 5.5 V		0	0.9	0	0.9	0	0.9	
		1.8 V ≤ EV _{DD} ≤ 5.5 V				0	0.9	0	0.9	
Setup time of stop condition	t _{SU:STO}	2.7 V ≤ EV _{DD} ≤ 5.5 V		0.6		0.6		0.6		μs
		2.4 V ≤ EV _{DD} ≤ 5.5 V		0.6		0.6		0.6		
		1.8 V ≤ EV _{DD} ≤ 5.5 V				0.6		0.6		
Bus-free time	t _{BUF}	2.7 V ≤ EV _{DD} ≤ 5.5 V		1.3		1.3		1.3		μs
		2.4 V ≤ EV _{DD} ≤ 5.5 V		1.3		1.3		1.3		
		1.8 V ≤ EV _{DD} ≤ 5.5 V				1.3		1.3		

Notes 1. The first clock pulse is generated after this period when the start/restart condition is detected.2. The maximum value (MAX.) of t_{HD:DAT} is during normal transfer and a wait state is inserted in the ACK (acknowledge) timing.**Remark** The maximum value of C_b (communication line capacitance) and the value of R_b (communication line pull-up resistor) at that time in each mode are as follows.Fast mode: C_b = 320 pF, R_b = 1.1 kΩ

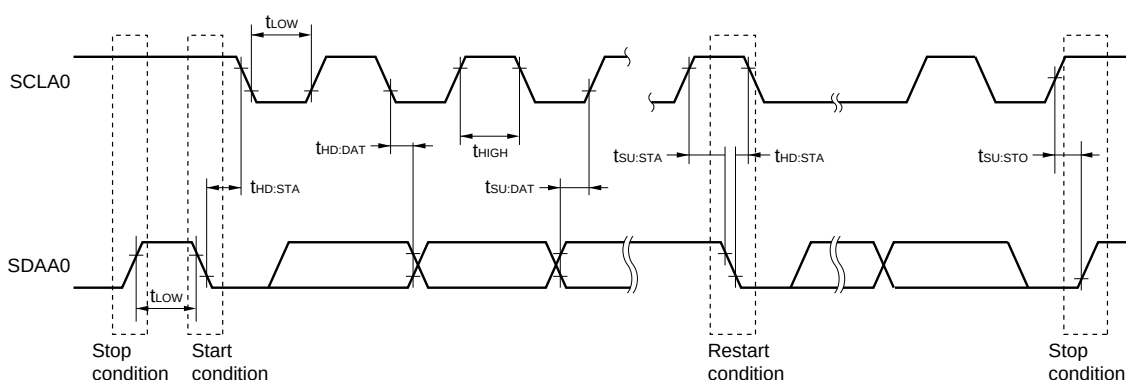
(3) I²C fast mode plus(T_A = -40 to +85°C, 1.6 V ≤ EV_{DD} = V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS} = 0 V)

Parameter	Symbol	Conditions	HS (high-speed main) Mode		LS (low-speed main) Mode		LV (low-voltage main) Mode		Unit
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
SCLA0 clock frequency	f _{SCL}	Fast mode plus: f _{CLK} ≥ 10 MHz 2.7 V ≤ EV _{DD} ≤ 5.5 V	0	1000	—	—	—	—	kHz
Setup time of restart condition	t _{SU:STA}	2.7 V ≤ EV _{DD} ≤ 5.5 V	0.26		—	—	—	—	μs
Hold time ^{Note 1}	t _{HD:STA}	2.7 V ≤ EV _{DD} ≤ 5.5 V	0.26		—	—	—	—	μs
Hold time when SCLA0 = "L"	t _{LOW}	2.7 V ≤ EV _{DD} ≤ 5.5 V	0.5		—	—	—	—	μs
Hold time when SCLA0 = "H"	t _{HIGH}	2.7 V ≤ EV _{DD} ≤ 5.5 V	0.26		—	—	—	—	μs
Data setup time (reception)	t _{SU:DAT}	2.7 V ≤ EV _{DD} ≤ 5.5 V	50		—	—	—	—	μs
Data hold time (transmission) ^{Note 2}	t _{HD:DAT}	2.7 V ≤ EV _{DD} ≤ 5.5 V	0	0.45	—	—	—	—	μs
Setup time of stop condition	t _{SU:STO}	2.7 V ≤ EV _{DD} ≤ 5.5 V	0.26		—	—	—	—	μs
Bus-free time	t _{BUF}	2.7 V ≤ EV _{DD} ≤ 5.5 V	0.5		—	—	—	—	μs

Notes 1. The first clock pulse is generated after this period when the start/restart condition is detected.2. The maximum value (MAX.) of t_{HD:DAT} is during normal transfer and a wait state is inserted in the ACK (acknowledge) timing.

Caution The values in the above table are applied even when bit 2 (PIOR2) in the peripheral I/O redirection register (PIOR) is 1. At this time, the pin characteristics (I_{OH1}, I_{OL1}, V_{OH1}, V_{OL1}) must satisfy the values in the redirect destination.

Remark The maximum value of C_b (communication line capacitance) and the value of R_b (communication line pull-up resistor) at that time in each mode are as follows.

Fast mode plus: C_b = 120 pF, R_b = 1.1 kΩ**IICA serial transfer timing**

2.6 Analog Characteristics

2.6.1 A/D converter characteristics

Classification of A/D converter characteristics

Input channel	Reference Voltage		
	Reference voltage (+) = AV _{REFP} Reference voltage (-) = AV _{REFM}	Reference voltage (+) = V _{DD} Reference voltage (-) = V _{SS}	Reference voltage (+) = V _{BGR} Reference voltage (-) = AV _{REFM}
ANI0, ANI1	—	Refer to 2.6.1 (3).	Refer to 2.6.1 (4).
ANI16 to ANI23	Refer to 2.6.1 (2).		
Internal reference voltage Temperature sensor output voltage	Refer to 2.6.1 (1).		—

(1) When reference voltage (+) = AV_{REFP}/ANI0 (ADREFP1 = 0, ADREFP0 = 1), reference voltage (-) = AV_{REFM}/ANI1 (ADREFM = 1), target pin : internal reference voltage, and temperature sensor output voltage

(T_A = -40 to +85°C, 2.4 V ≤ EV_{DD} = V_{DD} ≤ 5.5 V, 1.6 V ≤ AV_{REFP} ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS} = 0 V, Reference voltage (+) = AV_{REFP}, Reference voltage (-) = AV_{REFM} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Resolution	RES		8		10	bit
Overall error ^{Note 1}	AINL	10-bit resolution AV _{REFP} = V _{DD} ^{Note 3}	1.8 V ≤ V _{DD} ≤ 5.5 V		±3.5	LSB
			1.6 V ≤ V _{DD} ≤ 5.5 V ^{Note 4}	1.2	±7.0	LSB
Conversion time	t _{CONV}	10-bit resolution Target pin: Internal reference voltage, and temperature sensor output voltage (HS (high-speed main) mode)	3.6 V ≤ V _{DD} ≤ 5.5 V	2.375	39	μs
			2.7 V ≤ V _{DD} ≤ 5.5 V	3.5625	39	μs
			2.4 V ≤ V _{DD} ≤ 5.5 V	17	39	μs
Zero-scale error ^{Notes 1, 2}	E _{zs}	10-bit resolution AV _{REFP} = V _{DD} ^{Note 3}	1.8 V ≤ AV _{REFP} ≤ 5.5 V		±0.25	%FSR
			1.6 V ≤ AV _{REFP} ≤ 5.5 V ^{Note 4}		±0.50	%FSR
Full-scale error ^{Notes 1, 2}	E _{fs}	10-bit resolution AV _{REFP} = V _{DD} ^{Note 3}	1.8 V ≤ AV _{REFP} ≤ 5.5 V		±0.25	%FSR
			1.6 V ≤ AV _{REFP} ≤ 5.5 V ^{Note 4}		±0.50	%FSR
Integral linearity error ^{Note 1}	ILE	10-bit resolution AV _{REFP} = V _{DD} ^{Note 3}	1.8 V ≤ V _{DD} ≤ 5.5 V		±2.5	LSB
			1.6 V ≤ V _{DD} ≤ 5.5 V ^{Note 4}		±5.0	LSB
Differential linearity error ^{Note 1}	DLE	10-bit resolution AV _{REFP} = V _{DD} ^{Note 3}	1.8 V ≤ V _{DD} ≤ 5.5 V		±1.5	LSB
			1.6 V ≤ V _{DD} ≤ 5.5 V ^{Note 4}		±2.0	LSB
Analog input voltage	V _{AIN}	Internal reference voltage (2.4 V ≤ V _{DD} ≤ 5.5 V, HS (high-speed main) mode)	V _{BGR} ^{Note 5}			V
	V _{BGR}	Temperature sensor output voltage (2.4 V ≤ V _{DD} ≤ 5.5 V, HS (high-speed main) mode)	V _{TMPS25} ^{Note 5}			V

Notes 1. Excludes quantization error (±1/2 LSB).

2. This value is indicated as a ratio (%FSR) to the full-scale value.

3. When AV_{REFP} < V_{DD}, the MAX. values are as follows.

Overall error: Add ±1.0 LSB to the MAX. value when AV_{REFP} = V_{DD}.

Zero-scale error/Full-scale error: Add ±0.05%FSR to the MAX. value when AV_{REFP} = V_{DD}.

Integral linearity error/Differential linearity error: Add ±0.5 LSB to the MAX. value when AV_{REFP} = V_{DD}.

4. Values when the conversion time is set to 57 μs (min.) and 95 μs (max.).

5. Refer to 2.6.2 Temperature sensor/internal reference voltage characteristics.

(2) When reference voltage (+) = $AV_{REFP}/ANI0$ (ADREFP1 = 0, ADREFP0 = 1), reference voltage (-) = $AV_{REFM}/ANI1$ (ADREFM = 1), target pin : ANI16 to ANI23

(T_A = -40 to +85°C, $1.6\text{ V} \leq EV_{DD} = V_{DD} \leq 5.5\text{ V}$, $1.6\text{ V} \leq AV_{REFP} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = EV_{SS} = 0\text{ V}$, Reference voltage (+) = AV_{REFP} , Reference voltage (-) = $AV_{REFM} = 0\text{ V}$)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Resolution	RES		8		10	bit
Overall error ^{Note 1}	AINL	10-bit resolution $AV_{REFP} = EV_{DD} = V_{DD}$ Note 3	$1.8\text{ V} \leq AV_{REFP} \leq 5.5\text{ V}$	1.2	±5.0	LSB
			$1.6\text{ V} \leq AV_{REFP} \leq 5.5\text{ V}$ Note 4	1.2	±8.5	LSB
Conversion time	t _{CONV}	10-bit resolution $AV_{REFP} = EV_{DD} = V_{DD}$ Note 3	$3.6\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	2.125	39	μs
			$2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	3.1875	39	μs
			$1.8\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	17	39	μs
			$1.6\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	57	95	μs
Zero-scale error ^{Notes 1, 2}	E _{ZS}	10-bit resolution $AV_{REFP} = EV_{DD} = V_{DD}$ Note 3	$1.8\text{ V} \leq AV_{REFP} \leq 5.5\text{ V}$		±0.35	%FSR
			$1.6\text{ V} \leq AV_{REFP} \leq 5.5\text{ V}$ Note 4		±0.60	%FSR
Full-scale error ^{Notes 1, 2}	E _{FS}	10-bit resolution $AV_{REFP} = EV_{DD} = V_{DD}$ Note 3	$1.8\text{ V} \leq AV_{REFP} \leq 5.5\text{ V}$		±0.35	%FSR
			$1.6\text{ V} \leq AV_{REFP} \leq 5.5\text{ V}$ Note 4		±0.60	%FSR
Integral linearity error ^{Note 1}	ILE	10-bit resolution $AV_{REFP} = EV_{DD} = V_{DD}$ Note 3	$1.8\text{ V} \leq AV_{REFP} \leq 5.5\text{ V}$		±3.5	LSB
			$1.6\text{ V} \leq AV_{REFP} \leq 5.5\text{ V}$ Note 4		±6.0	LSB
Differential linearity error Note 1	DLE	10-bit resolution $AV_{REFP} = EV_{DD} = V_{DD}$ Note 3	$1.8\text{ V} \leq AV_{REFP} \leq 5.5\text{ V}$		±2.0	LSB
			$1.6\text{ V} \leq AV_{REFP} \leq 5.5\text{ V}$ Note 4		±2.5	LSB
Analog input voltage	V _{AIN}		0		AV_{REFP} and EV_{DD}	V

Notes 1. Excludes quantization error (±1/2 LSB).

2. This value is indicated as a ratio (%FSR) to the full-scale value.

3. When $AV_{REFP} < EV_{DD} = V_{DD}$, the MAX. values are as follows.

Overall error: Add ±4.0 LSB to the MAX. value when $AV_{REFP} = V_{DD}$.

Zero-scale error/Full-scale error: Add ±0.20%FSR to the MAX. value when $AV_{REFP} = V_{DD}$.

Integral linearity error/Differential linearity error: Add ±2.0 LSB to the MAX. value when $AV_{REFP} = V_{DD}$.

4. When the conversion time is set to 57 μs (min.) and 95 μs (max.).

(3) When reference voltage (+) = V_{DD} (ADREFP1 = 0, ADREFP0 = 0), reference voltage (-) = V_{SS} (ADREFM = 0), target pin : ANI0, ANI1, ANI16 to ANI23, internal reference voltage, and temperature sensor output voltage

(T_A = -40 to +85°C, 1.6 V ≤ EV_{DD} = V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS} = 0 V, Reference voltage (+) = V_{DD}, Reference voltage (-) = V_{SS})

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Resolution	RES			8		10	bit
Overall error ^{Note 1}	AINL	10-bit resolution	1.8 V ≤ V _{DD} ≤ 5.5 V		1.2	±7.0	LSB
			1.6 V ≤ V _{DD} ≤ 5.5 V Note 3		1.2	±10.5	LSB
Conversion time	t _{CONV}	10-bit resolution	3.6 V ≤ V _{DD} ≤ 5.5 V	2.125		39	μs
			2.7 V ≤ V _{DD} ≤ 5.5 V	3.1875		39	μs
			1.8 V ≤ V _{DD} ≤ 5.5 V	17		39	μs
			1.6 V ≤ V _{DD} ≤ 5.5 V	57		95	μs
		10-bit resolution Target pin: Internal reference voltage, and temperature sensor output voltage (HS (high-speed main) mode)	3.6 V ≤ V _{DD} ≤ 5.5 V	2.375		39	μs
			2.7 V ≤ V _{DD} ≤ 5.5 V	3.5625		39	μs
			2.4 V ≤ V _{DD} ≤ 5.5 V	17		39	μs
Zero-scale error ^{Notes 1, 2}	E _{ZS}	10-bit resolution	1.8 V ≤ V _{DD} ≤ 5.5 V			±0.60	%FSR
			1.6 V ≤ V _{DD} ≤ 5.5 V Note 3			±0.85	%FSR
Full-scale error ^{Notes 1, 2}	E _{FS}	10-bit resolution	1.8 V ≤ V _{DD} ≤ 5.5 V			±0.60	%FSR
			1.6 V ≤ V _{DD} ≤ 5.5 V Note 3			±0.85	%FSR
Integral linearity error ^{Note 1}	ILE	10-bit resolution	1.8 V ≤ V _{DD} ≤ 5.5 V			±4.0	LSB
			1.6 V ≤ V _{DD} ≤ 5.5 V Note 3			±6.5	LSB
Differential linearity error ^{Note 1}	DLE	10-bit resolution	1.8 V ≤ V _{DD} ≤ 5.5 V			±2.0	LSB
			1.6 V ≤ V _{DD} ≤ 5.5 V Note 3			±2.5	LSB
Analog input voltage	V _{AIN}	ANI0, ANI1		0		V _{DD}	V
		ANI16 to ANI23		0		EV _{DD}	V
		Internal reference voltage (2.4 V ≤ V _{DD} ≤ 5.5 V, HS (high-speed main) mode)		V _{BGR} ^{Note 4}			V
		Temperature sensor output voltage (2.4 V ≤ V _{DD} ≤ 5.5 V, HS (high-speed main) mode)		V _{TMPS25} ^{Note 4}			V

Notes 1. Excludes quantization error (±1/2 LSB).

2. This value is indicated as a ratio (%FSR) to the full-scale value.

3. When the conversion time is set to 57 μs (min.) and 95 μs (max.).

4. Refer to 2.6.2 Temperature sensor/internal reference voltage characteristics.

(4) When reference voltage (+) = Internal reference voltage (ADREFP1 = 1, ADREFP0 = 0), reference voltage (-) = AV_{REFM}/ANI1 (ADREFM = 1), target pin : ANI0, ANI16 to ANI23

(T_A = -40 to +85°C, 2.4 V ≤ EV_{DD} = V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS} = 0 V, Reference voltage (+) = V_{BGR}^{Note 3}, Reference voltage (-) = AV_{REFM}^{Note 4} = 0 V, HS (high-speed main) mode)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Resolution	RES			8			bit
Conversion time	t _{CONV}	8-bit resolution	2.4 V ≤ V _{DD} ≤ 5.5 V	17		39	μs
Zero-scale error ^{Notes 1, 2}	E _{ZS}	8-bit resolution	2.4 V ≤ V _{DD} ≤ 5.5 V			±0.60	%FSR
Integral linearity error ^{Note 1}	ILE	8-bit resolution	2.4 V ≤ V _{DD} ≤ 5.5 V			±2.0	LSB
Differential linearity error ^{Note 1}	DLE	8-bit resolution	2.4 V ≤ V _{DD} ≤ 5.5 V			±1.0	LSB
Analog input voltage	V _{AIN}			0		V _{BGR} ^{Note 3}	V

Notes 1. Excludes quantization error (±1/2 LSB).

2. This value is indicated as a ratio (%FSR) to the full-scale value.

3. Refer to **2.6.2 Temperature sensor/internal reference voltage characteristics**.

4. When reference voltage (-) = V_{SS}, the MAX. values are as follows.

Zero-scale error: Add ±0.35%FSR to the MAX. value when reference voltage (-) = AV_{REFM}.

Integral linearity error: Add ±0.5 LSB to the MAX. value when reference voltage (-) = AV_{REFM}.

Differential linearity error: Add ±0.2 LSB to the MAX. value when reference voltage (-) = AV_{REFM}.

2.6.2 Temperature sensor/internal reference voltage characteristics

(T_A = -40 to +85°C, 2.4 V ≤ EV_{DD} = V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS} = 0 V) (HS (high-speed main) mode)

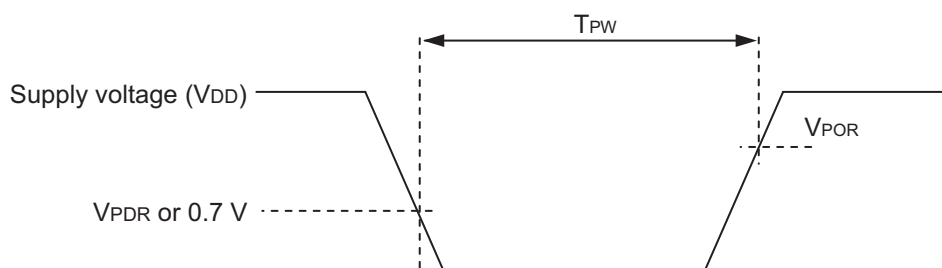
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Temperature sensor output voltage	V _{TMPS25}	Setting ADS register = 80H, T _A = +25°C		1.05		V
Internal reference voltage	V _{BGR}	Setting ADS register = 81H	1.38	1.45	1.5	V
Temperature coefficient	F _{VTMPS}	Temperature sensor that depends on the temperature		-3.6		mV/°C
Operation stabilization wait time	t _{AMP}		5			μs

2.6.3 POR circuit characteristics

(T_A = -40 to $+85^{\circ}\text{C}$, V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Detection voltage	V _{POR}	Power supply rise time	1.47	1.51	1.55	V
	V _{PDR}	Power supply fall time	1.46	1.50	1.54	V
Minimum pulse width ^{Note}	T _{PW}		300			μs

Note Minimum time required for a POR reset when V_{DD} exceeds below V_{PDR}. This is also the minimum time required for a POR reset from when V_{DD} exceeds below 0.7 V to when V_{DD} exceeds V_{POR} while STOP mode is entered or the main system clock is stopped through setting bit 0 (HIOSTOP) and bit 7 (MSTOP) in the clock operation status control register (CSC).



2.6.4 LVD circuit characteristics

(T_A = -40 to +85°C, V_{PDR} ≤ EV_{DD} = V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS} = 0 V)

Parameter		Symbol	Conditions	MIN.	TYP.	MAX.	Unit		
Detection voltage	Supply voltage level	V _{LVD0}	Power supply rise time	3.98	4.06	4.14	V		
			Power supply fall time	3.90	3.98	4.06	V		
		V _{LVD1}	Power supply rise time	3.68	3.75	3.82	V		
			Power supply fall time	3.60	3.67	3.74	V		
		V _{LVD2}	Power supply rise time	3.07	3.13	3.19	V		
			Power supply fall time	3.00	3.06	3.12	V		
		V _{LVD3}	Power supply rise time	2.96	3.02	3.08	V		
			Power supply fall time	2.90	2.96	3.02	V		
		V _{LVD4}	Power supply rise time	2.86	2.92	2.97	V		
			Power supply fall time	2.80	2.86	2.91	V		
		V _{LVD5}	Power supply rise time	2.76	2.81	2.87	V		
			Power supply fall time	2.70	2.75	2.81	V		
		V _{LVD6}	Power supply rise time	2.66	2.71	2.76	V		
			Power supply fall time	2.60	2.65	2.70	V		
		V _{LVD7}	Power supply rise time	2.56	2.61	2.66	V		
			Power supply fall time	2.50	2.55	2.60	V		
		V _{LVD8}	Power supply rise time	2.45	2.50	2.55	V		
			Power supply fall time	2.40	2.45	2.50	V		
		V _{LVD9}	Power supply rise time	2.05	2.09	2.13	V		
			Power supply fall time	2.00	2.04	2.08	V		
		V _{LVD10}	Power supply rise time	1.94	1.98	2.02	V		
			Power supply fall time	1.90	1.94	1.98	V		
		V _{LVD11}	Power supply rise time	1.84	1.88	1.91	V		
			Power supply fall time	1.80	1.84	1.87	V		
		V _{LVD12}	Power supply rise time	1.74	1.77	1.81	V		
			Power supply fall time	1.70	1.73	1.77	V		
		V _{LVD13}	Power supply rise time	1.64	1.67	1.70	V		
			Power supply fall time	1.60	1.63	1.66	V		
		Minimum pulse width		t _{LW}		300			μs
		Detection delay time		t _{LD}				300	μs

LVD Detection Voltage of Interrupt & Reset Mode(T_A = -40 to +85°C, V_{PDR} ≤ EV_{DD} = V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS} = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Interrupt and reset mode	VLVDA0	VPOC2, VPOC1, VPOC0 = 0, 0, 0, falling reset voltage		1.60	1.63	1.66	V
	VLVDA1	LVIS1, LVIS0 = 1, 0	Rising release reset voltage	1.74	1.77	1.81	V
			Falling interrupt voltage	1.70	1.73	1.77	V
	VLVDA2	LVIS1, LVIS0 = 0, 1	Rising release reset voltage	1.84	1.88	1.91	V
			Falling interrupt voltage	1.80	1.84	1.87	V
	VLVDA3	LVIS1, LVIS0 = 0, 0	Rising release reset voltage	2.86	2.92	2.97	V
			Falling interrupt voltage	2.80	2.86	2.91	V
	VLVDB1	VPOC2, VPOC1, VPOC0 = 0, 0, 1, falling reset voltage		1.80	1.84	1.87	V
	VLVDB2	LVIS1, LVIS0 = 1, 0	Rising release reset voltage	1.94	1.98	2.02	V
			Falling interrupt voltage	1.90	1.94	1.98	V
	VLVDB3	LVIS1, LVIS0 = 0, 1	Rising release reset voltage	2.05	2.09	2.13	V
			Falling interrupt voltage	2.00	2.04	2.08	V
	VLVDB4	LVIS1, LVIS0 = 0, 0	Rising release reset voltage	3.07	3.13	3.19	V
			Falling interrupt voltage	3.00	3.06	3.12	V
	VLVDC0	VPOC2, VPOC1, VPOC0 = 0, 1, 0, falling reset voltage		2.40	2.45	2.50	V
	VLVDC1	LVIS1, LVIS0 = 1, 0	Rising release reset voltage	2.56	2.61	2.66	V
			Falling interrupt voltage	2.50	2.55	2.60	V
	VLVDC2	LVIS1, LVIS0 = 0, 1	Rising release reset voltage	2.66	2.71	2.76	V
			Falling interrupt voltage	2.60	2.65	2.70	V
	VLVDC3	LVIS1, LVIS0 = 0, 0	Rising release reset voltage	3.68	3.75	3.82	V
			Falling interrupt voltage	3.60	3.67	3.74	V
	VLVDD0	VPOC2, VPOC1, VPOC0 = 0, 1, 1, falling reset voltage		2.70	2.75	2.81	V
	VLVDD1	LVIS1, LVIS0 = 1, 0	Rising release reset voltage	2.86	2.92	2.97	V
			Falling interrupt voltage	2.80	2.86	2.91	V
	VLVDD2	LVIS1, LVIS0 = 0, 1	Rising release reset voltage	2.96	3.02	3.08	V
			Falling interrupt voltage	2.90	2.96	3.02	V
	VLVDD3	LVIS1, LVIS0 = 0, 0	Rising release reset voltage	3.98	4.06	4.14	V
			Falling interrupt voltage	3.90	3.98	4.06	V

2.6.5 Supply voltage rise time(T_A = -40 to +85°C, V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Power supply voltage rising slope	S _{VDD}				54	V/ms

Caution Make sure to keep the internal reset state by the LVD circuit or an external reset until V_{DD} reaches the operating voltage range shown in 30.4 AC Characteristics.

2.7 LCD Characteristics

2.7.1 Resistance division method

(1) Static display mode

(T_A = -40 to +85°C, V_{L4} (MIN.) ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
LCD drive voltage	V _{L4}		2.0		V _{DD}	V

(2) 1/2 bias method, 1/4 bias method

(T_A = -40 to +85°C, V_{L4} (MIN.) ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
LCD drive voltage	V _{L4}		2.7		V _{DD}	V

(3) 1/3 bias method

(T_A = -40 to +85°C, V_{L4} (MIN.) ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
LCD drive voltage	V _{L4}		2.5		V _{DD}	V

2.7.2 Internal voltage boosting method

(1) 1/3 bias method

(T_A = -40 to +85°C, 1.8 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
LCD output voltage variation range	V _{L1}	C1 to C4 ^{Note 1} = 0.47 μF	VLCD = 04H	0.90	1.00	1.08	V
			VLCD = 05H	0.95	1.05	1.13	V
			VLCD = 06H	1.00	1.10	1.18	V
			VLCD = 07H	1.05	1.15	1.23	V
			VLCD = 08H	1.10	1.20	1.28	V
			VLCD = 09H	1.15	1.25	1.33	V
			VLCD = 0AH	1.20	1.30	1.38	V
			VLCD = 0BH	1.25	1.35	1.43	V
			VLCD = 0CH	1.30	1.40	1.48	V
			VLCD = 0DH	1.35	1.45	1.53	V
			VLCD = 0EH	1.40	1.50	1.58	V
			VLCD = 0FH	1.45	1.55	1.63	V
			VLCD = 10H	1.50	1.60	1.68	V
			VLCD = 11H	1.55	1.65	1.73	V
			VLCD = 12H	1.60	1.70	1.78	V
			VLCD = 13H	1.65	1.75	1.83	V
Doubler output voltage	V _{L2}	C1 to C4 ^{Note 1} = 0.47 μF	2 V _{L1} − 0.1	2 V _{L1}	2 V _{L1}	V	
Tripler output voltage	V _{L4}	C1 to C4 ^{Note 1} = 0.47 μF	3 V _{L1} − 0.15	3 V _{L1}	3 V _{L1}	V	
Reference voltage setup time ^{Note 2}	t _{WAIT1}		5			ms	
Voltage boost wait time ^{Note 3}	t _{WAIT2}	C1 to C4 ^{Note 1} = 0.47 μF	500			ms	

Notes 1. This is a capacitor that is connected between voltage pins used to drive the LCD.

C1: A capacitor connected between CAPH and CAPL

C2: A capacitor connected between V_{L1} and GNDC3: A capacitor connected between V_{L2} and GNDC4: A capacitor connected between V_{L4} and GND

C1 = C2 = C3 = C4 = 0.47 μF±30%

- This is the time required to wait from when the reference voltage is specified by using the VLCD register (or when the internal voltage boosting method is selected [by setting the MDSET1 and MDSET0 bits of the LCDM0 register to 01B] if the default value reference voltage is used) until voltage boosting starts (VLCON = 1).
- This is the wait time from when voltage boosting is started (VLCON = 1) until display is enabled (LCDON = 1).

(2) 1/4 bias method

(T_A = -40 to +85°C, 1.8 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
LCD output voltage variation range	V _{L1} ^{Note 4}	C1 to C5 ^{Note 1} = 0.47 μF	VLCD = 04H	0.90	1.00	1.08	V
			VLCD = 05H	0.95	1.05	1.13	V
			VLCD = 06H	1.00	1.10	1.18	V
			VLCD = 07H	1.05	1.15	1.23	V
			VLCD = 08H	1.10	1.20	1.28	V
			VLCD = 09H	1.15	1.25	1.33	V
			VLCD = 0AH	1.20	1.30	1.38	V
			VLCD = 0BH	1.25	1.35	1.43	V
			VLCD = 0CH	1.30	1.40	1.48	V
			VLCD = 0DH	1.35	1.45	1.53	V
			VLCD = 0EH	1.40	1.50	1.58	V
			VLCD = 0FH	1.45	1.55	1.63	V
			VLCD = 10H	1.50	1.60	1.68	V
			VLCD = 11H	1.55	1.65	1.73	V
			VLCD = 12H	1.60	1.70	1.78	V
			VLCD = 13H	1.65	1.75	1.83	V
Doubler output voltage	V _{L2}	C1 to C5 ^{Note 1} = 0.47 μF	2 V _{L1} - 0.08	2 V _{L1}	2 V _{L1}	V	
Tripler output voltage	V _{L3}	C1 to C5 ^{Note 1} = 0.47 μF	3 V _{L1} - 0.12	3 V _{L1}	3 V _{L1}	V	
Quadruply output voltage	V _{L4} ^{Note 4}	C1 to C5 ^{Note 1} = 0.47 μF	4 V _{L1} - 0.16	4 V _{L1}	4 V _{L1}	V	
Reference voltage setup time ^{Note 2}	t _{WAIT1}		5			ms	
Voltage boost wait time ^{Note 3}	t _{WAIT2}	C1 to C5 ^{Note 1} = 0.47 μF	500			ms	

Notes 1. This is a capacitor that is connected between voltage pins used to drive the LCD.

C1: A capacitor connected between CAPH and CAPL

C2: A capacitor connected between V_{L1} and GNDC3: A capacitor connected between V_{L2} and GNDC4: A capacitor connected between V_{L3} and GNDC5: A capacitor connected between V_{L4} and GND

C1 = C2 = C3 = C4 = C5 = 0.47 μF ± 30%

2. This is the time required to wait from when the reference voltage is specified by using the VLCD register (or when the internal voltage boosting method is selected [by setting the MDSET1 and MDSET0 bits of the LCDM0 register to 01B] if the default value reference voltage is used) until voltage boosting starts (VLCON = 1).

3. This is the wait time from when voltage boosting is started (VLCON = 1) until display is enabled (LCDON = 1).

4. V_{L4} must be 5.5 V or lower.

2.7.3 Capacitor split method

1/3 bias method

(T_A = -40 to +85°C, 2.2 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
V _{L4} voltage	V _{L4}	C1 to C4 = 0.47 μF ^{Note 2}		V _{DD}		V
V _{L2} voltage	V _{L2}	C1 to C4 = 0.47 μF ^{Note 2}	2/3 V _{L4} - 0.1	2/3 V _{L4}	2/3 V _{L4} + 0.1	V
V _{L1} voltage	V _{L1}	C1 to C4 = 0.47 μF ^{Note 2}	1/3 V _{L4} - 0.1	1/3 V _{L4}	1/3 V _{L4} + 0.1	V
Capacitor split wait time ^{Note 1}	t _{WAIT}		100			ms

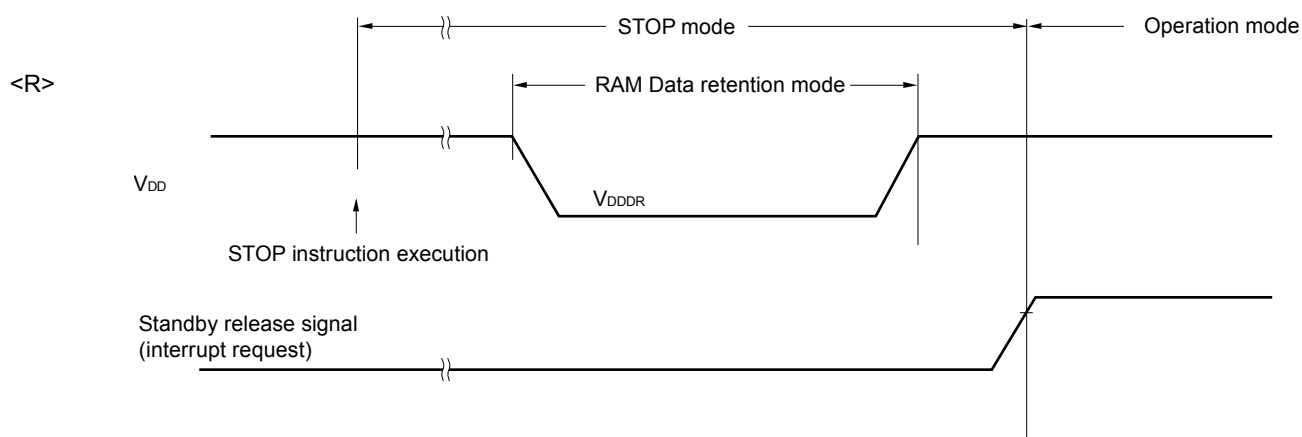
- Notes**
1. This is the wait time from when voltage bucking is started (VLCON = 1) until display is enabled (LCDON = 1).
 2. This is a capacitor that is connected between voltage pins used to drive the LCD.
 - C1: A capacitor connected between CAPH and CAPL
 - C2: A capacitor connected between V_{L1} and GND
 - C3: A capacitor connected between V_{L2} and GND
 - C4: A capacitor connected between V_{L4} and GND
- C1 = C2 = C3 = C4 = 0.47 μ F $\pm$ 30%

<R> 2.8 RAM Data Retention Characteristics

(T_A = -40 to +85°C, V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Data retention supply voltage	V _{DDDR}		1.46 ^{Note}		5.5	V

<R> **Note** This depends on the POR detection voltage. For a falling voltage, data in RAM are retained until the voltage reaches the level that triggers a POR reset but not once it reaches the level at which a POR reset is generated.



2.9 Flash Memory Programming Characteristics

(T_A = -40 to +85°C, 1.8 V ≤ EV_{DD} = V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
System clock frequency	f _{CLK}	1.8 V ≤ V _{DD} ≤ 5.5 V	1		24	MHz
<R> Number of code flash rewrites Note 1, 2, 3	C _{enwr}	Retained for 20 years T _A = 85°C	1,000			Times
<R> Number of data flash rewrites Note 1, 2, 3		Retained for 1 year T _A = 25°C		1,000,000		
<R>		Retained for 5 years T _A = 85°C	100,000			
<R>		Retained for 20 years T _A = 85°C	10,000			

Notes 1. 1 erase + 1 write after the erase is regarded as 1 rewrite.

The retaining years are until next rewrite after the rewrite.

2. When using flash memory programmer and Renesas Electronics self programming library

3. This characteristic indicates the flash memory characteristic and based on Renesas Electronics reliability test.

Remark When updating data multiple times, use the flash memory as one for updating data.

2.10 Dedicated Flash Memory Programmer Communication (UART)

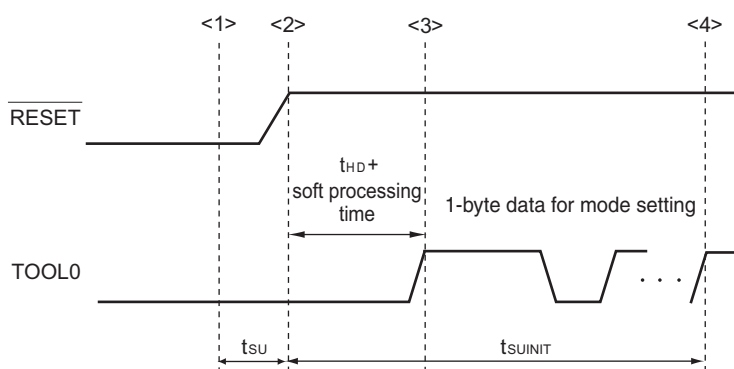
(T_A = -40 to +85°C, 1.8 V ≤ EV_{DD} = V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Transfer rate		During flash memory programming	115,200		1,000,000	bps

2.11 Timing Specifications for Switching Flash Memory Programming Modes

(T_A = -40 to +85°C, 1.8 V ≤ EV_{DD} = V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Time to complete the communication for the initial setting after the external reset is released	t _{SUINIT}	POR and LVD reset must be released before the external reset is released.			100	ms
Time to release the external reset after the TOOL0 pin is set to the low level	t _{SU}	POR and LVD reset must be released before the external reset is released.	10			μs
Time to hold the TOOL0 pin at the low level after the external reset is released (excluding the processing time of the firmware to control the flash memory)	t _{HD}	POR and LVD reset must be released before the external reset is released.	1			ms



- <1> The low level is input to the TOOL0 pin.
- <2> The external reset is released (POR and LVD reset must be released before the external reset is released.).
- <3> The TOOL0 pin is set to the high level.
- <4> Setting of the flash memory programming mode by UART reception and complete the baud rate setting.

Remark t_{SUINIT}: Communication for the initial setting must be completed within 100 ms after a reset is released during this period.

t_{SU}: Time to release the external reset after the TOOL0 pin is set to the low level

t_{HD}: Time to hold the TOOL0 pin at the low level after the external reset is released (excluding the processing time of the firmware to control the flash memory)

3. ELECTRICAL SPECIFICATIONS (G: $T_A = -40$ to $+105^{\circ}\text{C}$)

This chapter describes the electrical specifications for the products "G: Industrial applications ($T_A = -40$ to $+105^{\circ}\text{C}$)".

- Cautions**
1. The RL78 microcontrollers have an on-chip debug function, which is provided for development and evaluation. Do not use the on-chip debug function in products designated for mass production, because the guaranteed number of rewritable times of the flash memory may be exceeded when this function is used, and product reliability therefore cannot be guaranteed. Renesas Electronics is not liable for problems occurring when the on-chip debug function is used.
 2. With products not provided with an EV_{DD} or EV_{SS} pin, replace EV_{DD} with V_{DD} , or replace EV_{SS} with V_{SS} .
 3. For derating with $T_A = +85$ to $+105^{\circ}\text{C}$, contact our Sales Division or the vender's sales division. Derating means the specified reduction in an operating parameter to improve reliability.

There are following differences between the products "G: Industrial applications (T_A = -40 to +105°C)" and the products "A: Consumer applications, and G: Industrial applications (T_A = -40 to +85°C)".

Parameter	Application	
	A: Consumer applications, G: Industrial applications (with T _A = -40 to +85°C)	G: Industrial applications
Operating ambient temperature	T _A = -40 to +85°C	T _A = -40 to +105°C
Operating mode Operating voltage range	HS (high-speed main) mode: 2.7 V ≤ V _{DD} ≤ 5.5 V@1 MHz to 32 MHz 2.4 V ≤ V _{DD} ≤ 5.5 V@1 MHz to 16 MHz LS (low-speed main) mode: 1.8 V ≤ V _{DD} ≤ 5.5 V@1 MHz to 8 MHz LV (low-voltage main) mode: 1.6 V ≤ V _{DD} ≤ 5.5 V@1 MHz to 4 MHz	HS (high-speed main) mode only: 2.7 V ≤ V _{DD} ≤ 5.5 V@1 MHz to 32 MHz 2.4 V ≤ V _{DD} ≤ 5.5 V@1 MHz to 16 MHz
High-speed on-chip oscillator clock accuracy	1.8 V ≤ V _{DD} ≤ 5.5 V: ±1.0%@ T _A = -20 to +85°C ±1.5%@ T _A = -40 to -20°C 1.6 V ≤ V _{DD} < 1.8 V: ±5.0%@ T _A = -20 to +85°C ±5.5%@ T _A = -40 to -20°C	2.4 V ≤ V _{DD} ≤ 5.5 V: ±2.0%@ T _A = +85 to +105°C ±1.0%@ T _A = -20 to +85°C ±1.5%@ T _A = -40 to -20°C
Serial array unit	UART CSI00: f _{CLK} /2 (supporting 16 Mbps), f _{CLK} /4 CSI01 Simplified I ² C communication	UART CSI00: f _{CLK} /4 CSI01 Simplified I ² C communication
IICA	Normal mode Fast mode Fast mode plus	Normal mode Fast mode
Voltage detector	Rise detection voltage: 1.67 V to 4.06 V (14 levels) Fall detection voltage: 1.63 V to 3.98 V (14 levels)	Rise detection voltage: 2.61 V to 4.06 V (8 levels) Fall detection voltage: 2.55 V to 3.98 V (8 levels)

Remark The electrical characteristics of the products G: Industrial applications (T_A = -40 to +105°C) are different from those of the products "A: Consumer applications, and G: Industrial applications (only with T_A = -40 to +85°C)". For details, refer to **3.1** to **3.10**.

3.1 Absolute Maximum Ratings

Absolute Maximum Ratings (T_A = 25°C)

(1/3)

Parameter	Symbols	Conditions	Ratings	Unit
Supply voltage	V _{DD}	V _{DD} = EV _{DD}	-0.5 to +6.5	V
	EV _{DD}	V _{DD} = EV _{DD}	-0.5 to +6.5	V
	EV _{SS}		-0.5 to +0.3	V
REGC pin input voltage	V _{I REGC}	REGC	-0.3 to +2.8 and -0.3 to V _{DD} + 0.3 ^{Note 1}	V
Input voltage	V _{I1}	P10 to P17, P30 to P32, P40 to P43, P50 to P54, P70 to P74, P120, P125 to P127, P140 to P147	-0.3 to EV _{DD} + 0.3 and -0.3 to V _{DD} + 0.3 ^{Note 2}	V
	V _{I2}	P60, P61 (N-ch open-drain)	-0.3 to EV _{DD} + 0.3 and -0.3 to V _{DD} + 0.3 ^{Note 2}	V
	V _{I3}	P20, P21, P121 to P124, P137, EXCLK, EXCLKS, RESET	-0.3 to V _{DD} + 0.3 ^{Note 2}	V
Output voltage	V _{O1}	P10 to P17, P30 to P32, P40 to P43, P50 to P54, P60, P61, P70 to P74, P120, P125 to P127, P130, P140 to P147	-0.3 to EV _{DD} + 0.3 and -0.3 to V _{DD} + 0.3 ^{Note 2}	V
	V _{O2}	P20, P21	-0.3 to V _{DD} + 0.3 ^{Note 2}	V
Analog input voltage	V _{AI1}	ANI16 to ANI23	-0.3 to EV _{DD} + 0.3 and -0.3 to AV _{REF} (+) + 0.3 ^{Notes 2, 3}	V
	V _{AI2}	ANI0, ANI1	-0.3 to V _{DD} + 0.3 and -0.3 to AV _{REF} (+) + 0.3 ^{Notes 2, 3}	V

Notes 1. Connect the REGC pin to V_{SS} via a capacitor (0.47 to 1 μF). This value regulates the absolute maximum rating of the REGC pin. Do not use this pin with voltage applied to it.

2. Must be 6.5 V or lower.

3. Do not exceed AV_{REF}(+) + 0.3 V in case of A/D conversion target pin.

Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

Remarks 1. Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

2. AV_{REF}(+) : + side reference voltage of the A/D converter.

3. V_{SS} : Reference voltage

Absolute Maximum Ratings (T_A = 25°C)**(2/3)**

Parameter	Symbols	Conditions		Ratings	Unit
LCD voltage	V _{L1}	V _{L1} voltage ^{Note 1}		−0.3 to +2.8 and −0.3 to V _{L4} + 0.3	V
	V _{L2}	V _{L2} voltage ^{Note 1}		−0.3 to V _{L4} + 0.3 ^{Note 2}	V
	V _{L3}	V _{L3} voltage ^{Note 1}		−0.3 to V _{L4} + 0.3 ^{Note 2}	V
	V _{L4}	V _{L4} voltage ^{Note 1}		−0.3 to +6.5	V
	V _{LCAP}	CAPL, CAPH voltage ^{Note 1}		−0.3 to V _{L4} + 0.3 ^{Note 2}	V
	V _{LOUT}	COM0 to COM7, SEG0 to SEG38, output voltage	External resistance division method	−0.3 to V _{DD} + 0.3 ^{Note 2}	V
			Capacitor split method	−0.3 to V _{DD} + 0.3 ^{Note 2}	
Internal voltage boosting method			−0.3 to V _{L4} + 0.3 ^{Note 2}		

Notes 1. This value only indicates the absolute maximum ratings when applying voltage to the V_{L1}, V_{L2}, V_{L3}, and V_{L4} pins; it does not mean that applying voltage to these pins is recommended. When using the internal voltage boosting method or capacitance split method, connect these pins to V_{SS} via a capacitor (0.47 μF ± 30%) and connect a capacitor (0.47 μF ± 30%) between the CAPL and CAPH pins.

2. Must be 6.5 V or lower.

Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

Remark V_{SS} : Reference voltage

Absolute Maximum Ratings (T_A = 25°C)**(3/3)**

Parameter	Symbols	Conditions		Ratings	Unit
Output current, high	I _{OH1}	Per pin	P10 to P17, P30 to P32, P40 to P43, P50 to P54, P70 to P74, P120, P125 to P127, P130, P140 to P147	−40	mA
		Total of all pins −170 mA	P10 to P14, P40 to P43, P120, P130, P140 to P147	−70	mA
			P15 to P17, P30 to P32, P50 to P54, P70 to P74, P125 to P127	−100	mA
	I _{OH2}	Per pin	P20, P21	−0.5	mA
		Total of all pins		−1	mA
Output current, low	I _{OL1}	Per pin	P10 to P17, P30 to P32, P40 to P43, P50 to P54, P60, P61, P70 to P74, P120, P125 to P127, P130, P140 to P147	40	mA
		Total of all pins 170 mA	P10 to P14, P40 to P43, P120, P130, P140 to P147	70	mA
			P15 to P17, P30 to P32, P50 to P54, P60, P61, P70 to P74, P125 to P127	100	mA
	I _{OL2}	Per pin	P20, P21	1	mA
		Total of all pins		2	mA
Operating ambient temperature	T _A	In normal operation mode		−40 to +105	°C
		In flash memory programming mode			
Storage temperature	T _{stg}			−65 to +150	°C

Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

3.2 Oscillator Characteristics

3.2.1 X1, XT1 oscillator characteristics

(T_A = -40 to +105°C, 2.4 V ≤ E_{VDD} = V_{DD} ≤ 5.5 V, V_{SS} = E_{VSS} = 0 V)

Parameter	Resonator	Conditions	MIN.	TYP.	MAX.	Unit
X1 clock oscillation frequency (f _X) ^{Note}	Ceramic resonator/ crystal resonator	2.7 V ≤ V _{DD} ≤ 5.5 V	1.0		20.0	MHz
		2.4 V ≤ V _{DD} < 2.7 V	1.0		16.0	MHz
XT1 clock oscillation frequency (f _{XT}) ^{Note}	Crystal resonator		32	32.768	35	kHz

Note Indicates only permissible oscillator frequency ranges. Refer to **3.4 AC Characteristics** for instruction execution time. Request evaluation by the manufacturer of the oscillator circuit mounted on a board to check the oscillator characteristics.

Caution Since the CPU is started by the high-speed on-chip oscillator clock after a reset release, check the X1 clock oscillation stabilization time using the oscillation stabilization time counter status register (OSTC) by the user. Determine the oscillation stabilization time of the OSTC register and the oscillation stabilization time select register (OSTS) after sufficiently evaluating the oscillation stabilization time with the resonator to be used.

3.2.2 On-chip oscillator characteristics

(T_A = -40 to +105°C, 2.4 V ≤ E_{VDD} = V_{DD} ≤ 5.5 V, V_{SS} = E_{VSS} = 0 V)

Oscillators	Parameters	Conditions		MIN.	TYP.	MAX.	Unit
High-speed on-chip oscillator clock frequency ^{Notes 1, 2}	f _{IH}			1		24	MHz
High-speed on-chip oscillator clock frequency accuracy		-20 to +85°C	2.4 V ≤ V _{DD} ≤ 5.5 V	-1		+1	%
		-40 to -20°C	2.4 V ≤ V _{DD} ≤ 5.5 V	-1.5		+1.5	%
		+85 to +105°C	2.4 V ≤ V _{DD} ≤ 5.5 V	-2.0		+2.0	%
Low-speed on-chip oscillator clock frequency	f _{IL}				15		kHz
Low-speed on-chip oscillator clock frequency accuracy				-15		+15	%

Notes 1. High-speed on-chip oscillator frequency is selected by bits 0 to 3 of option byte (000C2H) and bits 0 to 2 of HOCODIV register.

2. This indicates the oscillator characteristics only. Refer to **3.4 AC Characteristics** for instruction execution time.

3.3 DC Characteristics

3.3.1 Pin characteristics

(T_A = -40 to +105°C, 2.4 V ≤ EV_{DD} = V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS} = 0 V)

(1/5)

Items	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Output current, high ^{Note 1}	I _{OH1}	Per pin for P10 to P17, P30 to P32, P40 to P43, P50 to P54, P70 to P74, P120, P125 to P127, P130, P140 to P147				-3.0 ^{Note 2}	mA
		Total of P10 to P14, P40 to P43, P120, P130, P140 to P147 (When duty = 70% ^{Note 3})	4.0 V ≤ EV _{DD} ≤ 5.5 V			-30.0	mA
			2.7 V ≤ EV _{DD} < 4.0 V			-8.0	mA
			2.4 V ≤ EV _{DD} < 2.7 V			-4.0	mA
		Total of P15 to P17, P30 to P32, P50 to P54, P70 to P74, P125 to P127 (When duty = 70% ^{Note 3})	4.0 V ≤ EV _{DD} ≤ 5.5 V			-30.0	mA
			2.7 V ≤ EV _{DD} < 4.0 V			-15.0	mA
			2.4 V ≤ EV _{DD} < 2.7 V			-8.0	mA
		Total of all pins (When duty = 70% ^{Note 3})				-60.0	mA
	I _{OH2}	P20, P21	Per pin			-0.1	mA
			Total of all pins	2.4 V ≤ V _{DD} ≤ 5.5 V		-0.2	mA

Notes 1. Value of current at which the device operation is guaranteed even if the current flows from the V_{DD} and EV_{DD} pins to an output pin.

2. Do not exceed the total current value.

3. Specification under conditions where the duty factor ≤ 70%.

The output current value that has changed to the duty factor > 70% the duty ratio can be calculated with the following expression (when changing the duty factor from 70% to n%).

- Total output current of pins = (I_{OH} × 0.7)/(n × 0.01)

<Example> Where n = 80% and I_{OH} = -30.0 mA

$$\text{Total output current of pins} = (-30.0 \times 0.7) / (80 \times 0.01) \cong -26.25 \text{ mA}$$

However, the current that is allowed to flow into one pin does not vary depending on the duty factor. A current higher than the absolute maximum rating must not flow into one pin.

Caution P10, P12, P15, and P17 do not output high level in N-ch open-drain mode.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

(T_A = -40 to +105°C, 2.4 V ≤ EV_{DD} = V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS} = 0 V)

(2/5)

Items	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Output current, low ^{Note 1}	I _{OL1}	Per pin for P10 to P17, P30 to P32, P40 to P43, P50 to P54, P70 to P74, P120, P125 to P127, P130, P140 to P147				8.5 ^{Note 2}	mA
		Per pin for P60, P61				15.0 ^{Note 2}	mA
		Total of P10 to P14, P40 to P43, P120, P130, P140 to P147 (When duty = 70% ^{Note 3})	4.0 V ≤ EV _{DD} ≤ 5.5 V			40.0	mA
			2.7 V ≤ EV _{DD} < 4.0 V			15.0	mA
			2.4 V ≤ EV _{DD} < 2.7 V			9.0	mA
		Total of P15 to P17, P30 to P32, P50 to P54, P60, P61, P70 to P74, P125 to P127 (When duty = 70% ^{Note 3})	4.0 V ≤ EV _{DD} ≤ 5.5 V			40.0	mA
			2.7 V ≤ EV _{DD} < 4.0 V			35.0	mA
			2.4 V ≤ EV _{DD} < 2.7 V			20.0	mA
	Total of all pins (When duty = 70% ^{Note 3})				80.0	mA	
	I _{OL2}	P20, P21	Per pin				0.4
Total of all pins			2.4 V ≤ V _{DD} ≤ 5.5 V			0.8	mA

- Notes**
1. Value of current at which the device operation is guaranteed even if the current flows from the V_{DD} and EV_{DD} pins to an output pin.
 2. Do not exceed the total current value.
 3. Specification under conditions where the duty factor ≤ 70%.

The output current value that has changed to the duty factor > 70% the duty ratio can be calculated with the following expression (when changing the duty factor from 70% to n%).

- Total output current of pins = (I_{OL} × 0.7)/(n × 0.01)

<Example> Where n = 80% and I_{OL} = 40.0 mA

$$\text{Total output current of pins} = (40.0 \times 0.7)/(80 \times 0.01) \cong 35.0 \text{ mA}$$

However, the current that is allowed to flow into one pin does not vary depending on the duty factor. A current higher than the absolute maximum rating must not flow into one pin.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

(T_A = -40 to +105°C, 2.4 V ≤ EV_{DD} = V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS} = 0 V)

(3/5)

Items	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Input voltage, high	V _{IH1}	P10 to P17, P30 to P32, P40 to P43, P50 to P54, P70 to P74, P120, P125 to P127, P140 to P147	Normal input buffer	0.8EV _{DD}	EV _{DD}	V
	V _{IH2}	P10, P11, P15, P16	TTL input buffer 4.0 V ≤ EV _{DD} ≤ 5.5 V	2.2	EV _{DD}	V
			TTL input buffer 3.3 V ≤ EV _{DD} < 4.0 V	2.0	EV _{DD}	V
			TTL input buffer 2.4 V ≤ EV _{DD} < 3.3 V	1.50	EV _{DD}	V
	V _{IH3}	P20, P21	0.7V _{DD}		V _{DD}	V
	V _{IH4}	P60, P61	0.7EV _{DD}		EV _{DD}	V
	V _{IH5}	P121 to P124, P137, EXCLK, EXCLKS, RESET	0.8V _{DD}		V _{DD}	V
Input voltage, low	V _{IL1}	P10 to P17, P30 to P32, P40 to P43, P50 to P54, P70 to P74, P120, P125 to P127, P140 to P147	Normal input buffer	0	0.2EV _{DD}	V
	V _{IL2}	P10, P11, P15, P16	TTL input buffer 4.0 V ≤ EV _{DD} ≤ 5.5 V	0	0.8	V
			TTL input buffer 3.3 V ≤ EV _{DD} < 4.0 V	0	0.5	V
			TTL input buffer 2.4 V ≤ EV _{DD} < 3.3 V	0	0.32	V
	V _{IL3}	P20, P21	0		0.3V _{DD}	V
	V _{IL4}	P60, P61	0		0.3EV _{DD}	V
	V _{IL5}	P121 to P124, P137, EXCLK, EXCLKS, RESET	0		0.2V _{DD}	V

Caution The maximum value of V_{IH} of pins P10, P12, P15, and P17 is EV_{DD}, even in the N-ch open-drain mode.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

(T_A = -40 to +105°C, 2.4 V ≤ EV_{DD} = V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS} = 0 V)

(4/5)

Items	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Output voltage, high	V _{OH1}	P10 to P17, P30 to P32, P40 to P43, P50 to P54, P70 to P74, P120, P125 to P127, P130, P140 to P147	4.0 V ≤ EV _{DD} ≤ 5.5 V, I _{OH1} = -3.0 mA	EV _{DD} - 0.7		V
			2.7 V ≤ EV _{DD} ≤ 5.5 V, I _{OH1} = -2.0 mA	EV _{DD} - 0.6		V
			2.4 V ≤ EV _{DD} ≤ 5.5 V, I _{OH1} = -1.5 mA	EV _{DD} - 0.5		V
	V _{OH2}	P20, P21	2.4 V ≤ V _{DD} ≤ 5.5 V, I _{OH2} = -100 μA	V _{DD} - 0.5		V
Output voltage, low	V _{OL1}	P10 to P17, P30 to P32, P40 to P43, P50 to P54, P70 to P74, P120, P125 to P127, P130, P140 to P147	4.0 V ≤ EV _{DD} ≤ 5.5 V, I _{OL1} = 8.5 mA		0.7	V
			2.7 V ≤ EV _{DD} ≤ 5.5 V, I _{OL1} = 3.0 mA		0.6	V
			2.7 V ≤ EV _{DD} ≤ 5.5 V, I _{OL1} = 1.5 mA		0.4	V
			2.4 V ≤ EV _{DD} ≤ 5.5 V, I _{OL1} = 0.6 mA		0.4	V
	V _{OL2}	P20, P21	2.4 V ≤ V _{DD} ≤ 5.5 V, I _{OL2} = 400 μA		0.4	V
	V _{OL3}	P60, P61	4.0 V ≤ EV _{DD} ≤ 5.5 V, I _{OL3} = 15.0 mA		2.0	V
			4.0 V ≤ EV _{DD} ≤ 5.5 V, I _{OL3} = 5.0 mA		0.4	V
			2.7 V ≤ EV _{DD} ≤ 5.5 V, I _{OL3} = 3.0 mA		0.4	V
			2.4 V ≤ EV _{DD} ≤ 5.5 V, I _{OL3} = 2.0 mA		0.4	V

Caution P10, P12, P15, and P17 do not output high level in N-ch open-drain mode.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

(T_A = -40 to +105°C, 2.4 V ≤ EV_{DD} = V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS} = 0 V)

(5/5)

Items	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Input leakage current, high	I _{LIH1}	P10 to P17, P30 to P32, P40 to P43, P50 to P54, P60, P61, P70 to P74, P120, P125 to P127, P140 to P147	V _I = EV _{DD}			1	μA
	I _{LIH2}	P20, P21, P137, RESET	V _I = V _{DD}			1	μA
	I _{LIH3}	P121 to P124 (X1, X2, XT1, XT2, EXCLK, EXCLKS)	V _I = V _{DD}	In input port or external clock input		1	μA
				In resonator connection		10	μA
Input leakage current, low	I _{LIL1}	P10 to P17, P30 to P32, P40 to P43, P50 to P54, P60, P61, P70 to P74, P120, P125 to P127, P140 to P147	V _I = EV _{SS}			-1	μA
	I _{LIL2}	P20, P21, P137, RESET	V _I = V _{SS}			-1	μA
	I _{LIL3}	P121 to P124 (X1, X2, XT1, XT2, EXCLK, EXCLKS)	V _I = V _{SS}	In input port or external clock input		-1	μA
				In resonator connection		-10	μA
On-chip pll-up resistance	R _{U1}	V _I = EV _{SS}	SEGxx port				
			2.4 V ≤ EV _{DD} = V _{DD} ≤ 5.5 V		10	20	100
	R _{U2}		Ports other than above (Except for P60, P61, and P130)		10	20	100

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

3.3.2 Supply current characteristics

(T_A = -40 to +105°C, 2.4 V ≤ EV_{DD} = V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS} = 0 V)

(1/3)

Parameter	Symbol	Conditions					MIN.	TYP.	MAX.	Unit
Supply current Note 1	I _{DD1}	Operating mode	HS (high-speed main) mode Note 5	f _{IH} = 24 MHz Note 3	Basic operation	V _{DD} = 5.0 V		1.5		mA
						V _{DD} = 3.0 V		1.5		mA
					Normal operation	V _{DD} = 5.0 V		3.3	5.3	mA
						V _{DD} = 3.0 V		3.3	5.3	mA
				f _{IH} = 16 MHz Note 3	Normal operation	V _{DD} = 5.0 V		2.5	3.9	mA
						V _{DD} = 3.0 V		2.5	3.9	mA
			HS (high-speed main) mode Note 5	f _{MX} = 20 MHz Note 2, V _{DD} = 5.0 V	Normal operation	Square wave input		2.8	4.7	mA
						Resonator connection		3.0	4.8	mA
				f _{MX} = 20 MHz Note 2, V _{DD} = 3.0 V	Normal operation	Square wave input		2.8	4.7	mA
						Resonator connection		3.0	4.8	mA
				f _{MX} = 10 MHz Note 2, V _{DD} = 5.0 V	Normal operation	Square wave input		1.8	2.8	mA
						Resonator connection		1.8	2.8	mA
				f _{MX} = 10 MHz Note 2, V _{DD} = 3.0 V	Normal operation	Square wave input		1.8	2.8	mA
						Resonator connection		1.8	2.8	mA
		Subsystem clock operation		f _{SUB} = 32.768 kHz Note 4 T _A = -40°C	Normal operation	Square wave input		3.5	4.9	μA
						Resonator connection		3.6	5.0	μA
				f _{SUB} = 32.768 kHz Note 4 T _A = +25°C	Normal operation	Square wave input		3.6	4.9	μA
						Resonator connection		3.7	5.0	μA
				f _{SUB} = 32.768 kHz Note 4 T _A = +50°C	Normal operation	Square wave input		3.7	5.5	μA
						Resonator connection		3.8	5.6	μA
				f _{SUB} = 32.768 kHz Note 4 T _A = +70°C	Normal operation	Square wave input		3.8	6.3	μA
						Resonator connection		3.9	6.4	μA
				f _{SUB} = 32.768 kHz Note 4 T _A = +85°C	Normal operation	Square wave input		4.1	7.7	μA
						Resonator connection		4.2	7.8	μA
				f _{SUB} = 32.768 kHz Note 4 T _A = +105°C	Normal operation	Square wave input		6.4	19.7	μA
						Resonator connection		6.5	19.8	μA

(Notes and Remarks are listed on the next page.)

- Notes**
1. Total current flowing into V_{DD} and EV_{DD}, including the input leakage current flowing when the level of the input pin is fixed to V_{DD}, EV_{DD} or V_{SS}, EV_{SS}. The values below the MAX. column include the peripheral operation current. However, not including the current flowing into the A/D converter, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors and the current flowing during data flash rewrite.
 2. When high-speed on-chip oscillator and subsystem clock are stopped.
 3. When high-speed system clock and subsystem clock are stopped.
 4. When high-speed on-chip oscillator and high-speed system clock are stopped. When AMPHS1 = 1 (Ultra-low power consumption oscillation). However, not including the current flowing into the RTC, 12-bit interval timer, watchdog timer, and LCD controller/driver.
 5. Relationship between operation voltage width, operation frequency of CPU and operation mode is as below.
 HS (high-speed main) mode: $2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}@1\text{ MHz to }24\text{ MHz}$
 $2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}@1\text{ MHz to }16\text{ MHz}$

- Remarks**
1. f_{MX}: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)
 2. f_{IH}: High-speed on-chip oscillator clock frequency
 3. f_{SUB}: Subsystem clock frequency (XT1 clock oscillation frequency)
 4. Except subsystem clock operation, temperature condition of the TYP. value is T_A = 25°C

(T_A = -40 to +105°C, 2.4 V ≤ E_{VDD} = V_{DD} ≤ 5.5 V, V_{SS} = E_{VSS} = 0 V)

(2/3)

Parameter	Symbol	Conditions				MIN.	TYP.	MAX.	Unit	
Supply current Note 1	I _{DD2} Note 2	HALT mode	HS (high-speed main) mode Note 7	f _{IH} = 24 MHz Note 4	V _{DD} = 5.0 V		0.44	2.3	mA	
					V _{DD} = 3.0 V		0.44	2.3	mA	
				f _{IH} = 16 MHz Note 4	V _{DD} = 5.0 V		0.40	1.7	mA	
					V _{DD} = 3.0 V		0.40	1.7	mA	
			HS (high-speed main) mode Note 7	f _{MX} = 20 MHz Note 3, V _{DD} = 5.0 V	Square wave input		0.28	1.9	mA	
					Resonator connection		0.45	2.0	mA	
				f _{MX} = 20 MHz Note 3, V _{DD} = 3.0 V	Square wave input		0.28	1.9	mA	
					Resonator connection		0.45	2.0	mA	
				f _{MX} = 10 MHz Note 3, V _{DD} = 5.0 V	Square wave input		0.19	1.02	mA	
					Resonator connection		0.26	1.10	mA	
				f _{MX} = 10 MHz Note 3, V _{DD} = 3.0 V	Square wave input		0.19	1.02	mA	
					Resonator connection		0.26	1.10	mA	
		Subsystem clock operation	f _{SUB} = 32.768 kHz Note 5 T _A = −40°C	Square wave input		0.31	0.57	μA		
				Resonator connection		0.50	0.76	μA		
			f _{SUB} = 32.768 kHz Note 5 T _A = +25°C	Square wave input		0.37	0.57	μA		
				Resonator connection		0.56	0.76	μA		
			f _{SUB} = 32.768 kHz Note 5 T _A = +50°C	Square wave input		0.46	1.17	μA		
				Resonator connection		0.65	1.36	μA		
			f _{SUB} = 32.768 kHz Note 5 T _A = +70°C	Square wave input		0.57	1.97	μA		
				Resonator connection		0.76	2.16	μA		
			f _{SUB} = 32.768 kHz Note 5 T _A = +85°C	Square wave input		0.85	3.37	μA		
				Resonator connection		1.04	3.56	μA		
			f _{SUB} = 32.768 kHz Note 5 T _A = +105°C	Square wave input		3.04	15.37	μA		
				Resonator connection		3.23	15.56	μA		
	I _{DD3} Note 6	STOP mode Note 8	T _A = −40°C					0.17	0.50	μA
			T _A = +25°C					0.23	0.50	μA
			T _A = +50°C					0.32	1.10	μA
			T _A = +70°C					0.43	1.90	μA
			T _A = +85°C					0.71	3.30	μA
			T _A = +105°C					2.90	15.30	μA

(Notes and Remarks are listed on the next page.)

- Notes**
1. Total current flowing into V_{DD} and EV_{DD}, including the input leakage current flowing when the level of the input pin is fixed to V_{DD}, EV_{DD} or V_{SS}, EV_{SS}. The values below the MAX. column include the peripheral operation current. However, not including the current flowing into the A/D converter, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors and the current flowing during data flash rewrite.
 2. During HALT instruction execution by flash memory.
 3. When high-speed on-chip oscillator and subsystem clock are stopped.
 4. When high-speed system clock and subsystem clock are stopped.
 5. When high-speed on-chip oscillator and high-speed system clock are stopped. When RTCLPC = 1 and setting ultra-low current consumption (AMPHS1 = 1). The current flowing into the RTC is included. However, not including the current flowing into the 12-bit interval timer, watchdog timer, and LCD controller/driver.
 6. Not including the current flowing into the RTC, 12-bit interval timer, and watchdog timer.
 7. Relationship between operation voltage width, operation frequency of CPU and operation mode is as below.
 HS (high-speed main) mode: $2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}@1\text{ MHz to }24\text{ MHz}$
 $2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}@1\text{ MHz to }16\text{ MHz}$
 8. Regarding the value for current operate the subsystem clock in STOP mode, refer to that in HALT mode.

- Remarks**
1. f_{MX}: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)
 2. f_{IH}: High-speed on-chip oscillator clock frequency
 3. f_{SUB}: Subsystem clock frequency (XT1 clock oscillation frequency)
 4. Except subsystem clock operation and STOP mode, temperature condition of the TYP. value is T_A = 25°C

(T_A = -40 to +105°C, 2.4 V ≤ EV_{DD} = V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS} = 0 V)

(3/3)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Low-speed on-chip oscillator operating current	I _{FIL} ^{Note 1}				0.20		μA
RTC operating current	I _{RTC} ^{Notes 1, 2, 3}	f _{MAIN} is stopped			0.08		μA
12-bit interval timer current	I _{IT} ^{Notes 1, 2, 4}				0.08		μA
Watchdog timer operating current	I _{WDT} ^{Notes 1, 2, 5}	f _{IL} = 15 kHz			0.24		μA
A/D converter operating current	I _{ADC} ^{Notes 1, 6}	When conversion at maximum speed	Normal mode, AV _{REFP} = V _{DD} = 5.0 V		1.3	1.7	mA
			Low voltage mode, AV _{REFP} = V _{DD} = 3.0 V		0.5	0.7	mA
A/D converter reference voltage current	I _{ADREF} ^{Note 1}				75.0		μA
Temperature sensor operating current	I _{TMPS} ^{Note 1}				75.0		μA
LVD operating current	I _{LVD} ^{Notes 1, 7}				0.08		μA
Self-programming operating current	I _{FSP} ^{Notes 1, 9}				2.50	12.20	mA
BGO operating current	I _{BGO} ^{Notes 1, 8}				2.50	12.20	mA
LCD operating current	I _{LCD1} ^{Notes 11, 12}	External resistance division method	V _{DD} = EV _{DD} = 5.0 V V _{L4} = 5.0 V		0.04	0.20	μA
	I _{LCD2} ^{Note 11}	Internal voltage boosting method	V _{DD} = EV _{DD} = 5.0 V V _{L4} = 5.1 V (VLCD = 12H)		1.12	3.70	μA
			V _{DD} = EV _{DD} = 3.0 V V _{L4} = 3.0 V (VLCD = 04H)		0.63	2.20	μA
	I _{LCD3} ^{Note 11}	Capacitor split method	V _{DD} = EV _{DD} = 3.0 V V _{L4} = 3.0 V		0.12	0.50	μA
SNOOZE operating current	I _{SNOZ} ^{Note 1}	ADC operation	The mode is performed ^{Note 10}		0.50	1.10	mA
			The A/D conversion operations are performed, Low voltage mode, AV _{REFP} = V _{DD} = 3.0 V		1.20	2.04	mA
		CSI/UART operation			0.70	1.54	mA

(Notes and Remarks are listed on the next page.)

Notes 1. Current flowing to V_{DD}.

2. When high speed on-chip oscillator and high-speed system clock are stopped.
3. Current flowing only to the real-time clock (RTC) (excluding the operating current of the low-speed on-chip oscillator and the XT1 oscillator). The supply current of the RL78 microcontrollers is the sum of the values of either I_{DD1} or I_{DD2}, and I_{RTC}, when the real-time clock operates in operation mode or HALT mode. When the low-speed on-chip oscillator is selected, I_{FIL} should be added. I_{DD2} subsystem clock operation includes the operational current of the real-time clock.
4. Current flowing only to the 12-bit interval timer (excluding the operating current of the low-speed on-chip oscillator and the XT1 oscillator). The supply current of the RL78 microcontrollers is the sum of the values of either I_{DD1} or I_{DD2}, and I_{IT}, when the 12-bit interval timer operates in operation mode or HALT mode. When the low-speed on-chip oscillator is selected, I_{FIL} should be added.
5. Current flowing only to the watchdog timer (including the operating current of the low-speed on-chip oscillator). The supply current of the RL78 microcontrollers is the sum of I_{DD1}, I_{DD2} or I_{DD3} and I_{WDT} when the watchdog timer is in operation.
6. Current flowing only to the A/D converter. The supply current of the RL78 microcontrollers is the sum of I_{DD1} or I_{DD2} and I_{ADC} when the A/D converter operates in an operation mode or the HALT mode.
7. Current flowing only to the LVD circuit. The supply current of the RL78 microcontrollers is the sum of I_{DD1}, I_{DD2} or I_{DD3} and I_{LVD} when the LVD circuit is in operation.
8. Current flowing only during data flash rewrite.
9. Current flowing only during self programming.
10. For shift time to the SNOOZE mode.
11. Current flowing only to the LCD controller/driver. The supply current value of the RL78 microcontrollers is the sum of the LCD operating current (I_{LCD1}, I_{LCD2} or I_{LCD3}) to the supply current (I_{DD1} or I_{DD2}) when the LCD controller/driver operates in an operation mode or HALT mode. Not including the current that flows through the LCD panel.
The TYP. value and MAX. value are following conditions.
 - When f_{SUB} is selected for system clock, LCD clock = 128 Hz (LCDC0 = 07H)
 - 4-Time-Slice, 1/3 Bias Method
12. Not including the current that flows through the external divider resistor when the external resistance division method is used.

Remarks 1. f_{IL}: Low-speed on-chip oscillator clock frequency

2. f_{SUB}: Subsystem clock frequency (XT1 clock oscillation frequency)
3. f_{CLK}: CPU/peripheral hardware clock frequency
4. Temperature condition of the TYP. value is T_A = 25°C

3.4 AC Characteristics

3.4.1 Basic operation

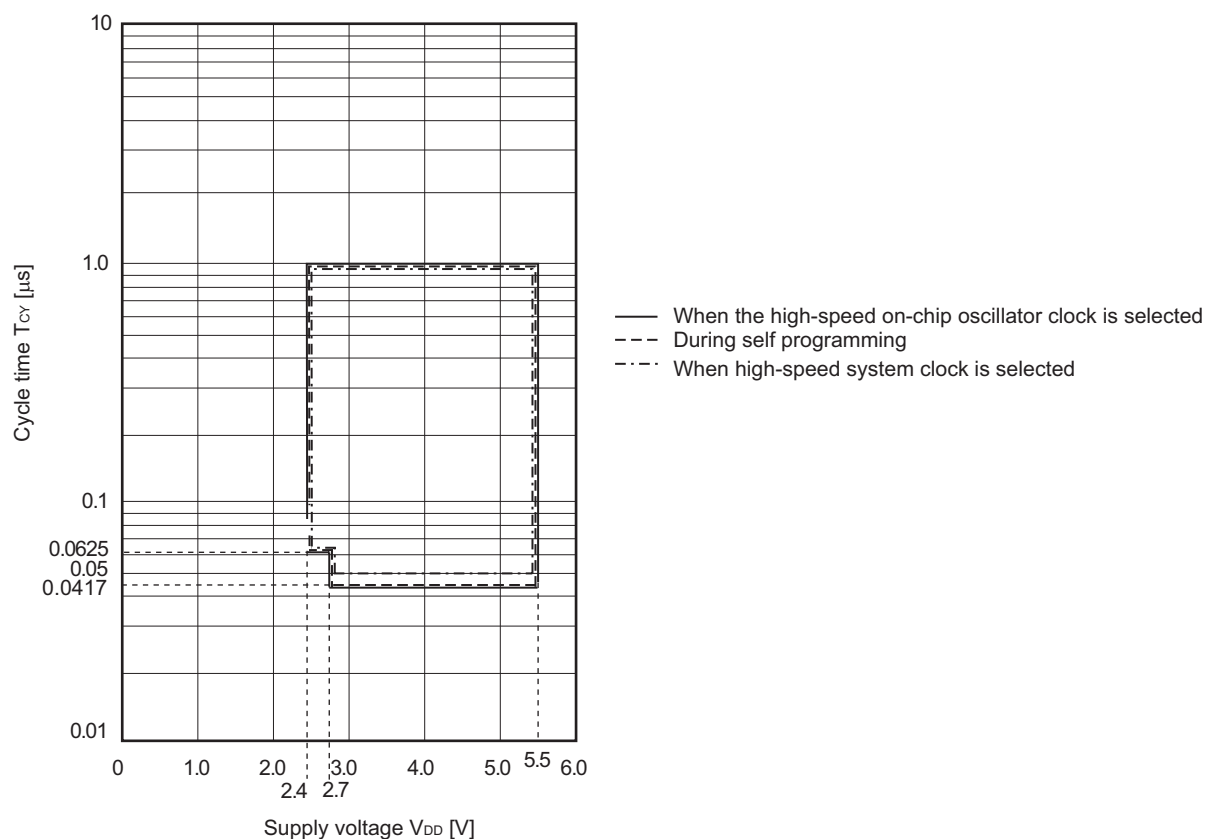
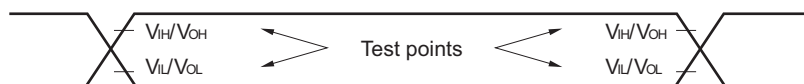
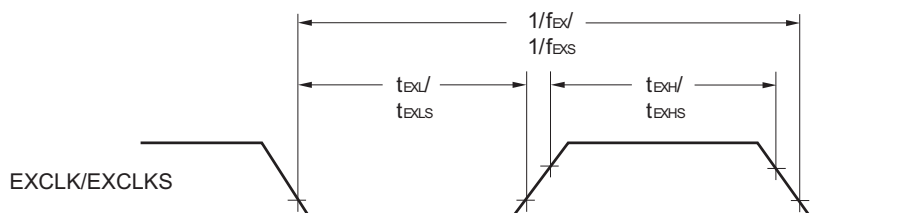
(T_A = -40 to +105°C, 2.4 V ≤ E_{VDD} = V_{DD} ≤ 5.5 V, V_{SS} = E_{VSS} = 0 V)

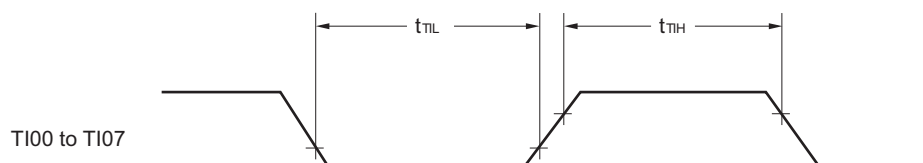
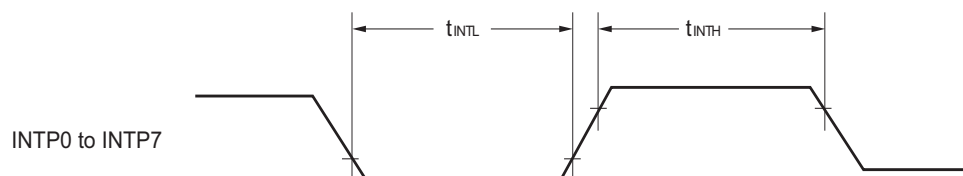
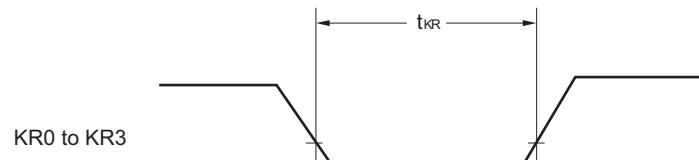
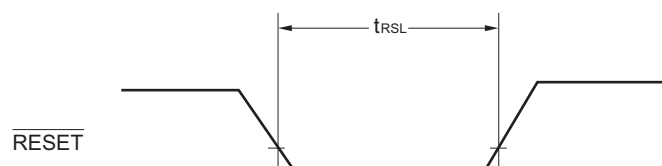
Items	Symbol	Conditions			MIN.	TYP.	MAX.	Unit
Instruction cycle (minimum instruction execution time)	T _{CY}	Main system clock (f _{MAIN}) operation	HS (high-speed main) mode	2.7 V ≤ V _{DD} ≤ 5.5 V	0.04167		1	μs
				2.4 V ≤ V _{DD} < 2.7 V	0.0625		1	μs
		Subsystem clock (f _{SUB}) operation		2.4 V ≤ V _{DD} ≤ 5.5 V	28.5	30.5	31.3	μs
		In the self programming mode	HS (high-speed main) mode	2.7 V ≤ V _{DD} ≤ 5.5 V	0.04167		1	μs
				2.4 V ≤ V _{DD} < 2.7 V	0.0625		1	μs
External system clock frequency	f _{EX}	2.7 V ≤ V _{DD} ≤ 5.5 V			1.0		20.0	MHz
		2.4 V ≤ V _{DD} < 2.7 V			1.0		16.0	MHz
	f _{EXS}				32		35	kHz
External system clock input high-level width, low-level width	t _{EXH} , t _{EXL}	2.7 V ≤ V _{DD} ≤ 5.5 V			24			ns
		2.4 V ≤ V _{DD} < 2.7 V			30			ns
	t _{EXHS} , t _{EXLS}				13.7			μs
TI00 to TI07 input high-level width, low-level width	t _{TIH} , t _{TIL}				1/f _{MCK} +10			ns
TO00 to TO07 output frequency	f _{TO}	HS (high-speed main) mode	4.0 V ≤ EV _{DD} ≤ 5.5 V				16	MHz
			2.7 V ≤ EV _{DD} < 4.0 V				8	MHz
			2.4 V ≤ EV _{DD} < 2.7 V				4	MHz
PCLBUZ0, PCLBUZ1 output frequency	f _{PCL}	HS (high-speed main) mode	4.0 V ≤ EV _{DD} ≤ 5.5 V				16	MHz
			2.7 V ≤ EV _{DD} < 4.0 V				8	MHz
			2.4 V ≤ EV _{DD} < 2.7 V				4	MHz
Interrupt input high-level width, low-level width	t _{INTH} , t _{INTL}	INTP0	2.4 V ≤ V _{DD} ≤ 5.5 V		1			μs
		INTP1 to INTP7	2.4 V ≤ EV _{DD} ≤ 5.5 V		1			μs
Key interrupt input low-level width	t _{KR}	KR0 to KR3	2.4 V ≤ EV _{DD} ≤ 5.5 V		250			ns
RESET low-level width	t _{RSL}				10			μs

Remark f_{MCK}: Timer array unit operation clock frequency

(Operation clock to be set by the CKS0n bit of timer mode register 0n (TMR0n).

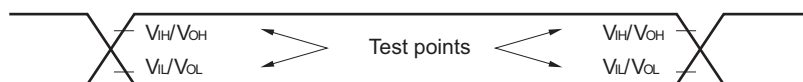
n: Channel number (n = 0 to 7))

Minimum Instruction Execution Time during Main System Clock Operation T_{CY} vs V_{DD} (HS (high-speed main) mode)**AC Timing Test Points****External System Clock Timing**

TI/TO Timing**Interrupt Request Input Timing****Key Interrupt Input Timing****RESET Input Timing**

3.5 Peripheral Functions Characteristics

AC Timing Test Points



3.5.1 Serial array unit

(1) During communication at same potential (UART mode)

(T_A = -40 to +105°C, 2.4 V ≤ EV_{DD} = V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS} = 0 V)

Parameter	Symbol	Conditions	HS (high-speed main) Mode		Unit
			MIN.	MAX.	
Transfer rate ^{Note 1}				f _{MCK} /12	bps
		Theoretical value of the maximum transfer rate f _{MCK} = f _{CLK} ^{Note 2}		2.0	Mbps

Notes 1. Transfer rate in the SNOOZE mode is 4800 bps only.

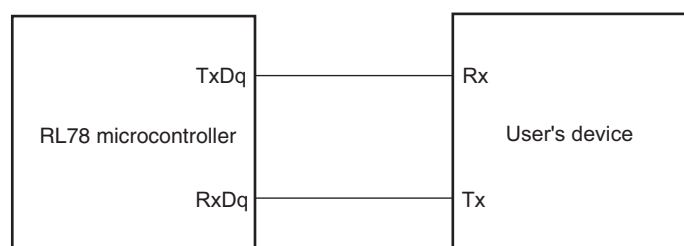
2. The maximum operating frequencies of the CPU/peripheral hardware clock (f_{CLK}) are:

HS (high-speed main) mode: 24 MHz (2.7 V ≤ V_{DD} ≤ 5.5 V)

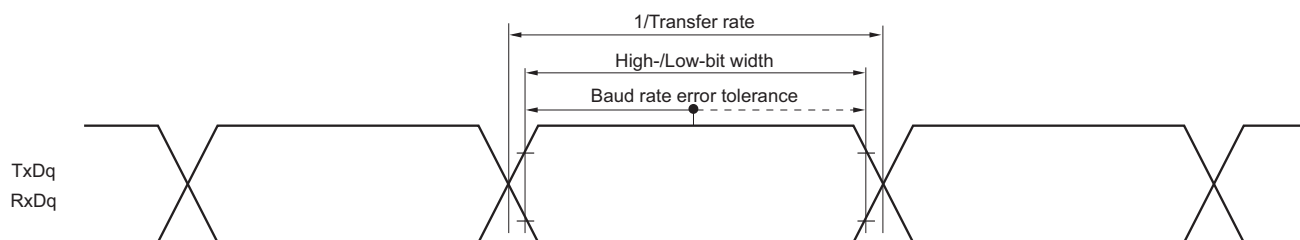
16 MHz (2.4 V ≤ V_{DD} ≤ 5.5 V)

Caution Select the normal input buffer for the RxDq pin and the normal output mode for the TxDq pin by using port input mode register g (PIMg) and port output mode register g (POMg).

UART mode connection diagram (during communication at same potential)



UART mode bit width (during communication at same potential) (reference)



Remarks 1. q: UART number (q = 0), g: PIM and POM number (g = 1)

2. f_{MCK}: Serial array unit operation clock frequency

(Operation clock to be set by the serial clock select register m (SPSm) and the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00, 01))

(2) During communication at same potential (CSI mode) (master mode, SCKp... internal clock output)**(T_A = -40 to +105°C, 2.4 V ≤ EV_{DD} = V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS} = 0 V)**

Parameter	Symbol	Conditions	HS (high-speed main) Mode		Unit
			MIN.	MAX.	
SCKp cycle time	t _{KCY1}	2.7 V ≤ EV _{DD} ≤ 5.5 V	334 ^{Note 1}		ns
		2.4 V ≤ EV _{DD} ≤ 5.5 V	500 ^{Note 1}		ns
SCKp high-/low-level width	t _{KH1} , t _{KL1}	4.0 V ≤ EV _{DD} ≤ 5.5 V	t _{KCY1} /2 – 24		ns
		2.7 V ≤ EV _{DD} ≤ 5.5 V	t _{KCY1} /2 – 36		ns
		2.4 V ≤ EV _{DD} ≤ 5.5 V	t _{KCY1} /2 – 76		ns
Slp setup time (to SCKp↑) ^{Note 2}	t _{SIK1}	2.7 V ≤ EV _{DD} ≤ 5.5 V	66		ns
		2.4 V ≤ EV _{DD} ≤ 5.5 V	113		ns
Slp hold time (from SCKp↑) ^{Note 3}	t _{KSI1}	2.4 V ≤ EV _{DD} ≤ 5.5 V	38		ns
Delay time from SCKp↓ to SOp output ^{Note 4}	t _{KSO1}	C = 30 pF ^{Note 5} 2.4 V ≤ EV _{DD} ≤ 5.5 V		50	ns

Notes 1. Set a cycle of 4/f_{MCK} or longer.

2. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The Slp setup time becomes “to SCKp↓” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

3. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The Slp hold time becomes “from SCKp↓” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

4. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The delay time to SOp output becomes “from SCKp↑” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

5. C is the load capacitance of the SCKp and SOp output lines.

Caution Select the normal input buffer for the Slp pin and the normal output mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg).**Remarks** 1. p: CSI number (p = 00, 01), m: Unit number (m = 0), n: Channel number (n = 0, 1),
g: PIM and POM numbers (g = 1)2. f_{MCK}: Serial array unit operation clock frequency
(Operation clock to be set by the serial clock select register m (SPSm) and the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00, 01))

(3) During communication at same potential (CSI mode) (slave mode, SCKp... external clock input)
(T_A = -40 to +105°C, 2.4 V ≤ EV_{DD} = V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS} = 0 V)

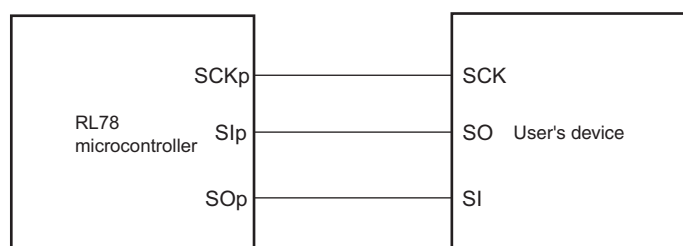
Parameter	Symbol	Conditions		HS (high-speed main) Mode		Unit
				MIN.	MAX.	
SCKp cycle time ^{Note 5}	t _{KCY2}	4.0 V ≤ EV _{DD} ≤ 5.5 V	20 MHz < f _{MCK}	16/f _{MCK}		ns
			f _{MCK} ≤ 20 MHz	12/f _{MCK}		ns
		2.7 V ≤ EV _{DD} < 4.0 V	16 MHz < f _{MCK}	16/f _{MCK}		ns
			f _{MCK} ≤ 16 MHz	12/f _{MCK}		ns
		2.4 V ≤ EV _{DD} ≤ 5.5 V		12/f _{MCK} and 1000		ns
SCKp high-/low-level width	t _{KH2} , t _{KL2}	4.0 V ≤ EV _{DD} ≤ 5.5 V		t _{KCY2} /2 – 14		ns
		2.7 V ≤ EV _{DD} < 4.0 V		t _{KCY2} /2 – 16		ns
		2.4 V ≤ EV _{DD} < 2.7 V		t _{KCY2} /2 – 36		ns
Slp setup time (to SCKp↑) ^{Note 1}	t _{SIK2}	2.7 V ≤ EV _{DD} ≤ 5.5 V		1/f _{MCK} + 40		ns
		2.4 V ≤ EV _{DD} < 2.7 V		1/f _{MCK} + 60		ns
Slp hold time (from SCKp↑) ^{Note 2}	t _{KSI2}	2.4 V ≤ EV _{DD} ≤ 5.5 V		1/f _{MCK} + 62		ns
Delay time from SCKp↓ to SOp output ^{Note 3}	t _{KSO2}	C = 30 pF ^{Note 4}	4.0 V ≤ EV _{DD} ≤ 5.5 V		2/f _{MCK} + 66	ns
			2.7 V ≤ EV _{DD} < 4.0 V		2/f _{MCK} + 66	ns
			2.4 V ≤ EV _{DD} < 2.7 V		2/f _{MCK} + 113	Ns

- Notes**
1. When DAP_{mn} = 0 and CKP_{mn} = 0, or DAP_{mn} = 1 and CKP_{mn} = 1. The Slp setup time becomes “to SCKp↓” when DAP_{mn} = 0 and CKP_{mn} = 1, or DAP_{mn} = 1 and CKP_{mn} = 0.
 2. When DAP_{mn} = 0 and CKP_{mn} = 0, or DAP_{mn} = 1 and CKP_{mn} = 1. The Slp hold time becomes “from SCKp↓” when DAP_{mn} = 0 and CKP_{mn} = 1, or DAP_{mn} = 1 and CKP_{mn} = 0.
 3. When DAP_{mn} = 0 and CKP_{mn} = 0, or DAP_{mn} = 1 and CKP_{mn} = 1. The delay time to SOp output becomes “from SCKp↑” when DAP_{mn} = 0 and CKP_{mn} = 1, or DAP_{mn} = 1 and CKP_{mn} = 0.
 4. C is the load capacitance of the SOp output lines.
 5. Transfer rate in the SNOOZE mode : MAX. 1 Mbps

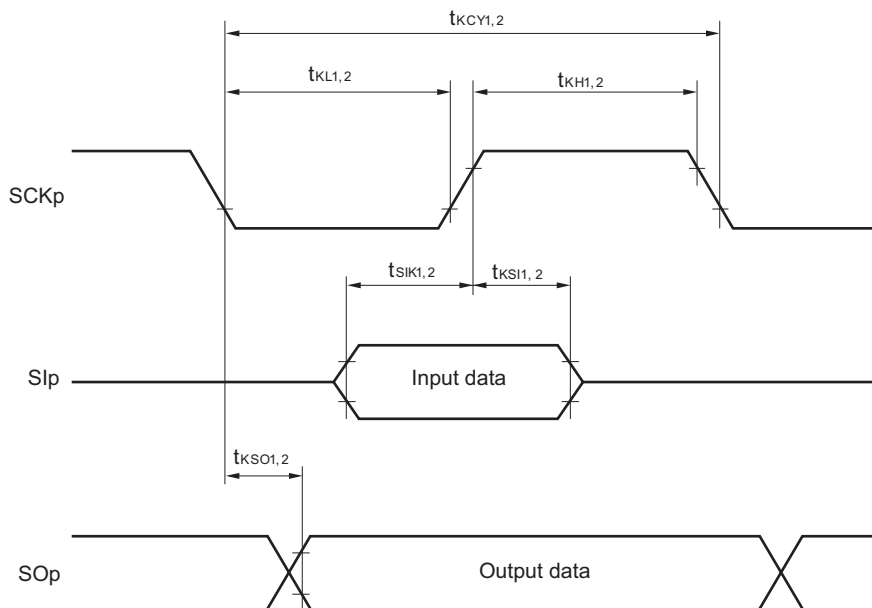
Caution Select the normal input buffer for the Slp pin and SCKp pin and the normal output mode for the SOp pin by using port input mode register g (PIMg) and port output mode register g (POMg).

- Remarks**
1. p: CSI number (p = 00, 01), m: Unit number (m = 0), n: Channel number (n = 0, 1),
g: PIM number (g = 1)
 2. f_{MCK}: Serial array unit operation clock frequency
(Operation clock to be set by the serial clock select register m (SPSm) and the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00, 01))

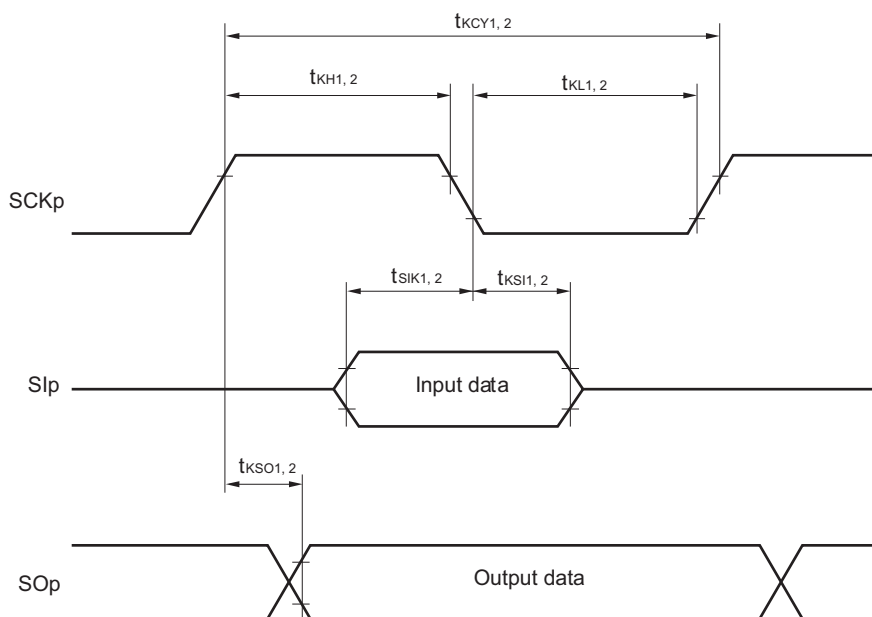
CSI mode connection diagram (during communication at same potential)



CSI mode serial transfer timing (during communication at same potential)
(When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.)



CSI mode serial transfer timing (during communication at same potential)
(When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.)



- Remarks**
1. p: CSI number (p = 00, 01)
 2. m: Unit number, n: Channel number (mn = 00, 01)

(4) Communication at different potential (1.8 V, 2.5 V, 3 V) (UART mode) (1/2)**(T_A = -40 to +105°C, 2.4 V ≤ EV_{DD} = V_{DD} ≤ 5.5 V, V_{SS} = 0 V)**

Parameter	Symbol	Conditions		HS (high-speed main) Mode		Unit	
				MIN.	MAX.		
Transfer rate		Reception	4.0 V ≤ EV _{DD} ≤ 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V			f _{MCK} /12 ^{Note 1}	bps
					Theoretical value of the maximum transfer rate f _{MCK} = f _{CLK} ^{Note 2}		2.0
			2.7 V ≤ EV _{DD} < 4.0 V, 2.3 V ≤ V _b ≤ 2.7 V			f _{MCK} /12 ^{Note 1}	bps
					Theoretical value of the maximum transfer rate f _{MCK} = f _{CLK} ^{Note 2}		2.0
			2.4 V ≤ EV _{DD} < 3.3 V, 1.6 V ≤ V _b ≤ 2.0 V			f _{MCK} /12 ^{Note 1}	bps
					Theoretical value of the maximum transfer rate f _{MCK} = f _{CLK} ^{Note 2}		2.0

Notes 1. Transfer rate in the SNOOZE mode is 4800 bps only.**2.** The maximum operating frequencies of the CPU/peripheral hardware clock (f_{CLK}) are:HS (high-speed main) mode: 24 MHz (2.7 V ≤ V_{DD} ≤ 5.5 V)16 MHz (2.4 V ≤ V_{DD} ≤ 5.5 V)

Caution Select the TTL input buffer for the Rx_{Dq} pin and the N-ch open drain output (V_{DD} tolerance (32- to 52-pin products)/EV_{DD} tolerance (64-pin products)) mode for the Tx_{Dq} pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V_{IH} and V_{IL}, see the DC characteristics with TTL input buffer selected.

Remarks 1. V_b[V]: Communication line voltage**2.** q: UART number (q = 0), g: PIM and POM number (g = 1)**3.** f_{MCK}: Serial array unit operation clock frequency

(Operation clock to be set by the serial clock select register m (SPSm) and the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00, 01))

(4) Communication at different potential (1.8 V, 2.5 V, 3 V) (UART mode)

(2/2)

(T_A = -40 to +105°C, 2.4 V ≤ EV_{DD} = V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS} = 0 V)

Parameter	Symbol	Conditions	HS (high-speed main) Mode		Unit
			MIN.	MAX.	
Transfer rate		Transmission	4.0 V ≤ EV _{DD} ≤ 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V	Note 1	bps
			Theoretical value of the maximum transfer rate C _b = 50 pF, R _b = 1.4 kΩ, V _b = 2.7 V	2.0 ^{Note 2}	Mbps
			2.7 V ≤ EV _{DD} < 4.0 V, 2.3 V ≤ V _b ≤ 2.7 V	Note 3	bps
			Theoretical value of the maximum transfer rate C _b = 50 pF, R _b = 2.7 kΩ, V _b = 2.3 V	1.2 ^{Note 4}	Mbps
			2.4 V ≤ EV _{DD} < 3.3 V, 1.6 V ≤ V _b ≤ 2.0 V	Note 5	bps
			Theoretical value of the maximum transfer rate C _b = 50 pF, R _b = 5.5 kΩ, V _b = 1.6 V	0.43 ^{Note 6}	Mbps

Notes 1. The smaller maximum transfer rate derived by using f_{MCK}/6 or the following expression is the valid maximum transfer rate.

Expression for calculating the transfer rate when 4.0 V ≤ EV_{DD} ≤ 5.5 V and 2.7 V ≤ V_b ≤ 4.0 V

$$\text{Maximum transfer rate} = \frac{1}{\{-C_b \times R_b \times \ln(1 - \frac{2.2}{V_b})\} \times 3} \text{ [bps]}$$

$$\text{Baud rate error (theoretical value)} = \frac{\frac{1}{\text{Transfer rate} \times 2} - \{-C_b \times R_b \times \ln(1 - \frac{2.2}{V_b})\}}{(\frac{1}{\text{Transfer rate}}) \times \text{Number of transferred bits}} \times 100 \text{ [%]}$$

* This value is the theoretical value of the relative difference between the transmission and reception sides.

2. This value as an example is calculated when the conditions described in the “Conditions” column are met. Refer to Note 1 above to calculate the maximum transfer rate under conditions of the customer.

3. The smaller maximum transfer rate derived by using f_{MCK}/6 or the following expression is the valid maximum transfer rate.

Expression for calculating the transfer rate when 2.7 V ≤ EV_{DD} < 4.0 V and 2.3 V ≤ V_b ≤ 2.7 V

$$\text{Maximum transfer rate} = \frac{1}{\{-C_b \times R_b \times \ln(1 - \frac{2.0}{V_b})\} \times 3} \text{ [bps]}$$

$$\text{Baud rate error (theoretical value)} = \frac{\frac{1}{\text{Transfer rate} \times 2} - \{-C_b \times R_b \times \ln(1 - \frac{2.0}{V_b})\}}{(\frac{1}{\text{Transfer rate}}) \times \text{Number of transferred bits}} \times 100 \text{ [%]}$$

* This value is the theoretical value of the relative difference between the transmission and reception sides.

4. This value as an example is calculated when the conditions described in the “Conditions” column are met. Refer to Note 3 above to calculate the maximum transfer rate under conditions of the customer.

5. The smaller maximum transfer rate derived by using $f_{MCK}/6$ or the following expression is the valid maximum transfer rate.

Expression for calculating the transfer rate when $1.8\text{ V} \leq E_{VDD} < 3.3\text{ V}$ and $1.6\text{ V} \leq V_b \leq 2.0\text{ V}$

$$\text{Maximum transfer rate} = \frac{1}{\{-C_b \times R_b \times \ln(1 - \frac{1.5}{V_b})\} \times 3} \text{ [bps]}$$

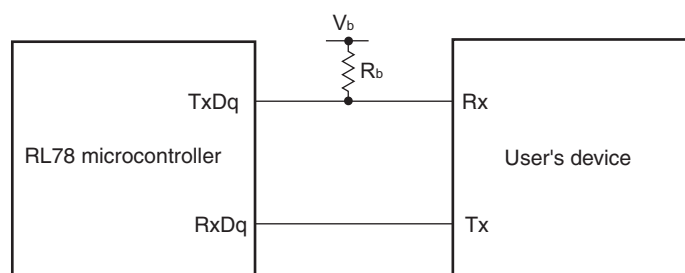
$$\text{Baud rate error (theoretical value)} = \frac{\frac{1}{\text{Transfer rate} \times 2} - \{-C_b \times R_b \times \ln(1 - \frac{1.5}{V_b})\}}{(\frac{1}{\text{Transfer rate}}) \times \text{Number of transferred bits}} \times 100 \text{ [%]}$$

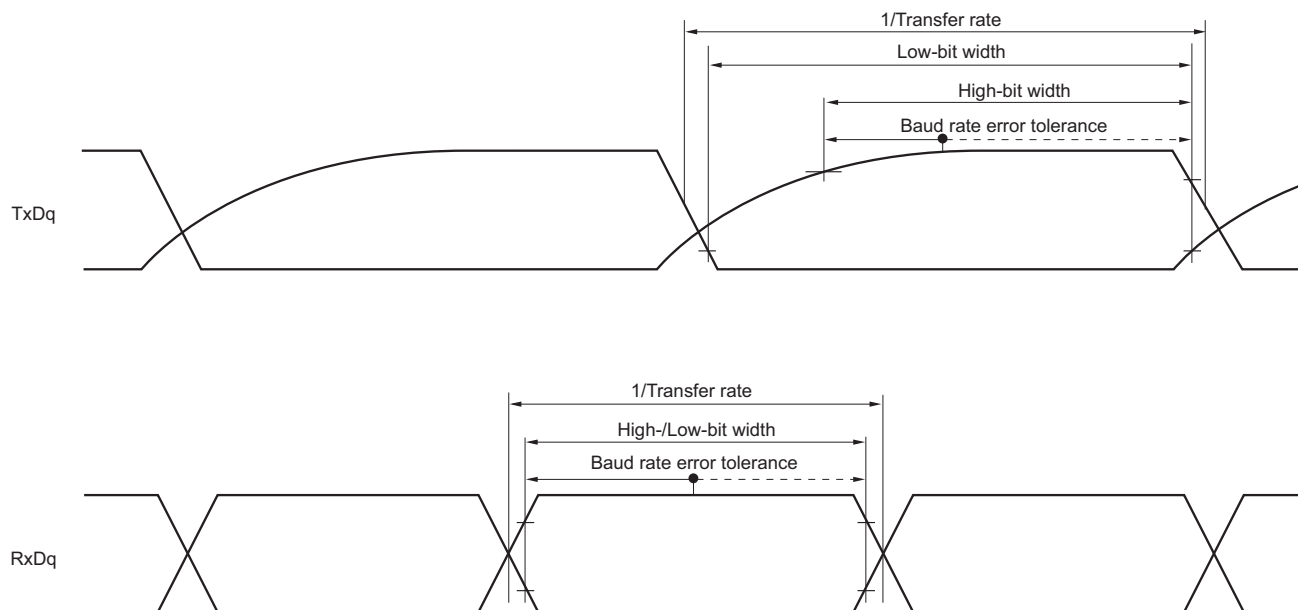
* This value is the theoretical value of the relative difference between the transmission and reception sides.

6. This value as an example is calculated when the conditions described in the "Conditions" column are met. Refer to Note 5 above to calculate the maximum transfer rate under conditions of the customer.

Caution Select the TTL input buffer for the RxDq pin and the N-ch open drain output (V_{DD} tolerance (32- to 52-pin products)/E_{VDD} tolerance (64-pin products)) mode for the TxDq pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V_{IH} and V_{IL}, see the DC characteristics with TTL input buffer selected.

UART mode connection diagram (during communication at different potential)



UART mode bit width (during communication at different potential) (reference)

- Remarks 1.** $R_b[\Omega]$: Communication line (TxDq) pull-up resistance,
 $C_b[F]$: Communication line (TxDq) load capacitance, $V_b[V]$: Communication line voltage
- 2.** q: UART number (q = 0, 1), g: PIM and POM number (g = 1)
- 3.** f_{MCK} : Serial array unit operation clock frequency
 (Operation clock to be set by the serial clock select register m (SPSm) and the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00, 01))

(5) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (master mode, SCKp... internal clock output)**(1/2)****($T_A = -40$ to $+105^\circ\text{C}$, $2.4\text{ V} \leq \text{EV}_{\text{DD}} = \text{V}_{\text{DD}} \leq 5.5\text{ V}$, $\text{V}_{\text{SS}} = \text{EV}_{\text{SS}} = 0\text{ V}$)**

Parameter	Symbol	Conditions	HS (high-speed main) Mode		Unit
			MIN.	MAX.	
SCKp cycle time	t_{KCY1}	$t_{\text{KCY1}} \geq 4/f_{\text{CLK}}$ $4.0\text{ V} \leq \text{EV}_{\text{DD}} \leq 5.5\text{ V}$, $2.7\text{ V} \leq \text{V}_b \leq 4.0\text{ V}$, $C_b = 30\text{ pF}$, $R_b = 1.4\text{ k}\Omega$	600		ns
		$2.7\text{ V} \leq \text{EV}_{\text{DD}} < 4.0\text{ V}$, $2.3\text{ V} \leq \text{V}_b \leq 2.7\text{ V}$, $C_b = 30\text{ pF}$, $R_b = 2.7\text{ k}\Omega$	600		ns
		$2.4\text{ V} \leq \text{EV}_{\text{DD}} < 3.3\text{ V}$, $1.6\text{ V} \leq \text{V}_b \leq 2.0\text{ V}$, $C_b = 30\text{ pF}$, $R_b = 5.5\text{ k}\Omega$	2300		ns
SCKp high-level width	t_{KH1}	$4.0\text{ V} \leq \text{EV}_{\text{DD}} \leq 5.5\text{ V}$, $2.7\text{ V} \leq \text{V}_b \leq 4.0\text{ V}$, $C_b = 30\text{ pF}$, $R_b = 1.4\text{ k}\Omega$	$t_{\text{KCY1}}/2 - 150$		ns
		$2.7\text{ V} \leq \text{EV}_{\text{DD}} < 4.0\text{ V}$, $2.3\text{ V} \leq \text{V}_b \leq 2.7\text{ V}$, $C_b = 30\text{ pF}$, $R_b = 2.7\text{ k}\Omega$	$t_{\text{KCY1}}/2 - 340$		ns
		$2.4\text{ V} \leq \text{EV}_{\text{DD}} < 3.3\text{ V}$, $1.6\text{ V} \leq \text{V}_b \leq 2.0\text{ V}$, $C_b = 30\text{ pF}$, $R_b = 5.5\text{ k}\Omega$	$t_{\text{KCY1}}/2 - 916$		ns
SCKp low-level width	t_{KL1}	$4.0\text{ V} \leq \text{EV}_{\text{DD}} \leq 5.5\text{ V}$, $2.7\text{ V} \leq \text{V}_b \leq 4.0\text{ V}$, $C_b = 30\text{ pF}$, $R_b = 1.4\text{ k}\Omega$	$t_{\text{KCY1}}/2 - 24$		ns
		$2.7\text{ V} \leq \text{EV}_{\text{DD}} < 4.0\text{ V}$, $2.3\text{ V} \leq \text{V}_b \leq 2.7\text{ V}$, $C_b = 30\text{ pF}$, $R_b = 2.7\text{ k}\Omega$	$t_{\text{KCY1}}/2 - 36$		ns
		$2.4\text{ V} \leq \text{EV}_{\text{DD}} < 3.3\text{ V}$, $1.6\text{ V} \leq \text{V}_b \leq 2.0\text{ V}$, $C_b = 30\text{ pF}$, $R_b = 5.5\text{ k}\Omega$	$t_{\text{KCY1}}/2 - 100$		ns

Caution Select the TTL input buffer for the SIp pin and the N-ch open drain output (V_{DD} tolerance (32- to 52-pin products)/ EV_{DD} tolerance (64-pin products)) mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V_{IH} and V_{IL} , see the DC characteristics with TTL input buffer selected.

(5) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (master mode, SCKp... internal clock output)**(2/2)****(T_A = -40 to +105°C, 2.4 V ≤ EV_{DD} = V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS} = 0 V)**

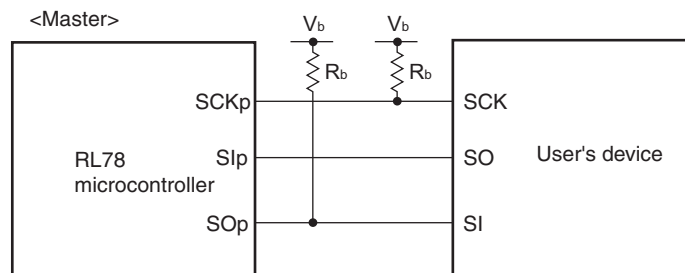
Parameter	Symbol	Conditions	HS (high-speed main) Mode		Unit
			MIN.	MAX.	
Slp setup time (to SCKp↑) ^{Note 1}	t _{SIK1}	4.0 V ≤ EV _{DD} ≤ 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V, C _b = 30 pF, R _b = 1.4 kΩ	162		ns
		2.7 V ≤ EV _{DD} < 4.0 V, 2.3 V ≤ V _b ≤ 2.7 V, C _b = 30 pF, R _b = 2.7 kΩ	354		ns
		2.4 V ≤ EV _{DD} < 3.3 V, 1.6 V ≤ V _b ≤ 2.0 V, C _b = 30 pF, R _b = 5.5 kΩ	958		ns
Slp hold time (from SCKp↑) ^{Note 1}	t _{SIH1}	4.0 V ≤ EV _{DD} ≤ 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V, C _b = 30 pF, R _b = 1.4 kΩ	38		ns
		2.7 V ≤ EV _{DD} < 4.0 V, 2.3 V ≤ V _b ≤ 2.7 V, C _b = 30 pF, R _b = 2.7 kΩ	38		ns
		2.4 V ≤ EV _{DD} < 3.3 V, 1.6 V ≤ V _b ≤ 2.0 V, C _b = 30 pF, R _b = 5.5 kΩ	38		ns
Delay time from SCKp↓ to SOp output ^{Note 1}	t _{KSO1}	4.0 V ≤ EV _{DD} ≤ 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V, C _b = 30 pF, R _b = 1.4 kΩ		200	ns
		2.7 V ≤ EV _{DD} < 4.0 V, 2.3 V ≤ V _b ≤ 2.7 V, C _b = 30 pF, R _b = 2.7 kΩ		390	ns
		2.4 V ≤ EV _{DD} < 3.3 V, 1.6 V ≤ V _b ≤ 2.0 V, C _b = 30 pF, R _b = 2.7 kΩ		966	ns
Slp setup time (to SCKp↓) ^{Note}	t _{SIK1}	4.0 V ≤ EV _{DD} ≤ 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V, C _b = 30 pF, R _b = 1.4 kΩ	88		ns
		2.7 V ≤ EV _{DD} < 4.0 V, 2.3 V ≤ V _b ≤ 2.7 V, C _b = 30 pF, R _b = 2.7 kΩ	88		ns
		2.4 V ≤ EV _{DD} < 3.3 V, 1.6 V ≤ V _b ≤ 2.0 V, C _b = 30 pF, R _b = 5.5 kΩ	220		ns
Slp hold time (from SCKp↓) ^{Note 2}	t _{SIH1}	4.0 V ≤ EV _{DD} ≤ 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V, C _b = 30 pF, R _b = 1.4 kΩ	38		ns
		2.7 V ≤ EV _{DD} < 4.0 V, 2.3 V ≤ V _b ≤ 2.7 V, C _b = 30 pF, R _b = 2.7 kΩ	38		ns
		2.4 V ≤ EV _{DD} < 3.3 V, 1.6 V ≤ V _b ≤ 2.0 V, C _b = 30 pF, R _b = 5.5 kΩ	38		ns
Delay time from SCKp↑ to SOp output ^{Note 2}	t _{KSO1}	4.0 V ≤ EV _{DD} ≤ 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V, C _b = 30 pF, R _b = 1.4 kΩ		50	ns
		2.7 V ≤ EV _{DD} < 4.0 V, 2.3 V ≤ V _b ≤ 2.7 V, C _b = 30 pF, R _b = 2.7 kΩ		50	ns
		2.4 V ≤ EV _{DD} < 3.3 V, 1.6 V ≤ V _b ≤ 2.0 V, C _b = 30 pF, R _b = 5.5 kΩ		50	ns

(Notes, Caution and Remarks are listed on the page after the next page.)

- Notes** 1. When $\text{DAPmn} = 0$ and $\text{CKPmn} = 0$, or $\text{DAPmn} = 1$ and $\text{CKPmn} = 1$.
 2. When $\text{DAPmn} = 0$ and $\text{CKPmn} = 1$, or $\text{DAPmn} = 1$ and $\text{CKPmn} = 0$.

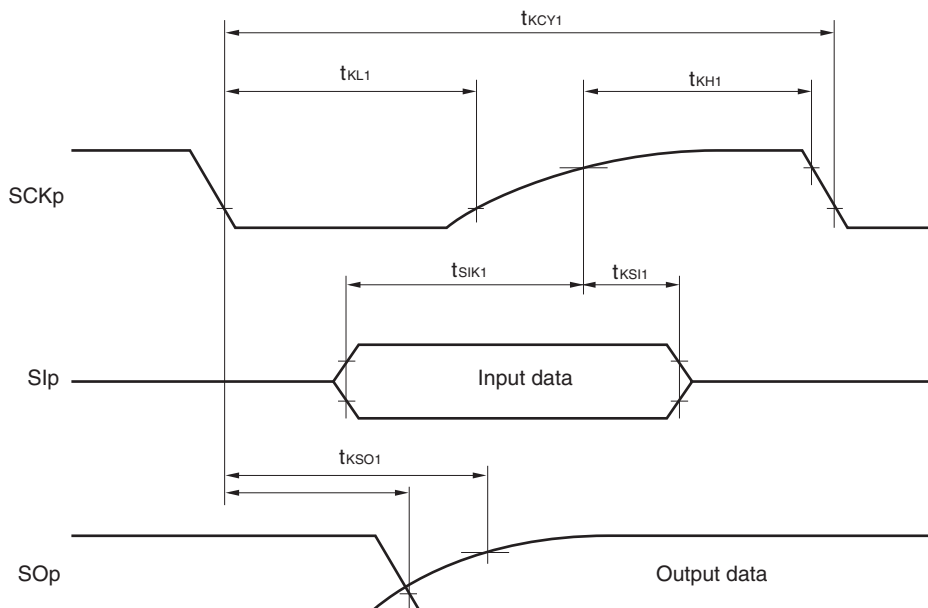
Caution Select the TTL input buffer for the SIp pin and the N-ch open drain output (V_{DD} tolerance (32- to 52-pin products)/ E_{VDD} tolerance (64-pin products)) mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V_{IH} and V_{IL} , see the DC characteristics with TTL input buffer selected.

CSI mode connection diagram (during communication at different potential)

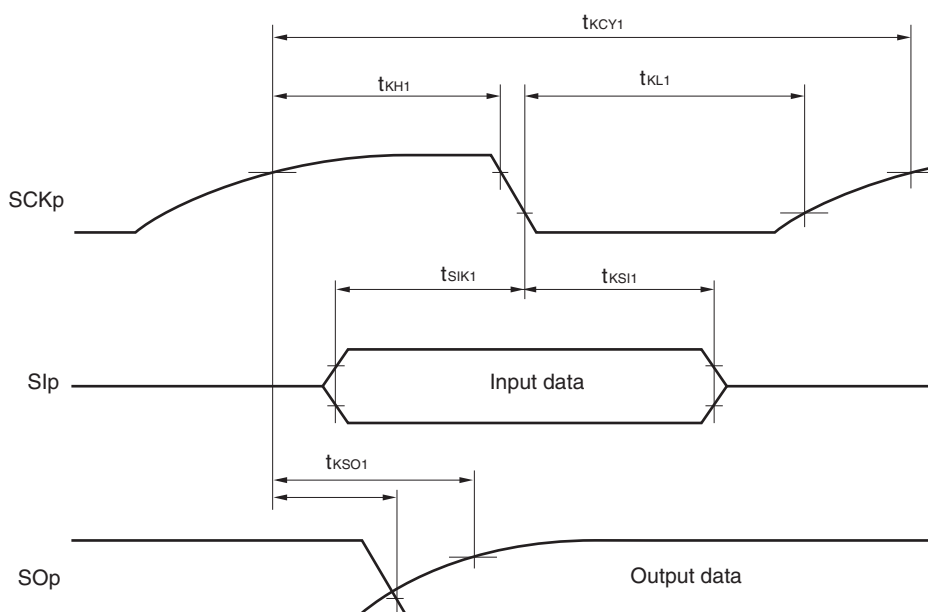


- Remarks** 1. $R_b[\Omega]$: Communication line (SCKp, SOp) pull-up resistance,
 $C_b[\text{F}]$: Communication line (SCKp, SOp) load capacitance, $V_b[\text{V}]$: Communication line voltage
 2. p: CSI number (p = 00, 01), m: Unit number (m = 0), n: Channel number (n = 0, 1),
 g: PIM and POM number (g = 1)
 3. f_{MCK} : Serial array unit operation clock frequency
 (Operation clock to be set by the serial clock select register m (SPSm) and the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00))

CSI mode serial transfer timing (master mode) (during communication at different potential)
(When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.)



CSI mode serial transfer timing (master mode) (during communication at different potential)
(When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.)



Remark p: CSI number (p = 00, 01), m: Unit number (m = 0), n: Channel number (n = 0, 1),
g: PIM and POM number (g = 1)

(6) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (slave mode, SCKp... external clock input)
(T_A = -40 to +105°C, 2.4 V ≤ EV_{DD} = V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS} = 0 V)

Parameter	Symbol	Conditions		HS (high-speed main) Mode		Unit
				MIN.	MAX.	
SCKp cycle time ^{Note 1}	t _{KCY2}	4.0 V ≤ EV _{DD} ≤ 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V	20 MHz < f _{MCK} ≤ 24 MHz	24/f _{MCK}		ns
			8 MHz < f _{MCK} ≤ 20 MHz	20/f _{MCK}		ns
			4 MHz < f _{MCK} ≤ 8 MHz	16/f _{MCK}		ns
			f _{MCK} ≤ 4 MHz	12/f _{MCK}		ns
		2.7 V ≤ EV _{DD} < 4.0 V, 2.3 V ≤ V _b ≤ 2.7 V	20 MHz < f _{MCK} ≤ 24 MHz	32/f _{MCK}		ns
			16 MHz < f _{MCK} ≤ 20 MHz	28/f _{MCK}		ns
			8 MHz < f _{MCK} ≤ 16 MHz	24/f _{MCK}		ns
			4 MHz < f _{MCK} ≤ 8 MHz	16/f _{MCK}		ns
			f _{MCK} ≤ 4 MHz	12/f _{MCK}		ns
		2.4 V ≤ EV _{DD} < 3.3 V, 1.6 V ≤ V _b ≤ 2.0 V	20 MHz < f _{MCK} ≤ 24 MHz	72/f _{MCK}		ns
			16 MHz < f _{MCK} ≤ 20 MHz	64/f _{MCK}		ns
			8 MHz < f _{MCK} ≤ 16 MHz	52/f _{MCK}		ns
			4 MHz < f _{MCK} ≤ 8 MHz	32/f _{MCK}		ns
			f _{MCK} ≤ 4 MHz	20/f _{MCK}		ns
SCKp high-/low-level width	t _{KH2} , t _{KL2}	4.0 V ≤ EV _{DD} ≤ 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V		t _{KCY2} /2 – 24		ns
		2.7 V ≤ EV _{DD} < 4.0 V, 2.3 V ≤ V _b ≤ 2.7 V		t _{KCY2} /2 – 36		ns
		2.4 V ≤ EV _{DD} < 3.3 V, 1.6 V ≤ V _b ≤ 2.0 V		t _{KCY2} /2 – 100		ns
Slp setup time (to SCKp↑) ^{Note 2}	t _{SIK2}	4.0 V ≤ EV _{DD} < 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V		1/f _{MCK} + 40		ns
		2.7 V ≤ EV _{DD} < 4.0 V, 2.3 V ≤ V _b ≤ 2.7 V		1/f _{MCK} + 40		ns
		2.4 V ≤ EV _{DD} < 3.3 V, 1.6 V ≤ V _b ≤ 2.0 V		1/f _{MCK} + 60		ns
Slp hold time (from SCKp↑) ^{Note 3}	t _{KSI2}	4.0 V ≤ EV _{DD} < 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V		1/f _{MCK} + 62		ns
		2.7 V ≤ EV _{DD} < 4.0 V, 2.3 V ≤ V _b ≤ 2.7 V		1/f _{MCK} + 62		ns
		2.4 V ≤ EV _{DD} < 3.3 V, 1.6 V ≤ V _b ≤ 2.0 V		1/f _{MCK} + 62		ns
Delay time from SCKp↓ to SOp output ^{Note 4}	t _{KSO2}	4.0 V ≤ EV _{DD} ≤ 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V, C _b = 30 pF, R _b = 1.4 kΩ			2/f _{MCK} + 240	ns
		2.7 V ≤ EV _{DD} < 4.0 V, 2.3 V ≤ V _b ≤ 2.7 V, C _b = 30 pF, R _b = 2.7 kΩ			2/f _{MCK} + 428	ns
		2.4 V ≤ EV _{DD} < 3.3 V, 1.6 V ≤ V _b ≤ 2.0 V C _b = 30 pF, R _b = 5.5 kΩ			2/f _{MCK} + 1146	ns

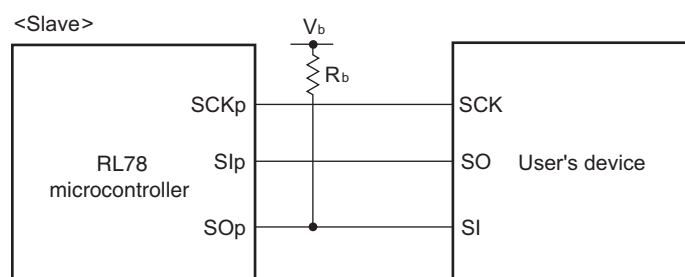
(Notes, Caution and Remarks are listed on the page after the next page.)

Notes 1. Transfer rate in the SNOOZE mode : MAX. 1 Mbps

2. When $\text{DAPmn} = 0$ and $\text{CKPmn} = 0$, or $\text{DAPmn} = 1$ and $\text{CKPmn} = 1$. The Slp setup time becomes “to $\text{SCKp}\downarrow$ ” when $\text{DAPmn} = 0$ and $\text{CKPmn} = 1$, or $\text{DAPmn} = 1$ and $\text{CKPmn} = 0$.
3. When $\text{DAPmn} = 0$ and $\text{CKPmn} = 0$, or $\text{DAPmn} = 1$ and $\text{CKPmn} = 1$. The Slp hold time becomes “from $\text{SCKp}\downarrow$ ” when $\text{DAPmn} = 0$ and $\text{CKPmn} = 1$, or $\text{DAPmn} = 1$ and $\text{CKPmn} = 0$.
4. When $\text{DAPmn} = 0$ and $\text{CKPmn} = 0$, or $\text{DAPmn} = 1$ and $\text{CKPmn} = 1$. The delay time to SOp output becomes “from $\text{SCKp}\uparrow$ ” when $\text{DAPmn} = 0$ and $\text{CKPmn} = 1$, or $\text{DAPmn} = 1$ and $\text{CKPmn} = 0$.

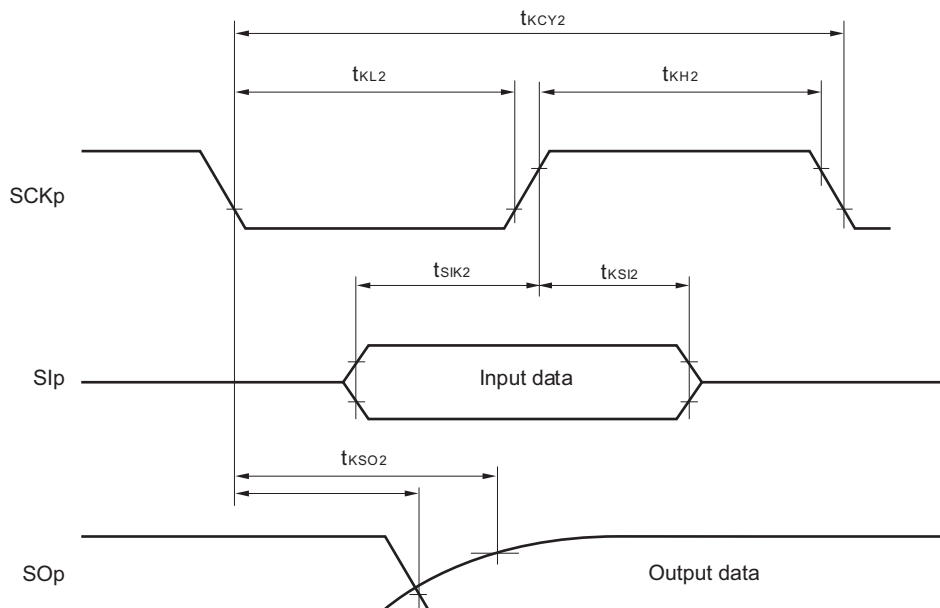
Caution Select the TTL input buffer for the Slp pin and SCKp pin and the N-ch open drain output (V_{DD} tolerance (32- to 52-pin products)/ EV_{DD} tolerance (64-pin products)) mode for the SOp pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V_{IH} and V_{IL} , see the DC characteristics with TTL input buffer selected.

CSI mode connection diagram (during communication at different potential)

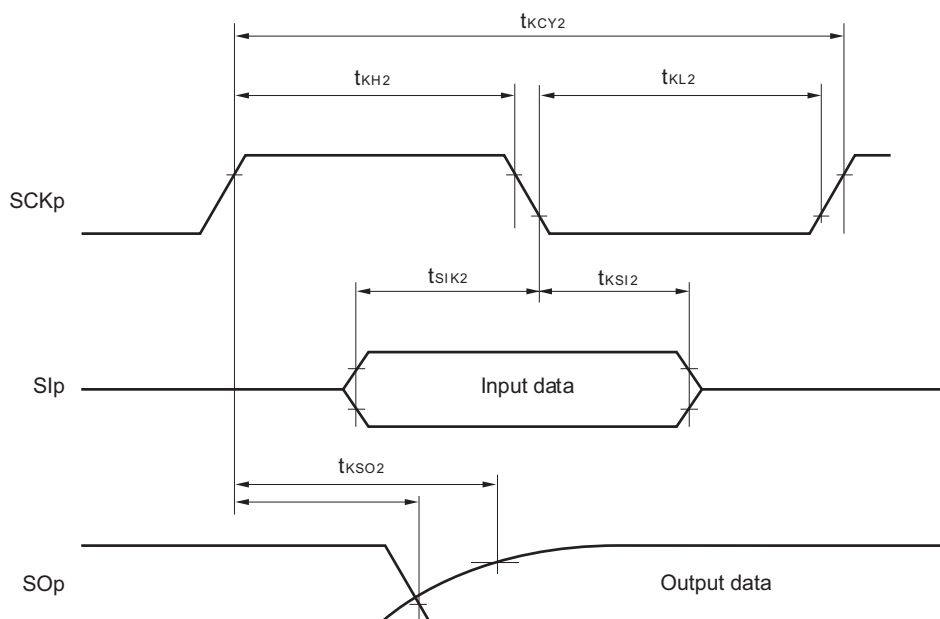


- Remarks** 1. $R_b[\Omega]$: Communication line (SOp) pull-up resistance,
 $C_b[\text{F}]$: Communication line (SOp) load capacitance, $V_b[\text{V}]$: Communication line voltage
2. p: CSI number ($p = 00, 01$), m: Unit number ($m = 0$), n: Channel number ($n = 0, 1$),
g: PIM and POM number ($g = 1$)
 3. f_{MCK} : Serial array unit operation clock frequency
(Operation clock to be set by the serial clock select register m (SPSM) and the CKSMn bit of serial mode register mn (SMRMn). m: Unit number, n: Channel number ($mn = 00, 01$))

CSI mode serial transfer timing (slave mode) (during communication at different potential)
(When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.)



CSI mode serial transfer timing (slave mode) (during communication at different potential)
(When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.)



Remark p: CSI number (p = 00, 01), m: Unit number (m = 0),
 n: Channel number (n = 0, 1), g: PIM and POM number (g = 1)

3.5.2 Serial interface IICA

(1) I²C standard mode(T_A = -40 to +105°C, 2.4 V ≤ EV_{DD} = V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS} = 0 V)

Parameter	Symbol	Conditions	HS (high-speed main) Mode		Unit
			MIN.	MAX.	
SCLA0 clock frequency	f _{SCL}	Standard mode: 2.7 V ≤ EV _{DD} ≤ 5.5 V	0	100	kHz
		f _{CLK} ≥ 1 MHz 2.4 V ≤ EV _{DD} ≤ 5.5 V	0	100	kHz
Setup time of restart condition	t _{SU:STA}	2.7 V ≤ EV _{DD} ≤ 5.5 V	4.7		μs
		2.4 V ≤ EV _{DD} ≤ 5.5 V	4.7		μs
Hold time ^{Note 1}	t _{HD:STA}	2.7 V ≤ EV _{DD} ≤ 5.5 V	4.0		μs
		2.4 V ≤ EV _{DD} ≤ 5.5 V	4.0		μs
Hold time when SCLA0 = "L"	t _{LOW}	2.7 V ≤ EV _{DD} ≤ 5.5 V	4.7		μs
		2.4 V ≤ EV _{DD} ≤ 5.5 V	4.7		μs
Hold time when SCLA0 = "H"	t _{HIGH}	2.7 V ≤ EV _{DD} ≤ 5.5 V	4.0		μs
		2.4 V ≤ EV _{DD} ≤ 5.5 V	4.0		μs
Data setup time (reception)	t _{SU:DAT}	2.7 V ≤ EV _{DD} ≤ 5.5 V	250		ns
		2.4 V ≤ EV _{DD} ≤ 5.5 V	250		ns
Data hold time (transmission) ^{Note 2}	t _{HD:DAT}	2.7 V ≤ EV _{DD} ≤ 5.5 V	0	3.45	μs
		2.4 V ≤ EV _{DD} ≤ 5.5 V	0	3.45	μs
Setup time of stop condition	t _{SU:STO}	2.7 V ≤ EV _{DD} ≤ 5.5 V	4.0		μs
		2.4 V ≤ EV _{DD} ≤ 5.5 V	4.0		μs
Bus-free time	t _{BUF}	2.7 V ≤ EV _{DD} ≤ 5.5 V	4.7		μs
		2.4 V ≤ EV _{DD} ≤ 5.5 V	4.7		μs

Notes 1. The first clock pulse is generated after this period when the start/restart condition is detected.2. The maximum value (MAX.) of t_{HD:DAT} is during normal transfer and a wait state is inserted in the ACK (acknowledge) timing.**Remark** The maximum value of C_b (communication line capacitance) and the value of R_b (communication line pull-up resistor) at that time in each mode are as follows.Standard mode: C_b = 400 pF, R_b = 2.7 kΩ

(2) I²C fast mode(T_A = -40 to +105°C, 2.4 V ≤ EV_{DD} = V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS} = 0 V)

Parameter	Symbol	Conditions		HS (high-speed main) Mode		Unit
				MIN.	MAX.	
SCLA0 clock frequency	f _{SCL}	Fast mode:	2.7 V ≤ EV _{DD} ≤ 5.5 V	0	400	kHz
		f _{CLK} ≥ 3.5 MHz	2.4 V ≤ EV _{DD} ≤ 5.5 V	0	400	
Setup time of restart condition	t _{SU:STA}	2.7 V ≤ EV _{DD} ≤ 5.5 V		0.6		μs
		2.4 V ≤ EV _{DD} ≤ 5.5 V		0.6		
Hold time ^{Note 1}	t _{HD:STA}	2.7 V ≤ EV _{DD} ≤ 5.5 V		0.6		μs
		2.4 V ≤ EV _{DD} ≤ 5.5 V		0.6		
Hold time when SCLA0 = "L"	t _{LOW}	2.7 V ≤ EV _{DD} ≤ 5.5 V		1.3		μs
		2.4 V ≤ EV _{DD} ≤ 5.5 V		1.3		
Hold time when SCLA0 = "H"	t _{HIGH}	2.7 V ≤ EV _{DD} ≤ 5.5 V		0.6		μs
		2.4 V ≤ EV _{DD} ≤ 5.5 V		0.6		
Data setup time (reception)	t _{SU:DAT}	2.7 V ≤ EV _{DD} ≤ 5.5 V		100		ns
		2.4 V ≤ EV _{DD} ≤ 5.5 V		100		
Data hold time (transmission) ^{Note 2}	t _{HD:DAT}	2.7 V ≤ EV _{DD} ≤ 5.5 V		0	0.9	μs
		2.4 V ≤ EV _{DD} ≤ 5.5 V		0	0.9	
Setup time of stop condition	t _{SU:STO}	2.7 V ≤ EV _{DD} ≤ 5.5 V		0.6		μs
		2.4 V ≤ EV _{DD} ≤ 5.5 V		0.6		
Bus-free time	t _{BUF}	2.7 V ≤ EV _{DD} ≤ 5.5 V		1.3		μs
		2.4 V ≤ EV _{DD} ≤ 5.5 V		1.3		

- Notes**
1. The first clock pulse is generated after this period when the start/restart condition is detected.
 2. The maximum value (MAX.) of t_{HD:DAT} is during normal transfer and a wait state is inserted in the ACK (acknowledge) timing.

Remark The maximum value of C_b (communication line capacitance) and the value of R_b (communication line pull-up resistor) at that time in each mode are as follows.

Fast mode: C_b = 320 pF, R_b = 1.1 kΩ

3.6 Analog Characteristics

3.6.1 A/D converter characteristics

Classification of A/D converter characteristics

Input channel	Reference Voltage		
	Reference voltage (+) = AV _{REFP} Reference voltage (-) = AV _{REFM}	Reference voltage (+) = V _{DD} Reference voltage (-) = V _{SS}	Reference voltage (+) = V _{BGR} Reference voltage (-) = AV _{REFM}
ANI0, ANI1	–	Refer to 3.6.1 (3).	Refer to 3.6.1 (4).
ANI16 to ANI23	Refer to 3.6.1 (2).		
Internal reference voltage Temperature sensor output voltage	Refer to 3.6.1 (1).		–

(1) When reference voltage (+) = AV_{REFP}/ANI0 (ADREFP1 = 0, ADREFP0 = 1), reference voltage (-) = AV_{REFM}/ANI1 (ADREFM = 1), target pin : internal reference voltage, and temperature sensor output voltage

(T_A = -40 to +105°C, 2.4 V ≤ EV_{DD} = V_{DD} ≤ 5.5 V, 2.4 V ≤ AV_{REFP} ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS} = 0 V, Reference voltage (+) = AV_{REFP}, Reference voltage (-) = AV_{REFM} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Resolution	RES		8		10	bit
Overall error ^{Note 1}	AINL	10-bit resolution AV _{REFP} = V _{DD} ^{Note 3}	2.4 V ≤ AV _{REFP} ≤ 5.5 V	1.2	±3.5	LSB
Conversion time	t _{CONV}	10-bit resolution Target pin: Internal reference voltage, and temperature sensor output voltage (HS (high-speed main) mode)	3.6 V ≤ V _{DD} ≤ 5.5 V	2.375	39	μs
			2.7 V ≤ V _{DD} ≤ 5.5 V	3.5625	39	μs
			2.4 V ≤ V _{DD} ≤ 5.5 V	17	39	μs
Zero-scale error ^{Notes 1, 2}	E _{ZS}	10-bit resolution AV _{REFP} = V _{DD} ^{Note 3}	1.8 V ≤ AV _{REFP} ≤ 5.5 V		±0.25	%FSR
Full-scale error ^{Notes 1, 2}	E _{FS}	10-bit resolution AV _{REFP} = V _{DD} ^{Note 3}	1.8 V ≤ AV _{REFP} ≤ 5.5 V		±0.25	%FSR
Integral linearity error ^{Note 1}	ILE	10-bit resolution AV _{REFP} = V _{DD} ^{Note 3}	1.8 V ≤ AV _{REFP} ≤ 5.5 V		±2.5	LSB
Differential linearity error ^{Note 1}	DLE	10-bit resolution AV _{REFP} = V _{DD} ^{Note 3}	1.8 V ≤ AV _{REFP} ≤ 5.5 V		±1.5	LSB
Analog input voltage	V _{AIN}	Internal reference voltage (2.4 V ≤ V _{DD} ≤ 5.5 V, HS (high-speed main) mode)	V _{BGR} ^{Note 4}			V
		Temperature sensor output voltage (2.4 V ≤ V _{DD} ≤ 5.5 V, HS (high-speed main) mode)	V _{TMPS25} ^{Note 4}			V

Notes 1. Excludes quantization error (±1/2 LSB).

2. This value is indicated as a ratio (%FSR) to the full-scale value.

3. When AV_{REFP} < V_{DD}, the MAX. values are as follows.

Overall error: Add ±1.0 LSB to the MAX. value when AV_{REFP} = V_{DD}.

Zero-scale error/Full-scale error: Add ±0.05%FSR to the MAX. value when AV_{REFP} = V_{DD}.

Integral linearity error/ Differential linearity error: Add ±0.5 LSB to the MAX. value when AV_{REFP} = V_{DD}.

4. Refer to 3.6.2 Temperature sensor/internal reference voltage characteristics.

(2) When reference voltage (+) = $AV_{REFP}/ANI0$ (ADREFP1 = 0, ADREFP0 = 1), reference voltage (-) = $AV_{REFM}/ANI1$ (ADREFM = 1), target pin : ANI16 to ANI23

(T_A = -40 to +105°C, 2.4 V ≤ EV_{DD} = V_{DD} ≤ 5.5 V, 2.4 V ≤ AV_{REFP} ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS} = 0 V, Reference voltage (+) = AV_{REFP}, Reference voltage (-) = AV_{REFM} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Resolution	RES		8		10	bit
Overall error ^{Note 1}	AINL	10-bit resolution AV _{REFP} = EV _{DD} = V _{DD} ^{Note 3}	2.4 V ≤ AV _{REFP} ≤ 5.5 V		±5.0	LSB
Conversion time	t _{CONV}	10-bit resolution AV _{REFP} = EV _{DD} = V _{DD} ^{Note 3}	3.6 V ≤ V _{DD} ≤ 5.5 V	2.125	39	μs
			2.7 V ≤ V _{DD} ≤ 5.5 V	3.1875	39	μs
			2.4 V ≤ V _{DD} ≤ 5.5 V	17	39	μs
Zero-scale error ^{Notes 1, 2}	E _{ZS}	10-bit resolution AV _{REFP} = EV _{DD} = V _{DD} ^{Note 3}	2.4 V ≤ AV _{REFP} ≤ 5.5 V		±0.35	%FSR
Full-scale error ^{Notes 1, 2}	E _{FS}	10-bit resolution AV _{REFP} = EV _{DD} = V _{DD} ^{Note 3}	2.4 V ≤ AV _{REFP} ≤ 5.5 V		±0.35	%FSR
Integral linearity error ^{Note 1}	ILE	10-bit resolution AV _{REFP} = EV _{DD} = V _{DD} ^{Note 3}	2.4 V ≤ AV _{REFP} ≤ 5.5 V		±3.5	LSB
Differential linearity error ^{Note 1}	DLE	10-bit resolution AV _{REFP} = EV _{DD} = V _{DD} ^{Note 3}	2.4 V ≤ AV _{REFP} ≤ 5.5 V		±2.0	LSB
Analog input voltage	V _{AIN}	ANI16 to ANI23	0		AV _{REFP} and EV _{DD}	V

Notes 1. Excludes quantization error (±1/2 LSB).

2. This value is indicated as a ratio (%FSR) to the full-scale value.

3. When AV_{REFP} < EV_{DD} = V_{DD}, the MAX. values are as follows.

Overall error: Add ±4.0 LSB to the MAX. value when AV_{REFP} = V_{DD}.

Zero-scale error/Full-scale error: Add ±0.20%FSR to the MAX. value when AV_{REFP} = V_{DD}.

Integral linearity error/ Differential linearity error: Add ±2.0 LSB to the MAX. value when AV_{REFP} = V_{DD}.

(3) When reference voltage (+) = V_{DD} (ADREFP1 = 0, ADREFP0 = 0), reference voltage (-) = V_{SS} (ADREFM = 0), target pin : ANI0, ANI1, ANI16 to ANI23, internal reference voltage, and temperature sensor output voltage

(T_A = -40 to +105°C, 2.4 V ≤ EV_{DD} = V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS} = 0 V, Reference voltage (+) = V_{DD}, Reference voltage (-) = V_{SS})

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Resolution	RES			8		10	bit
Overall error ^{Note 1}	AINL	10-bit resolution	2.4 V ≤ V _{DD} ≤ 5.5 V		1.2	±7.0	LSB
Conversion time	t _{CONV}	10-bit resolution	3.6 V ≤ V _{DD} ≤ 5.5 V	2.125		39	μs
			2.7 V ≤ V _{DD} ≤ 5.5 V	3.1875		39	μs
			2.4 V ≤ V _{DD} ≤ 5.5 V	17		39	μs
		10-bit resolution Target pin: Internal reference voltage, and temperature sensor output voltage (HS (high-speed main) mode)	3.6 V ≤ V _{DD} ≤ 5.5 V	2.375		39	μs
			2.7 V ≤ V _{DD} ≤ 5.5 V	3.5625		39	μs
			2.4 V ≤ V _{DD} ≤ 5.5 V	17		39	μs
Zero-scale error ^{Notes 1, 2}	E _{ZS}	10-bit resolution	2.4 V ≤ V _{DD} ≤ 5.5 V			±0.60	%FSR
Full-scale error ^{Notes 1, 2}	E _{FS}	10-bit resolution	2.4 V ≤ V _{DD} ≤ 5.5 V			±0.60	%FSR
Integral linearity error ^{Note 1}	ILE	10-bit resolution	2.4 V ≤ V _{DD} ≤ 5.5 V			±4.0	LSB
Differential linearity error ^{Note 1}	DLE	10-bit resolution	2.4 V ≤ V _{DD} ≤ 5.5 V			±2.0	LSB
Analog input voltage	V _{AIN}	ANI0, ANI1		0		V _{DD}	V
		ANI16 to ANI23		0		EV _{DD}	V
		Internal reference voltage output (2.4 V ≤ V _{DD} ≤ 5.5 V, HS (high-speed main) mode)		V _{BGR} ^{Note 3}			V
		Temperature sensor output voltage (2.4 V ≤ V _{DD} ≤ 5.5 V, HS (high-speed main) mode)		V _{TMPS25} ^{Note 3}			V

Notes 1. Excludes quantization error (±1/2 LSB).

2. This value is indicated as a ratio (%FSR) to the full-scale value.

3. Refer to 3.6.2 Temperature sensor/internal reference voltage characteristics.

(4) When reference voltage (+) = Internal reference voltage (ADREFP1 = 1, ADREFP0 = 0), reference voltage (-) = AV_{REFM}/ANI1 (ADREFM = 1), target pin : ANI0, ANI16 to ANI23

(T_A = -40 to +105°C, 2.4 V ≤ EV_{DD} = V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS} = 0 V, Reference voltage (+) = V_{BGR}^{Note 3}, Reference voltage (-) = AV_{REFM}^{Note 4} = 0 V, HS (high-speed main) mode)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Resolution	RES			8			bit
Conversion time	t _{CONV}	8-bit resolution	2.4 V ≤ V _{DD} ≤ 5.5 V	17		39	μs
Zero-scale error ^{Notes 1, 2}	E _{zs}	8-bit resolution	2.4 V ≤ V _{DD} ≤ 5.5 V			±0.60	%FSR
Integral linearity error ^{Note 1}	ILE	8-bit resolution	2.4 V ≤ V _{DD} ≤ 5.5 V			±2.0	LSB
Differential linearity error ^{Note 1}	DLE	8-bit resolution	2.4 V ≤ V _{DD} ≤ 5.5 V			±1.0	LSB
Analog input voltage	V _{AIN}			0		V _{BGR} ^{Note 3}	V

Notes 1. Excludes quantization error (±1/2 LSB).

2. This value is indicated as a ratio (%FSR) to the full-scale value.

3. Refer to **3.6.2 Temperature sensor/internal reference voltage characteristics**.

4. When reference voltage (-) = V_{SS}, the MAX. values are as follows.

Zero-scale error: Add ±0.35%FSR to the MAX. value when reference voltage (-) = AV_{REFM}.

Integral linearity error: Add ±0.5 LSB to the MAX. value when reference voltage (-) = AV_{REFM}.

Differential linearity error: Add ±0.2 LSB to the MAX. value when reference voltage (-) = AV_{REFM}.

3.6.2 Temperature sensor/internal reference voltage characteristics

(TA = -40 to $+105^{\circ}\text{C}$, $2.4\text{ V} \leq \text{EV}_{\text{DD}} = \text{V}_{\text{DD}} \leq 5.5\text{ V}$, $\text{V}_{\text{SS}} = \text{EV}_{\text{SS}} = 0\text{ V}$, HS (high-speed main) mode)

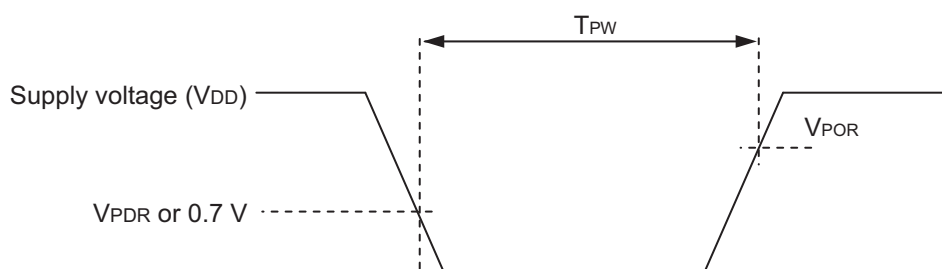
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Temperature sensor output voltage	V_{TMPS25}	Setting ADS register = 80H, $T_A = +25^{\circ}\text{C}$		1.05		V
Internal reference voltage	V_{BGR}	Setting ADS register = 81H	1.38	1.45	1.5	V
Temperature coefficient	F_{VTMPS}	Temperature sensor that depends on the temperature		-3.6		mV/ $^{\circ}\text{C}$
Operation stabilization wait time	t_{AMP}		5			μs

3.6.3 POR circuit characteristics

(TA = -40 to $+105^{\circ}\text{C}$, $\text{V}_{\text{SS}} = 0\text{ V}$)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Detection voltage	V_{POR}	Power supply rise time	1.45	1.51	1.57	V
	V_{PDR}	Power supply fall time	1.44	1.50	1.56	V
Minimum pulse width	T_{PW}		300			μs

Note Minimum time required for a POR reset when V_{DD} exceeds below V_{PDR} . This is also the minimum time required for a POR reset from when V_{DD} exceeds below 0.7 V to when V_{DD} exceeds V_{POR} while STOP mode is entered or the main system clock is stopped through setting bit 0 (HISTOP) and bit 7 (MSTOP) in the clock operation status control register (CSC).



3.6.4 LVD circuit characteristics

(T_A = -40 to +105°C, V_{PDR} ≤ EV_{DD} = V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS} = 0 V)

Parameter		Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Detection voltage	Supply voltage level	VLVD0	Power supply rise time	3.90	4.06	4.22	V
			Power supply fall time	3.83	3.98	4.13	V
		VLVD1	Power supply rise time	3.60	3.75	3.90	V
			Power supply fall time	3.53	3.67	3.81	V
		VLVD2	Power supply rise time	3.01	3.13	3.25	V
			Power supply fall time	2.94	3.06	3.18	V
		VLVD3	Power supply rise time	2.90	3.02	3.14	V
			Power supply fall time	2.85	2.96	3.07	V
		VLVD4	Power supply rise time	2.81	2.92	3.03	V
			Power supply fall time	2.75	2.86	2.97	V
		VLVD5	Power supply rise time	2.70	2.81	2.92	V
			Power supply fall time	2.64	2.75	2.86	V
		VLVD6	Power supply rise time	2.61	2.71	2.81	V
			Power supply fall time	2.55	2.65	2.75	V
		VLVD7	Power supply rise time	2.51	2.61	2.71	V
			Power supply fall time	2.45	2.55	2.65	V
Minimum pulse width		tLW		300			μs
Detection delay time						300	μs

LVD Detection Voltage of Interrupt & Reset Mode

(T_A = -40 to +105°C, V_{PDR} ≤ EV_{DD} = V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS} = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Interrupt and reset mode	V _{LVDD0}	V _{POC2} , V _{POC1} , V _{POC0} = 0, 1, 1, falling reset voltage		2.64	2.75	2.86	V
	V _{LVDD1}	LVIS1, LVIS0 = 1, 0	Rising release reset voltage	2.81	2.92	3.03	V
			Falling interrupt voltage	2.75	2.86	2.97	V
	V _{LVDD2}	LVIS1, LVIS0 = 0, 1	Rising release reset voltage	2.90	3.02	3.14	V
			Falling interrupt voltage	2.85	2.96	3.07	V
	V _{LVDD3}	LVIS1, LVIS0 = 0, 0	Rising release reset voltage	3.90	4.06	4.22	V
			Falling interrupt voltage	3.83	3.98	4.13	V

3.6.5 Power supply voltage rising slope characteristics

(T_A = -40 to +105°C, V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Power supply voltage rising slope	S _{VDD}				54	V/ms

Caution Make sure to keep the internal reset state by the LVD circuit or an external reset until V_{DD} reaches the operating voltage range shown in 31.4 AC Characteristics.

3.7 LCD Characteristics

3.7.1 Resistance division method

(1) Static display mode

(T_A = -40 to +105°C, V_{L4} (MIN.) ≤ V_{DD}^{Note} ≤ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
LCD drive voltage	V _{L4}		2.0		V _{DD}	V

Note Must be 2.4 V or higher.

(2) 1/2 bias method, 1/4 bias method

(T_A = -40 to +105°C, V_{L4} (MIN.) ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
LCD drive voltage	V _{L4}		2.7		V _{DD}	V

(3) 1/3 bias method

(T_A = -40 to +105°C, V_{L4} (MIN.) ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
LCD drive voltage	V _{L4}		2.5		V _{DD}	V

3.7.2 Internal voltage boosting method

(1) 1/3 bias method

(T_A = -40 to +105°C, 2.4 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit	
LCD output voltage variation range	V _{L1}	C1 to C4 ^{Note 1} = 0.47 μF	VLCD = 04H	0.90	1.00	1.08	V
			VLCD = 05H	0.95	1.05	1.13	V
			VLCD = 06H	1.00	1.10	1.18	V
			VLCD = 07H	1.05	1.15	1.23	V
			VLCD = 08H	1.10	1.20	1.28	V
			VLCD = 09H	1.15	1.25	1.33	V
			VLCD = 0AH	1.20	1.30	1.38	V
			VLCD = 0BH	1.25	1.35	1.43	V
			VLCD = 0CH	1.30	1.40	1.48	V
			VLCD = 0DH	1.35	1.45	1.53	V
			VLCD = 0EH	1.40	1.50	1.58	V
			VLCD = 0FH	1.45	1.55	1.63	V
			VLCD = 10H	1.50	1.60	1.68	V
			VLCD = 11H	1.55	1.65	1.73	V
			VLCD = 12H	1.60	1.70	1.78	V
			VLCD = 13H	1.65	1.75	1.83	V
Doubler output voltage	V _{L2}	C1 to C4 ^{Note 1} = 0.47 μF	2 V _{L1} -0.1	2 V _{L1}	2 V _{L1}	V	
Tripler output voltage	V _{L4}	C1 to C4 ^{Note 1} = 0.47 μF	3 V _{L1} -0.15	3 V _{L1}	3 V _{L1}	V	
Reference voltage setup time ^{Note 2}	t _{WAIT1}		5			ms	
Voltage boost wait time ^{Note 3}	t _{WAIT2}	C1 to C4 ^{Note 1} = 0.47 μF	500			ms	

Notes 1. This is a capacitor that is connected between voltage pins used to drive the LCD.

C1: A capacitor connected between CAPH and CAPL

C2: A capacitor connected between V_{L1} and GNDC3: A capacitor connected between V_{L2} and GNDC4: A capacitor connected between V_{L4} and GND

C1 = C2 = C3 = C4 = 0.47 μF±30%

- This is the time required to wait from when the reference voltage is specified by using the VLCD register (or when the internal voltage boosting method is selected [by setting the MDSET1 and MDSET0 bits of the LCDM0 register to 01B] if the default value reference voltage is used) until voltage boosting starts (VLCON = 1).
- This is the wait time from when voltage boosting is started (VLCON = 1) until display is enabled (LCDON = 1).

(2) 1/4 bias method

(T_A = -40 to +105°C, 2.4 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
LCD output voltage variation range	V _{L1} ^{Note 4}	C1 to C5 ^{Note 1} = 0.47 μF	VLCD = 04H	0.90	1.00	1.08	V
			VLCD = 05H	0.95	1.05	1.13	V
			VLCD = 06H	1.00	1.10	1.18	V
			VLCD = 07H	1.05	1.15	1.23	V
			VLCD = 08H	1.10	1.20	1.28	V
			VLCD = 09H	1.15	1.25	1.33	V
			VLCD = 0AH	1.20	1.30	1.38	V
			VLCD = 0BH	1.25	1.35	1.43	V
			VLCD = 0CH	1.30	1.40	1.48	V
			VLCD = 0DH	1.35	1.45	1.53	V
			VLCD = 0EH	1.40	1.50	1.58	V
			VLCD = 0FH	1.45	1.55	1.63	V
			VLCD = 10H	1.50	1.60	1.68	V
			VLCD = 11H	1.55	1.65	1.73	V
			VLCD = 12H	1.60	1.70	1.78	V
			VLCD = 13H	1.65	1.75	1.83	V
Doubler output voltage	V _{L2}	C1 to C5 ^{Note 1} = 0.47 μF	2 V _{L1} – 0.08	2 V _{L1}	2 V _{L1}	V	
Tripler output voltage	V _{L3}	C1 to C5 ^{Note 1} = 0.47 μF	3 V _{L1} – 0.12	3 V _{L1}	3 V _{L1}	V	
Quadruply output voltage	V _{L4} ^{Note 4}	C1 to C5 ^{Note 1} = 0.47 μF	4 V _{L1} – 0.16	4 V _{L1}	4 V _{L1}	V	
Reference voltage setup time ^{Note 2}	t _{VWAIT1}		5			ms	
Voltage boost wait time ^{Note 3}	t _{VWAIT2}	C1 to C5 ^{Note 1} = 0.47 μF	500			ms	

Notes 1. This is a capacitor that is connected between voltage pins used to drive the LCD.

C1: A capacitor connected between CAPH and CAPL

C2: A capacitor connected between V_{L1} and GNDC3: A capacitor connected between V_{L2} and GNDC4: A capacitor connected between V_{L3} and GNDC5: A capacitor connected between V_{L4} and GND

C1 = C2 = C3 = C4 = C5 = 0.47 μF ± 30%

2. This is the time required to wait from when the reference voltage is specified by using the VLCD register (or when the internal voltage boosting method is selected [by setting the MDSET1 and MDSET0 bits of the LCDM0 register to 01B] if the default value reference voltage is used) until voltage boosting starts (VLCON = 1).
3. This is the wait time from when voltage boosting is started (VLCON = 1) until display is enabled (LCDON = 1).
4. V_{L4} must be 5.5 V or lower.

3.7.3 Capacitor split method

1/3 bias method

(T_A = -40 to +105°C, 2.4 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
V _{L4} voltage	V _{L4}	C1 to C4 = 0.47 μF ^{Note 2}		V _{DD}		V
V _{L2} voltage	V _{L2}	C1 to C4 = 0.47 μF ^{Note 2}	2/3 V _{L4} - 0.1	2/3 V _{L4}	2/3 V _{L4} + 0.1	V
V _{L1} voltage	V _{L1}	C1 to C4 = 0.47 μF ^{Note 2}	1/3 V _{L4} - 0.1	1/3 V _{L4}	1/3 V _{L4} + 0.1	V
Capacitor split wait time ^{Note 1}	t _{WAIT}		100			ms

Notes 1. This is the wait time from when voltage bucking is started (VLCON = 1) until display is enabled (LCDON = 1).

2. This is a capacitor that is connected between voltage pins used to drive the LCD.

C1: A capacitor connected between CAPH and CAPL

C2: A capacitor connected between V_{L1} and GND

C3: A capacitor connected between V_{L2} and GND

C4: A capacitor connected between V_{L4} and GND

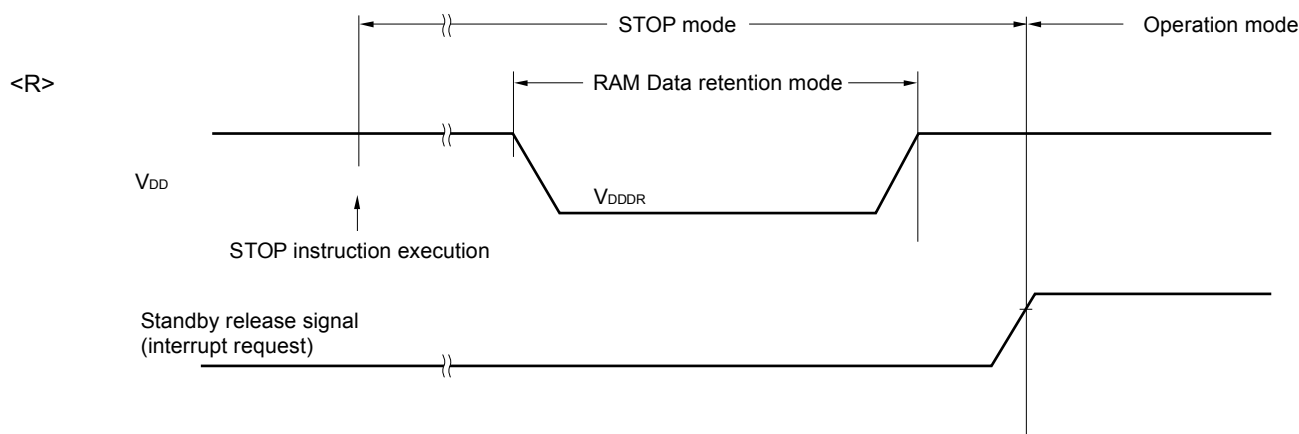
C1 = C2 = C3 = C4 = 0.47 μF±30%

<R> 3.8 RAM Data Retention Characteristics

(T_A = -40 to +105°C, V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Data retention supply voltage	V _{DDDR}		1.44 ^{Note}		5.5	V

<R> **Note** This depends on the POR detection voltage. For a falling voltage, data in RAM are retained until the voltage reaches the level that triggers a POR reset but not once it reaches the level at which a POR reset is generated.



3.9 Flash Memory Programming Characteristics

(T_A = -40 to +105°C, 2.4 V ≤ EV_{DD} = V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
System clock frequency	f _{CLK}	1.8 V ≤ V _{DD} ≤ 5.5 V	1		24	MHz
<R> Number of code flash rewrites Notes 1, 2, 3	C _{enwr}	Retained for 20 years T _A = 85°C ^{Note 4}	1,000			Times
<R> Number of data flash rewrites Notes 1, 2, 3		Retained for 1 year T _A = 25°C ^{Note 4}		1,000,000		
<R>		Retained for 5 years T _A = 85°C ^{Note 4}	100,000			
<R>		Retained for 20 years T _A = 85°C ^{Note 4}	10,000			

Notes 1. 1 erase + 1 write after the erase is regarded as 1 rewrite.

The retaining years are until next rewrite after the rewrite.

2. When using flash memory programmer and Renesas Electronics self programming library

3. This characteristic indicates the flash memory characteristic and based on Renesas Electronics reliability test.

<R> **4.** This temperature is the average value at which data are retained.

3.10 Dedicated Flash Memory Programmer Communication (UART)

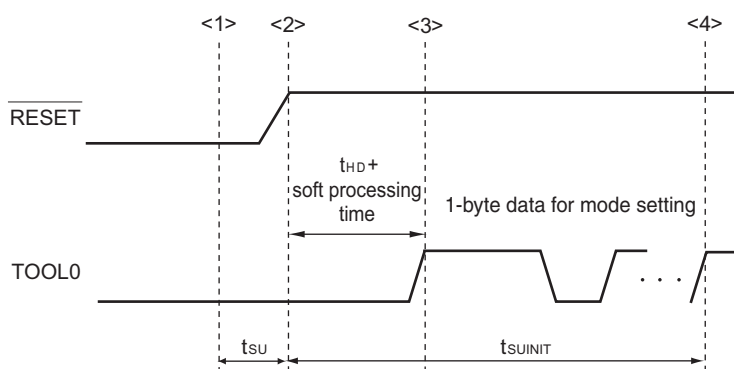
(T_A = -40 to +105°C, 2.4 V ≤ EV_{DD} = V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Transfer rate		During flash memory programming	115,200		1,000,000	bps

3.11 Timing Specifications for Switching Flash Memory Programming Modes

(T_A = -40 to $+105^{\circ}\text{C}$, $2.4\text{ V} \leq \text{EV}_{\text{DD}} = \text{V}_{\text{DD}} \leq 5.5\text{ V}$, $\text{V}_{\text{SS}} = \text{EV}_{\text{SS}} = 0\text{ V}$)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Time to complete the communication for the initial setting after the external reset is released	t _{SUINIT}	POR and LVD reset must be released before the external reset is released.			100	ms
Time to release the external reset after the TOOL0 pin is set to the low level	t _{SU}	POR and LVD reset must be released before the external reset is released.	10			μs
Time to hold the TOOL0 pin at the low level after the external reset is released (excluding the processing time of the firmware to control the flash memory)	t _{HD}	POR and LVD reset must be released before the external reset is released.	1			ms



<1> The low level is input to the TOOL0 pin.

<2> The external reset is released (POR and LVD reset must be released before the external reset is released.).

<3> The TOOL0 pin is set to the high level.

<4> Setting of the flash memory programming mode by UART reception and complete the baud rate setting.

Remark t_{SUINIT}: Communication for the initial setting must be completed within 100 ms after the external reset is released during this period.

t_{SU}: Time to release the external reset after the TOOL0 pin is set to the low level

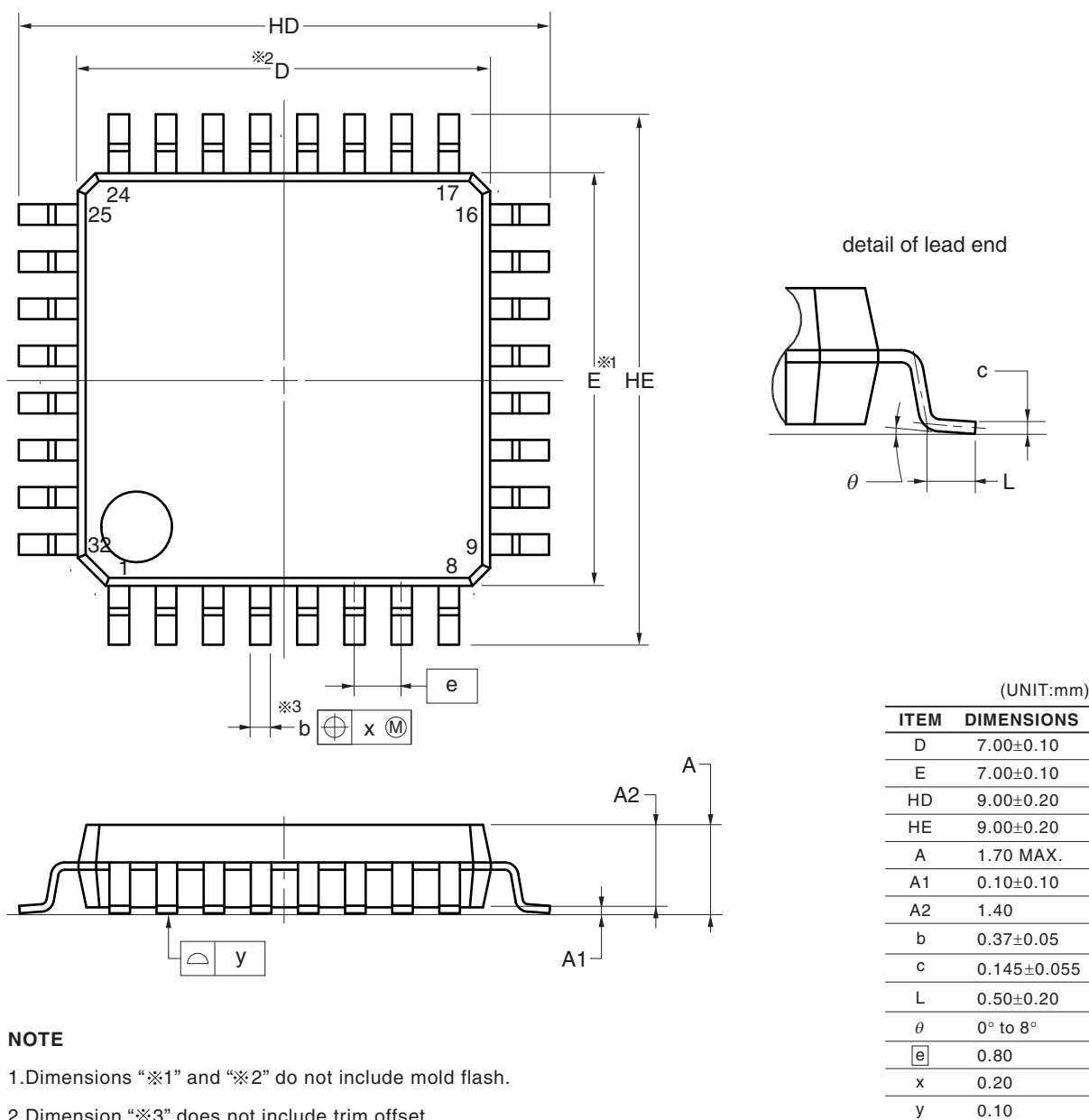
t_{HD}: Time to hold the TOOL0 pin at the low level after the external reset is released (excluding the processing time of the firmware to control the flash memory)

4. PACKAGE DRAWINGS

4.1 32-pin Products

R5F10RB8AFP, R5F10RBAAFP, R5F10RBCAFP
R5F10RB8GFP, R5F10RBAGFP, R5F10RBCGFP

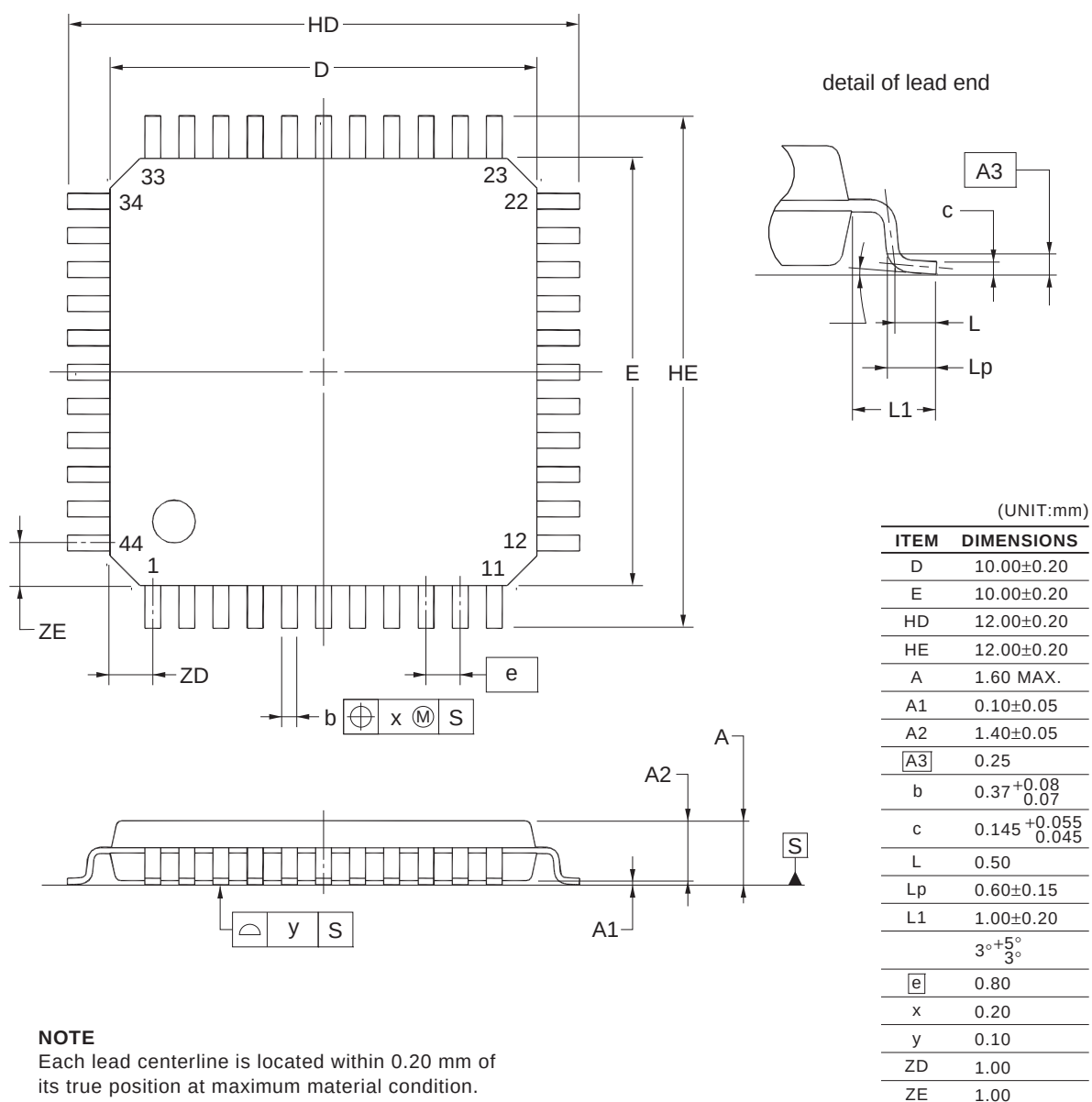
JEITA Package Code	RENESAS Code	Previous Code	MASS (TYP.) [g]
P-LQFP32-7x7-0.80	PLQP0032GB-A	P32GA-80-GBT-1	0.2



4.2 44-pin Products

R5F10RF8AFP, R5F10RFAAFP, R5F10RFCAFP
 R5F10RF8GFP, R5F10RFAGFP, R5F10RFCGFP

JEITA Package Code	RENESAS Code	Previous Code	MASS (TYP.) [g]
P-LQFP44-10x10-0.80	PLQP0044GC-A	P44GB-80-UES-2	0.36

**NOTE**

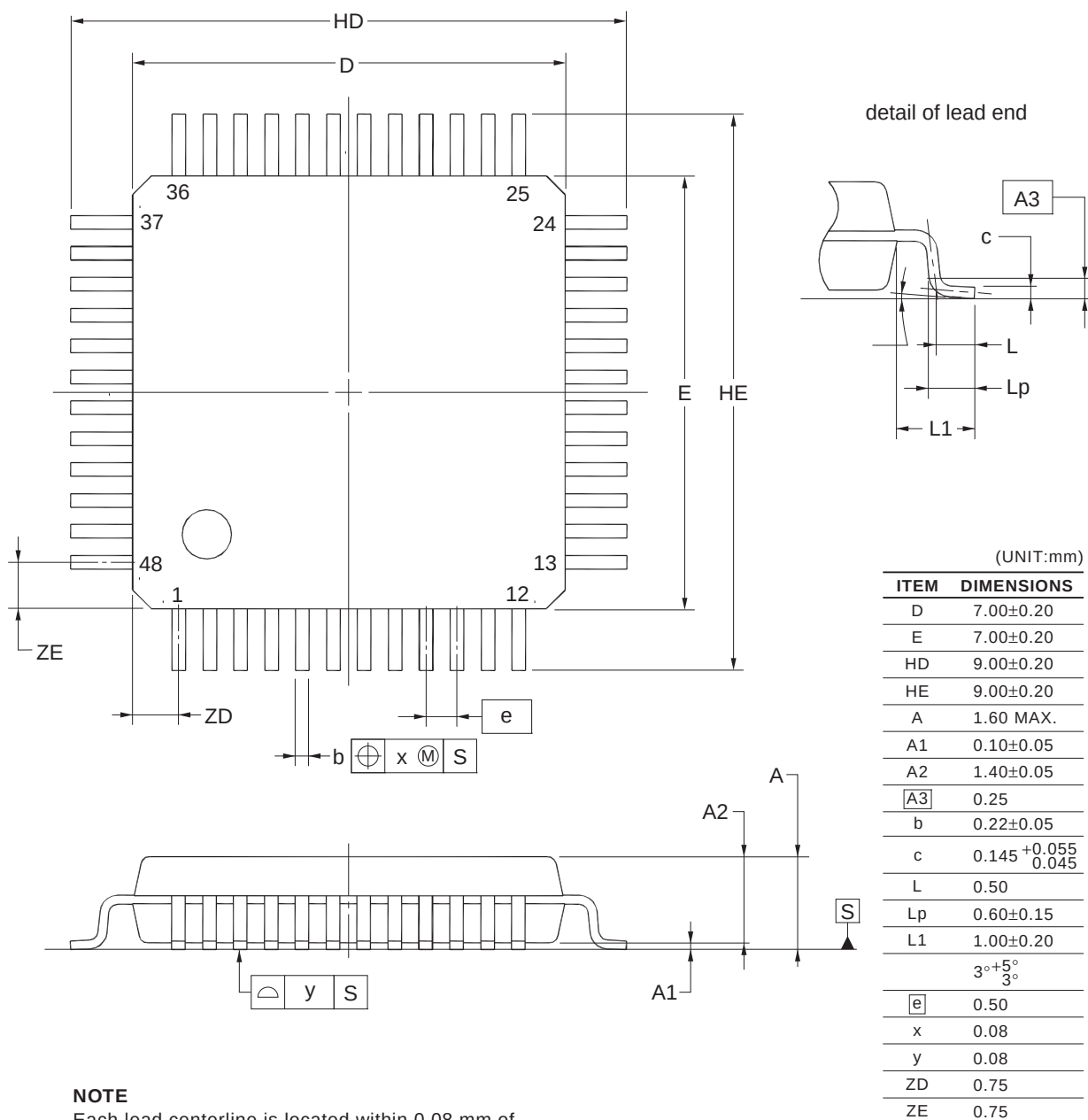
Each lead centerline is located within 0.20 mm of its true position at maximum material condition.

4.3 48-pin Products

R5F10RG8AFB, R5F10RGAAFB, R5F10RGCAFB

R5F10RG8GFB, R5F10RGAGFB, R5F10RGCGFB

JEITA Package Code	RENESAS Code	Previous Code	MASS (TYP.) [g]
P-LFQFP48-7x7-0.50	PLQP0048KF-A	P48GA-50-8EU-1	0.16

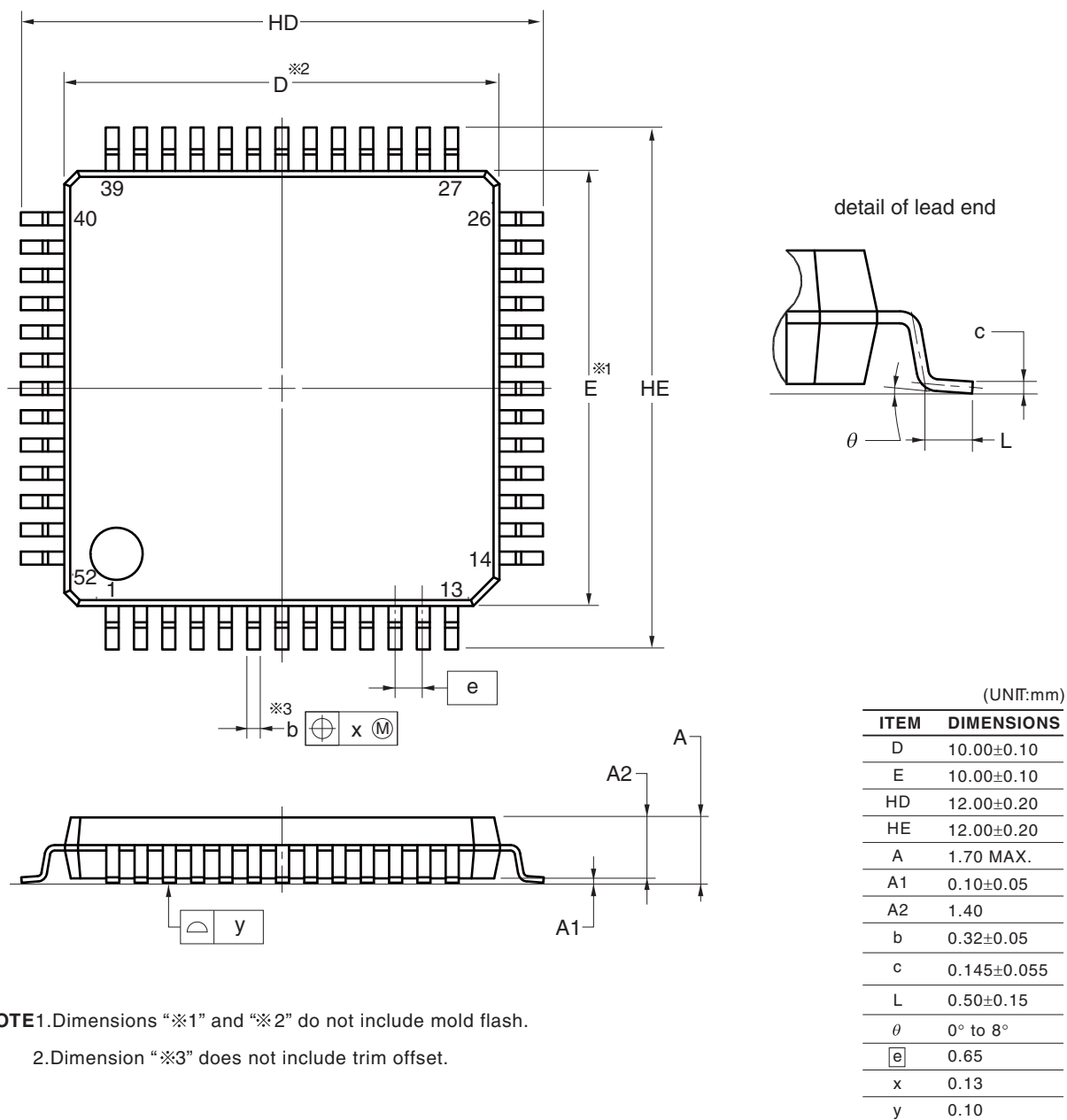
**NOTE**

Each lead centerline is located within 0.08 mm of its true position at maximum material condition.

4.4 52-pin Products

R5F10RJ8AFA, R5F10RJAAFA, R5F10RJCAFA
 R5F10RJ8GFA, R5F10RJAGFA, R5F10RJCGFA

JEITA Package Code	RENESAS Code	Previous Code	MASS (TYP.) [g]
P-LQFP52-10x10-0.65	PLQP0052JA-A	P52GB-65-GBS-1	0.3



NOTE1. Dimensions “※1” and “※2” do not include mold flash.

2. Dimension “※3” does not include trim offset.

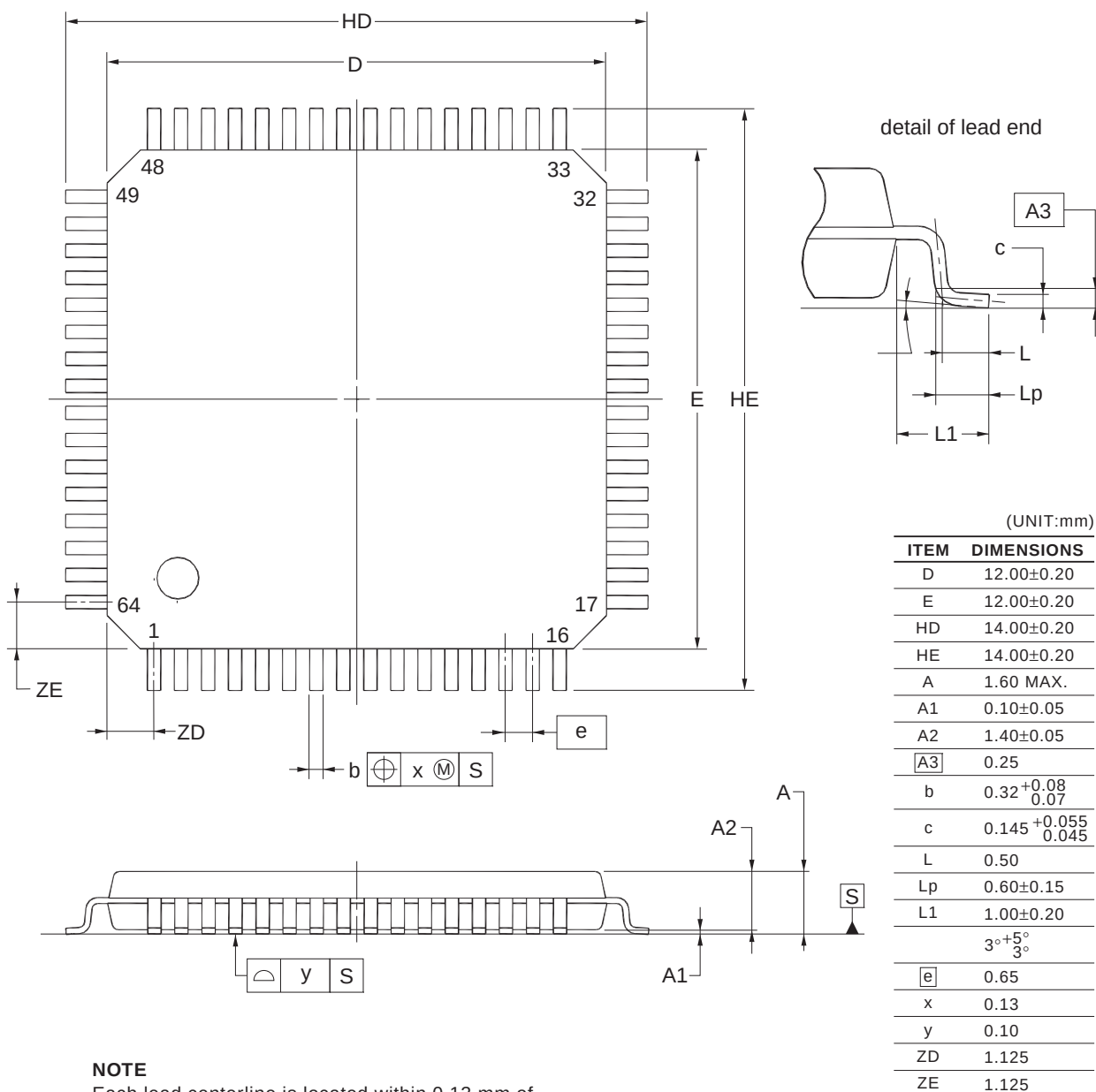
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4.5 64-pin Products

R5F10RLAAFA, R5F10RLCAFA

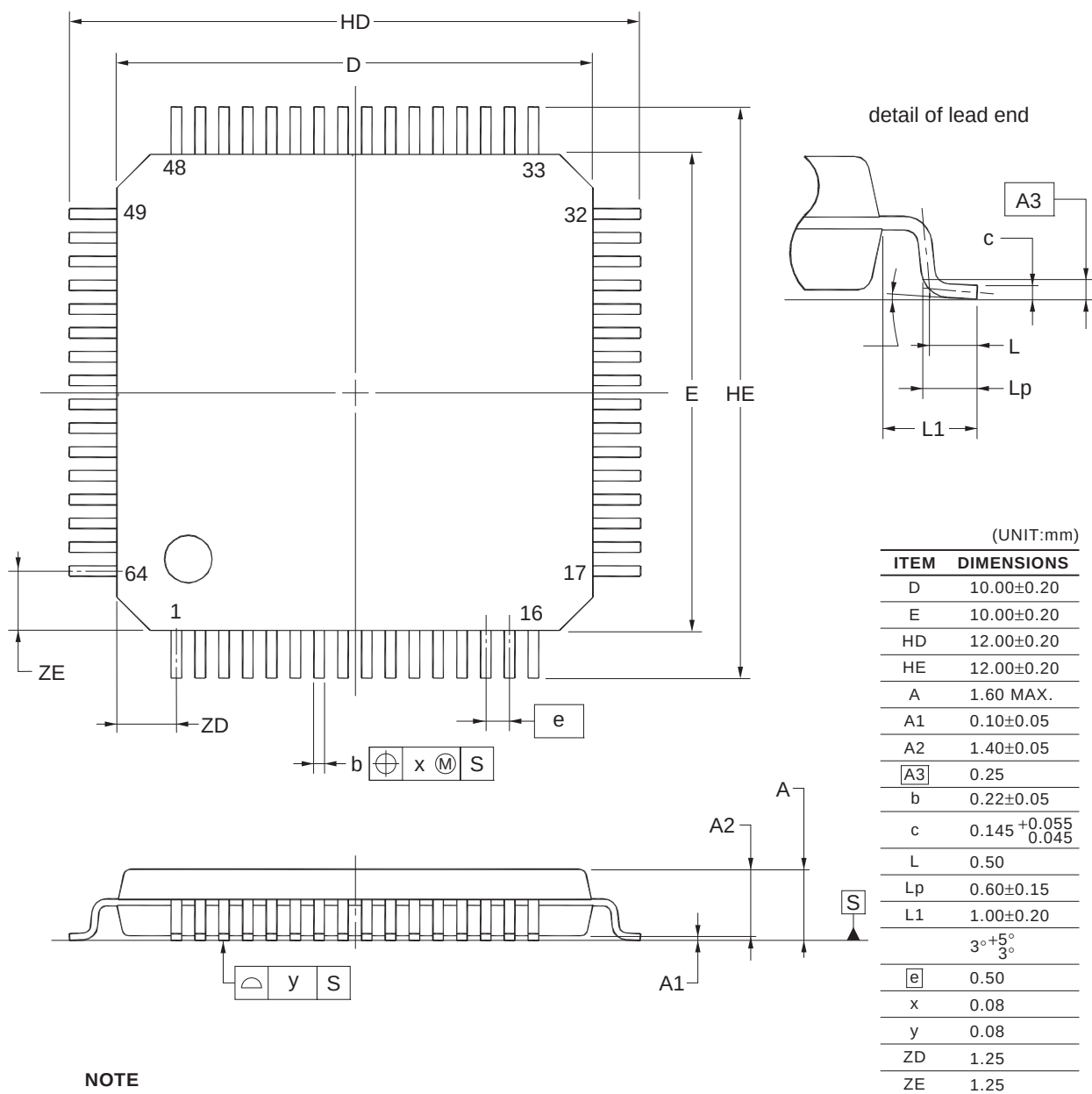
R5F10RLAGFA, R5F10RLCGFA

JEITA Package Code	RENESAS Code	Previous Code	MASS (TYP.) [g]
P-LQFP64-12x12-0.65	PLQP0064JA-A	P64GK-65-UET-2	0.51



R5F10RLAAFB, R5F10RLCAFB
R5F10RLAGFB, R5F10RLCGFB

JEITA Package Code	RENESAS Code	Previous Code	MASS (TYP.) [g]
P-LFQFP64-10x10-0.50	PLQP0064KF-A	P64GB-50-UEU-2	0.35



NOTE

Each lead centerline is located within 0.08 mm of its true position at maximum material condition.

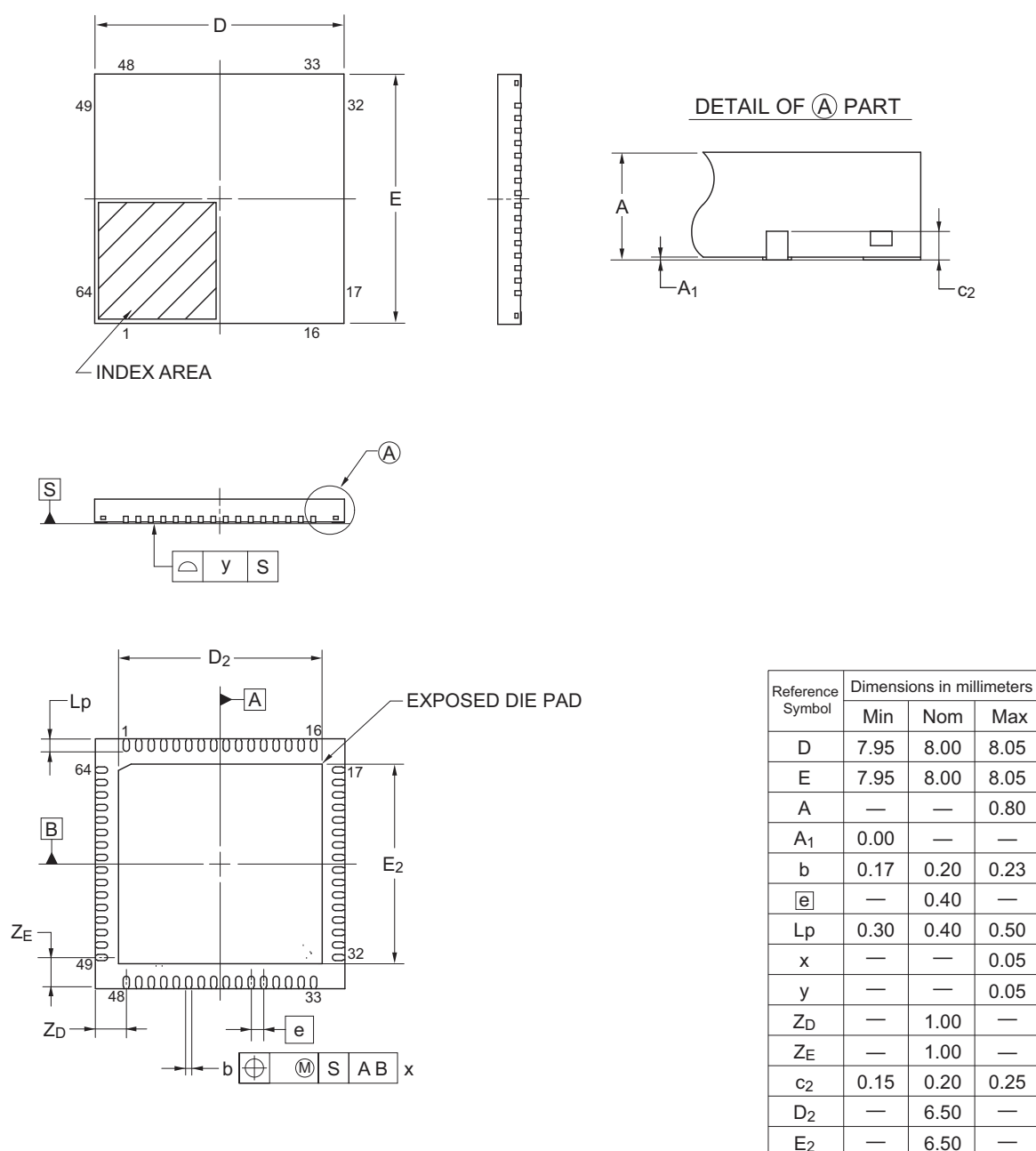
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R5F10RLAANB, R5F10RLCANB
R5F10RLAGNB, R5F10RLCGNB

<R>

JEITA Package Code	RENESAS Code	Previous Code	MASS (Typ) [g]
P-HWQFN64-8x8-0.40	PWQN0064LA-A	P64K8-40-9B5-4	0.16

Unit: mm



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Revision History	RL78/L12 Datasheet
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Rev.	Date	Description	
		Page	Summary
0.01	Feb 20, 2012	-	First Edition issued
0.02	Sep 26, 2012	7, 8	Modification of caution 2 in 1.3.5 64-pin products
		15	Modification of I/O port in 1.6 Outline of Functions
		-	Modification of 2. ELECTRICAL SPECIFICATIONS (TARGET)
		-	Update of package drawings in 3. PACKAGE DRAWINGS
1.00	Jan 31, 2013	11 to 15	Modification of 1.5 Block Diagram
		16	Modification of Note 2 in 1.6 Outline of Functions
		17	Modification of 1.6 Outline of Functions
		-	Deletion of target in 2. ELECTRICAL SPECIFICATIONS
		18	Addition of caution 2 to 2. ELECTRICAL SPECIFICATIONS
		19	Addition of description, note 3, and remark 2 to 2.1 Absolute Maximum Ratings
		20	Modification of description and addition of note to 2.1 Absolute Maximum Ratings
		22, 23	Modification of 2.2 Oscillator Characteristics
		30	Modification of notes 1 to 4 in 2.3.2 Supply current characteristics
		32	Modification of notes 1, 3 to 6, 8 in 2.3.2 Supply current characteristics
		34	Modification of notes 7, 9, 11, and addition of notes 8, 12 to 2.3.2 Supply current characteristics
		36	Addition of description to 2.4 AC Characteristics
		38, 40 to 42, 44 to 46, 48 to 52, 54, 55	Modification of 2.5.1 Serial array unit
		57, 58	Modification of 2.5.2 Serial interface IICA
		62	Modification of 2.6.2 Temperature sensor/internal reference voltage characteristics
		64	Addition of note and caution in 2.6.5 Supply voltage rise time
		69	Modification of 2.8 Data Memory STOP Mode Low Supply Voltage Data Retention Characteristics
		69	Modification of conditions in 2.9 Timing Specs for Switching Flash Memory Programming Modes
		70	Modification of 2.10 Timing Specifications for Switching Flash Memory Programming Modes
2.00	Jan 10, 2014	1	Modification of 1.1 Features
		3	Modification of Figure 1-1
		4	Modification of part number, note, and caution
		5 to 10	Deletion of COMEXP pin in 1.3.1 to 1.3.5.
		11	Modification of description in 1.4 Pin Identification
		12 to 16	Deletion of COMEXP pin in 1.5.1 to 1.5.5
		17	Modification of table and note 2 in 1.6 Outline of Functions
		20	Modification of description in Absolute Maximum Ratings (T _A = 25°C) (1/3)
		21	Modification of description and note 2 in Absolute Maximum Ratings (T _A = 25°C) (2/3)
		23	Modification of table, note, caution, and remark in 2.2.1 X1, XT1 oscillator characteristics
		23	Modification of table in 2.2.2 On-chip oscillator characteristics
		24	Modification of table, notes 2 and 3 in 2.3.1 Pin characteristics (1/5)
		25	Modification of notes 1 and 3 in 2.3.1 Pin characteristics (2/5)
		30	Modification of notes 1 and 4 in 2.3.2 Supply current characteristics (1/3)
		31, 32	Modification of table, notes 1, 5, and 6 in 2.3.2 Supply current characteristics (2/3)
		33, 34	Modification of table, notes 1, 3, 4, and 5 to 10 in 2.3.2 Supply current characteristics (3/3)

Rev.	Date	Description	
		Page	Summary
2.00	Jan 10, 2014	35	Modification of table in 2.4 AC Characteristics
		36	Addition of Minimum Instruction Execution Time during Main System Clock Operation
		37	Modification of AC Timing Test Points and External System Clock Timing
		39	Modification of AC Timing Test Points
		39	Modification of description, notes 1 and 2 in (1) During communication at same potential (UART mode)
		41, 42	Modification of description, remark 2 in (2) During communication at same potential (CSI mode)
		42, 43	Modification of description in (3) During communication at same potential (CSI mode)
		45	Modification of description, notes 1 and 3, and remark 3 in (4) Communication at different potential (1.8 V, 2.5 V, 3 V) (UART mode) (1/2)
		46, 48	Modification of description, and remark 3 in (4) Communication at different potential (1.8 V, 2.5 V, 3 V) (UART mode) (2/2)
		49, 50	Modification of table, and note 1, caution, and remark 3 in (5) Communication at different potential (2.5 V, 3 V) (CSI mode)
		51	Modification of table and note in (6) Communication at different potential (1.8 V, 2.5 V, 3 V) (1/3)
		52	Modification of table and notes 1 to 3 in (6) Communication at different potential (1.8 V, 2.5 V, 3 V) (2/3)
		53, 54	Modification of table, note 3, and remark 3 in (6) Communication at different potential (1.8 V, 2.5 V, 3 V) (3/3)
		56	Modification of table in (7) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (1/2)
		57	Modification of table in (7) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (2/2)
		59, 60	Addition of (1) I ² C standard mode
		61	Addition of (2) I ² C fast mode
		62	Addition of (3) I ² C fast mode plus
		63	Addition of table in 2.6.1 A/D converter characteristics
		63, 64	Modification of description and notes 3 to 5 in 2.6.1 (1)
		65	Modification of description, notes 3 and 4 in 2.6.1 (2)
		66	Modification of description, notes 3 and 4 in 2.6.1 (3)
		67	Modification of description, notes 3 and 4 in 2.6.1 (4)
		67	Modification of the table in 2.6.2 Temperature sensor/internal reference voltage characteristics
		68	Modification of the table and note in 2.6.3 POR circuit characteristics
		70	Modification of the table of LVD Detection Voltage of Interrupt & Reset Mode
		70	Modification from V _{DD} rise slope to Power supply voltage rising slope in 2.6.5 Supply voltage rise time
		75	Modification of description in 2.10 Dedicated Flash Memory Programmer Communication (UART)
		76	Modification of the figure in 2.11 Timing Specifications for Switching Flash Memory Programming Modes
		77 to 126	Addition of products for industrial applications (G: T _A = -40 to +105°C)
		127 to 133	Addition of product names for industrial applications (G: T _A = -40 to +105°C)
2.10	Sep 30, 2016	5	Modification of pin configuration in 1.3.1 32-pin products
		6	Modification of pin configuration in 1.3.2 44-pin products
		7	Modification of pin configuration in 1.3.3 48-pin products
		8	Modification of pin configuration in 1.3.4 52-pin products
		9, 10	Modification of pin configuration in 1.3.5 64-pin products
		17	Modification of description of main system clock in 1.6 Outline of Functions
		74	Modification of title of 2.8 RAM Data Retention Characteristics, Note, and figure
		74	Modification of table of 2.9 Flash Memory Programming Characteristics
		123	Modification of title of 3.8 RAM Data Retention Characteristics, Note, and figure
		123	Modification of table of 3.9 Flash Memory Programming Characteristics and addition of Note 4
		131	Modification of 4.5 64-pin Products

The mark “<R>” shows major revised points. The revised points can be easily searched by copying an “<R>” in the PDF file and specifying it in the “Find what:” field.

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NOTES FOR CMOS DEVICES

- (1) **VOLTAGE APPLICATION WAVEFORM AT INPUT PIN:** Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (MAX) and V_{IH} (MIN) due to noise, etc., the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (MAX) and V_{IH} (MIN).
- (2) **HANDLING OF UNUSED INPUT PINS:** Unconnected CMOS device inputs can be cause of malfunction. If an input pin is unconnected, it is possible that an internal input level may be generated due to noise, etc., causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using pull-up or pull-down circuitry. Each unused pin should be connected to VDD or GND via a resistor if there is a possibility that it will be an output pin. All handling related to unused pins must be judged separately for each device and according to related specifications governing the device.
- (3) **PRECAUTION AGAINST ESD:** A strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it when it has occurred. Environmental control must be adequate. When it is dry, a humidifier should be used. It is recommended to avoid using insulators that easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors should be grounded. The operator should be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with mounted semiconductor devices.
- (4) **STATUS BEFORE INITIALIZATION:** Power-on does not necessarily define the initial status of a MOS device. Immediately after the power source is turned ON, devices with reset functions have not yet been initialized. Hence, power-on does not guarantee output pin levels, I/O settings or contents of registers. A device is not initialized until the reset signal is received. A reset operation must be executed immediately after power-on for devices with reset functions.
- (5) **POWER ON/OFF SEQUENCE:** In the case of a device that uses different power supplies for the internal operation and external interface, as a rule, switch on the external power supply after switching on the internal power supply. When switching the power supply off, as a rule, switch off the external power supply and then the internal power supply. Use of the reverse power on/off sequences may result in the application of an overvoltage to the internal elements of the device, causing malfunction and degradation of internal elements due to the passage of an abnormal current. The correct power on/off sequence must be judged separately for each device and according to related specifications governing the device.
- (6) **INPUT OF SIGNAL DURING POWER OFF STATE :** Do not input signals or an I/O pull-up power supply while the device is not powered. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Input of signals during the power off state must be judged separately for each device and according to related specifications governing the device.

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