



9-Bit Odd/Even Parity Generator/Checker

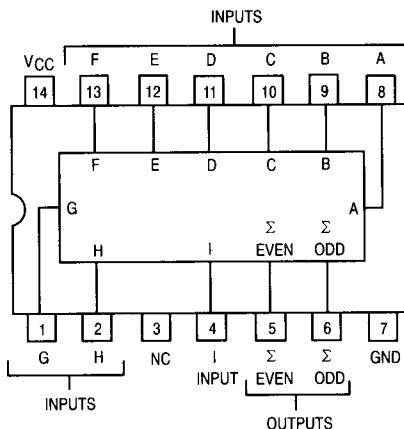
ELECTRICALLY TESTED PER:
MIL-M-38510/32901

The 54LS280 is a Universal 9-Bit Parity Generator/Checker. It features odd/even outputs to facilitate either odd or even parity. By cascading, the word length is easily expanded.

The 'LS280 is designed without the expander input implementation, but the corresponding function is provided by an input at pin 4 and the absence of any connection at pin 3. This design permits the 'LS280 to be substituted for the 'LS180 which results in improved performance. The 'LS280 has buffered inputs to lower the drive requirements to one LS unit load.

- Generates Either Odd or Even Parity for Nine Data Lines
- Typical Data-to-Output Delays of Only 33 ns
- Cascadable for n-Bits
- Can Be Used to Upgrade Systems Using MSI Parity Circuits
- Typical Power Dissipation = 80 mW

CONNECTION DIAGRAM



Military 54LS280



AVAILABLE AS:

- 1) JAN: JM38510/32901BXA
- 2) SMD: N/A
- 3) 883: 54LS280/BXAJC

X = CASE OUTLINE AS FOLLOWS:
PACKAGE: CERDIP: C
CERFLAT: D
LCC: 2

THE LETTER "M" APPEARS BEFORE THE / ON LCC.

PIN ASSIGNMENTS

FUNCT.	DIL 632-08	FLATS 717-04	LCC 756A-02	BURN-IN (COND. A)
G	1	1	2	VCC
H	2	2	3	VCC
NC	3	3	4	OPEN
I	4	4	6	GND
ΣE	5	5	8	VCC
ΣO	6	6	9	OPEN
GND	7	7	10	GND
A	8	8	12	VCC
B	9	9	13	VCC
C	10	10	14	GND
D	11	11	16	VCC
E	12	12	18	VCC
F	13	13	19	GND
VCC	14	14	20	VCC

BURN-IN CONDITIONS:
VCC = 5.0 V MIN/6.0 V MAX

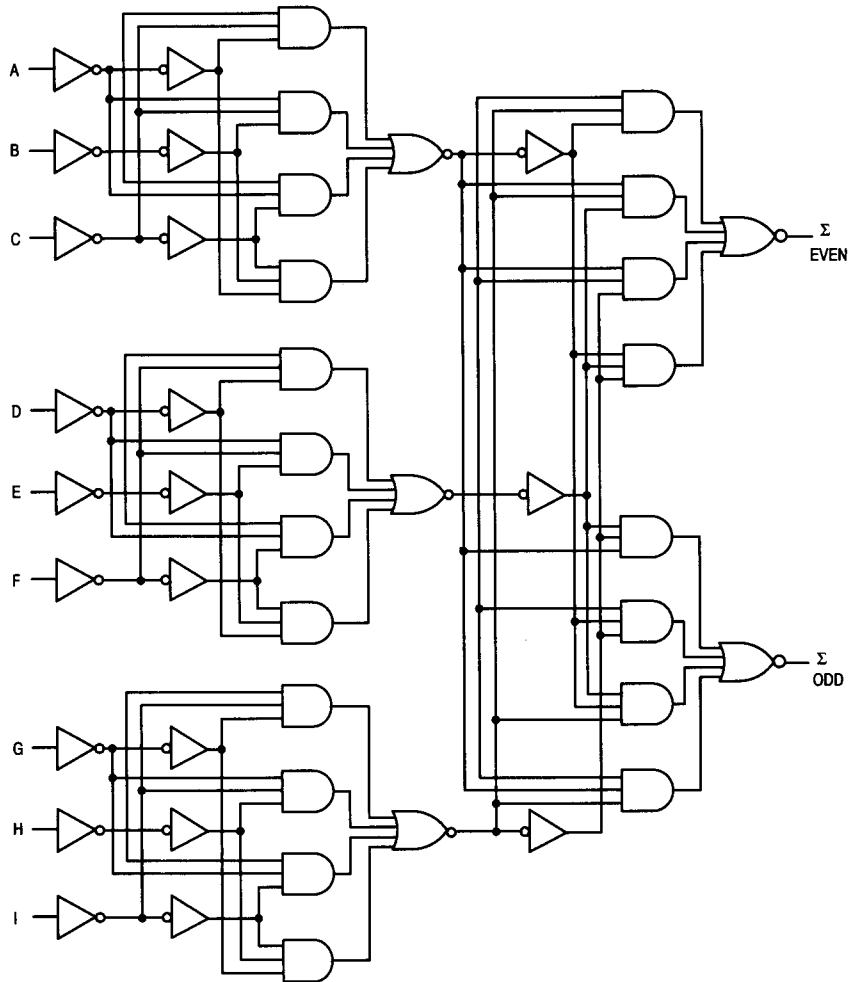
FUNCTION TABLE

Number of Inputs A thru I that are High	Outputs	
	Σ Even	Σ Odd
0, 2, 4, 6, 8	H	L
1, 3, 5, 7, 9	L	H

H = HIGH Voltage Level
L = LOW Voltage Level

54LS280

LOGIC DIAGRAM



5

Figure 1: Load circuit and timing diagram.

The top diagram shows the load circuit for the output under test. It includes a load resistor R_L connected to V_{CC} , a load capacitor $C_L = 50 \text{ pF}$ connected to ground, and a series of three diodes connected to ground. The input is labeled "FROM OUTPUT UNDER TEST".

The bottom diagram shows the timing diagram for the output under test. It includes three waveforms: INPUT WAVEFORM, OUTPUT WAVEFORM A (Σ ODD), and OUTPUT WAVEFORM B (Σ EVEN). The input waveform is a square wave with a high level of 2.7 V and a low level of 0.7 V . The output waveforms show the signal after the load, with high levels V_{OH} and low levels V_{OL} . Timing parameters are indicated: t_r (rise time), t_f (fall time), t_{PLH2} (propagation delay to high level), t_{PLH1} (propagation delay to low level), and t_{PLH} (propagation delay to high level).

1. The input pulse generator has the following characteristics:
 $t_r \leq 15 \text{ ns}$, $t_f \leq 6.0 \text{ ns}$, $\text{PRR} \leq 1.0 \text{ MHz}$.
2. $C_L = 50 \text{ pF} \pm 10\%$, including scope probe, wiring and stray capacitance.
3. $R_L = 2.0 \text{ k}\Omega \pm 5.0\%$. All diodes are 1N3064 or 1N916.
4. Voltage measurements are to be made with respect to network ground terminal.
5. The limits specified for $C_L = 15 \text{ pF}$ are guaranteed but not tested.
6. Terminal conditions (pins not designated may be high $\geq 2.0 \text{ V}$, or low $\leq 0.7 \text{ V}$, or open).

54LS280

Symbol	Parameter	Limits						Unit	Test Condition (Unless Otherwise Specified)
	Static Parameters:	+ 25°C		+ 125°C		– 55°C			
		Subgroup 1		Subgroup 2		Subgroup 3			
		Min	Max	Min	Max	Min	Max		
V _{OH}	Logical "1" Output Voltage	2.5		2.5		2.5		V	V _{CC} = 4.5 V, I _{OH} = – 0.4 mA, V _{IN} = 0.7 V all inputs, A = 0.7 V or 2.0 V.
V _{OL}	Logical "0" Output Voltage		0.4		0.4		0.4	V	V _{CC} = 4.5 V, I _{OL} = 4.0 mA, V _{IL} = 0.7 V (all inputs), A = 2.0 V or 0.7 V.
V _{IC}	Input Clamping Voltage		– 1.5					V	V _{CC} = 4.5 V, I _{IN} = –18 mA, other inputs are open.
I _{IH}	Logical "1" Input Current		20		20		20	μA	V _{CC} = 5.5 V, V _{IH} = 2.7 V, other inputs are open.
I _{IHH}	Logical "1" Input Current		100		100		100	μA	V _{CC} = 5.5 V, V _{IHH} = 5.5 V, other inputs are open.
I _{OS}	Output Short Circuit Current	– 15	– 100	– 15	– 100	– 15	– 100	mA	V _{CC} = 5.5 V, V _{IN} = GND, A = GND or 4.5 V, V _{OUT} = GND.
I _{IL}	Logical "0" Input Current	– 130	– 370	– 130	– 370	– 130	– 370	μA	V _{CC} = 5.5 V, V _{IN} = 0.4 V, other inputs are open.
I _{CC}	Power Supply Current Off		27		27		27	mA	V _{CC} = 5.5 V, V _{IN} = GND (all inputs).
V _{IH}	Logical "1" Input Voltage	2.0		2.0		2.0		V	V _{CC} = 4.5 V.
V _{IL}	Logical "0" Input Voltage		0.7		0.7		0.7	V	V _{CC} = 4.5 V.
	Functional Tests	Subgroup 7		Subgroup 8A		Subgroup 8B			per Truth Table with V _{CC} = 5.0 V, V _{INL} = 0.4 V, and V _{INH} = 2.5 V.

5

Symbol	Parameter	Limits						Unit	Test Condition (Unless Otherwise Specified)
	Switching Parameters:	+ 25°C		+ 125°C		– 55°C			
		Subgroup 9		Subgroup 10		Subgroup 11			
		Min	Max	Min	Max	Min	Max		
t _{PHL1}	Propagation Delay /Data-Output High-Low	2.0	50	2.0	65	2.0	65	ns	V _{CC} = 5.0 V, C _L = 50 pF, R _L = 2.0 kΩ.
t _{PLH1}	Propagation Delay /Data-Output Low-High	2.0	55	2.0	72	2.0	72	ns	V _{CC} = 5.0 V, C _L = 50 pF, R _L = 2.0 kΩ.
t _{PHL2}	Propagation Delay /Data-Output High-Low	2.0	40	2.0	72	2.0	72	ns	V _{CC} = 5.0 V, C _L = 50 pF, R _L = 2.0 kΩ.
t _{PLH2}	Propagation Delay /Data-Output Low-High	2.0	55	2.0	52	2.0	52	ns	V _{CC} = 5.0 V, C _L = 50 pF, R _L = 2.0 kΩ