ISL84521, ISL84522, ISL84523

Low-Voltage, Single and Dual Supply, Quad SPST, Analog Switches

FN6031
Rev 4.00
August 10, 2015

The Intersil ISL84521, ISL84523, ISL84523 devices are CMOS, precision, quad analog switches designed to operate from a single +2V to +12V supply or from a ±2V to ±6V supply. Targeted applications include battery powered equipment that benefit from the devices' low power consumption (<1µW), low leakage currents (1nA max), and fast switching speeds (t_{ON} = 45ns, t_{OFF} = 15ns). A12Ω maximum R_{ON} flatness ensures signal fidelity, while channel-to-channel mismatch is guaranteed to be less than 4Ω.

The ISL84521, ISL84522, ISL84523 are quad single-pole/ single-throw (SPST) devices. The ISL84521 has four normally closed (NC) switches; the ISL84522 has four normally open (NO) switches; the ISL84523 has two NO and two NC switches and can be used as a dual SPDT, or a dual 2:1 multiplexer.

Table 1 summarizes the performance of this family. For higher performance, pin compatible versions and 3mm x 3mm Quad No-Lead Flatpack (QFN) package see the ISL43140, ISL43142 data sheet.

TABLE 1. FEATURES AT A GLANCE

	ISL84521	ISL84522	ISL84523
Number of Switches	4	4	4
Configuration	All NC	All NO	2 NC/2 NO
±5V R_{ON}	65Ω	65Ω	65Ω
±5V t_{ON}/t_{OFF}	45ns/15ns	45ns/15ns	45ns/15ns
5V R_{ON}	125Ω	125Ω	125Ω
5V t_{ON}/t_{OFF}	60ns/20ns	60ns/20ns	60ns/20ns
3V R_{ON}	260Ω	260Ω	260Ω
3V t_{ON}/t_{OFF}	120ns/40ns	120ns/40ns	120ns/40ns
Packages	16 Ld SOIC (N), 16 Ld TSSOP		

Features

- Drop-in Replacements for MAX4521 - MAX4523
- Four Separately Controlled SPST Switches
- Pin Compatible with DG411, DG412, DG413
- ON Resistance (R_{ON} Max.) 100Ω
- R_{ON} Matching Between Channels. . . . . <1Ω
- Low Power Consumption (P_D) . . . . . <1µW
- Low Leakage Current (Max at 85°C) 10nA
- Fast Switching Action
  - t_{ON} 45ns
  - t_{OFF} 15ns
- Break before Make Timing
- Minimum 2000V ESD Protection per Method 3015.7
- TTL, CMOS Compatible
- Pb-free available

Applications

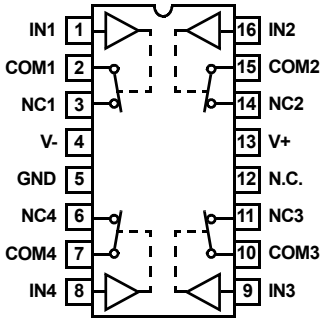
- Battery Powered, Handheld, and Portable Equipment
  - Cellular/Mobile Phones
  - Pagers
  - Laptops, Notebooks, Palmtops
- Communications Systems
  - Military Radios
  - RF "Tee" Switches
- Test Equipment
  - Ultrasound
  - Electrocardiograph
- Heads-Up Displays
- Audio and Video Switching
- General Purpose Circuits
  - +3V/+5V DACs and ADCs
  - Digital Filters
  - Operational Amplifier Gain Switching Networks
  - High Frequency Analog Switching
  - High Speed Multiplexing

Related Literature

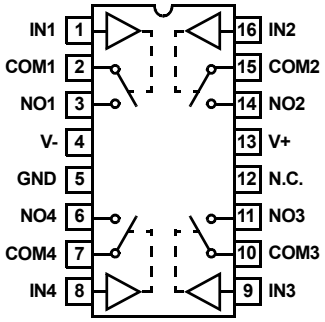
- Technical Brief TB363 "Guidelines for Handling and Processing Moisture Sensitive Surface Mount Devices (SMDs)"
- Application Note AN557 "Recommended Test Procedures for Analog Switches"

Pinouts (Note 1)

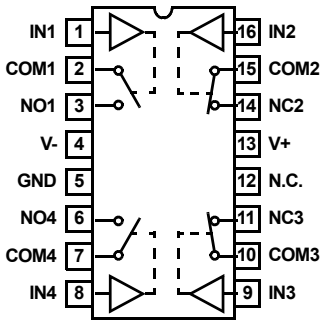
ISL84521 (SOIC, TSSOP)
TOP VIEW



ISL84522 (SOIC, TSSOP)
TOP VIEW



ISL84523 (SOIC, TSSOP)
TOP VIEW



NOTE:

1. Switches Shown for Logic “0” Input.

Truth Table

LOGIC	ISL84521	ISL84522	ISL84523	
	SW 1, 2, 3, 4	SW 1, 2, 3, 4	SW 1, 4	SW 2, 3
0	On	Off	Off	On
1	Off	On	On	Off
NOTE: Logic “0” ≤ 0.8V. Logic “1” ≥ 2.4V.				

Pin Descriptions

PIN	FUNCTION
V+	Positive Power Supply Input
V-	Negative Power Supply Input. Connect to GND for Single Supply Configurations.
GND	Ground Connection
IN	Digital Control Input
COM	Analog Switch Common Pin
NO	Analog Switch Normally Open Pin
NC	Analog Switch Normally Closed Pin
N.C.	No Internal Connection

Ordering Information

PART NO. (Note 2)	TEMP. RANGE (^{O}C)	PACKAGE (RoHS Compliant)	PKG. DWG. #
ISL84521IBZ*	-40 to 85	16 Ld SOIC (N)	M16.15
ISL84521IVZ*	-40 to 85	16 Ld TSSOP	M16.173
ISL84522IBZ*	-40 to 85	16 Ld SOIC (N)	M16.15
ISL84522IVZ*	-40 to 85	16 Ld TSSOP	M16.173
ISL84523IBZ* **No longer available, recommended replacement: ISL84524IUZ-T)**	-40 to 85	16 Ld SOIC (N)	M16.15
ISL84523IVZ* **No longer available, recommended replacement: ISL84524IUZ-T)**	-40 to 85	16 Ld TSSOP	M16.173

*Add “-T” suffix to part number for tape and reel packaging.

NOTE:

2. Intersil Pb-free products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which is compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J Std-020B.

Absolute Maximum Ratings

V+ to V- . . . . . -0.3 to15V
V+ to GND . . . . . -0.3 to15V
V- to GND . . . . . -15 to 0.3V
All Other Pins (Note 3) . . . . . ((V-) - 0.3V) to ((V+) + 0.3V)
Continuous Current (Any Terminal) 10mA
Peak Current, IN, NO, NC, or COM
(Pulsed 1ms, 10% Duty Cycle, Max) 20mA
ESD Rating (Per MIL-STD-883 Method 3015). . . . . > 2kV

Operating Conditions

Temperature Range
ISL8452XIX . . . . . -40°C to 85°C

Thermal Information

Thermal Resistance (Typical, Note 4)	θ_{JA} (°C/W)
16 Ld SOIC Package	115
16 Ld TSSOP Package	150

Maximum Junction Temperature (Plastic Package) . . . . . 150°C
Moisture Sensitivity (See Technical Brief TB363)
All Packages . . . . . Level 1
Maximum Storage Temperature Range. . . . . -65°C to 150°C
Maximum Lead Temperature (Soldering 10s) . . . . . 300°C
(Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTES:

3. Signals on NC, NO, COM, or IN exceeding V+ or V- are clamped by internal diodes. Limit forward diode current to maximum current ratings.
4. θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air. See Tech Brief TB379 for details.

Electrical Specifications +5V Supply

Test Conditions: V_{SUPPLY} = ±4.5V to ±5.5V, GND = 0V, V_{INH} = 2.4V, V_{INL} = 0.8V (Note 5), Unless Otherwise Specified

PARAMETER	TEST CONDITIONS	TEMP (°C)	(NOTE 6) MIN	TYP	(NOTE 6) MAX	UNITS
ANALOG SWITCH CHARACTERISTICS						
Analog Signal Range, V_{ANALOG}		Full	V-	-	V+	V
ON Resistance, R_{ON}	V_S = ±5V, I_{COM} = 1.0mA, V_{NO} or V_{NC} = ±3V (Figure 5)	25	-	65	100	Ω
		Full	-	-	125	Ω
R_{ON} Matching Between Channels, ΔR_{ON}	V_S = ±5V, I_{COM} = 1.0mA, V_{NO} or V_{NC} = ±3V	25	-	1	4	Ω
		Full	-	-	6	Ω
R_{ON} Flatness, $R_{FLAT(ON)}$	V_S = ±5V, I_{COM} = 1.0mA, V_{NO} or V_{NC} = ±3V (Note 8)	25	-	7	12	Ω
		Full	-	-	15	Ω
NO or NC OFF Leakage Current, $I_{NO(OFF)}$ or $I_{NC(OFF)}$	V_S = ±5.5V, V_{COM} = ±4.5V, V_{NO} or V_{NC} = ∓4.5V (Note 7)	25	-1	0.01	1	nA
		Full	-10	-	10	nA
COM OFF Leakage Current, $I_{COM(OFF)}$	V_S = ±5.5V, V_{COM} = ±4.5V, V_{NO} or V_{NC} = ∓4.5V (Note 7)	25	-1	0.01	1	nA
		Full	-10	-	10	nA
COM ON Leakage Current, $I_{COM(ON)}$	V_S = ±5.5V, V_{COM} = V_{NO} or V_{NC} = ±4.5V (Note 7)	25	-2	0.01	2	nA
		Full	-20	-	20	nA
DIGITAL INPUT CHARACTERISTICS						
Input Voltage High, V_{INH}		Full	-	1.6	2.4	V
Input Voltage Low, V_{INL}		Full	0.8	1.6	-	V
Input Current, I_{INH}, I_{INL}	V_S = ±5.5V, V_{IN} = 0V or V+	Full	-1	0.03	1	µA
DYNAMIC CHARACTERISTICS						
Turn-ON Time, t_{ON}	V_S = ±4.5V, V_{NO} or V_{NC} = ±3V, R_L = 300Ω, C_L = 35pF, V_{IN} = 0 to 3V (Figure 1)	25	-	45	80	ns
		Full	-	-	100	ns
Turn-OFF Time, t_{OFF}	V_S = ±4.5V, V_{NO} or V_{NC} = ±3V, R_L = 300Ω, C_L = 35pF, V_{IN} = 0 to 3V (Figure 1)	25	-	15	30	ns
		Full	-	-	40	ns
Break-Before-Make Time Delay (ISL84523), t_D	V_S = ±5.5V, V_{NO} or V_{NC} = ±3V, R_L = 300Ω, C_L = 35pF, V_{IN} = 0 to 3V (Figure 3)	25	5	20	-	ns
Charge Injection, Q	C_L = 1.0nF, V_G = 0V, R_G = 0Ω (Figure 2)	25	-	1	5	pC
NO or NC OFF Capacitance, C_{OFF}	f = 1MHz, V_{NO} or V_{NC} = V_{COM} = 0V (Figure 7)	25	-	2	-	pF
COM OFF Capacitance, $C_{COM(OFF)}$	f = 1MHz, V_{NO} or V_{NC} = V_{COM} = 0V (Figure 7)	25	-	2	-	pF
COM ON Capacitance, $C_{COM(ON)}$	f = 1MHz, V_{NO} or V_{NC} = V_{COM} = 0V (Figure 7)	25	-	5	-	pF

Electrical Specifications +5V Supply

Test Conditions: V_{SUPPLY} = ±4.5V to ±5.5V, GND = 0V, V_{INH} = 2.4V, V_{INL} = 0.8V (Note 5), Unless Otherwise Specified **(Continued)**

PARAMETER	TEST CONDITIONS	TEMP (°C)	(NOTE 6) MIN	TYP	(NOTE 6) MAX	UNITS
OFF Isolation	R_L = 50Ω, C_L = 15pF, f = 100kHz, V_{NO} or V_{NC} = 1V_{RMS}, (See Figures 4 and 6)	25	-	>90	-	dB
Crosstalk, (Note 9)		25	-	<-90	-	dB
POWER SUPPLY CHARACTERISTICS						
Power Supply Range		Full	±2	-	±6	V
Positive Supply Current, I+	V_S = ±5.5V, V_{IN} = 0V or V+, Switch On or Off	25	-1	0.05	1	µA
		Full	-1	-	1	µA
Negative Supply Current, I-		25	-1	0.05	1	µA
		Full	-1	-	1	µA

NOTES:

5. V_{IN} = Input voltage to perform proper function.
6. The algebraic convention, whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
7. Leakage parameter is 100% tested at high temp, and guaranteed by correlation at 25°C.
8. Flatness is defined as the delta between the maximum and minimum R_{ON} values over the specified voltage range.
9. Between any two switches.

Electrical Specifications 5V Supply

Test Conditions: V+ = +4.5V to +5.5V, V- = GND = 0V, V_{INH} = 2.4V, V_{INL} = 0.8V (Note 5), Unless Otherwise Specified

PARAMETER	TEST CONDITIONS	TEMP (°C)	MIN (NOTE 6)	TYP	MAX (NOTE 6)	UNITS
ANALOG SWITCH CHARACTERISTICS						
Analog Signal Range, V_{ANALOG}		Full	0	-	V+	V
ON Resistance, R_{ON}	V+ = 4.5V, I_{COM} = 1.0mA, V_{NO} or V_{NC} = 3.5V (Figure 5)	25	-	125	200	Ω
		Full	-	-	250	Ω
R_{ON} Matching Between Channels, ΔR_{ON}	V+ = 5V, I_{COM} = 1.0mA, V_{NO} or V_{NC} = 3.5V	25	-	2	8	Ω
		Full	-	-	10	Ω
NO or NC OFF Leakage Current, $I_{NO(OFF)}$ or $I_{NC(OFF)}$	V+ = 5.5V, V_{COM} = 1V, 4.5V, V_{NO} or V_{NC} = 4.5V, 1V (Note 7)	25	-1	0.01	1	nA
		Full	-10	-	10	nA
COM OFF Leakage Current, $I_{COM(OFF)}$	V+ = 5.5V, V_{COM} = 1V, 4.5V, V_{NO} or V_{NC} = 4.5V, 1V (Note 7)	25	-1	0.01	1	nA
		Full	-10	-	10	nA
COM ON Leakage Current, $I_{COM(ON)}$	V+ = 5.5V, V_{COM} = 1V, 4.5V (Note 7)	25	-2	-	2	nA
		Full	-20	-	20	nA
DIGITAL INPUT CHARACTERISTICS						
Input Voltage High, V_{INH}		Full	-	1.6	2.4	V
Input Voltage Low, V_{INL}		Full	0.8	1.6	-	V
Input Current, I_{INH}, I_{INL}	V+ = 5.5V, V_{IN} = 0V or V+	Full	-1	0.03	1	µA
DYNAMIC CHARACTERISTICS						
Turn-ON Time, t_{ON}	V+ = 4.5V, V_{NO} or V_{NC} = 3V, R_L = 300Ω, C_L = 35pF, V_{IN} = 0 to 3V (Figure 1)	25	-	60	100	ns
		Full	-	-	150	ns
Turn-OFF Time, t_{OFF}	V+ = 4.5V, V_{NO} or V_{NC} = 3V, R_L = 300Ω, C_L = 35pF, V_{IN} = 0 to 3V (Figure 1)	25	-	20	50	ns
		Full	-	-	75	ns
Break-Before-Make Time Delay (ISL84523), t_D	V+ = 5.5V, V_{NO} or V_{NC} = 3V, R_L = 300Ω, C_L = 35pF, V_{IN} = 0 to 3V (Figure 3)	25	10	30	-	ns
Charge Injection, Q	C_L = 1.0nF, V_G = 0V, R_G = 0Ω (Figure 2)	25	-	1	5	pC

Electrical Specifications 5V Supply

Test Conditions: V+ = +4.5V to +5.5V, V- = GND = 0V, V_{INH} = 2.4V, V_{INL} = 0.8V (Note 5), Unless Otherwise Specified **(Continued)**

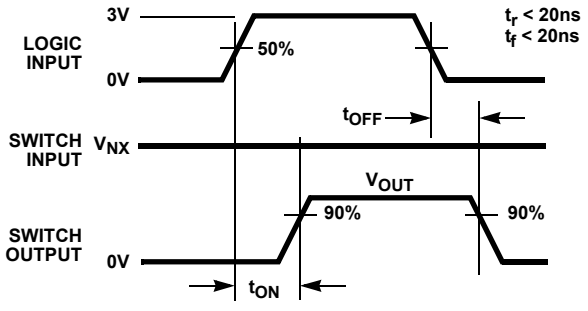
PARAMETER	TEST CONDITIONS	TEMP (°C)	MIN (NOTE 6)	TYP	MAX (NOTE 6)	UNITS
POWER SUPPLY CHARACTERISTICS						
Positive Supply Current, I+	V+ = 5.5V, V_{IN} = 0V or V+, Switch On or Off	25	-1	0.05	1	µA
		Full	-1	-	1	µA
Negative Supply Current, I-		25	-1	0.05	1	µA
		Full	-1	-	1	µA

Electrical Specifications 3V Supply

Test Conditions: V+ = +2.7V to +3.6V, V- = GND = 0V, V_{INH} = 2.4V, V_{INL} = 0.8V (Note 5), Unless Otherwise Specified

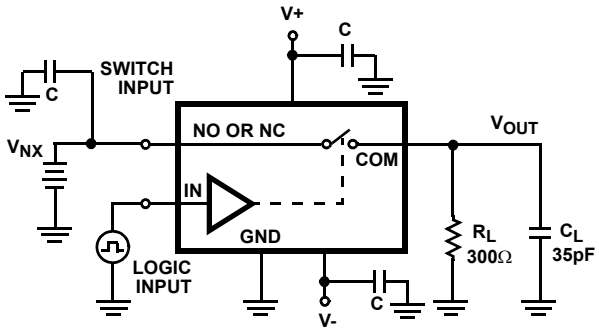
PARAMETER	TEST CONDITIONS	TEMP (°C)	MIN (NOTE 6)	TYP	MAX (NOTE 6)	UNITS
ANALOG SWITCH CHARACTERISTICS						
Analog Signal Range, V_{ANALOG}		Full	0	-	V+	V
ON Resistance, R_{ON}	V+ = 2.7V, I_{COM} = 0.1mA, V_{NO} or V_{NC} = 1V	25	-	260	500	Ω
		Full	-	-	600	Ω
DIGITAL INPUT CHARACTERISTICS						
Input Voltage High, V_{INH}		Full	-	1.6	2.4	V
Input Voltage Low, V_{INL}		Full	0.8	1.6	-	V
Input Current, I_{INH}, I_{INL}	V+ = 3.6V, V_{IN} = 0V or V+	Full	-1	0.03	1	µA
DYNAMIC CHARACTERISTICS						
Turn-ON Time, t_{ON}	V+ = 2.7V, V_{NO} or V_{NC} = 1.5V, R_L = 300Ω, C_L = 35pF, V_{IN} = 0 to V+ (Figure 1)	25	-	120	250	ns
		Full	-	-	300	ns
Turn-OFF Time, t_{OFF}	V+ = 2.7V, V_{NO} or V_{NC} = 1.5V, R_L = 300Ω, C_L = 35pF, V_{IN} = 0 to V+ (Figure 1)	25	-	40	80	ns
		Full	-	-	100	ns
Break-Before-Make Time Delay (ISL84523), t_D	V+ = 3.6V, V_{NO} or V_{NC} = 1.5V, R_L = 300Ω, C_L = 35pF, V_{IN} = 0 to 3V (Figure 3)	25	15	50	-	ns
Charge Injection, Q	C_L = 1.0nF, V_G = 0V, R_G = 0Ω (Figure 2)	25	-	0.5	5	pC
POWER SUPPLY CHARACTERISTICS						
Positive Supply Current, I+	V+ = 3.6V, V_{IN} = 0V or V+, Switch On or Off	25	-1	0.05	1	µA
		Full	-1	-	1	µA
Negative Supply Current, I-		25	-1	0.05	1	µA
		Full	-1	-	1	µA

Test Circuits and Waveforms



Logic input waveform is inverted for switches that have the opposite logic sense.

FIGURE 1A. MEASUREMENT POINTS



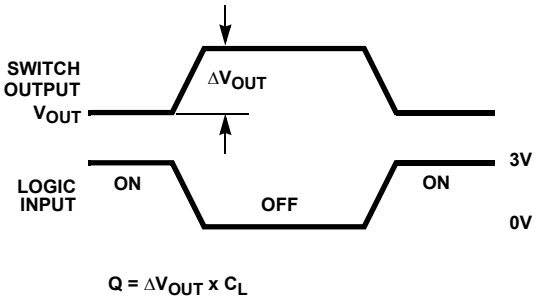
Repeat test for all switches. C_L includes fixture and stray capacitance.

$$V_{OUT} = V_{(NO\ or\ NC)} \frac{R_L}{R_L + R_{(ON)}}$$

FIGURE 1B. TEST CIRCUIT

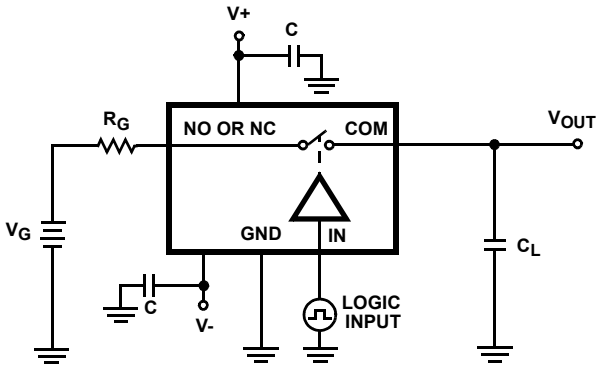
FIGURE 1. SWITCHING TIMES

Test Circuits and Waveforms (Continued)



Logic input waveform is inverted for switches that have the opposite logic sense.

FIGURE 2A. MEASUREMENT POINTS



Repeat test for all switches. C_L includes fixture and stray capacitance.

FIGURE 2B. TEST CIRCUIT

FIGURE 2. CHARGE INJECTION

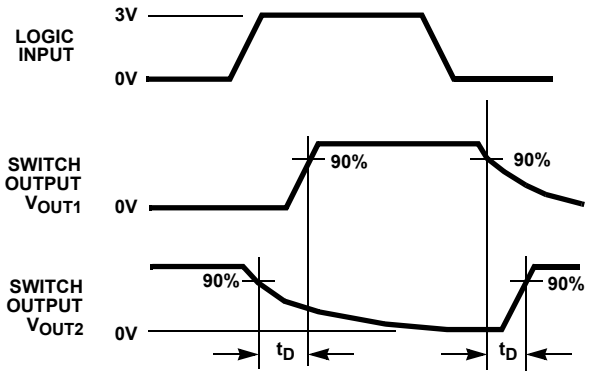
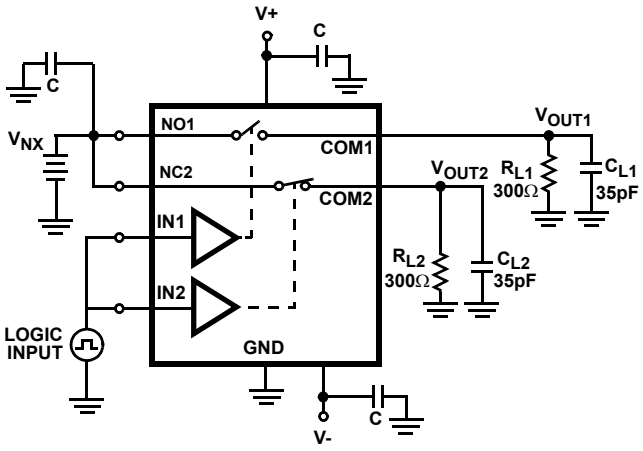


FIGURE 3A. MEASUREMENT POINTS

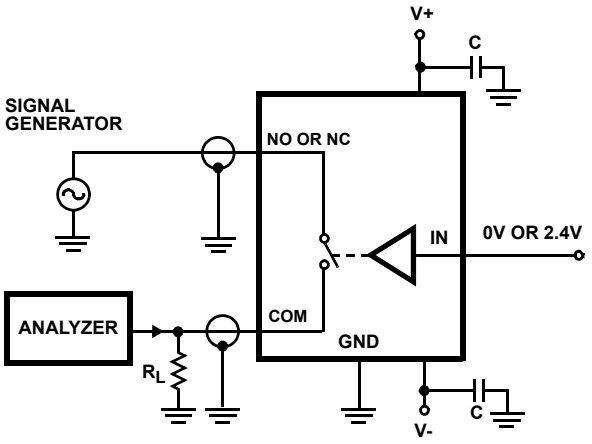


C_L includes fixture and stray capacitance.

Reconfigure accordingly to test SW3 and SW4.

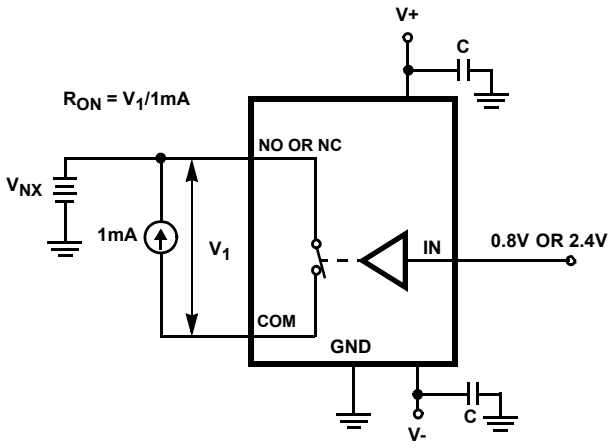
FIGURE 3B. TEST CIRCUIT

FIGURE 3. BREAK-BEFORE-MAKE TIME (ISL84523 ONLY)



Repeat test for all switches.

FIGURE 4. OFF ISOLATION TEST CIRCUIT



Repeat test for all switches.

FIGURE 5. R_{ON} TEST CIRCUIT

Test Circuits and Waveforms (Continued)

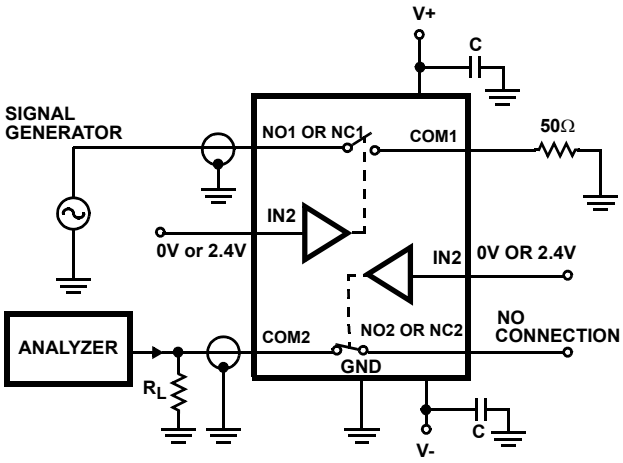


FIGURE 6. CROSSTALK TEST CIRCUIT

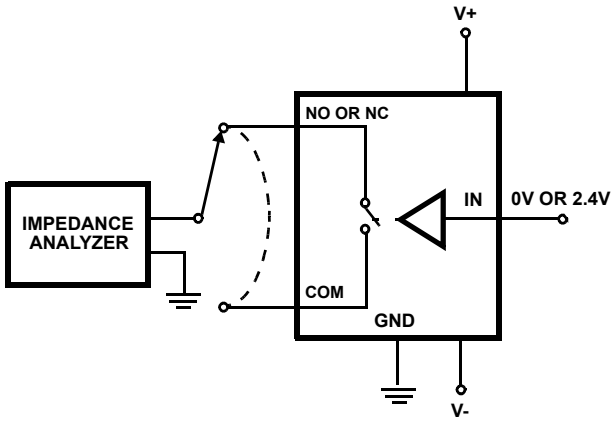


FIGURE 7. CAPACITANCE TEST CIRCUIT

Detailed Description

The ISL84521, ISL84522, ISL84523 quad analog switches offer precise switching capability from a bipolar ±2V to ±6V or a single 2V to 12V supply with low on-resistance (65Ω) and high speed switching (t_{ON} = 45ns, t_{OFF} = 15ns). The devices are especially well suited to portable battery powered equipment thanks to the low operating supply voltage (2V), low power consumption (1µW) and low leakage currents (1nA max). High frequency applications also benefit from the wide bandwidth, and the very high OFF isolation and crosstalk rejection.

Supply Sequencing And Overvoltage Protection

As with any CMOS device, proper power supply sequencing is required to protect the device from excessive input currents which might permanently damage the IC. All I/O pins contain ESD protection diodes from the pin to V+ and to V- (Figure 8). To prevent forward biasing these diodes, V+ and V- must be applied before any input signals, and input signal voltages must remain between V+ and V-. If these conditions cannot be guaranteed, then one of the following two protection methods should be employed.

Logic inputs can easily be protected by adding a 1kΩ resistor in series with the input (Figure 8). The resistor limits the input current below the threshold that produces permanent damage, and the sub-microamp input current produces an insignificant voltage drop during normal operation.

Adding a series resistor to the switch input defeats the purpose of using a low R_{ON} switch, so two small signal diodes can be added in series with the supply pins to provide overvoltage protection for all pins (Figure 8). These additional diodes limit the analog signal from 1V below V+ to 1V above V-. The low leakage current performance is unaffected by this approach, but the switch resistance may increase, especially at low supply voltages.

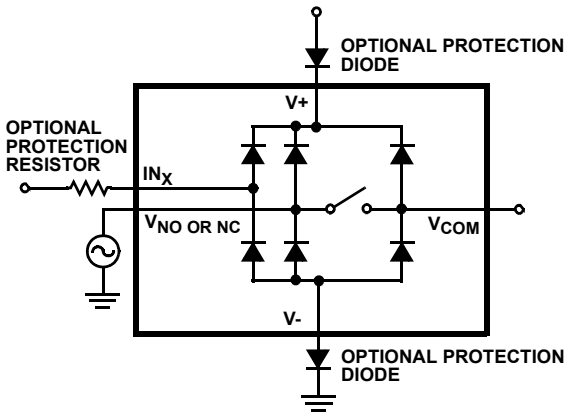


FIGURE 8. OVERVOLTAGE PROTECTION

Power-Supply Considerations

The ISL8452X construction is typical of most CMOS analog switches, in that they have three supply pins: V+, V-, and GND. V+ and V- drive the internal CMOS switches and set their analog voltage limits, so there are no connections between the analog signal path and GND. Unlike switches with a 13V maximum supply voltage, the ISL8452X 15V maximum supply voltage provides plenty of room for the 10% tolerance of 12V supplies (±6V or 12V single supply), as well as room for overshoot and noise spikes.

This family of switches performs equally well when operated with bipolar or single voltage supplies, and bipolar supplies need not be symmetrical. The minimum recommended supply voltage is 2V or ±2V. It is important to note that the input signal range, switching times, and ON-resistance degrade at lower supply voltages. Refer to the electrical specification tables and *Typical Performance Curves* for details.

V+ and GND power the internal logic (thus setting the digital switching point) and level shifters. The level shifters convert the logic levels to switched V+ and V- signals to drive the analog switch gate terminals, so switch parameters - especially R_{ON} - are strong functions of both supplies.

Logic-Level Thresholds

V+ and GND power the internal logic stages, so V- has no affect on logic thresholds. This switch family is TTL compatible (0.8V and 2.4V) over a V+ supply range of 2.5V to 10V. At 12V the V_{IH} level is about 2.7V, so for best results use a logic family the provides a V_{OH} greater than 3V.

The digital input stages draw supply current whenever the digital input voltage is not at one of the supply rails. Driving the digital input signals from GND to V+ with a fast transition time minimizes power dissipation.

High-Frequency Performance

In 50Ω systems, signal response is reasonably flat even past 300MHz (Figure 15), with a small signal -3dB bandwidth in excess of 400MHz, and a large signal bandwidth exceeding 300MHz.

An off switch acts like a capacitor and passes higher frequencies with less attenuation, resulting in signal feedthrough from a switch's input to its output. OFF Isolation is the resistance to this feedthrough, while Crosstalk indicates the amount of feedthrough from one switch to another. Figure 16 details the high OFF Isolation and Crosstalk rejection provided by this family. At 10MHz, OFF isolation is about 50dB in 50Ω systems, decreasing approximately 20dB per decade as frequency increases. Higher load impedances decrease OFF Isolation and Crosstalk rejection due to the voltage divider action of the switch OFF impedance and the load impedance.

Leakage Considerations

Reverse ESD protection diodes are internally connected between each analog-signal pin and both V+ and V-. One of these diodes conducts if any analog signal exceeds V+ or V-.

Virtually all the analog leakage current comes from the ESD diodes to V+ or V-. Although the ESD diodes on a given signal pin are identical and therefore fairly well balanced, they are reverse biased differently. Each is biased by either V+ or V- and the analog signal. This means their leakages will vary as the signal varies. The difference in the two diode leakages to the V+ and V- pins constitutes the analog-signal-path leakage current. All analog leakage current flows between each pin and one of the supply terminals, not to the other switch terminal. This is why both sides of a given switch can show leakage currents of the same or opposite polarity. There is no connection between the analog signal paths and GND.

Typical Performance Curves $T_A = 25^oC$, Unless Otherwise Specified

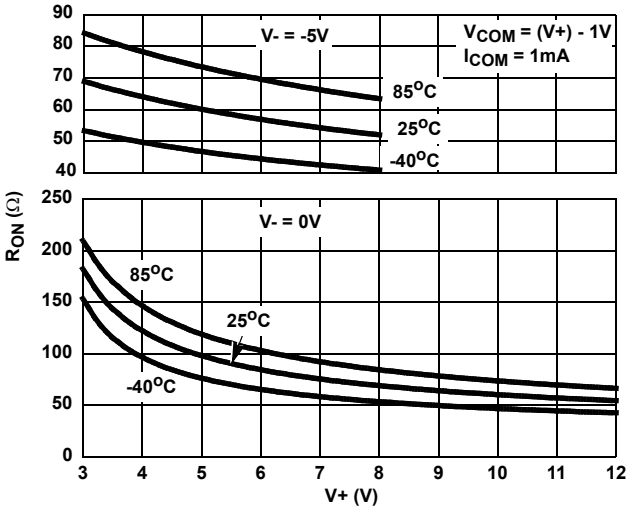


FIGURE 9. ON RESISTANCE vs SUPPLY VOLTAGE

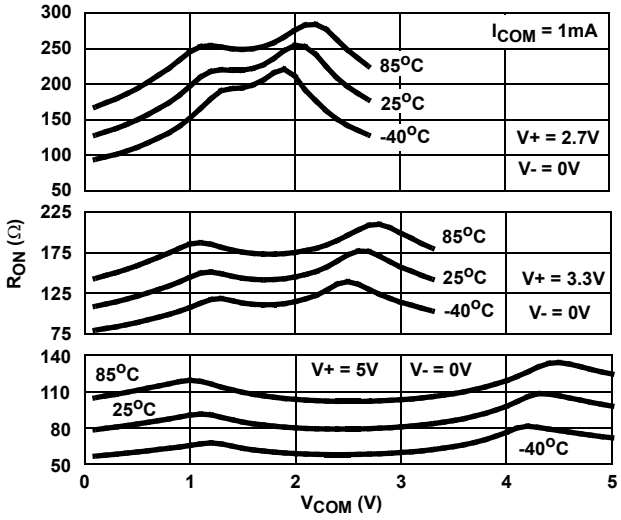


FIGURE 10. ON RESISTANCE vs SWITCH VOLTAGE

Typical Performance Curves $T_A = 25^oC$, Unless Otherwise Specified **(Continued)**

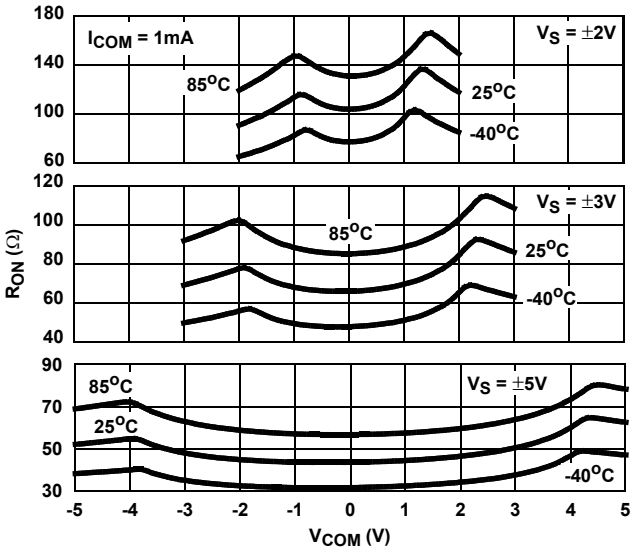


FIGURE 11. ON RESISTANCE vs SWITCH VOLTAGE

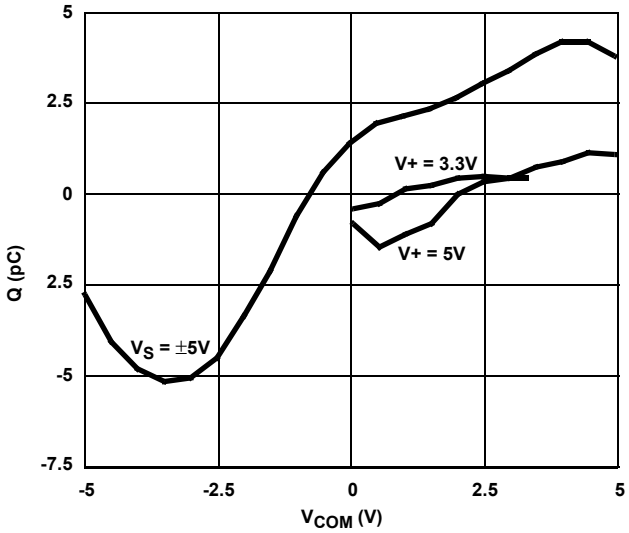


FIGURE 12. CHARGE INJECTION vs SWITCH VOLTAGE

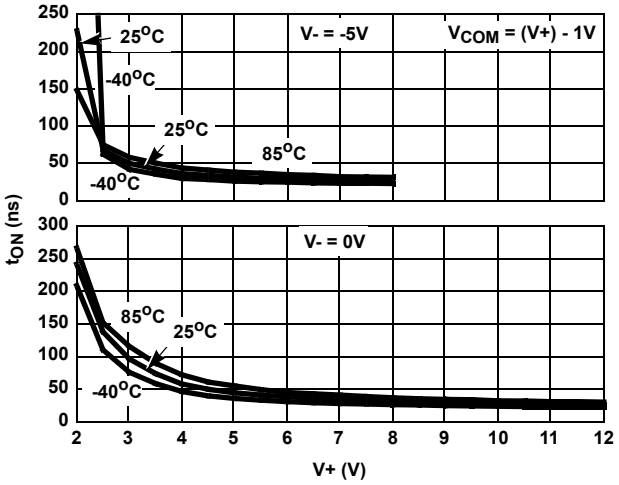


FIGURE 13. TURN - ON TIME vs SUPPLY VOLTAGE

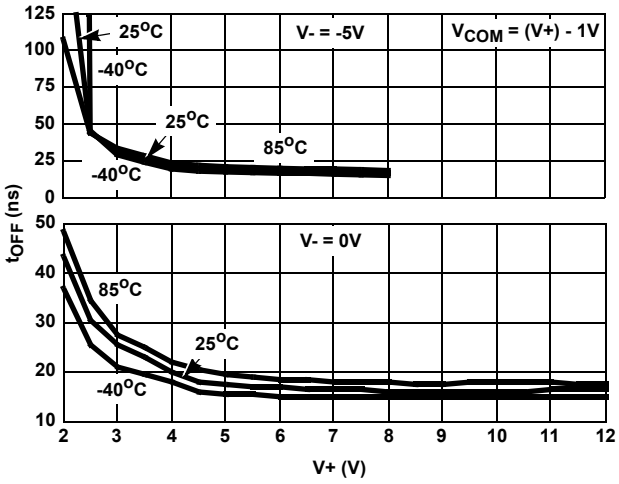


FIGURE 14. TURN - OFF TIME vs SUPPLY VOLTAGE

Typical Performance Curves $T_A = 25^oC$, Unless Otherwise Specified **(Continued)**

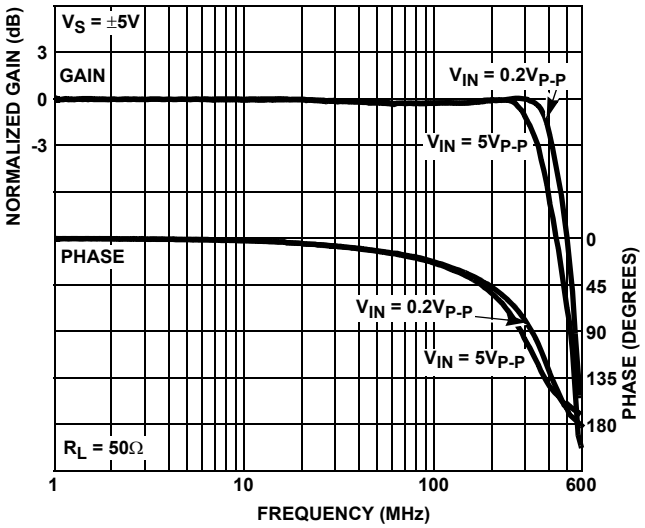


FIGURE 15. FREQUENCY RESPONSE

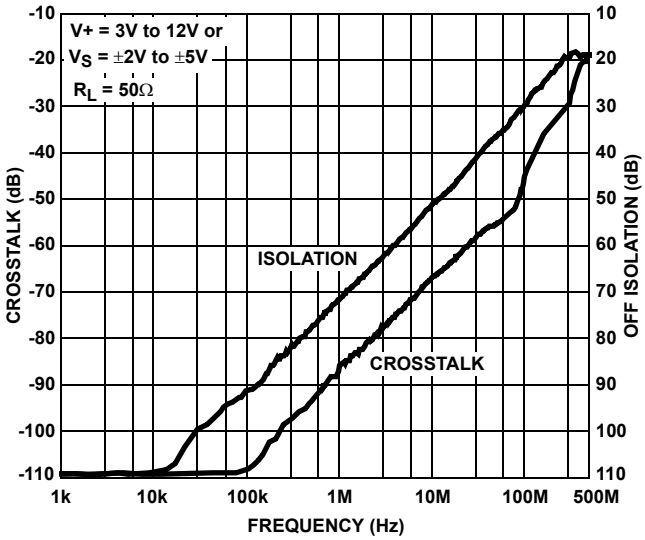


FIGURE 16. CROSSTALK AND OFF ISOLATION

Die Characteristics

SUBSTRATE POTENTIAL (POWERED UP):

V-

TRANSISTOR COUNT:

ISL84521: 188
ISL84522: 188
ISL84523: 188

PROCESS:

Si Gate CMOS

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please go to the web to make sure that you have the latest revision.

DATE	REVISION	CHANGE
August 10, 2015	FN6031.4	Updated Ordering Information table on page 2. Added Revision History and About Intersil sections. Updated Package Outline Drawing (POD) M16.173 with the latest version. Changes from Rev. 1 to Rev 2 are as follows: -Convert to new POD format by moving dimensions from table onto drawing and adding land pattern. No dimension changes.

About Intersil

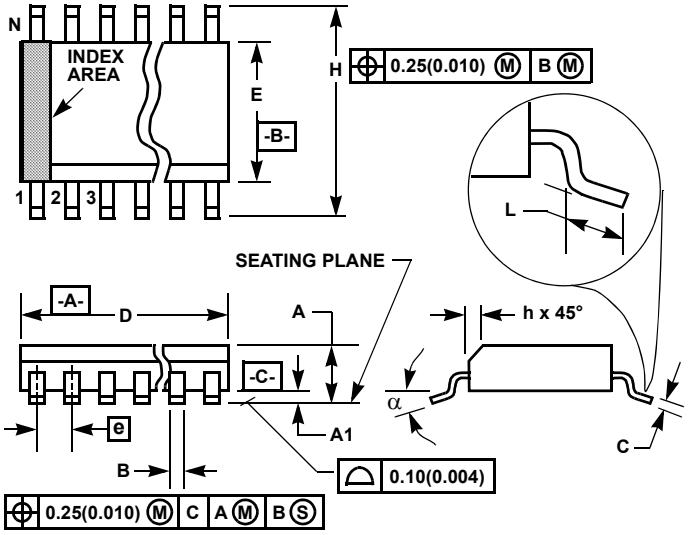
Intersil Corporation is a leading provider of innovative power management and precision analog solutions. The company's products address some of the largest markets within the industrial and infrastructure, mobile computing and high-end consumer markets.

For the most updated datasheet, application notes, related documentation and related parts, please see the respective product information page found at www.intersil.com.

You may report errors or suggestions for improving this datasheet by visiting www.intersil.com/ask.

Reliability reports are also available from our website at www.intersil.com/support

Small Outline Plastic Packages (SOIC)



NOTES:

1. Symbols are defined in the “MO Series Symbol List” in Section 2.2 of Publication Number 95.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension “D” does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension “E” does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. “L” is the length of terminal for soldering to a substrate.
7. “N” is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. The lead width “B”, as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch).
10. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.

M16.15 (JEDEC MS-012-AC ISSUE C)
16 LEAD NARROW BODY SMALL OUTLINE PLASTIC PACKAGE

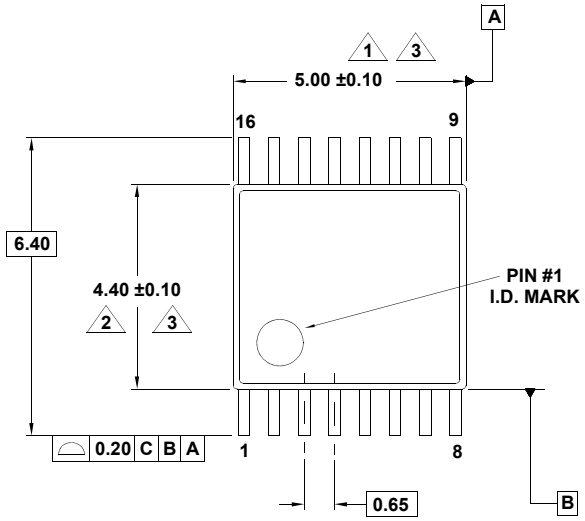
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.0532	0.0688	1.35	1.75	-
A1	0.0040	0.0098	0.10	0.25	-
B	0.013	0.020	0.33	0.51	9
C	0.0075	0.0098	0.19	0.25	-
D	0.3859	0.3937	9.80	10.00	3
E	0.1497	0.1574	3.80	4.00	4
e	0.050 BSC		1.27 BSC		-
H	0.2284	0.2440	5.80	6.20	-
h	0.0099	0.0196	0.25	0.50	5
L	0.016	0.050	0.40	1.27	6
N	16		16		7
α	0°	8°	0°	8°	-

Rev. 1 6/05

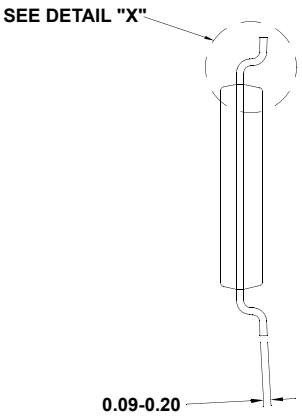
Package Outline Drawing

M16.173

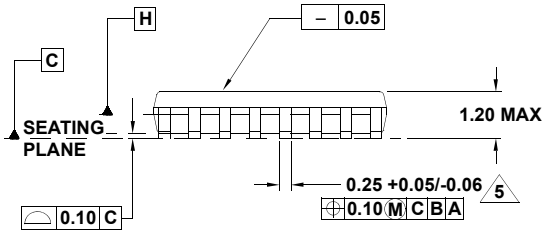
16 LEAD THIN SHRINK SMALL OUTLINE PACKAGE (TSSOP)
Rev 2, 5/10



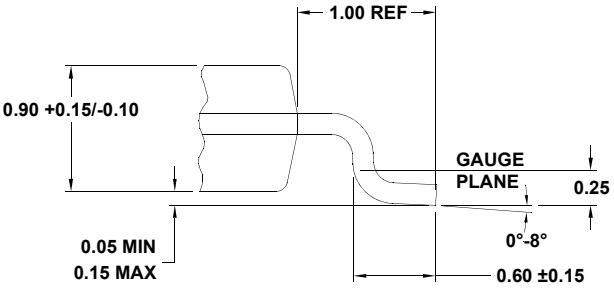
TOP VIEW



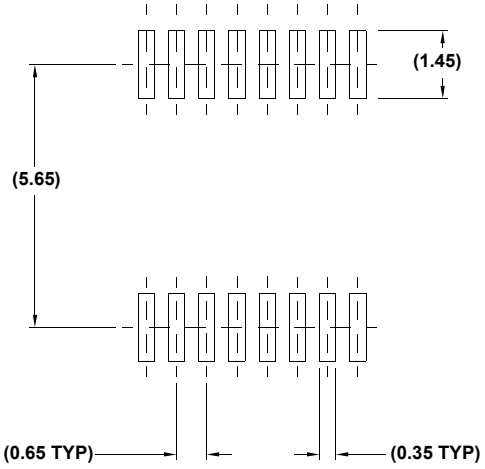
END VIEW



SIDE VIEW



DETAIL "X"



TYPICAL RECOMMENDED LAND PATTERN

NOTES:

1. Dimension does not include mold flash, protrusions or gate burrs. Mold flash, protrusions or gate burrs shall not exceed 0.15 per side.
2. Dimension does not include interlead flash or protrusion. Interlead flash or protrusion shall not exceed 0.25 per side.
3. Dimensions are measured at datum plane H.
4. Dimensioning and tolerancing per ASME Y14.5M-1994.
5. Dimension does not include dambar protrusion. Allowable protrusion shall be 0.08mm total in excess of dimension at maximum material condition. Minimum space between protrusion and adjacent lead is 0.07mm.
6. Dimension in ( ) are for reference only.
7. Conforms to JEDEC MO-153.