ATA6625

LIN Bus Transceiver with Integrated Voltage Regulator

DATASHEET

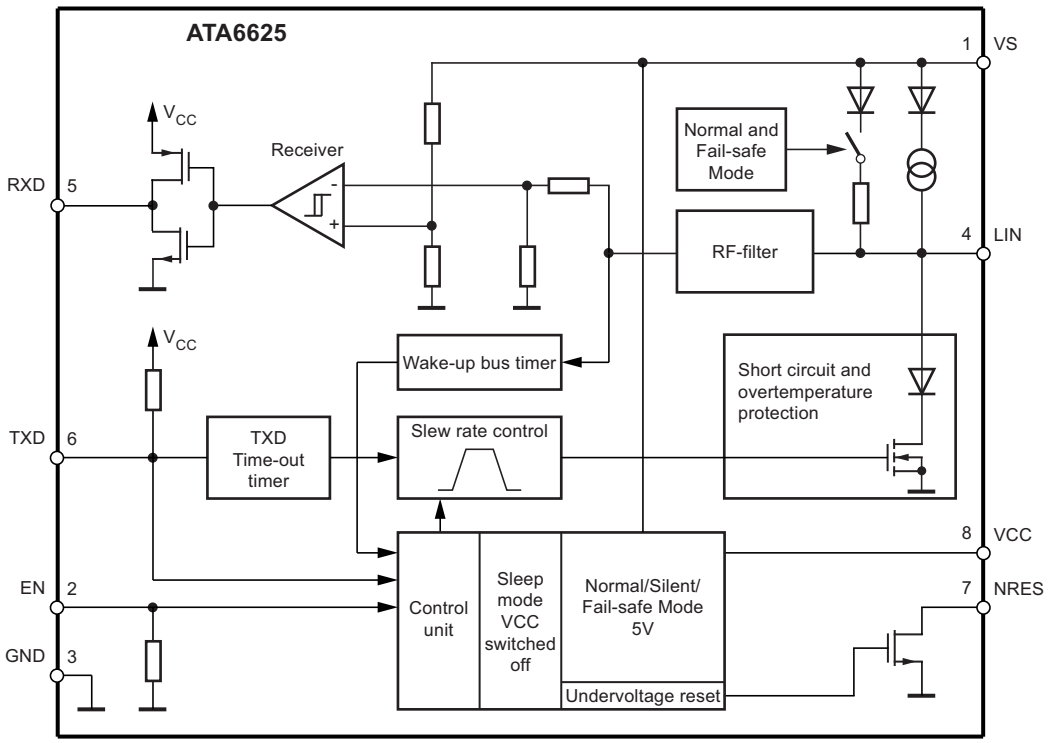
Features

- Supply voltage up to 40V
- Operating voltage V_S = 5V to 28V
- Typically 9µA supply current during sleep mode
- Typically 47µA Supply current in silent mode
- Very low current consumption at low supply voltages (2V < V_S < 5.5V): typically 130µA
- Linear low-drop voltage regulator, 85mA current capability:
  - MLC (multi-layer ceramic) capacitor with 0Ω ESR
  - Normal, fail-safe, and silent mode:
    - V_{CC} = 5.0V ±2%
  - Sleep mode: V_{CC} is switched off
- V_{CC} undervoltage detection with reset open drain output NRES (4ms reset time)
- Voltage regulator is short-circuit and over-temperature protected
- LIN physical layer according to LIN 2.0, 2.1, 2.2, 2.2A and SAEJ2602-2
- Wake-up capability via LIN bus (100µs dominant)
- TXD time-out timer
- Bus pin is overtemperature and short-circuit protected versus GND and battery
- Advanced EMC and ESD performance
- Fulfills the OEM “Hardware Requirements for LIN in Automotive Applications Rev1.3”
- Interference and damage protection according to ISO7637
- Qualified according to AEC-Q100
- Package: SO8 and DFN8 with wettable flanks (Moisture Sensitivity Level 1)

1. Description

The Atmel® ATA6625 is a fully integrated LIN transceiver, designed according to the LIN specification 2.0, 2.1, 2.2, 2.2A and SAEJ2602-2, with a low-drop voltage regulator (5V/85mA). The combination of voltage regulator and bus transceiver makes it possible to develop simple, but powerful, slave nodes in LIN Bus systems. The Atmel ATA6625 is designed to handle the low-speed data communication in vehicles (for example, in convenience electronics). Improved slope control at the LIN driver ensures secure data communication up to 20kBaud. The bus output is designed to withstand high voltage. Sleep mode (voltage regulator switched off) and silent mode (communication off; V_{CC} voltage on) guarantee minimized current consumption.

Figure 1-1. Block Diagram



2. Pin Configuration

Figure 2-1. Pinning

Table 2-1. Pin Description

Pin	Symbol	Function
1	VS	Battery supply
2	EN	Enables normal mode if the input is high
3	GND	Ground, heat sink
4	LIN	LIN bus line input/output
5	RXD	Receive data output
6	TXD	Transmit data input
7	NRES	Output undervoltage reset, low at reset
8	VCC	Output voltage regulator 5V/85mA
Backside		Heat slug, internally connected to the GND pin (only DFN8 package)

3. Functional Description

3.1 Physical Layer Compatibility

Since the LIN physical layer is independent from higher LIN layers (e.g., LIN protocol layer), all nodes with a LIN physical layer according to revision 2.x can be mixed with LIN physical layer nodes, which are according to older versions (i.e., LIN 1.0, LIN 1.1, LIN 1.2, LIN 1.3) without any restrictions.

3.2 Supply Pin (VS)

LIN operating voltage is V_S = 5V to 28V. An undervoltage detection is implemented to disable transmission if V_S falls below 5V, in order to avoid false bus messages. After switching on V_S, the IC starts with the fail-safe mode and the voltage regulator is switched on.

The supply current in sleep mode is typically 9µA and 47µA in silent mode.

3.3 Ground Pin (GND)

The IC does not affect the LIN Bus in the event of GND disconnection. It is able to handle a ground shift up to 11.5% of V_S.

3.4 Voltage Regulator Output Pin (VCC)

The internal 5V voltage regulator is capable of driving loads up to 85mA, supplying the microcontroller and other ICs on the PCB and is protected against overload by means of current limitation and overtemperature shut-down. Furthermore, the output voltage is monitored and will cause a reset signal at the NRES output pin if it drops below a defined threshold V_{thun}.

3.5 Undervoltage Reset Output (NRES)

If the V_{CC} voltage falls below the undervoltage detection threshold of V_{thun}, NRES switches to low after tres_f (Figure 6-1 on page 11). Even if V_{CC} = 0V the NRES stays low, because it is internally driven from the V_S voltage. If V_S voltage ramps down, NRES stays low until V_S < 1.5V and then becomes highly resistant.

The implemented undervoltage delay keeps NRES low for t_{Reset} = 4ms after V_{CC} reaches its nominal value.

3.6 Bus Pin (LIN)

A low-side driver with internal current limitation and thermal shutdown as well as an internal pull-up resistor according to LIN specification 2.x is implemented. The voltage range is from –27V to +40V. This pin exhibits no reverse current from the LIN bus to V_S, even in the event of a GND shift or V_{Batt} disconnection. The LIN receiver thresholds are compatible with the LIN protocol specification.

The fall time (from recessive to dominant) and the rise time (from dominant to recessive) are slope controlled.

3.7 Input Pin (TXD)

In normal mode the TXD pin is the microcontroller interface to control the state of the LIN output. TXD must be pulled to ground in order to drive the LIN bus low. If TXD is high or unconnected (internal pull-up resistor), the LIN output transistor is turned off and the bus is in the recessive state.

3.8 Dominant Time-out Function (TXD)

The TXD input has an internal pull-up resistor. An internal timer prevents the bus line from being driven permanently in the dominant state. If TXD is forced to low longer than t_{dom} (typ. 40ms), the LIN bus driver is switched to the recessive state.

To reactivate the LIN bus driver, switch TXD to high (> 10µs).

3.9 Output Pin (RXD)

In normal mode this pin reports the state of the LIN bus to the microcontroller. LIN high (recessive state) is indicated by a high level at RXD; LIN low (dominant state) is indicated by a low level at RXD.

The output is a push-pull stage switching between VCC and GND. The AC characteristics are measured by an external load capacitor of 20pF.

In silent mode the RXD output switches to high.

3.10 Enable Input Pin (EN)

The Enable Input pin controls the operation mode of the device. If EN is high, the circuit is in normal mode, with transmission paths from TXD to LIN and from LIN to RXD both active. The VCC voltage regulator operates with 5V/85mA output capability.

If EN is switched to low while TXD is still high, the device is forced to silent mode. No data transmission is then possible, and the current consumption is reduced to I_{VS} typ. 47µA. The VCC regulator has its full functionality.

If EN is switched to low while TXD is low, the device is forced to sleep mode. No data transmission is possible, and the voltage regulator is switched off.

4. Modes of Operation

Figure 4-1. Modes of Operation

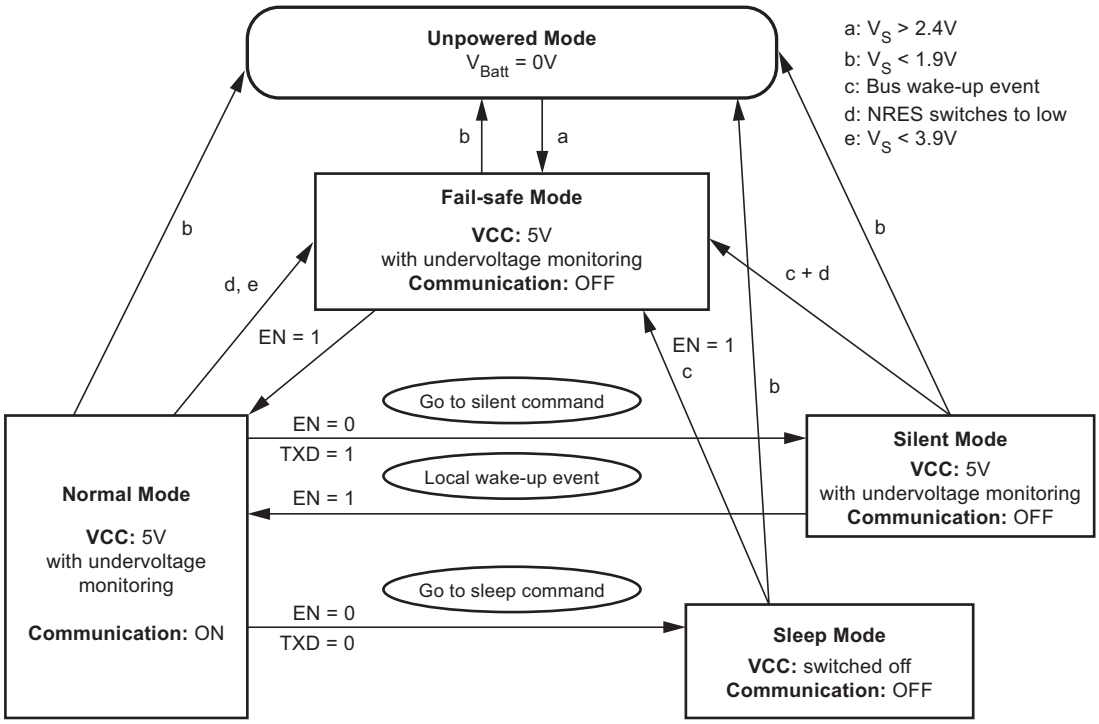


Table 4-1. Modes of Operation

Mode of Operation	Transceiver	V_{CC}	RXD	LIN
Fail safe	OFF	5V	High, Except after wake-up	Recessive
Normal	ON	5V	LIN depending	TXD depending
Silent	OFF	5V	High	Recessive
Sleep	OFF	0V	0V	Recessive

4.1 Normal Mode

This is the normal transmitting and receiving mode of the LIN Interface, in accordance with LIN specification 2.x. The V_{CC} voltage regulator operates with a 5V output voltage, with a low tolerance of ±2% and a maximum output current of 85mA.

If an undervoltage condition occurs, NRES is switched to low and the IC changes its state to fail-safe mode.

4.2 Silent Mode

A falling edge at EN while TXD is high switches the IC into silent mode. The TXD Signal has to be logic high during the mode select window (Figure 4-2 on page 6). The transmission path is disabled in silent mode. The overall supply current from V_{Batt} is a combination of the I_{VSsi} = 47µA plus the V_{CC} regulator output current I_{VCC}.

In silent mode the internal slave termination between pin LIN and pin VS is disabled, and only a weak pull-up current (typically 9µA) between pin LIN and pin VS is present. The silent mode can be activated independently from the current level on pin LIN.

If an undervoltage condition occurs, NRES is switched to low and the IC changes its state to fail-safe mode.

A voltage less than the LIN Pre-wake detection V_{LINL} at pin LIN activates the internal LIN receiver and starts the wake-up detection timer.

A falling edge at the LIN pin followed by a dominant bus level maintained for a certain time period (> t_{bus}) and the following rising edge at pin LIN (see Figure 4-3 on page 7) results in a remote wake-up request.

The device switches from silent mode to fail-safe mode, the voltage regulator remains on and the internal LIN slave termination resistor between the LIN pin and the VS pin is switched on.

The remote wake-up request is indicated by a low level at pin RXD to interrupt the microcontroller (Figure 4-3 on page 7). EN high can be used to switch directly to normal mode.

Figure 4-2. Switch to Silent Mode

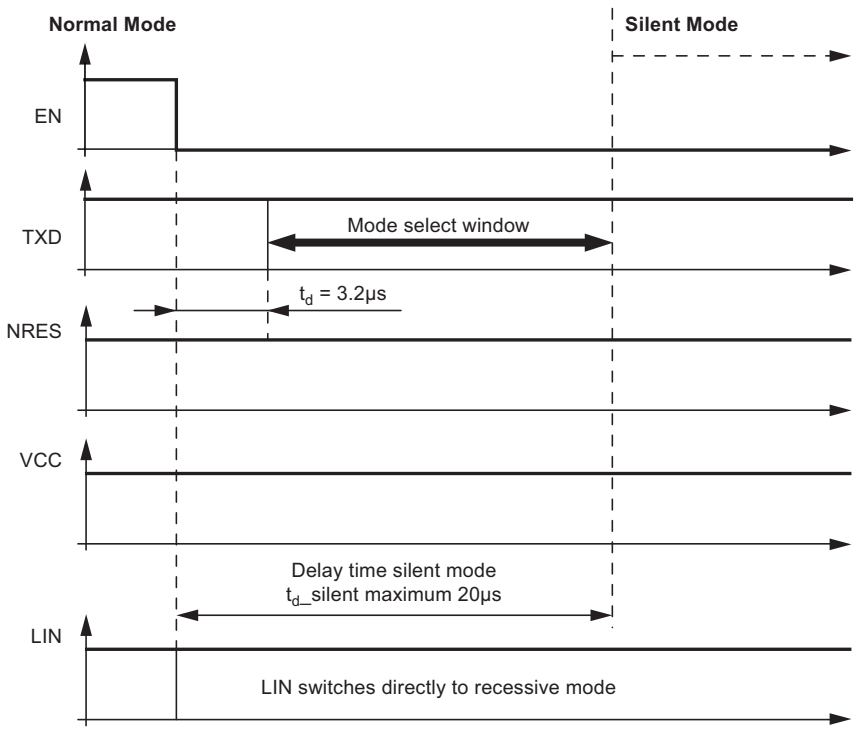
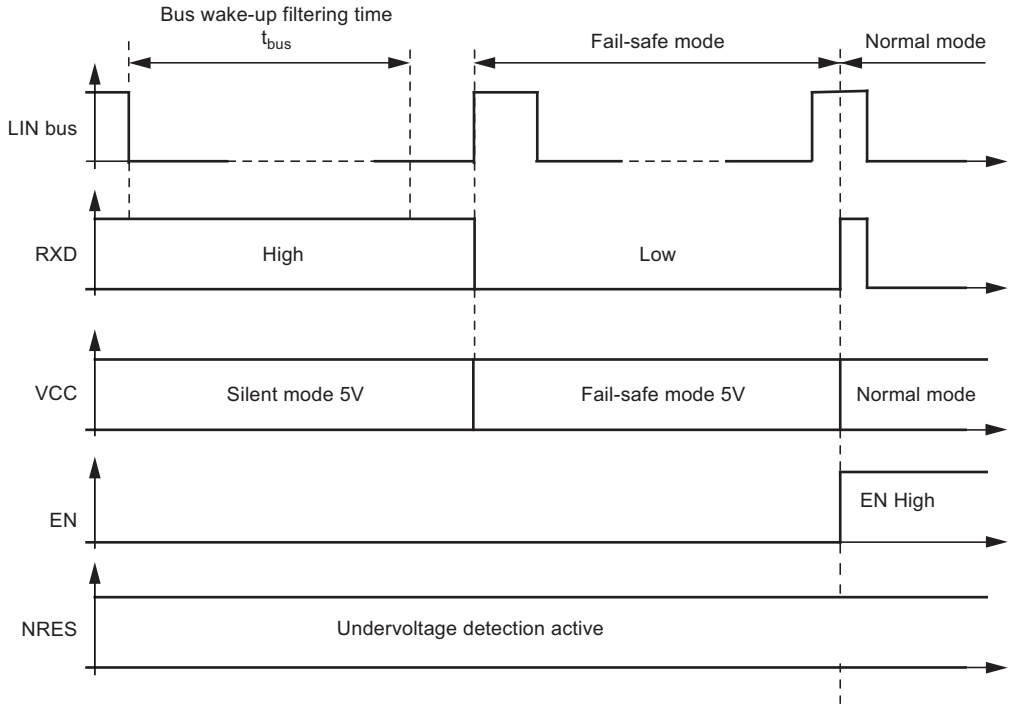


Figure 4-3. LIN Wake-up Waveform Diagram from Silent Mode



4.3 Sleep Mode

A falling edge at EN while TXD is low switches the IC into sleep mode. The TXD Signal has to be logic low during the mode select window (Figure 4-4 on page 8). To avoid influencing the LIN-pin during the switch to sleep mode, it is possible to switch the EN up to 3.2µs earlier to LOW than the TXD. Even if the two falling edges at TXD and EN occur at the same time, the LIN line will remain uninfluenced.

In sleep mode the transmission path is disabled. The supply current $I_{VSsleep}$ from V_{Batt} is typically 9µA. The V_{CC} regulator is switched off, NRES and RXD are low. The internal slave termination between pin LIN and pin VS is disabled, only a weak pull-up current (typically 10µA) between pin LIN and pin VS is present. Sleep mode can be activated independently from the current level on pin LIN.

A voltage less than the LIN Pre-wake detection V_{LINL} at pin LIN activates the internal LIN receiver and starts the wake-up detection timer.

A falling edge at the LIN pin followed by a dominant bus level maintained for a certain time period (> t_{bus}) and a following rising edge at pin LIN results in a remote wake-up request. The device switches from sleep mode to fail-safe mode.

The V_{CC} regulator is activated and the internal LIN slave termination resistor between the LIN pin and the VS pin is switched on.

The remote wake-up request is indicated by a low level at the RXD pin to interrupt the microcontroller (Figure 4-5 on page 8).

EN high can be used to switch directly from sleep to fail-safe mode. If EN is still high after VCC ramp up and undervoltage reset time, the IC switches to normal mode.

Figure 4-4. Switch to Sleep Mode

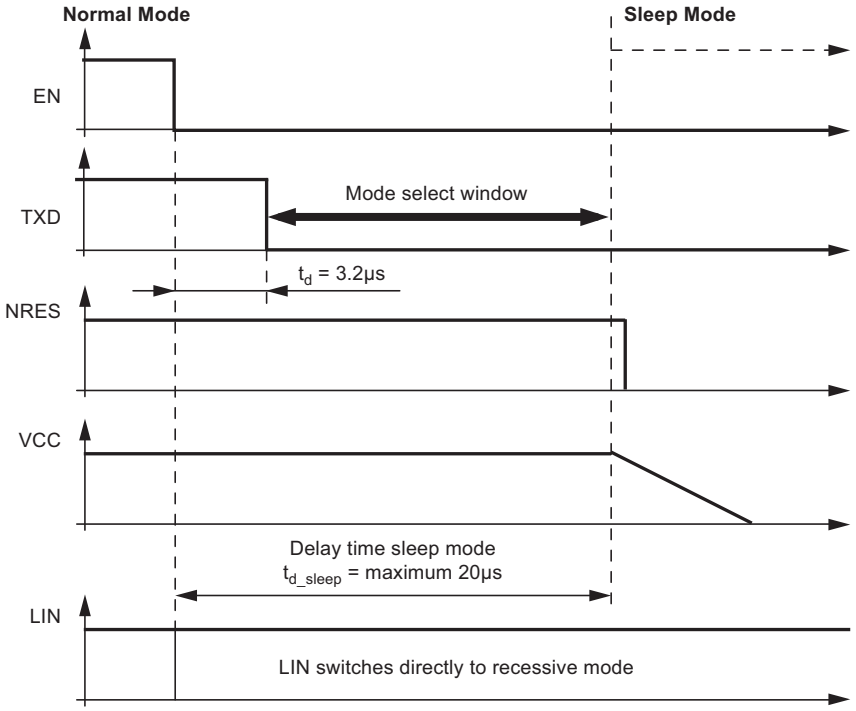
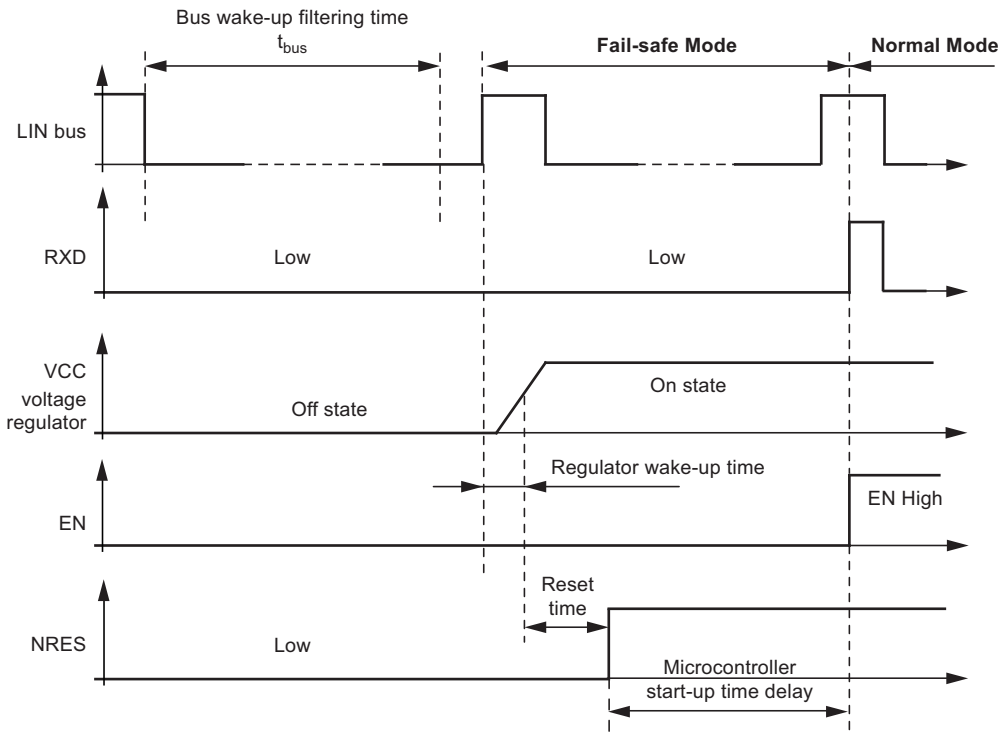


Figure 4-5. LIN Wake-up Diagram from Sleep Mode



4.4 Fail-safe Mode

At system power-up the device automatically switches to fail-safe mode. The voltage regulator is switched on (see Figure 6-1 on page 11). The NRES output switches to low for t_{res} = 4ms and gives a reset to the microcontroller. LIN communication is switched off. The IC stays in this mode until EN is switched to high, and changes then to the normal mode. A power down of V_{Batt} (V_S < 1.9V) during silent or sleep mode switches the IC into the unpowered mode after power up. A logic low at NRES switches the IC into fail-safe mode directly.

4.5 Unpowered Mode

If you connect battery voltage to the application circuit, the voltage at the VS pin increases according to the block capacitor (see Figure 6-1 on page 11). After VS is higher than 2.4V, the IC mode changes from unpowered mode to fail-safe mode. The VCC output voltage reaches its nominal value after t_{VCC}. This time, t_{VCC}, depends on the VCC capacitor and the load.

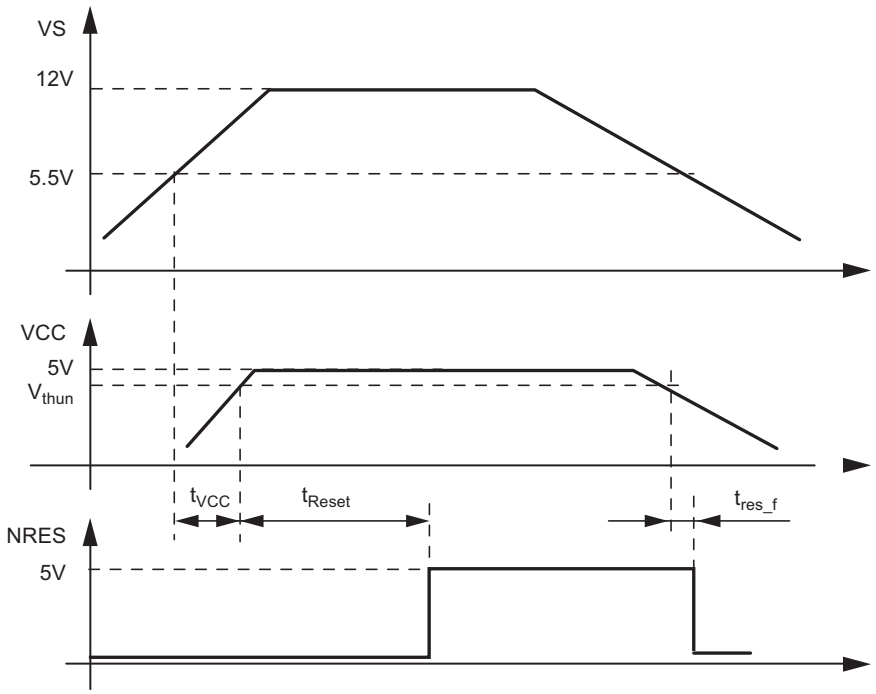
NRES is low for the reset time delay t_{Reset}; no mode change is possible during this time.

5. Fail-safe Features

- During a short-circuit at LIN to $V_{Battery}$, the output limits the output current to I_{BUS_lim}. Due to the power dissipation, the chip temperature exceeds T_{LINoff} and the LIN output is switched off. The chip cools down and after a hysteresis of T_{hys}, switches the output on again. RXD stays on high because LIN is high. During LIN overtemperature switch-off, the V_{CC} regulator is working independently.
- During a short-circuit from LIN to GND the IC can be switched into sleep or silent mode. If the short-circuit disappears, the IC starts with a remote wake-up.
- The reverse current is very low < 2µA at pin LIN during loss of V_{Batt}. This is optimal behavior for bus systems where some slave nodes are supplied from battery or ignition.
- During a short circuit at VCC, the output limits the output current to I_{VCClim}. Because of undervoltage, NRES switches to low and sends a reset to the microcontroller. The IC switches into fail-safe mode. If the chip temperature exceeds the value T_{VCCoff}, the V_{CC} output switches off. The chip cools down and after a hysteresis of T_{hys}, switches the output on again. Because of fail-safe mode, the V_{CC} voltage will switch on again although EN is switched off from the microcontroller. The microcontroller can then start with normal operation.
- Pin EN provides a pull-down resistor to force the transceiver into recessive mode if EN is disconnected.
- Pin RXD is set floating if V_{Batt} is disconnected.
- Pin TXD provides a pull-up resistor to force the transceiver into recessive mode if TXD is disconnected.
- If TXD is short-circuited to GND, it is possible to switch to sleep mode via ENABLE after t_{dom} > 20ms.
- If the TXD pin stays at GND level while switching into normal mode, it must be pulled to high level longer than 10µs before the LIN driver can be activated. This feature prevents the bus line from being accidentally driven to dominant state after normal mode has been activated (e.g., in the case of a short circuit at TXD to GND).

6. Voltage Regulator

Figure 6-1. V_{CC} Voltage Regulator: Ramp Up and Undervoltage



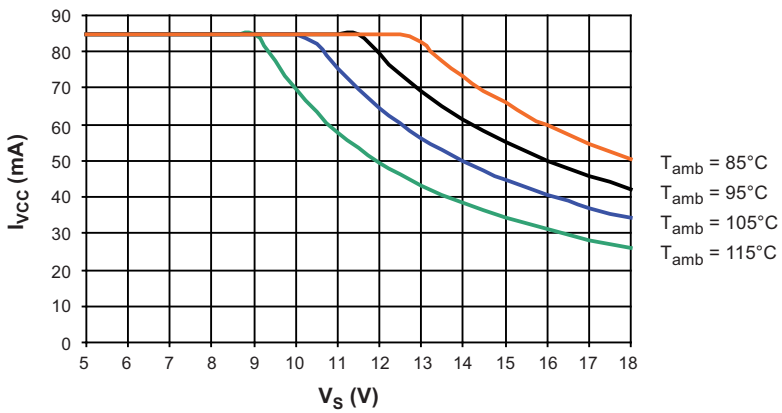
The voltage regulator needs an external capacitor for compensation and to smooth the disturbances from the microcontroller. It is recommended to use an MLC capacitor with C > 1.8µF and a ceramic capacitor with C = 100nF. The values of these capacitors can be varied by the customer, depending on the application.

With a special SO8 package (fused lead frame to pin 3) an R_{thja} of 80K/W is achieved.
Therefore, it is recommended to connect pin 3 with a wide GND plate on the printed board to get a good heat sink.

The main power dissipation of the IC is created from the V_{CC} output current I_{VCC}, which is needed for the application.

Figure 6-2 shows the safe operating area of the Atmel® ATA6625 in the SO8 package.

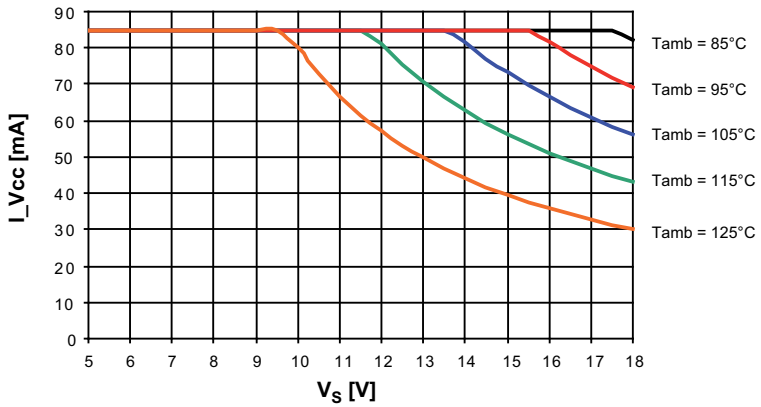
Figure 6-2. SO8 Package Power Dissipation: Safe Operating Area: V_{CC} Output Current versus Supply Voltage V_S at Different Ambient Temperatures Due to R_{thja} = 80K/W



When the Atmel® ATA6625 in the DFN8 package is being soldered onto the PCB it is mandatory to connect the heat slug with a wide GND plate on the printed board to get a good heat sink. With this an R_{thja} of 50K/W can be achieved.

Figure 6-3 shows the safe operating area of the Atmel ATA6625 in the DFN8 package.

Figure 6-3. DFN8 Power Dissipation: Safe Operating Area: Regulator's Output Current versus Supply Voltage V_S at Different Ambient Temperatures due to R_{thja} = 50K/W



To program the microcontroller it may be necessary to supply the V_{CC} output via an external power supply while the V_S Pin of the system basis chip is disconnected. This will not affect the system basis chip.

7. Absolute Maximum Ratings

Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Parameters	Symbol	Min.	Typ.	Max.	Unit
Supply voltage V_S	V_S	–0.3		+40	V
Pulse time ≤ 500ms T_a = 25°C Output current I_{VCC} ≤ 85mA	V_S			+43.5	V
Pulse time ≤ 2min T_a = 25°C Output current I_{VCC} ≤ 85mA	V_S			28	V
Logic pins (RxD, TxD, EN, NRES)		–0.3		+5.5	V
Output current NRES	I_{NRES}			+2	mA
LIN - DC voltage - Pulse time < 500ms	V_{LIN}	–27		+40 +43.5	V V
V_{CC} - DC voltage - DC input current		–0.3		+5.5 +200	V mA
ESD according to IBEE LIN EMC Test specification 1.0 following IEC 61000-4-2 - Pin VS, LIN to GND		±6			KV
ESD HBM following STM5.1 with 1.5kΩ/100pF - Pin VS, LIN to GND		±6			KV
HBM ESD ANSI/ESD-STM5.1 JESD22-A114 AEC-Q100 (002)		±3			KV
CDM ESD STM 5.3.1		±750			V
Machine Model ESD AEC-Q100-RevF(003)		±200			V
Junction temperature	T_j	–40		+150	°C
Storage temperature	T_s	–55		+150	°C

8. Thermal Characteristics SO8

Parameters	Symbol	Min.	Typ.	Max.	Unit
Thermal resistance junction to ambient, with a heat sink at GND (pin3) on the PCB	R_{thja}		80		K/W
Thermal shutdown of V_{CC} regulator	T_{VCCoff}	150	165	180	°C
Thermal shutdown of LIN output	T_{LINoff}	150	165	180	°C
Thermal shutdown hysteresis	T_{hys}		10		°C

9. Thermal Characteristics DFN8

Parameters	Symbol	Min.	Typ.	Max.	Unit
Thermal resistance junction to heat slug	R_{thjC}		10		K/W
Thermal resistance junction to ambient, where heat slug is soldered to PCB according to JEDEC	R_{thja}		50		K/W
Thermal shutdown of V_{CC} regulator	T_{VCCoff}	150	165	180	°C
Thermal shutdown of LIN output	T_{LINoff}	150	165	180	°C
Thermal shutdown hysteresis	T_{hys}		10		°C

10. Electrical Characteristics

5V < V_S < 28V, –40°C < T_j < 150°C; unless otherwise specified all values refer to GND pins.

No.	Parameters	Test Conditions	Pin	Symbol	Min.	Typ.	Max.	Unit	Type*
1	VS Pin								
1.1	Nominal DC voltage range		VS	V_S	5	13.5	28	V	A
1.2	Supply current in sleep mode	Sleep mode $V_{LIN} > V_S – 0.5V$ V_S < 14V, T = 27°C	VS	$I_{VSsleep}$	6	9	12	µA	B
		Sleep mode $V_{LIN} > V_S – 0.5V$ V_S < 14V	VS	$I_{VSsleep}$	3	10	15	µA	A
		Sleep mode, V_{LIN} = 0V bus shorted to GND V_S < 14V	VS	$I_{VSsleep\_short}$	20	50	100	µA	A
1.3	Supply current in silent mode (SBC) / Active mode (voltage regulator)	Bus recessive 5.5V< V_S < 14V without load at VCC T = 27°C	VS	$I_{VSsilent}$	30	47	58	µA	B
		Bus recessive 5.5V< V_S < 14V without load at VCC	VS	$I_{VSsilent}$	30	50	64	µA	A
		Bus recessive 2.0V< V_S < 5,5V without load at VCC	VS	$I_{VSsilent}$	50	130	170	µA	A
		Silent mode 5.5V< V_S < 14V bus shorted to GND without load at VCC	VS	$I_{VSsilent\_short}$	50	80	120	µA	A
1.4	Supply current in normal mode	Bus recessive V_S < 14V without load at VCC	VS	I_{VSrec}	150	230	300	µA	A
1.5	Supply current in normal mode	Bus dominant (internal LIN pull-up resistor active) V_S < 14V without load at VCC	VS	I_{VSdom}	200	700	950	µA	A

*) Type means: A = 100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter

10. Electrical Characteristics (Continued)

5V < V_S < 28V, –40°C < T_j < 150°C; unless otherwise specified all values refer to GND pins.

No.	Parameters	Test Conditions	Pin	Symbol	Min.	Typ.	Max.	Unit	Type*
1.6	Supply current in fail-safe mode	Bus recessive 5.5V < V_S < 14V without load at VCC	VS	I_{VSfail}	40	55	80	µA	A
		Bus recessive 2.0V < V_S < 5.5V without load at VCC	VS	I_{VSfail}	50	130	170	µA	A
1.7	V_S undervoltage threshold (switching from normal to fail-safe mode)		VS	V_{Sth}	3.9	4.4	4.9	V	A
1.8	V_S undervoltage threshold hysteresis		VS	V_{Sth_hys}	0.1	0.25	0.4	V	A
1.9	V_S operation threshold (switching to unpowered mode)		VS	V_{Sth_U}	1.9	2.15	2.4	V	A
1.10	V_S undervoltage threshold hysteresis		VS	$V_{Sth\_hys\_U}$	0.1	0.2	0.3	V	A
2	RXD Output Pin								
2.1	Low level output sink capability	Normal mode V_{LIN} = 0V I_{RXD} = 2mA	RXD	V_{RXDL}		0.2	0.4	V	A
2.2	High level output source capability	Normal mode V_{LIN} = V_S I_{RXD} = –2mA	RXD	V_{RXDH}	V_{CC} – 0.4V	V_{CC} – 0.2V		V	A
3	TXD Input Pin								
3.1	Low level voltage input		TXD	V_{TXDL}	–0.3		+0.8	V	A
3.2	High level voltage input		TXD	V_{TXDH}	2		V_{CC} + 0.3V	V	A
3.3	Pull-up resistor	V_{TXD} = 0V	TXD	R_{TXD}	40	70	100	kΩ	A
3.4	High level leakage current	V_{TXD} = VCC	TXD	I_{TXD}	–3		+3	µA	A
4	EN Input Pin								
4.1	Low level voltage input		EN	V_{ENL}	–0.3		+0.8	V	A
4.2	High level voltage input		EN	V_{ENH}	2		V_{CC} + 0.3V	V	A
4.3	Pull-down resistor	V_{EN} = VCC	EN	R_{EN}	50	125	200	kΩ	A
4.4	Low level input current	V_{EN} = 0V	EN	I_{EN}	–3		+3	µA	A
5	NRES Open Drain Output Pin								
5.1	Low level output voltage	V_S ≥ 5.5V I_{NRES} = 2mA	NRES	V_{NRESL}			0.25	V	A
5.2	Low level output low	10kΩ to 5V V_{CC} = 0V	NRES	V_{NRESLL}			0.14	V	D
5.3	Undervoltage reset time	V_S ≥ 5.5V C_{NRES} = 20pF	NRES	t_{Reset}	2	4	6	ms	A

*) Type means: A = 100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter

10. Electrical Characteristics (Continued)

5V < V_S < 28V, –40°C < T_j < 150°C; unless otherwise specified all values refer to GND pins.

No.	Parameters	Test Conditions	Pin	Symbol	Min.	Typ.	Max.	Unit	Type*
5.4	Reset debounce time for falling edge	V_S ≥ 5.5V C_{NRES} = 20pF	NRES	t_{res_f}	1.5		10	µs	A
5.5	Switch off leakage current	V_{NRES} = 5.5V	NRES	I_{NRES_Lf}	–3		+3	µA	A
7	VCC Voltage Regulator								
7.1	Output voltage VCC	5.5V < V_S < 18V (0mA to 50mA)	VCC	VCC_{nor}	4.9		5.1	V	A
		6V < V_S < 18V (0mA to 85mA)	VCC	VCC_{nor}	4.9		5.1	V	C
7.2	Output voltage V_{CC} at low V_S	4V < VS < 5.5V	VCC	VCC_{low}	$V_S – V_D$		5.1	V	A
7.3	Regulator drop voltage	VS > 4V, I_{VCC} = –20mA	VCC	V_{D1}		100	200	mV	A
7.4	Regulator drop voltage	VS > 4V, I_{VCC} = –50mA	VCC	V_{D2}		300	500	mV	A
7.5	Regulator drop voltage	VS > 3.3V, I_{VCC} = –15mA	VCC	V_{D3}			150	mV	A
7.6	Line regulation	5.5V < VS < 18V	VCC	VCC_{line}		0.1	0.2	%	A
7.7	Load regulation	5mA < I_{VCC} < 50mA	VCC	VCC_{load}		0.1	0.5	%	A
7.8	Power supply ripple rejection	10Hz to 100kHz C_{VCC} = 10µF VS = 14V, I_{VCC} = –15mA	VCC		50			dB	D
7.9	Output current limitation	VS > 5.5V	VCC	I_{VCClim}		–180	–120	mA	A
7.10	External load capacity	MLC capacitor	VCC	C_{load}	1.8	10		µF	D
7.11	VCC undervoltage threshold	Referred to VCC VS > 5.5V	VCC	V_{thunN}	4.2		4.8	V	A
7.12	Hysteresis of undervoltage threshold	Referred to VCC VS > 5.5V	VCC	$Vhys_{thun}$		250		mV	A
7.13	Ramp up time VS > 5.5V to VCC = 5V	C_{VCC} = 2.2µF I_{load} = –5mA at VCC	VCC	t_{VCC}		1	1.5	ms	A
8	LIN Bus Driver: Bus Load Conditions: Load 1 (Small): 1nF, 1kΩ, Load 2 (Large): 10nF, 500Ω, C_{RXD} = 20pF, Load 3 (Medium): 6.8nF, 660Ω, Characterized on Samples 10.6 and 10.7 Specifies the Timing Parameters for Proper Operation at 20kBit/s and 10.8 and 10.9 at 10.4kBit/s								
8.1	Driver recessive output voltage	Load1/Load2	LIN	V_{BUSrec}	0.9 × V_S		V_S	V	A
8.2	Driver dominant voltage	V_{VS} = 7V, R_{load} = 500Ω	LIN	$V_{\_LoSUP}$			1.2	V	A
8.3	Driver dominant voltage	V_{VS} = 18V, R_{load} = 500Ω	LIN	$V_{\_HiSUP}$			2	V	A
8.4	Driver dominant voltage	V_{VS} = 7V, R_{load} = 1000Ω	LIN	$V_{\_LoSUP\_1k}$	0.6			V	A
8.5	Driver dominant voltage	V_{VS} = 18V, R_{load} = 1000Ω	LIN	$V_{\_HiSUP\_1k}$	0.8			V	A
8.6	Pull–up resistor to V_S	The serial diode is mandatory	LIN	R_{LIN}	20	30	47	kΩ	A
8.7	Voltage drop at the serial diodes	In pull-up path with R_{slave} $I_{SerDiode}$ = 10mA	LIN	$V_{SerDiode}$	0.4		1.0	V	D
8.8	LIN current limitation V_{BUS} = V_{Batt_max}		LIN	I_{BUS_lim}	40	120	200	mA	A

*) Type means: A = 100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter

10. Electrical Characteristics (Continued)

5V < V_S < 28V, –40°C < T_j < 150°C; unless otherwise specified all values refer to GND pins.

No.	Parameters	Test Conditions	Pin	Symbol	Min.	Typ.	Max.	Unit	Type*
8.9	Input leakage current at the receiver including pull-up resistor as specified	Input Leakage current Driver off V_{BUS} = 0V V_{Batt} = 12V	LIN	$I_{BUS\_PAS\_dom}$	–1	–0.35		mA	A
8.10	Leakage current LIN recessive	Driver off 8V < V_{Batt} < 18V 8V < V_{BUS} < 18V $V_{BUS} \geq V_{Batt}$	LIN	$I_{BUS\_PAS\_rec}$		10	20	µA	A
8.11	Leakage current when control unit disconnected from ground. Loss of local ground must not affect communication in the residual network	GND_{Device} = V_S V_{Batt} = 12V 0V < V_{BUS} < 18V	LIN	$I_{BUS\_NO\_gnd}$	–10	+0.5	+10	µA	A
8.12	Leakage current at disconnected battery. Node has to sustain the current that can flow under this condition. Bus must remain operational under this condition.	V_{Batt} disconnected V_{SUP_Device} = GND 0V < V_{BUS} < 18V	LIN	$I_{BUS\_NO\_bat}$		0.1	2	µA	A
8.13	Capacitance on Pin LIN to GND		LIN	C_{LIN}			20	pF	D
9	LIN Bus Receiver								
9.1	Center of receiver threshold	V_{BUS_CNT} = (V_{th_dom} + V_{th_rec})/2	LIN	V_{BUS_CNT}	0.475 × V_S	0.5 × V_S	0.525 × V_S	V	A
9.2	Receiver dominant state	V_{EN} = 5V	LIN	V_{BUSdom}	–27		0.4 × V_S	V	A
9.3	Receiver recessive state	V_{EN} = 5V	LIN	V_{BUSrec}	0.6 × V_S		40	V	A
9.4	Receiver input hysteresis	V_{hys} = V_{th_rec} – V_{th_dom}	LIN	V_{BUShys}	0.028 × V_S	0.1 x V_S	0.175 × V_S	V	A
9.5	Pre-wake detection LIN High level input voltage		LIN	V_{LINH}	V_S – 2V		V_S + 0.3V	V	A
9.6	Pre-wake detection LIN Low level input voltage	Activates the LIN receiver	LIN	V_{LINL}	–27		V_S – 3.3V	V	A
10	Internal Timers								
10.1	Dominant time for wake–up via LIN bus	V_{LIN} = 0V	LIN	t_{bus}	50	100	150	µs	A
10.2	Time delay for mode change from Fail-safe into normal mode via pin EN	V_{EN} = 5V	EN	t_{norm}	5		20	µs	A
10.3	Time delay for mode change from normal mode to sleep mode via pin EN	V_{EN} = 0V	EN	t_{sleep}	5	15	20	µs	A

*) Type means: A = 100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter

10. Electrical Characteristics (Continued)

5V < V_S < 28V, –40°C < T_j < 150°C; unless otherwise specified all values refer to GND pins.

No.	Parameters	Test Conditions	Pin	Symbol	Min.	Typ.	Max.	Unit	Type*
10.4	TXD dominant time out time	V_{TXD} = 0V	TXD	t_{dom}	20	40	60	ms	A
10.5	Time delay for mode change from silent mode into normal mode via EN	V_{EN} = 5V	EN	t_{s_n}	5	15	40	µs	A
10.6	Duty cycle 1	$TH_{Rec(max)}$ = 0.744 × V_S $TH_{Dom(max)}$ = 0.581 × V_S V_S = 7.0V to 18V t_{Bit} = 50µs D1 = $t_{bus\_rec(min)}/(2 \times t_{Bit})$	LIN	D1	0.396				A
10.7	Duty cycle 2	$TH_{Rec(min)}$ = 0.422 × V_S $TH_{Dom(min)}$ = 0.284 × V_S V_S = 7.6V to 18V t_{Bit} = 50µs D2 = $t_{bus\_rec(max)}/(2 \times t_{Bit})$	LIN	D2			0.581		A
10.8	Duty cycle 3	$TH_{Rec(max)}$ = 0.778 × V_S $TH_{Dom(max)}$ = 0.616 × V_S V_S = 7.0V to 18V t_{Bit} = 96µs D3 = $t_{bus\_rec(min)}/(2 \times t_{Bit})$	LIN	D3	0.417				A
10.9	Duty cycle 4	$TH_{Rec(min)}$ = 0.389 × V_S $TH_{Dom(min)}$ = 0.251 × V_S V_S = 7.6V to 18V t_{Bit} = 96µs D4 = $t_{bus\_rec(max)}/(2 \times t_{Bit})$	LIN	D4			0.590		A
10.10	Slope time falling and rising edge at LIN	V_S = 7.0V to 18V	LIN	t_{SLOPE_fall} t_{SLOPE_rise}	3.5		22.5	µs	A
11	Receiver Electrical AC Parameters of the LIN Physical Layer LIN Receiver, RXD Load Conditions: C_{RXD} = 20pF								
11.1	Propagation delay of receiver Figure 10-1	V_S = 7.0V to 18V t_{rx_pd} = max(t_{rx_pdr} , t_{rx_pdf})	RXD	t_{rx_pd}			6	µs	A
11.2	Symmetry of receiver propagation delay rising edge minus falling edge	V_S = 7.0V to 18V t_{rx_sym} = t_{rx_pdr} – t_{rx_pdf}	RXD	t_{rx_sym}	–2		+2	µs	A

*) Type means: A = 100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter

Figure 10-1. Definition of Bus Timing Characteristics

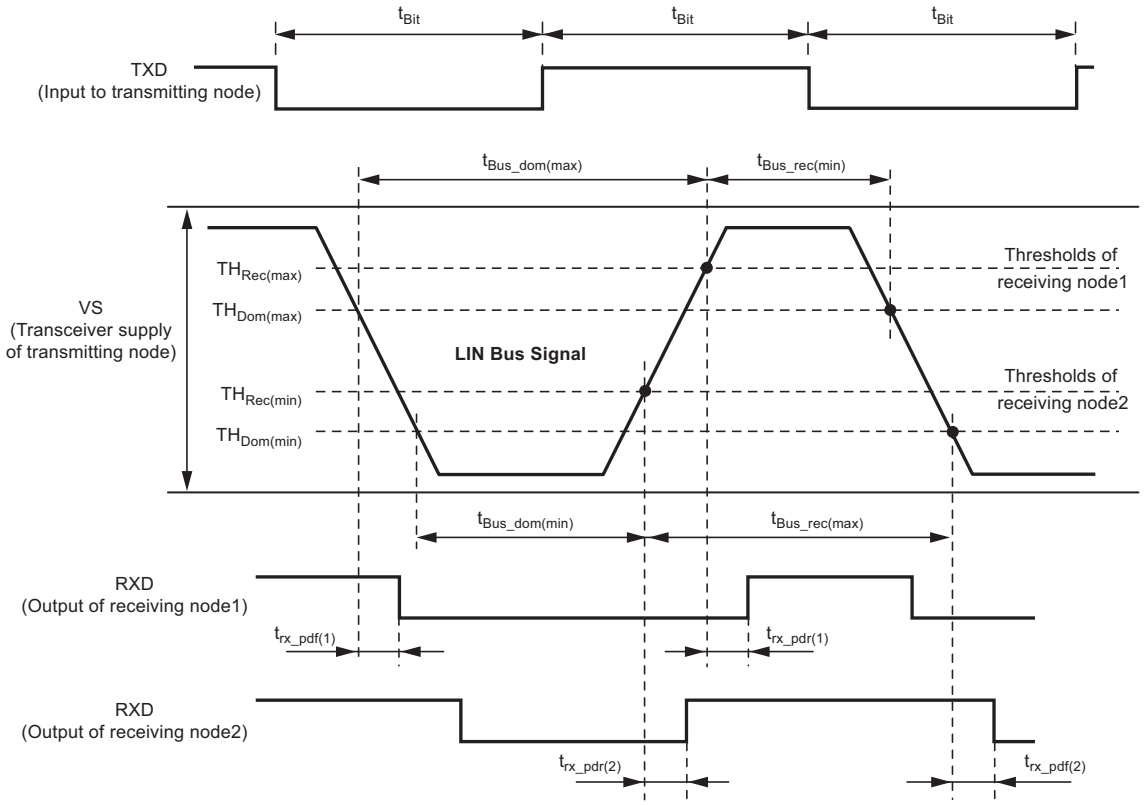
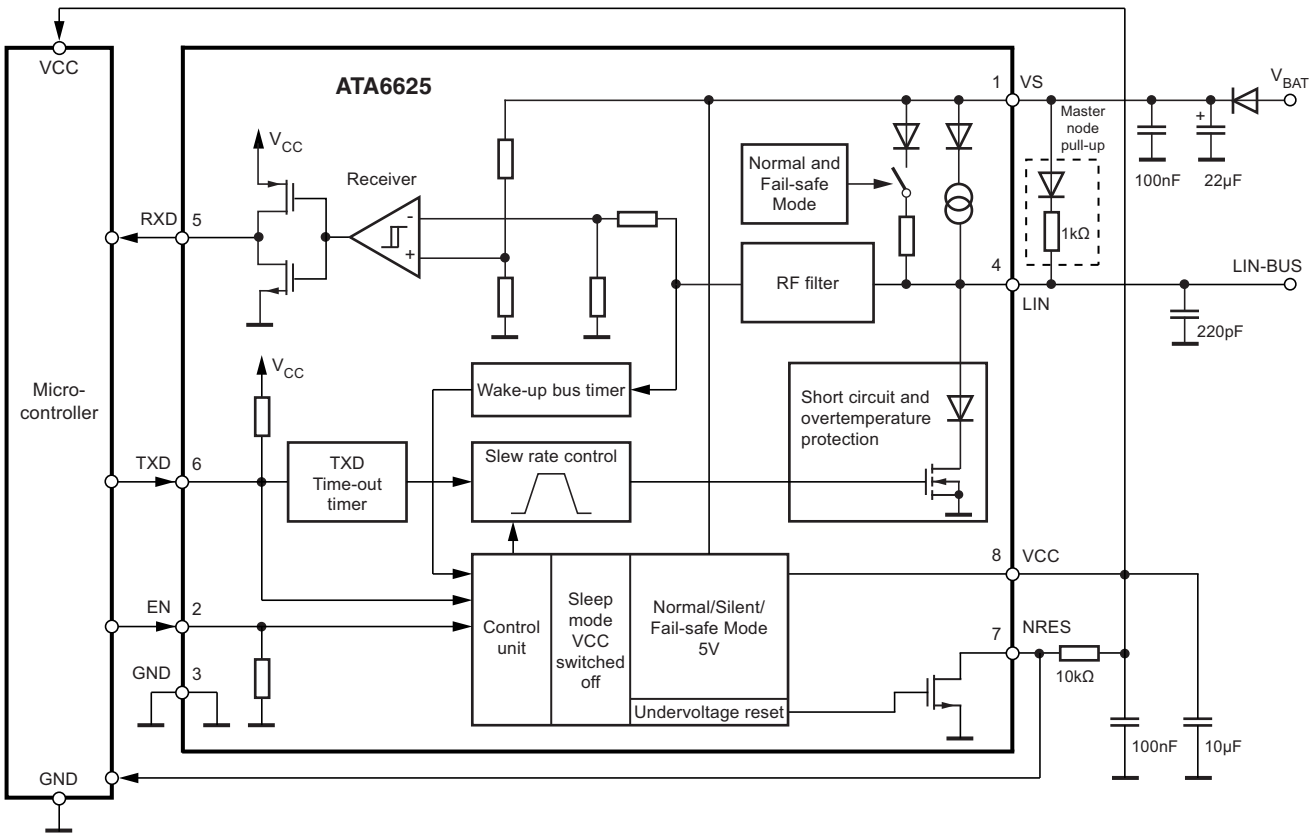


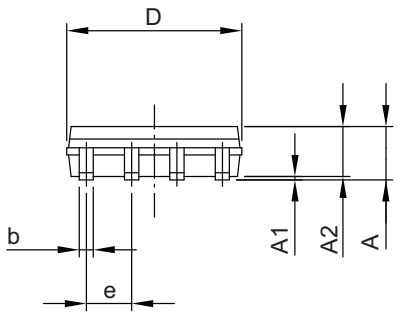
Figure 10-2. Application Circuit

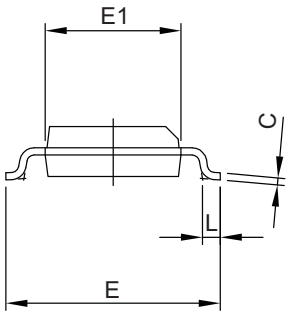


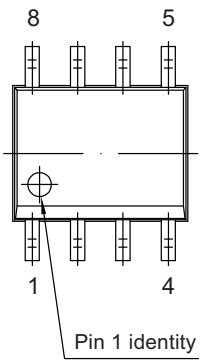
11. Ordering Information

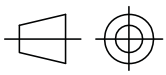
Extended Type Number	Package	Remarks
ATA6625-GAQW	SO8	5V LIN system basis chip, Pb-free, 4k, taped and reeled
ATA6625-GBQW	DFN8	5V LIN system basis chip, Pb-free, 6k, taped and reeled

Figure 11-1. Package SO8









technical drawings
according to DIN
specifications

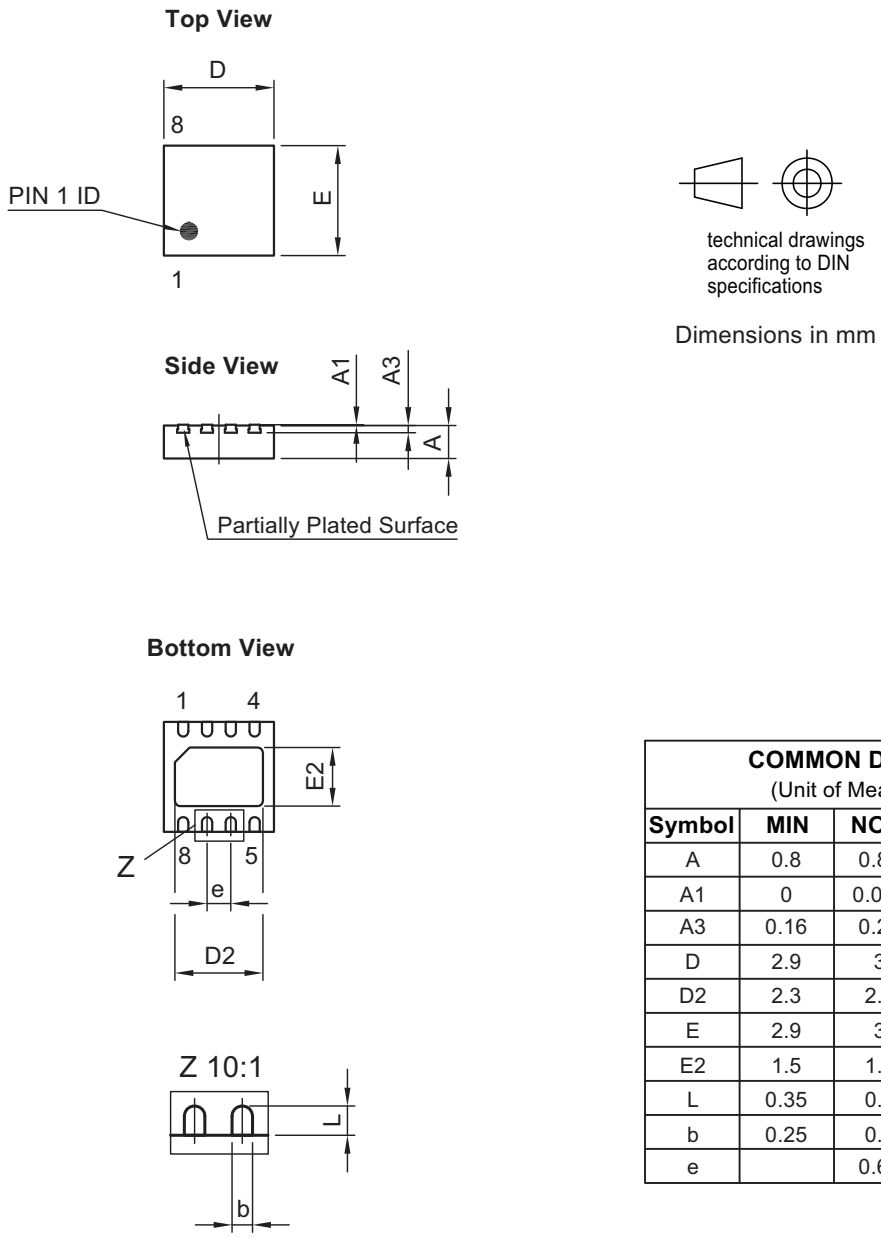
Dimensions in mm

COMMON DIMENSIONS (Unit of Measure = mm)				
Symbol	**MIN**	**NOM**	**MAX**	**NOTE**
A	1.5	1.65	1.8	
A1	0.1	0.15	0.25	
A2	1.4	1.47	1.55	
D	4.8	4.9	5	
E	5.8	6	6.2	
E1	3.8	3.9	4	
L	0.4	0.65	0.9	
C	0.15	0.2	0.25	
b	0.3	0.4	0.5	
e		1.27 BSC		

05/08/14

Atmel	TITLE	GPC	DRAWING NO.	REV.
Package Drawing Contact: packagedrawings@atmel.com	**Package: SO8**		6.543-5185.01-4	1

Figure 11-2. Package DFN8



COMMON DIMENSIONS (Unit of Measure = mm)				
Symbol	**MIN**	**NOM**	**MAX**	**NOTE**
A	0.8	0.85	0.9	
A1	0	0.035	0.05	
A3	0.16	0.21	0.26	
D	2.9	3	3.1	
D2	2.3	2.4	2.5	
E	2.9	3	3.1	
E2	1.5	1.6	1.7	
L	0.35	0.4	0.45	
b	0.25	0.3	0.35	
e		0.65		

10/11/13

	TITLE	GPC	DRAWING NO.	REV.
Atmel **Package Drawing Contact:** packagedrawings@atmel.com	**Package: VDFN_3x3_8L** Exposed pad 2.4x1.6		6.543-5165.03-4	1

12. Revision History

Please note that the following page numbers referred to in this section refer to the specific revision mentioned, not to this document.

Revision No.	History
9376B-AUTO-08/16	• ATA6625-GBQW in DFN8 package added
9376A-AUTO-01/16	• Initial version

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