Full-Featured, Dimmable AC Mains LED Driver with PFC

ISL1902

The ISL1902 is a high-performance, critical conduction mode (CrCM), single-ended controller used for single-stage conversion of the AC mains to a constant current source with power factor correction (PFC). This controller may be used in virtually any single-ended topology, isolated or non-isolated, including Boost, SEPIC, Flyback, and Forward converters. Operation in CrCM allows near zero-voltage switching (ZVS) for improved efficiency while maximizing magnetic core utilization.

The ISL1902 is compatible with both leading and trailing edge modulated AC mains dimmers as well as analog signal and ambient light sensor controlled dimming methods. The LED string may be dimmed either by modulation of the DC current or PWM dimming. In-rush current limiting minimizes current spikes caused by leading edge dimmers and prevents dimmer malfunction when one or more LED fixtures are connected. Two control loops are provided to improve transient response since one loop must have restricted bandwidth to allow PFC. The second control loop may be configured for higher bandwidth to respond to input transients quickly and prevent them from propagating to the load and appearing as flashing/flickering.

The ISL1902 LED driver controller provides all of the features required for high-performance dimmable LED ballast designs.

Applications

- Industrial and commercial LED lighting
- Architectural lighting LED drivers
- AC or DC input LED ballasts

Features

- Excellent LED current regulation over line, load, and temperature
- 0 - 100% dimming with leading-edge (triac) and trailing-edge dimmers
- Analog control signal dimming
- Configurable for PWM or DC Current Dimming Control of LEDs
- Dual control loops for PFC and fast transient response
- Compatible with ambient light sensors for uniform lamp-to-lamp performance
- Power factor correction for up to 0.995 power factor and less than 20% harmonic content
- Critical Conduction Mode (CrCM) operation for quasi-resonant high efficiency performance
- Supports universal AC mains input
- Active pre-load to eliminate power-off “afterglow”
- OFFREF feature sets dimming turn-off-threshold to improve fixture performance matching
- In-rush protection control for each AC half-cycle minimizes audible noise and eliminates dimmer resonance
- Input or Output Overvoltage Protection (OVP)
- Over-Temperature Protection (OTP)
- Bias Supply Under Voltage Lockout (UVLO)
- -40°C to +125°C operation
- Pb-free (RoHS compliant)

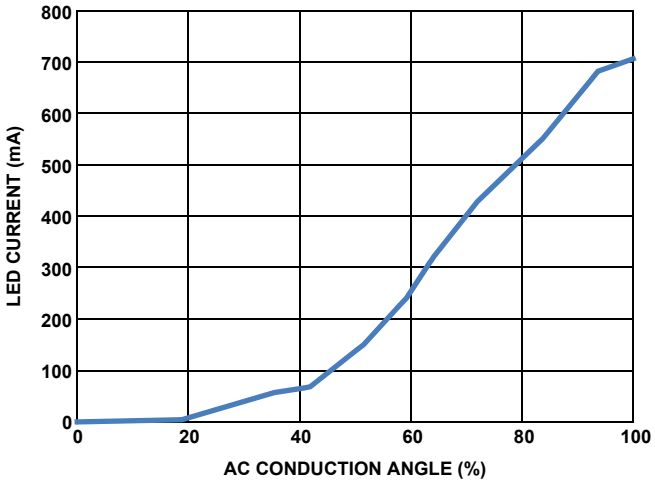


FIGURE 1. TYPICAL APPLICATION - DIMMING PERFORMANCE

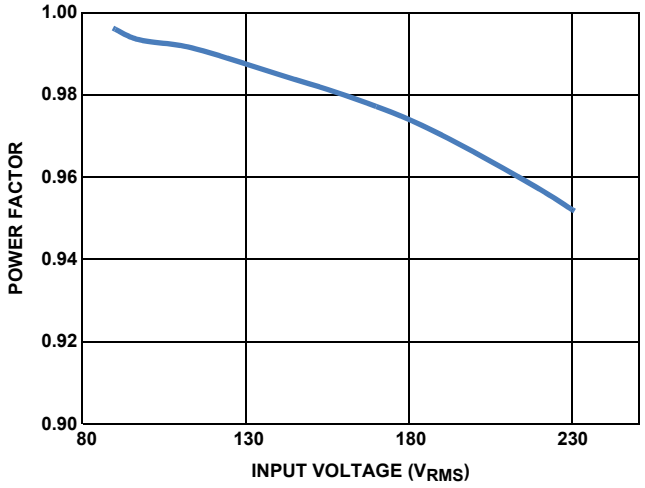
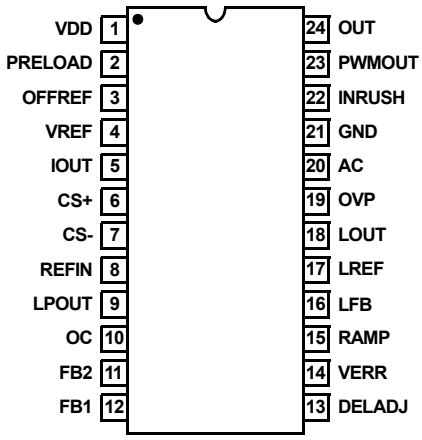


FIGURE 2. TYPICAL APPLICATION - POWER FACTOR

Pin Configuration

ISL1902
(24 LD QSOP
TOP VIEW



Pin Descriptions

PIN #	SYMBOL	DESCRIPTION
1	VDD	VDD is the power connection for the IC. To optimize noise immunity, bypass VDD to GND with a ceramic capacitor as close to the VDD and GND pins as possible.
2	PRELOAD	The output control signal to drive an external FET placed in parallel with the LED load. This feature allows the output capacitor to be quickly discharged to prevent continued low level illumination of the LEDs due to stored energy in the output capacitor.
3	OFFREF	Sets the reference level to disable the driver at light loading. The turn-off reference can be set at any level between 0V and 0.6V, corresponding to 0% to 100% of output loading. This feature is normally used in triac-based wall dimmer applications to disable the output before the dimmer becomes unstable due to insufficient holding current. OFFREF triggers PRELOAD to discharge the output capacitance with an external FET.
4	VREF	The 5.40V reference voltage output having ±100mV tolerance over line, load and operating temperature. Bypass to GND with a 0.1µF to 3.3µF low ESR capacitor.
5	IOUT	The output of the differential current sensing circuit. A pair of resistors and capacitors is placed on this output to form two low pass filters. IOUT creates the current feedback signals for the control loop and is normally filtered and scaled prior to inputing at FB1 and FB2 through separate input resistors to allow for different BWs.
6, 7	CS+, CS-	The differential inputs for the current sense circuit. This circuit generates a DC feedback signal for the control loop as well as the input to the CrCM circuit to determine the critical conduction operating point. CS± has a common mode range of -0.3V to 0.5V and a differential input range of 0V to1.5V
8	REFIN	The reference voltage input that sets the control loop reference. Normally connected to LPOUT or an external control reference.
9	LPOUT	Output of the digital low-pass filter. The output ranges from 0V to 0.5V in proportion to the AC conduction angle. This output may be used as is or manipulated (such as when used with an external light sensor or temperature monitor) and applied to REFIN to be used as the reference for the control loop.
10	OC	This is the input to the peak overcurrent comparator. The overcurrent comparator threshold is set at 600mV nominal. Peak OCP is required for cycle-by-cycle protection. It also protects against low AC line conditions. OCP includes leading-edge-blanking (LEB), which blocks the signal at the beginning of the OUT pulse for the duration of the blanking period, and also while the OUT pulse is low.
11, 12	FB2, FB1	FBx is the inverting input to the error amplifier (EAs). The current feedback signal is applied to EA1 and EA2. EA1 is the primary error amplifier and is used for steady state operation. EA2 is the secondary control loop for operation during transients. Normally EA1 is configured for low bandwidth operation, about 20Hz, to obtain power factor correction. EA2 is configured for higher BW to respond to transients. Both error amplifiers are externally compensated to give the user complete flexibility.
13	DELADJ	Sets delay before a new switching cycles starts. This adjustment allows the user to delay the next switching cycle until the switching FET drain-source voltage reaches a minimum value to allow quasi-ZVS (Zero Voltage Switching) operation. A resistor to ground programs the delay. Pulling DELADJ to VREF disables the CrCM oscillator.
14	VERR	Output of the error amplifiers and the control voltage input to the inverting input of the PWM comparator. VERR requires an external pull-up resistor to VREF.
15	RAMP	This is the input for the sawtooth waveform for the PWM comparator. Using an RC from VREF, a sawtooth waveform is created for use by the PWM. It is compared to the error amplifier output, VERR, to create the PWM control signal. The RAMP pin is shorted to GND at the termination of the PWM signal.
16	LFB	The inverting input to the uncommitted linear amplifier.

Pin Descriptions (Continued)

PIN #	SYMBOL	DESCRIPTION
17	LREF	The non-inverting input to the uncommitted linear amplifier.
18	LOUT	Output of the uncommitted linear amplifier.
19	OVP	Input to detect an overvoltage (OV) condition on the output with a nominal threshold of 1.5V. Since the control variable is output current, a fault that results in an open circuit will cause excessive output voltage. The circuit hysteresis is a switched current source that is active when the OV threshold is exceeded.
20	AC	Input to sense AC voltage presence and amplitude. A resistor divider from line and neutral/line and circuit ground is used to detect the AC voltage.
21	GND	Signal and power ground connections for this device. Due to high peak currents and high frequency operation, a low impedance layout is necessary. Ground planes and short traces are highly recommended.
22	INRUSH	Output to drive an isolation transformer to control an inrush current limiting device. Typically this would be a triac, back-to-back FETs, or anti-parallel SCRs, etc. The output is a 50% duty cycle ~80kHz square-wave capable of sourcing 10mA. The output is enabled in conjunction with an AC outage (such as from a wall dimmer). Operation is delayed for ~150µs after AC returns and is enabled until AC is interrupted again. The INRUSH output is also inhibited during normal AC zero-crossing even at full conduction angle.
23	PWMOUT	The PWM gate drive output for LED dimming. The output level is clamped to ~12V for V_{DD} greater than 12V. PWMOUT has pull-down capability when UVLO is active or when the IC is not biased. This output is used to drive the dimming FET in series with the LED string. The PWM operates at ~310Hz.
24	OUT	The gate drive output for the external power FET. OUT is capable of sourcing and sinking 1A @ V_{DD} = 8V. The output level is clamped to ~12V for V_{DD} greater than 12V. OUT has pull-down capability when UVLO is active or when the IC is not biased.

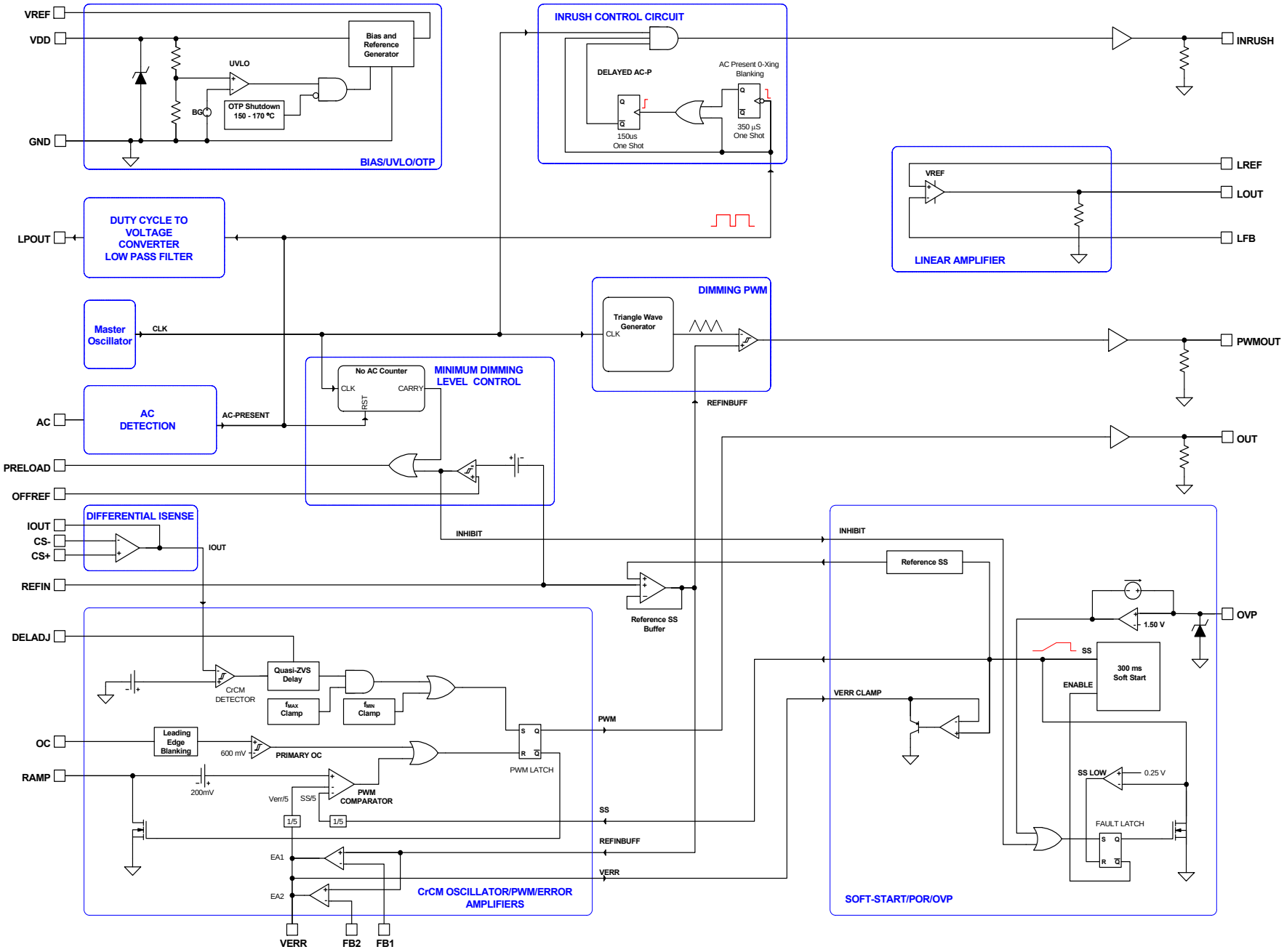
Ordering Information

PART NUMBER (Notes 1, 2, 3)	PART MARKING	TEMP. RANGE (°C)	PACKAGE (Pb-free)	PKG. DWG. #
ISL1902FAZ	ISL 1902FAZ	-40 to +125	24 Ld QSOP	M24.15

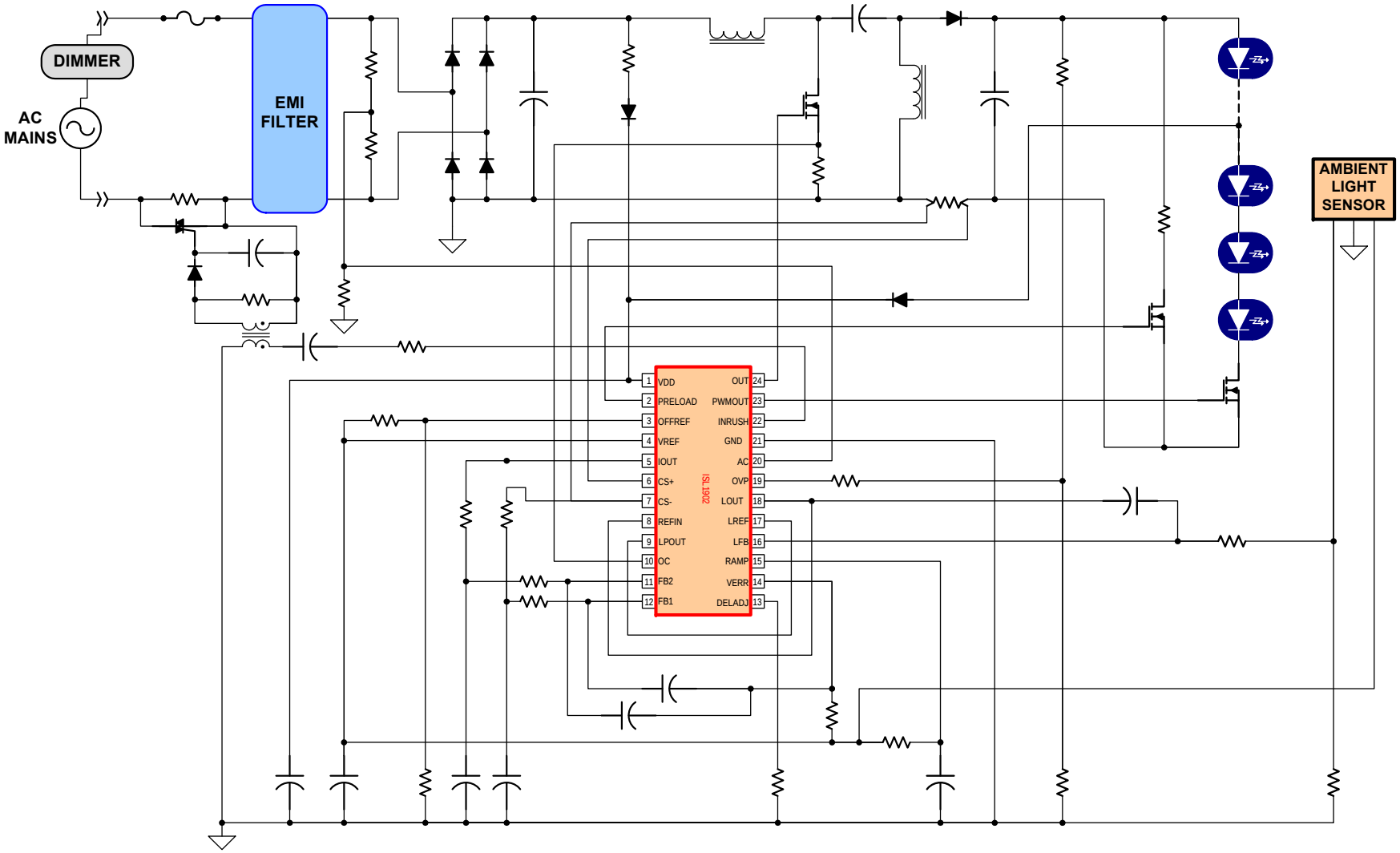
NOTES:

1. Add "-T*" suffix for tape and reel. Please refer to TB347 for details on reel specifications.
2. These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
3. For Moisture Sensitivity Level (MSL), please see device information page for ISL1902. For more information on MSL please see tech brief TB363.

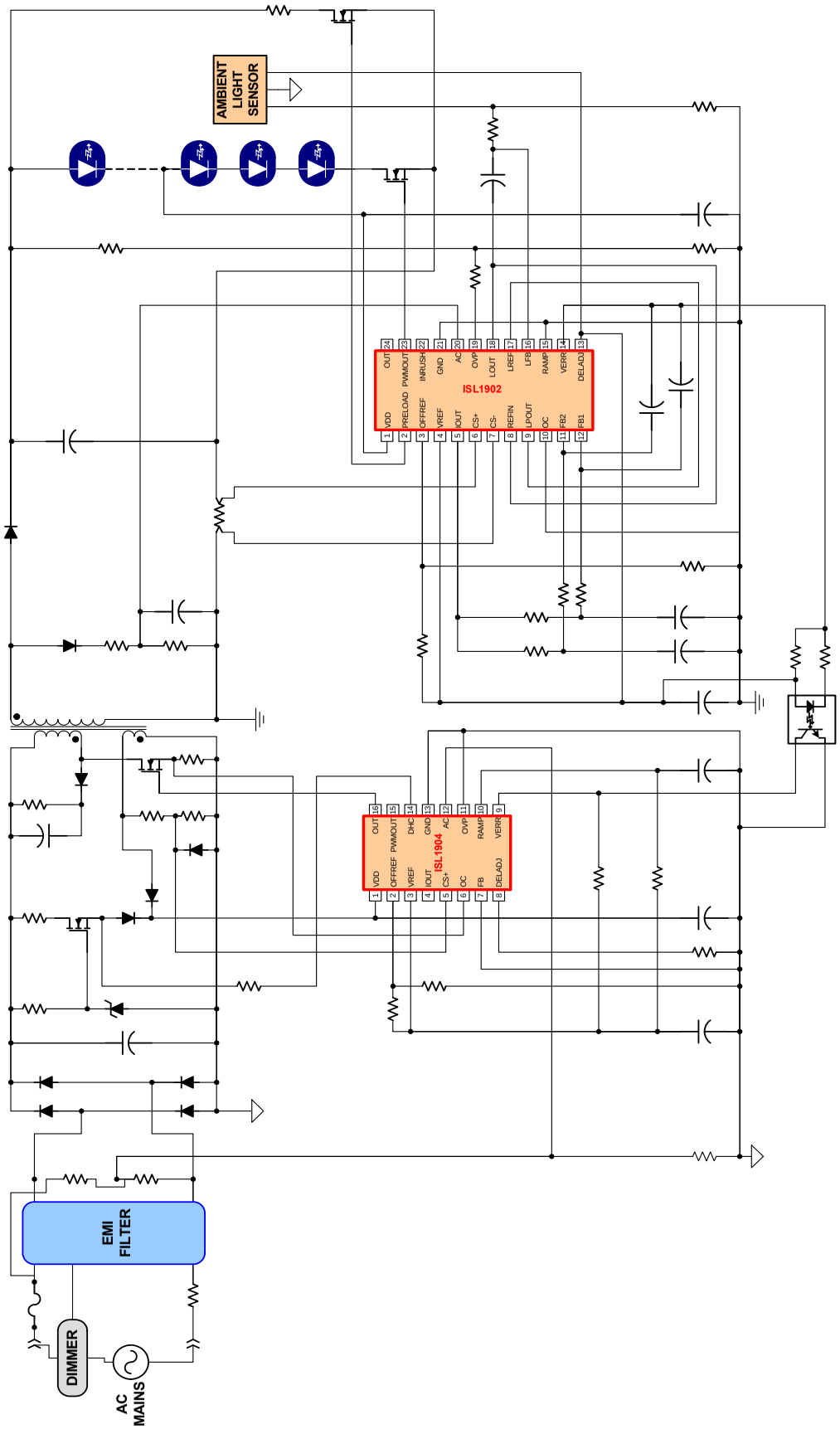
Functional Block Diagram - ISL1902



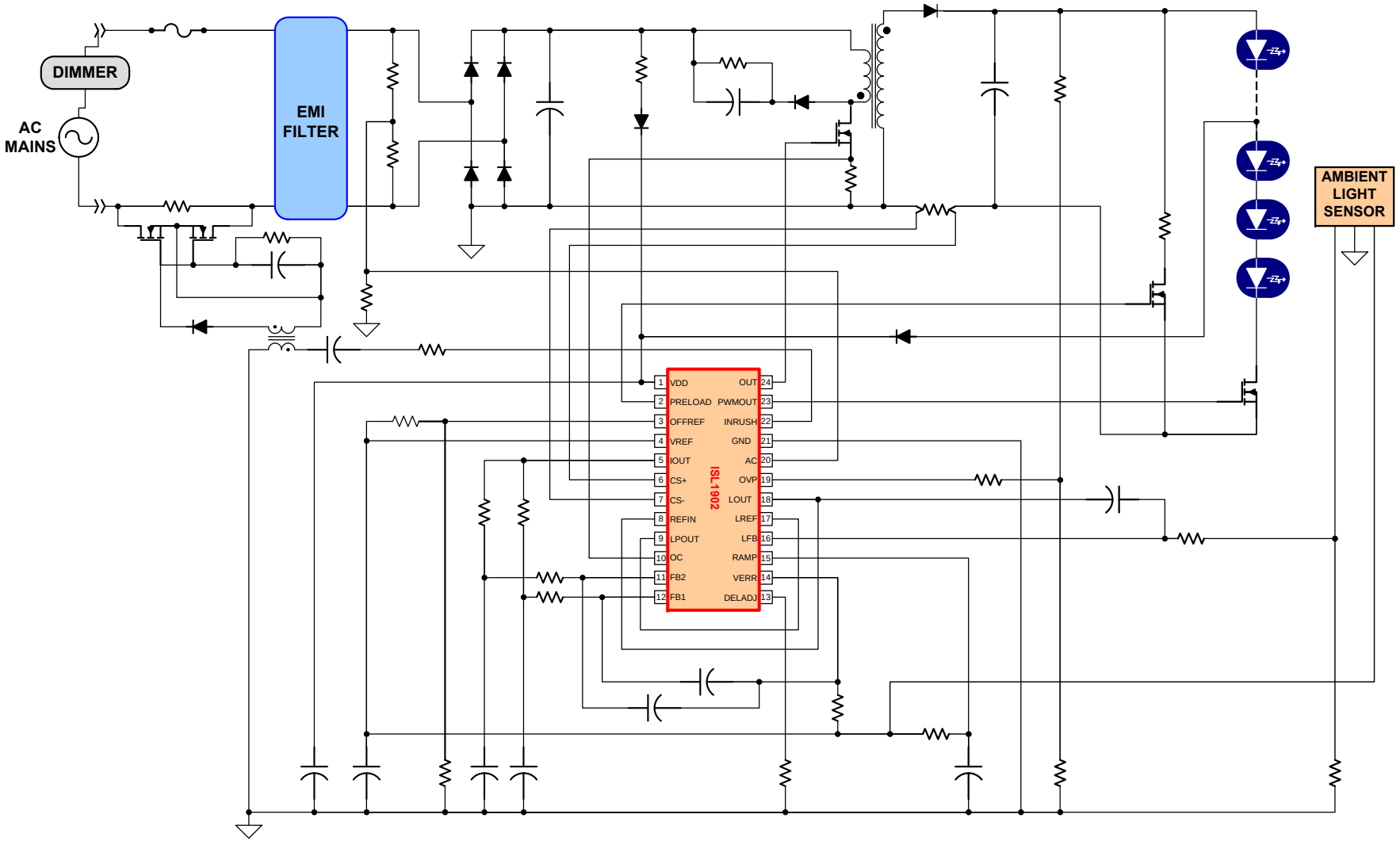
Typical Application - SEPIC Topology with PWM Dimming and Ambient Light Compensation



Typical Application - Isolated Flyback with PWM Dimming and Ambient Light Compensation



Typical Application - Non-Isolated Flyback with PWM Dimming and Ambient Light Compensation



Absolute Maximum Ratings

Supply Voltage, V_{DD} . . . . . GND - 0.3V to +28.0V
OUT, PWMOUT, INRUSH . . . . . GND - 0.3V to VDD
Signal Pins (except CS-) . . . . . GND - 0.3V to V_{REF} + 0.3V
Signal Pin CS- . . . . . GND - 0.6V to V_{REF} + 0.3V
VREF . . . . . GND - 0.3V to 6.0V
Peak OUT Current 2.0A
Peak PWMOUT Current 1.0A
ESD Classification
Human Body Model (Per MIL-STD-883 Method 3015.7) 1500V
Machine Model (Per EIAJ ED-4701 Method C-111) 150V
Charged Device Model (Per EOS/ESD DS5.3, 4/14/93) 750V
Latchup (Per JESD-78B; Class 2, Level A 100mA

Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
24 Lead QSOP (Notes 4, 5)	78	34

Maximum Junction Temperature . . . . . -55°C to +150°C
Maximum Storage Temperature Range . . . . . -65°C to +150°C
Pb-Free Reflow Profile . . . . . see link below
http://www.intersil.com/pbfree/Pb-FreeReflow.asp

Operating Conditions

Temperature Range . . . . . -40°C to +125°C
Supply Voltage Range (Typical) . . . . . 9VDC to 20VDC

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

4. θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air. See Tech Brief TB379 for details.
5. For θ_{JC}, the "case temp" location is taken at the package top center.
6. All voltages are with respect to GND.

Electrical Specifications

Recommended operating conditions unless otherwise noted. Refer to the Block Diagram on page 4 and Typical Application schematics starting on page 5. V_{DD} = 17V, R_{RAMP} = 54kΩ, C_{RAMP} = 470pF, T_A = -40°C to +125°C, Typical values are at T_A = +25°C. **Boldface limits apply over the operating temperature range, -40°C to +125°C.**

PARAMETER	TEST CONDITIONS	MIN (Note 7)	TYP	MAX (Note 7)	UNITS
SUPPLY VOLTAGE					
Supply Voltage				**26**	V
Start-Up Current, IDD	V_{DD} = 5.0V		100	**200**	µA
Operating Current, IDD	R_{LOAD}, C_{OUT} = 0		10	**14.5**	mA
UVLO START Threshold		**14.8**	15.5	**16.1**	V
UVLO STOP Threshold		**6.80**	7.10	**7.50**	V
Hysteresis		**7.50**	8.30	**9.30**	V
REFERENCE VOLTAGE (VREF)					
Overall Accuracy	I_{VREF} = 0mA to -10mA, 8V < V_{DD}< 26V	**5.30**	5.40	**5.50**	V
Long Term Stability	T_A = +125°C, 1000 hours (Note 8)		10	25	mV
Operational Current (Source)	8V < V_{DD}< 26V	-10			mA
Current Limit	V_{REF} = 5.00V, 8V < V_{DD}< 26V	**-15**		**-100**	mA
Load Capacitance	(Note 8)	**0.1**		**3.3**	µF
PEAK CURRENT SENSE (OC)					
Current Limit Threshold	VERR = VREF, RAMP = 0V	**577**	600	**623**	mV
Leading Edge Blanking (LEB) Duration	(Note 8)	**70**	120	**150**	ns
OC to OUT Delay + LEB	T_A = +25°C	110	170	200	ns
Input Bias Current	V_{OC} = 0.3V	**-1.0**		**1.0**	µA
RAMP					
RAMP Sink Current Device Impedance	I_{RAMP} = 10mA			**20**	Ω
RAMP to PWM Comparator Offset		**190**	235	**287**	mV
Input Bias Current	V_{RAMP} = 0.3V	**-1.0**		**1.0**	µA

Electrical Specifications Recommended operating conditions unless otherwise noted. Refer to the Block Diagram on page 4 and Typical Application schematics starting on page 5. V_{DD} = 17V, R_{RAMP} = 54kΩ, C_{RAMP} = 470pF, T_A = -40°C to +125°C, Typical values are at T_A = +25°C. **Boldface limits apply over the operating temperature range, -40°C to +125°C. (Continued)**

PARAMETER	TEST CONDITIONS	MIN (Note 7)	TYP	MAX (Note 7)	UNITS
PULSE WIDTH MODULATOR					
PWM Restart Delay Range	8V < V_{DD}< 26V	**0.2**		**2.0**	µs
PWM Restart Cycle Delay	RDELADJ = 20.0kΩ, 8V < V_{DD}< 26V	**240**	280	**320**	ns
	RDELADJ = 210kΩ, 8V < V_{DD}< 26V	**2.00**	2.20	**2.40**	µs
Maximum Frequency Clamp	R_{RAMP} = 100Ω, RAMP = 2V, 8V < V_{DD}< 26V	**0.7**	1.0	**1.2**	MHz
Minimum Frequency Clamp	R_{RAMP} = 23kΩ, 8V < V_{DD}< 26V	**20**	25	**31**	kHz
Minimum Duty Cycle	8V < V_{DD}< 26V, COMP = 0V			**0**	%
Minimum Non-Zero Output Duration	8V < V_{DD}< 26V	**70**	100	**130**	ns
Zero Current (CrCm) Detector Threshold, Falling	8V < V_{DD}< 26V	**7**		**28**	mV
VERR to PWM Gain	8V < V_{DD}< 26V		0.200		V/V
SS to PWM Gain	8V < V_{DD}< 26V		0.222		V/V
ERROR AMPLIFIERS (EA1 AND EA2)					
Input Common Mode (CM) Range	(Note 8)	**0**		**3.4**	V
GBWP	(Note 8)	**1.9**			MHz
VERR VOL EA1	I_{VERR} = 6mA, 8V < V_{DD}< 26V			**0.950**	V
VERR VOL EA2	I_{VERR} = 4mA, 8V < V_{DD}< 26V			**0.950**	V
VERR VOH	I_{VERR} = 1mA (Ext. pull-up) SS complete	**3.90**	4.00	**4.20**	V
Open Loop Gain	(Note 8)	**70**			dB
Offset Voltage (VOS)	8V < V_{DD}< 26V	**-7.5**		**7.5**	mV
Input Bias Current, FB1	REFIN = 0.5V, FB1 = 2.0V, FB2 = 0V, 8V < V_{DD}< 26V	**-1.0**		**1.0**	µA
Input Bias Current, FB2	REFIN = 0.5V, FB2 = 2.0V, FB1 = 0V, 8V < V_{DD}< 26V	**-1.0**		**1.0**	µA
DIFFERENTIAL CURRENT SENSE (CS+, CS-)					
IOUT Amplifier Gain	CS- = 0V, CS+ = 0.1V, 0.3V, 8V < V_{DD}< 26V	**2.910**	2.970	**3.030**	V/V
Common Mode (CM) Input Range	8V < V_{DD}< 26V	**-0.30**		**0.50**	V
Differential Input Range	8V < V_{DD}< 26V	**0**		**1.5**	V
Offset Voltage (VOS)	8V < V_{DD}< 26V	**-36**		**48**	mV
GBWP	(Note 8)	**8**			MHz
Slew Rate	(Note 8)		45		V/µs
Input Bias Current	CS- = 0V, 1.0V CS+ = 1.0V, 1.5V 8V < V_{DD}< 26V	**-1.0**		**1.0**	µA
IOUT High Level Output Voltage (VOH)	V_{IOUT} at 0µA - V_{IOUT} at -100µA, 8V < V_{DD} < 26V			**0.1**	V
IOUT Low Level Output Voltage (VOL)	V_{IOUT} at 100µA, 8V < V_{DD}< 26V			**0.1**	V
AC DETECTOR					
Input Bias Current	8V < V_{DD}< 26	**-50**		**50**	nA
Detection Threshold, Falling	AC_{PEAK} = 100mV, 8V < V_{DD}< 26V	**4.5**	20	**40.5**	mV
Detection Threshold Hysteresis	8V < V_{DD}< 26V		6		mV
Input Operating Range	8V < V_{DD}< 26V	**0**		**4.00**	V

Electrical Specifications Recommended operating conditions unless otherwise noted. Refer to the Block Diagram on page 4 and Typical Application schematics starting on page 5. V_{DD} = 17V, R_{RAMP} = 54kΩ, C_{RAMP} = 470pF, T_A = -40°C to +125°C, Typical values are at T_A = +25°C. **Boldface limits apply over the operating temperature range, -40°C to +125°C. (Continued)**

PARAMETER	TEST CONDITIONS	MIN (Note 7)	TYP	MAX (Note 7)	UNITS
Clamp Voltage	$I_{ACDETECT}$ = 1.0mA	**6.8**	7.2	**7.6**	V
INRUSH					
High Level Output Voltage (VOH)	V_{INRUSH} at 0mA - V_{INRUSH} at -10mA, V_{DD} = 8V operating			**1.00**	V
Low Level Output Voltage (VOL)	V_{INRUSH} = 10mA, V_{DD} = 8V operating			**1.00**	V
Inrush Duration (see t_{DELAY} Fig. 10)	8V < V_{DD}< 26V	**140**	180	**220**	µs
Output Clamp Voltage	V_{DD} = 20V, I_{INRUSH} = -10µA	**10.5**	12	**13.4**	V
Unbiased Output Voltage Clamp	V_{DD} = 6V, I_{LOAD} = 3mA			**2.3**	V
LOW PASS FILTER					
High Level Output Voltage (VOH)	V_{LPOUT} at 0µA - V_{LPOUT} at -100µA, 8V < V_{DD}< 26V			**0.1**	V
Low Level Output Voltage (VOL)	V_{LPOUT} at 100µA, 8V < V_{DD}< 26V			**0.1**	V
Output Range		**0**		**0.50**	V
LPOUT vs AC Conduction Angle	I_{LPOUT} = 0µA, f = 120Hz (rectified), 8V < V_{DD}< 26V				
	Duty Cycle (α) = 98%	**485**	514	**543**	mV
	Duty Cycle (α) = 75%	**273**	300	**323**	mV
	Duty Cycle (α) = 50%	**110**	130	**148**	mV
	Duty Cycle (α) = 25%	**16**	30	**41**	mV
	Duty Cycle (α) = 10%	**0**	1	**9**	mV
REFIN					
Input Common Mode (CM) Range		**0**		**VREF-1**	V
Input Bias Current	REFIN = 4.4V	**-1.0**		**1.0**	µA
Offset Voltage (VOS), Combined FBx + REFIN at EA	8V < V_{DD}< 26V, see Fig. 11	**-11**		**11**	mV
LINEAR AMPLIFIER					
Input Offset (VOS)	LFB = LOUT, LREF = 0.5V	**-4**		**4**	mV
High Level Output Voltage (VOH)	I_{LOUT} = -1mA, LFB = 0V, LREF = VREF (VOH at 0mA - VOH at -1mA)			**1.0**	V
Low Level Output Voltage (VOL)	I_{LOUT} = 8mA, LFB = VREF, LREF = 0V			**1.0**	V
Input Common Mode (CM) Range		**0**		**VREF**	V
Output Operating Range		**0.3**		**4.3**	V
GBWP	(Note 8)	**1**			MHz
Open Loop Gain	(Note 8)	**85**			dB
Input Bias Current LREF, LFB	LREF = 1.0V, LFB = 1.0V	**-1.0**		**1.0**	µA
Output Pull-Down Impedance	V_{DD} = 6.0V, I_{LOUT} = 100µA		10		kΩ
SOFT-START					
Duration		**282**	370	**483**	ms
Reference Soft-Start Initial Step			21		mV
OFFREF					
Input Bias Current	OFFREF = 0.5V	**-1.0**		**1.0**	µA

Electrical Specifications Recommended operating conditions unless otherwise noted. Refer to the Block Diagram on page 4 and Typical Application schematics starting on page 5. V_{DD} = 17V, R_{RAMP} = 54kΩ, C_{RAMP} = 470pF, T_A = -40°C to +125°C, Typical values are at T_A = +25°C. **Boldface limits apply over the operating temperature range, -40°C to +125°C. (Continued)**

PARAMETER	TEST CONDITIONS	MIN (Note 7)	TYP	MAX (Note 7)	UNITS
Operating Range (Excluding Offset)		**0**		**0.5**	V
Threshold Hysteresis		**48**	62	**76**	mV
Threshold Offset		**78**	104	**129**	mV
AC Dropout Disable Delay			32		ms
PRELOAD VOH	I_{LOAD} = 0mA		VREF		V
PRELOAD VOL	I_{LOAD} = 1mA		1.00		V
OUT					
High Level Output Voltage (VOH)	V_{OUT} at 0mA - V_{OUT} at -100mA, V_{DD} = 8V operating		0.35	**1.2**	V
Low Level Output Voltage (VOL)	V_{OUT} at 100mA, V_{DD} = 8V operating		0.7	**1.2**	V
Rise Time	C_{LOAD} = 2.2nF, V_{DD} = 8V, $t_{90\%}$ - $t_{10\%}$		35	**55**	ns
Fall Time	C_{LOAD} = 2.2nF, V_{DD} = 8V, $t_{10\%}$ - $t_{90\%}$		20	**40**	ns
Output Clamp Voltage	V_{DD} = 20V, I_{LOAD} = -10µA	**10.5**	12.0	**13.4**	V
Unbiased Output Voltage Clamp	V_{DD} = 6V, I_{LOAD} = 5mA			**1.9**	V
PWMOUT					
High Level Output Voltage (VOH)	V_{OUT} at 0mA - V_{OUT} at -10mA, V_{DD} = 8V operating		0.8	**1.2**	V
Low Level Output Voltage (VOL)	V_{OUT} at 10mA, V_{DD} = 8V operating		0.8	**1.2**	V
Rise Time	C_{LOAD} = 1nF, V_{DD} = 8V operating, $t_{90\%}$ - $t_{10\%}$		130	**240**	ns
Fall Time	C_{LOAD} = 1nF, V_{DD} = 8V operating, $t_{10\%}$ - $t_{90\%}$		130	**240**	ns
Output Voltage Clamp	V_{DD} = 20V, I_{LOAD} = -10µA	**10.5**	12.0	**13.4**	V
Unbiased Output Voltage Clamp	V_{DD} = 6V, I_{LOAD} = 3mA			**1.9**	V
Frequency		**291**	320	**349**	Hz
Maximum Duty Cycle	REFIN = 0.5V			**100**	%
Minimum On-Time	REFIN = 0V			**80**	µs
OVP					
OVP Threshold		**1.46**	1.50	**1.54**	V
OVP Hysteresis		**15**	20	**25**	µA
Input Bias Current	OVP = 1.0V	**-1.0**		**1.0**	µA
OVP Clamp Voltage	I_{OVP} = 5mA	**5.4**		**7.0**	V
THERMAL PROTECTION					
Thermal Shutdown	(Note 8)	**150**	160	**170**	°C
Hysteresis	(Note 8)		25		°C

NOTES:

7. Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested.
8. Limits established by characterization and are not production tested.

Typical Performance Curves

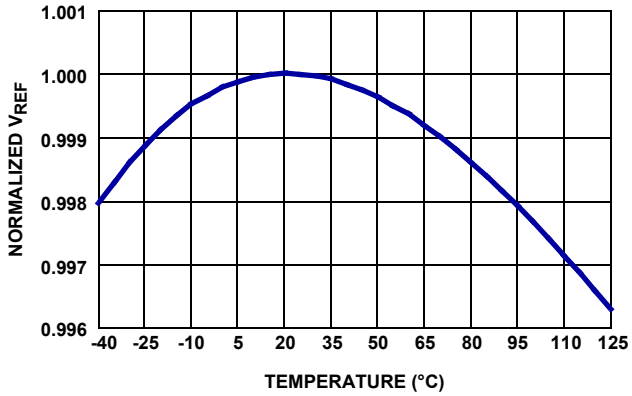


FIGURE 3. REFERENCE VOLTAGE vs TEMPERATURE

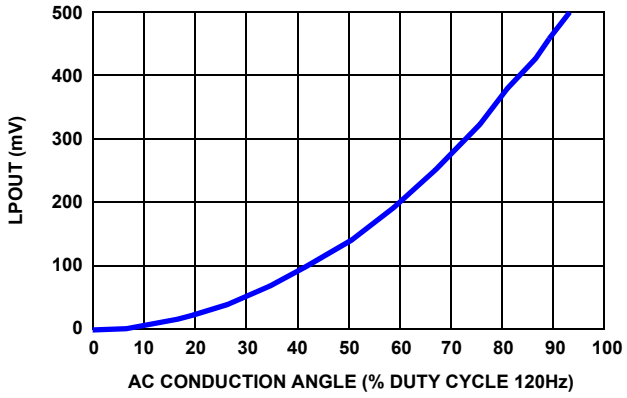


FIGURE 4. LPOUT vs AC SIGNAL DUTY CYCLE

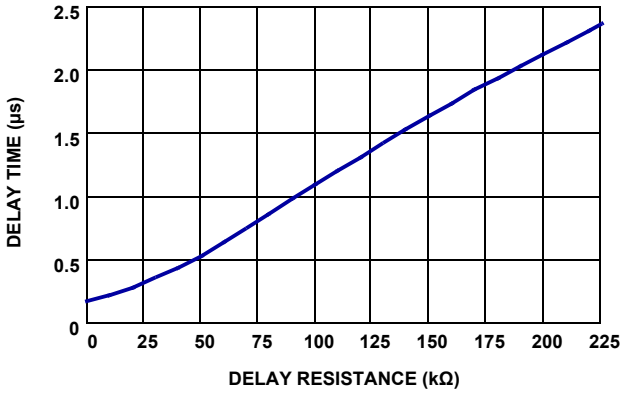


FIGURE 5. DELAY vs DELADJ RESISTANCE

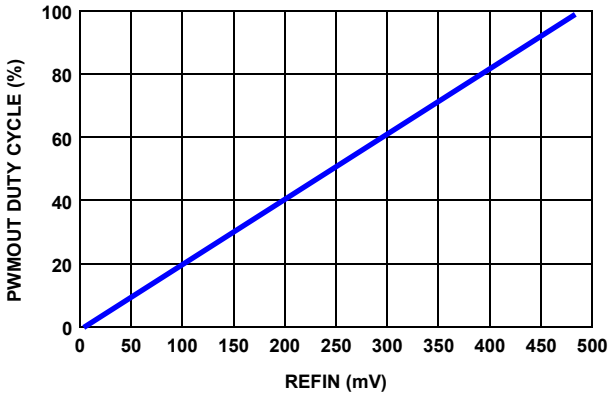
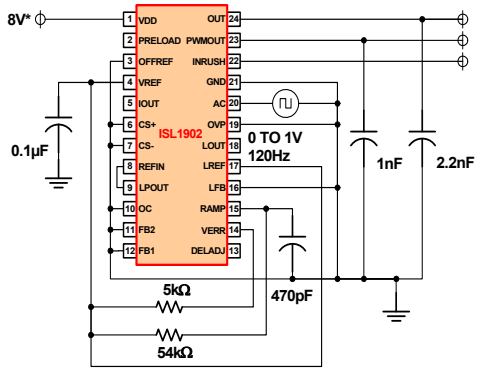


FIGURE 6. PWMOUT DUTY CYCLE vs REFIN

Test Waveforms and Circuits



*VDD set to 8V after exceeding UVLO start threshold

FIGURE 7. RISE/FALL TIME TEST CIRCUIT

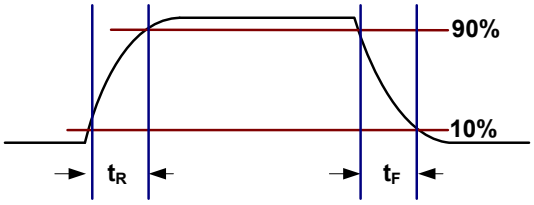


FIGURE 8. RISE/FALL TIMES

Test Waveforms and Circuits (Continued)

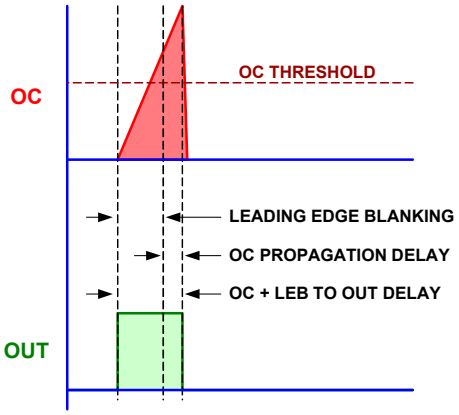


FIGURE 9. OC +LEB TO OUT DELAY

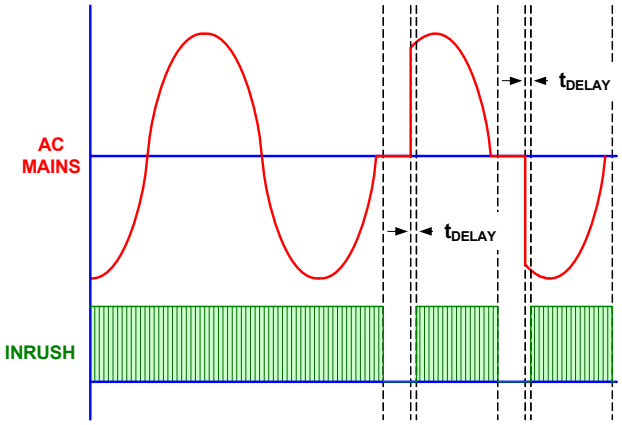


FIGURE 10. AC MAINS TO INRUSH TIMING

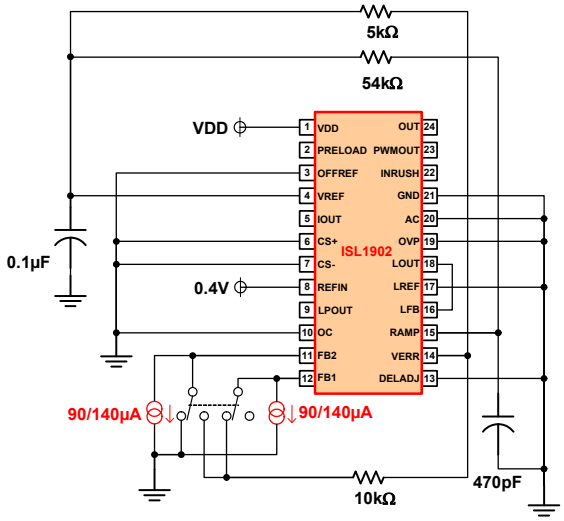


FIGURE 11. ERROR AMPLIFER INPUT OFFSET TEST CIRCUIT

Functional Description

Features

The ISL1902 LED driver is an excellent choice for low cost, AC mains powered single conversion LED lighting applications. It provides active power factor correction (PFC) to achieve high power factor using critical conduction mode operation, and incorporates additional features for compatibility with triac-based dimmers. The ISL1902 includes support for both PWM and DC current dimming of the output. Similar to the ISL1901, the ISL1902 adds additional features to facilitate the design of higher performance LED drivers.

Oscillator

The ISL1902 uses a critical conduction mode (CrCM) algorithm to control the switching behavior of the converter. The ON-time of the primary power switch is held virtually constant by the low bandwidth control loop. The OFF-time duration is determined by the time it takes the current or voltage to decay during the flyback period. When the MMF (Magneto Motive Force) of the magnetic element decays to zero (dB/dt=0), the winding voltages collapse and the winding currents are zero (flyback) or DC (SEPIC). Either may be monitored and used to initiate the next switching cycle to achieve CrCM operation. Additionally, there is a user adjustable threshold, DELADJ, to delay the initiation of the next switching cycle to allow the drain-source voltage of the primary switch to ring to a minimum. This allows quasi-ZVS operation to reduce capacitive switching losses and improve efficiency.

By its nature, the converter operation is variable frequency. There are both minimum and maximum frequency clamps that limit the range of operation. The minimum frequency clamp prevents the converter from operating in the audible frequency range while the maximum frequency clamp prevents operating at very high frequencies that may result in excessive losses.

An individual switching period is the sum of the ON-time, the OFF-time, and the restart delay duration. The ON-time is determined by the control loop error voltage, VERR, and the RAMP signal. As its name implies, the RAMP signal is a linearly increasing signal that starts at zero volts and ramps to a maximum of ~VERR/5 - 230mV. RAMP requires an external resistor and capacitor connected to VREF to form an RC charging network. If VERR is at its maximum level of VREF, the time required to charge RAMP to ~850mV determines the maximum ON-time of the converter. RAMP is discharged every switching cycle when the ON-time terminates.

The OFF-time duration is determined by the design of the magnetic element(s), which depends on the required energy storage/transfer and the inductance of the windings. The transformer/inductor design also determines the maximum ON-time that can be supported without saturation, so, in reality, the magnetic design is critical to every aspect of determining the switching frequency range.

THE FLYBACK TOPOLOGY

The design methodology is similar to designing a discontinuous mode (DCM) flyback transformer with the constraint that it must operate at the DCM/CCM boundary at maximum load and minimum input voltage. The difference is that the converter will always operate at the DCM/CCM boundary, whereas a DCM converter will be more discontinuous as the input voltage increases or the load decreases. For PFC applications, the design is further complicated by the input voltage waveform; a virtually unfiltered rectified AC mains sinewave.

Once the output power, P_O, the output current, I_O, the output voltage, V_O, and the minimum input AC voltage are known, the transformer design can be started. From the minimum AC input voltage, the minimum average input voltage must be determined. The converter behaves as if the input voltage is an equivalent DC value due to the low control loop bandwidth. P_O determines the amount of energy that must be stored in the transformer on each switching cycle, but must be corrected for efficiency. This includes leakage inductance losses, winding losses, and all secondary side losses. This can be estimated as a portion of the total efficiency, η, or as is typically done, includes all of the losses.

A typical minimum operating frequency and maximum duty cycle must be selected. These are somewhat arbitrary in their selection, but do ultimately determine core size. The typical frequency is what occurs when the instantaneous rectified input AC voltage is exactly at the equivalent DC value. The frequency will be higher when the instantaneous input voltage is lower, and lower when the instantaneous input voltage is higher. However, the duty cycle at the equivalent DC input voltage determines the ON-time for the entire AC half-cycle. The ON-time is constant due to the low bandwidth control loop, but the OFF-time and duty cycle vary with the instantaneous input voltage since the peak switch current follows V = Ldi/dt.

The lowest frequency may require adjustment once the initial calculations are complete to see if the operating frequency at the peak of the minimum AC input voltage is acceptable.

$$P_{IN} = \frac{P_o}{\eta} \quad W \qquad \text{(EQ. 1)}$$

TABLE 1. OSCILLATOR DEFINITIONS

V_{mINrms} =	Minimum RMS input voltage
$V_{maxINrms}$ =	Maximum RMS input voltage
$f_{typ(avg)}$ =	Typical frequency when V_{IN} (instantaneous) = V_{IN}(rms)
η =	Efficiency
D_{max} =	Maximum typical duty cycle desired
Dmin =	Minimum typical duty cycle
$t_{ON(MAX)}$ =	$f_{typ(avg)}$ x D_{max}
Ls =	Secondary inductance
Lp =	Primary inductance
Nsp =	Transformer turns ratio, Ns/Np
Ip(peak) =	Peak primary current within a switching cycle
t_{ON}	ON-time of the power FET controlled by OUT
t_{OFF}	OFF-time duration required for CrCM operation
t_{DELAY} =	User adjustable delay before the next switching cycle begins

The first calculation required is to determine the required secondary inductance.

$$L_s = \frac{V_o \cdot (1 - D_{max})^2}{f_{typ(avg)} \cdot 2 \cdot I_o} \quad H \qquad \text{(EQ. 2)}$$

The turns ratio N_{sp} is calculated next.

$$N_{sp} = \frac{V_o \cdot (1 - D_{max})}{\eta \cdot V_{mINrms} \cdot D_{max}} \qquad \text{(EQ. 3)}$$

Knowing the secondary inductance and the turns ratio, the primary inductance can be calculated.

$$L_p = \frac{L_s}{N_{sp}^2} \quad H \qquad \text{(EQ. 4)}$$

With this information, the lowest switching frequency, which occurs at maximum load and at the peak instantaneous input voltage at the minimum RMS voltage, can be determined. By setting the maximum duty cycle and picking a typical average frequency, the ON-time is already known.

$$t_{ON} = \frac{D_{max}}{f_{typ(avg)}} \quad s \qquad \text{(EQ. 5)}$$

The primary peak current at the end of the ON-time is:

$$I_{p(peak)} = \frac{V_{rms} \cdot \sqrt{2} \cdot t_{ON}}{L_p} \quad A \qquad \text{(EQ. 6)}$$

The peak secondary current is the peak primary current divided by the transformer turns ratio.

$$I_{s(peak)} = \frac{I_{p(peak)}}{N_{sp}} \quad s \qquad \text{(EQ. 7)}$$

And the OFF-time is:

$$t_{OFF} = \frac{L_s \cdot I_{s(peak)}}{V_o} \quad s \qquad \text{(EQ. 8)}$$

The lowest switching frequency is the reciprocal of the sum of the ON-time, the OFF-time, and the delay time.

$$f_{min} = \frac{1}{t_{ON} + t_{OFF} + t_{delay}} \quad Hz \qquad \text{(EQ. 9)}$$

The delay time can be approximated if the equivalent drain-source capacitance (C_{OSS}) of the primary switch is known. This value should also include any parasitic capacitance on the drain node. These parameters may not be known during the early stages of the design, but the required delay is typically on the order of 300ns to 500ns.

$$t_{delay} \approx \frac{\pi \cdot \sqrt{L_p \cdot (C_{oss} + C_{other})}}{2} \quad s \qquad \text{(EQ. 10)}$$

If the lowest frequency does not meet the design requirements, iterative calculations may be required.

The highest frequency is determined by the shortest ON-time summed with t_{delay}. The shortest ON-time occurs at high line and minimum load, and occurs at or near the AC zero crossing when the primary (and secondary) current is zero. The minimum non-zero ON-time is ~100ns, suggesting an operating frequency above 1MHz. In any event, the maximum frequency clamp would become active at around 800kHz. Once the primary and secondary inductances are known, the general formulae to calculate the ON-time and OFF-time at an equivalent DC input voltage are:

$$t_{OFF} = \frac{2 \cdot L_s \cdot I_o}{V_o} \cdot \left(1 + \frac{L_p \cdot N_{sp} \cdot V_o}{L_s \cdot V_{INrms}}\right) \quad s \qquad \text{(EQ. 11)}$$

$$t_{ON} = \frac{2 \cdot L_p \cdot N_{sp} \cdot I_o}{V_{INrms}} \cdot \left(1 + \frac{L_p \cdot N_{sp} \cdot V_o}{L_s \cdot V_{INrms}}\right) \quad s \qquad \text{(EQ. 12)}$$

It is clear from these equations that there is a linear relationship between load current and frequency. At some light load, the frequency will be limited by the maximum frequency clamp. The frequency has an inverse relationship to input voltage and has a less significant affect over a typical operating range.

It should be noted, however, that the above equations assume full conduction angle of the AC mains. When conduction angle modulating dimmers are used to block a portion of each AC half-cycle, the switching currents remain essentially unchanged during the conduction portion of the AC half-cycle as the conduction angle is reduced. The result being that the steady state frequency behavior will not vary much as the conduction angle is reduced from full. If an analog control signal is used instead, the frequency behavior will be as predicted above.

THE SEPIC TOPOLOGY

The SEPIC topology, in simplified form, is shown in Figure 12. The voltage source indicated may be either DC or rectified AC. The capacitance of C_{IN} is negligibly small for applications requiring PFC.

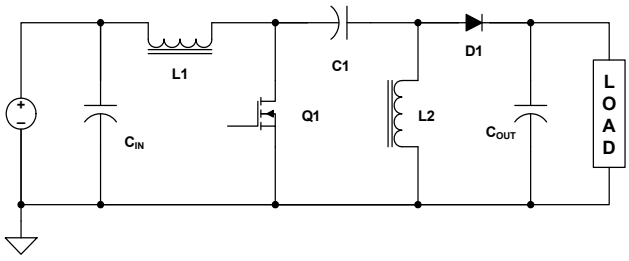


FIGURE 12. SEPIC TOPOLOGY

The terminology defined in Table 1 shall be reused, except Ls and Lp are replaced by L1 and L2 per Figure 12. In steady state operation, the average voltage across L1 and L2 must be zero. If this were not true, saturation would occur. Furthermore, this situation implies the voltage across C1 must be equal to the input source voltage, V_{IN}. During the ON-time, when switch Q1 is conducting, the voltage across each inductor is V_{IN}. During the OFF-time, Q1 is off, and the voltage across each inductor is $-V_{OUT}$. Since no DC current may flow through C1, the output current, I_O, must be equal to the average current flowing in L2. Additionally, I_O is also the average current that flows in both inductors during the OFF-time.

To determine the values of L1 and L2, the operating conditions must be defined. The lowest operating frequency occurs at maximum load and minimum input voltage. If operating from and AC source, the lowest frequency occurs at the instantaneous

peak of the AC voltage waveform at the lowest RMS input voltage. Therefore, the lowest DC or equivalent DC (RMS) input voltage is used as the design point with a corresponding selection of a minimum desired operating frequency.

During the ON-time, the current in L2 ramps from zero to a peak value, I_P.

$$I_P = \frac{V_{IN(minRMS)} \cdot t_{ON}}{L2} \quad A \qquad \text{(EQ. 13)}$$

where $V_{IN(minRMS)}$ is defined as the minimum DC or RMS input voltage. During the OFF-time, the current ramps from I_P back down to zero at a rate determined by V_{OUT}.

$$I_P = \frac{V_{OUT} \cdot t_{OFF}}{L2} \quad A \qquad \text{(EQ. 14)}$$

Since the average value of current in L2 must be the load current, I_O, Equations 13 and 14 can be used to relate the DC or RMS input voltage values for t_{ON} and t_{OFF} to I_O.

$$t_{ON} = \frac{I_O \cdot 2 \cdot L2}{V_{IN(minRMS)}} \quad s \qquad \text{(EQ. 15)}$$

$$t_{OFF} = \frac{I_O \cdot 2 \cdot L2}{V_{OUT}} \quad s \qquad \text{(EQ. 16)}$$

Equations 15 and 16 may be summed to provide an equivalent switching period for the equivalent DC (RMS) input and stated design parameters, and the value for L2 may be calculated. For DC input applications, the calculation is straight forward.

$$t_S = t_{ON} + t_{OFF} + t_{delay} \quad s \qquad \text{(EQ. 17)}$$

where t_{delay} is a constant and defined in the next section, “Quasi-Resonant Switching”.

$$L2 = \frac{t_S \cdot V_{OUT} \cdot V_{IN(minRMS)}}{2 \cdot I_{OUT} \cdot (V_{OUT} + V_{IN(minRMS)})} \quad H \qquad \text{(EQ. 18)}$$

When the input voltage is rectified AC, the desired switching period has to be modified to account for the difference between the RMS voltage and the instantaneous peak of the AC waveform. The frequency is lower at the AC peak than at the equivalent DC (RMS) input voltage.

$$t_S = \sqrt{2} \cdot (t_{ON} + t_{OFF}) + t_{delay} \quad s \qquad \text{(EQ. 19)}$$

Using Equation 19 for t_S and substituting into Equation 18 yields the appropriate value for L2 in rectified AC input applications.

As stated previously, both inductor currents flow to the output during the OFF-time. I_O may be solved for by averaging the sum of both inductor currents during the OFF-time over a complete switching cycle.

$$I_O = \frac{V_{OUT} \cdot t_{OFF}^2}{2 \cdot (t_{ON} + t_{OFF})} \cdot \left(\frac{1}{L1} + \frac{1}{L2}\right) \quad A \qquad \text{(EQ. 20)}$$

Using Equations 15 and 16 and solving for L1 yields:

$$L1 = \frac{V_{IN(minRMS)} \cdot L2}{V_{OUT}} \quad H \qquad \text{(EQ. 21)}$$

The final step in specifying the inductor requirements is to determine the DC bias on each inductor. Earlier it was assumed that each inductor current ramps from zero to some peak value during the ON-time. In reality each inductor has a DC bias current that does not contribute to the output current and may be ignored in the previous calculations, but its value is required to determine the RMS currents in each inductor. The reason the DC bias exists is that there can be no DC current through C1 (see Figure 12). The current flowing from L2 into C1 during the ON-time must equal the current flowing in the opposite direction from L1 during the OFF-time.

$$I_{C1} = I_{DC} + \frac{V_{OUT} \cdot t_{OFF}^2}{2 \cdot L1 \cdot t_S} - \frac{V_{IN(minRMS)} \cdot t_{OFF}^2}{2 \cdot L2 \cdot t_S} \quad A \qquad \text{(EQ. 22)}$$

where I_{C1} is the current through C1 during a complete switching cycle, I_{DC} is the DC bias current, and $T_S = T_{ON} + T_{OFF}$. Equation 22 can also be used on a cycle-by-cycle basis providing instantaneous values of T_{ON}, T_{OFF} and V_{IN} are used. Setting Equation 22 equal to zero and solving for I_{DC} yields Equation 23,

$$I_{DC} = I_O \cdot \frac{V_{IN(minRMS)} - V_{OUT}}{V_{IN(minRMS)} + V_{OUT}} \quad A \qquad \text{(EQ. 23)}$$

which represents the DC bias current flowing from L1 through C1 into L2 at the equivalent DC (RMS) input voltage. It may be thought of as the expected value of bias current. In rectified AC input applications, the bias current varies as needed each switching cycle to balance charge on C1 as the AC voltage varies from valley to peak to valley during each AC half-cycle.

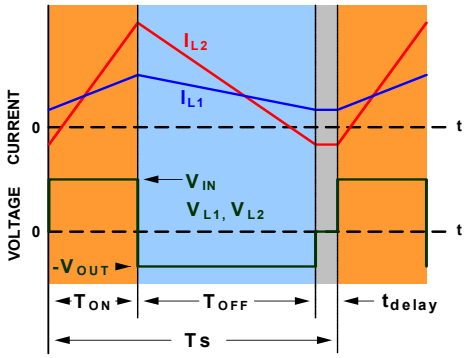


FIGURE 13. SEPIC WAVEFORMS

Quasi-Resonant Switching

The ISL1902 uses critical conduction mode PWM control algorithm. Near zero voltage switching (ZVS) or quasi-resonant switching, as it is sometimes referred to, can be achieved in the flyback topology by delaying the next switching cycle after the transformer current decays to zero (critical conduction mode). The delay allows the primary inductance and capacitance to oscillate, causing the switching FET drain-source voltage to ring down to a minima. If the FET is turned on at this minima, the capacitive switching loss ($1/2\ CV^2$) is greatly reduced.

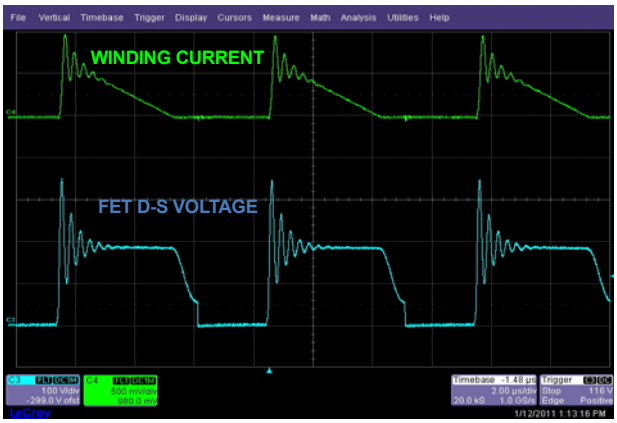


FIGURE 14. QUASI-RESONANT NEAR-ZVS SWITCHING

The delay duration is set with a resistor from DELADJ to ground. Figure 5 on page 12 presents the graphical relationship between the delay duration and the value of the DELADJ resistance. The relationship is linear for resistance values greater than ~ 20kΩ and can be estimated using Equation 24.

$$t_{delay} \approx 73.33 + 10.2 \cdot R_{DELADJ}(k\Omega) \quad ns \qquad \text{(EQ. 24)}$$

Soft-Start Operation

Soft-start is not user adjustable and is fixed at ~350ms. Both the duty cycle and control loop reference have soft-start. This ensures a well behaved closed loop soft-start that results in virtually no overshoot.

Biasing

The ISL1902 has a nominal V_{DD} start and stop threshold of 15.5V and 7.1V, respectively. The wide hysteresis allows resistive trickle charging from the high voltage input for start-up bias. Operating bias is then supplied from another source, such as an auxiliary transformer winding or in the case of a non-isolated design, directly from the output or from a tap in the LED string.

The V_{DD} bypass capacitance value is critical to a successful design. Unless there is a DC source available, such as the output, the V_{DD} capacitance must be able to store enough energy to provide bias during the AC voltage valleys and, if used with a dimmer, provide bias when the dimmer is blocking the AC voltage each half-cycle.

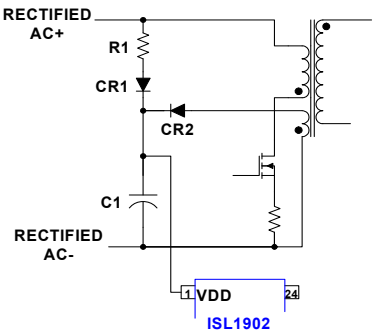


FIGURE 15. TRICKLE CHARGE START-UP W/AUX. WINDING

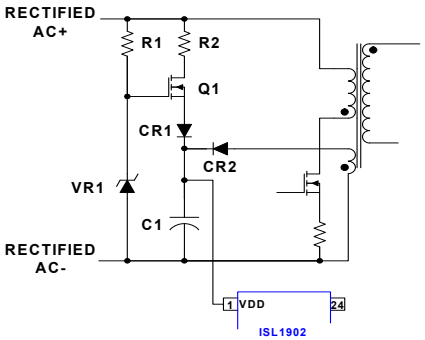


FIGURE 16. LINEAR REGULATOR START-UP W/AUX. WINDING

AC Detection and Reference Generation

The ISL1902 creates a 0V to -0.5V reference for the LED current control loop (EA reference) by directly measuring the conduction angle of the AC input voltage. The reference changes only with conduction angle and is virtually unaffected by variation in either voltage amplitude or frequency. The ISL1902 is compatible with both leading and trailing edge modulated dimmers.

The ISL1902 detects the conduction angle using a divider network across the AC line and connected to the AC pin, although it can also be located after the AC bridge rectifier.

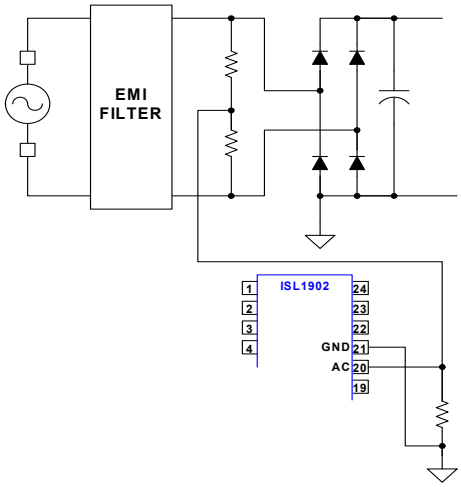


FIGURE 17. AC DETECTION

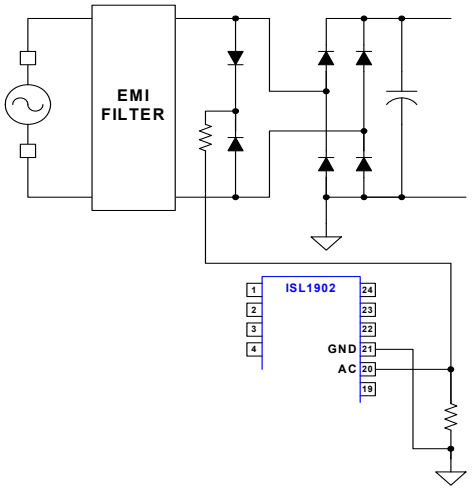


FIGURE 18. ALTERNATE AC DETECTION

The advantage to sensing the AC voltage directly, rather than the rectified voltage, is that there is no error in detecting the AC zero crossing. If monitored after the AC rectifier bridge, the AC signal tracks the filter capacitor voltage, which may not discharge in phase with the AC voltage. This can lead to incorrect detection of the AC zero crossing. At light load, the filter capacitor may not fully discharge before the AC voltage begins to increase again, resulting in no detection of the AC zero crossing at all.

The AC pin and has a usable input range of 0V to 4V. The peak of the input signal should range between 1V and 4V for uncompromised accuracy. The AC detection circuit measures both the duration of the AC conduction angle and half-cycle duration. By comparing them every half-cycle, the detection circuit creates a frequency independent reference that is updated each AC half-cycle.

The reference generated by the AC detection circuit is available as the LPOUT signal. Here it can be modified, or not, and connected to REFIN for setting the control loop reference. Examples of modification include interfacing with an external transducer, such as an ambient light sensor (ALS) or temperature sensor (NTC or PTC) to modify the reference based on the sensor input.

The ISL1902 also supports analog dimming control by allowing the control loop reference to be connected to REFIN, bypassing LPOUT completely.

AC may be directly coupled to a 90Hz to 130Hz PWM signal to generate a reference if dimming is desired without using an AC dimmer, or an independent reference may be input to REFIN with LPOUT not connected.

In the event of an AC outage, the AC mains frequency reference is lost. The ISL1902 will force the reference to zero volts and reset the soft-start circuit approximately 35ms after the last AC zero crossing is detected. If AC is held above its detection threshold for more than 35ms, the internal reference is forced to its maximum of 0.5V.

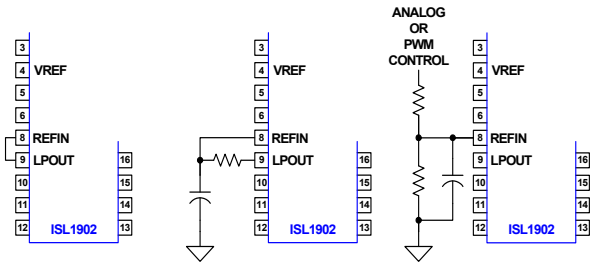


FIGURE 19. ALTERNATE CONFIGURATIONS FOR THE CONTROL LOOP REFERENCE

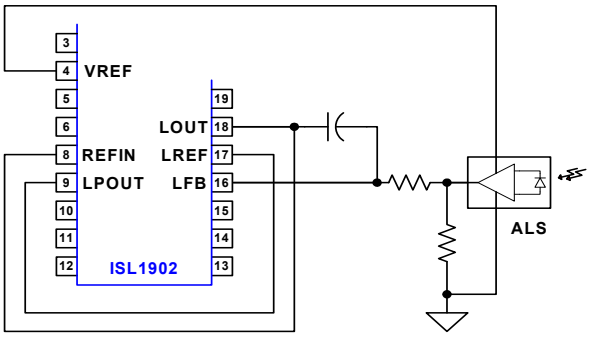


FIGURE 20. USING AN AMBIENT LIGHT SENSOR WITH AN AC LINE DIMMER

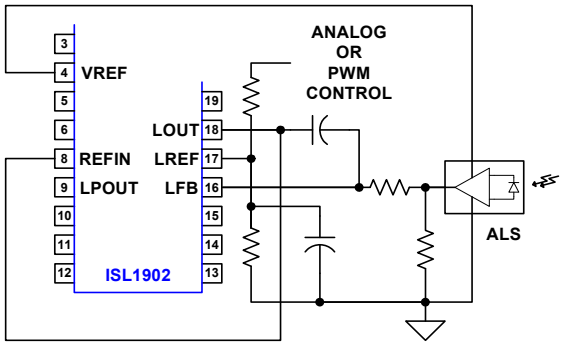


FIGURE 21. USING AN AMBIENT LIGHT SENSOR WITH ANALOG OR PWM INPUT

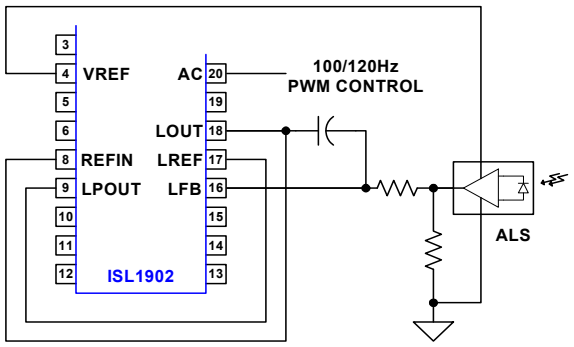


FIGURE 22. ALTERNATE METHOD FOR USING PWM INPUT CONTROL WITH AN AMBIENT LIGHT SENSOR

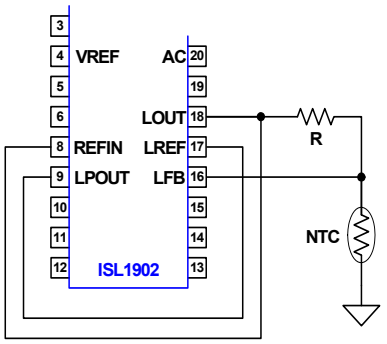


FIGURE 23. TEMPERATURE COMPENSATING THE REFERENCE USING AN NTC

Current Sensing

The ISL1902 is configured to regulate the output current by differentially monitoring the output switching current using the CS+ and CS- pins. The output switching current waveform is amplified 4x and output on IOUT where it must be scaled and filtered before being input to the control loop at the FB pin. The required filter time constant depends on the compensated error amplifier bandwidth. The filter bandwidth must be higher than the control loop bandwidth, typically an order of magnitude higher, but it is generally not necessary to filter the IOUT signal to form a nearly DC voltage. The compensated error amplifier performs that function.

The OC pin provides cycle-by-cycle overcurrent protection. The output FET drive signal OUT is terminated if OC exceeds 0.6V nominal. There is ~120ns of leading edge blanking (LEB) on OC to minimize or eliminate external filtering.

Dimming

The ISL1902 supports both PWM and DC current modulation dimming. DC current dimming is the lower cost method, but results in a non-linear dimming characteristic due to the increasing efficacy of the LEDs as current is reduced. PWM dimming results in linear dimming behavior.

An external FET, controlled by PWMOUT, switches the LED current on and off to achieve PWM dimming.

In either case, the control loop determines the average current delivered to the load. It does not matter if the load current is DC or pulsed, the converter output capacitance and control loop operate to filter and average the converter output current independently of the actual load current waveform.

The dimming PWM and control loop are linked together such that the PWM duty cycle tracks the main control loop reference setpoint. If the control loop is set for 50% load, for example, the dimming PWM duty cycle is set for 50%. The LED current will be at 100% load for 50% of the time and 0% load for 50% of the time, which averages to the 50% average load setpoint. See Figure 6 for a graphical representation of the relationship between REFIN and PWMOUT duty cycle. It should be noted that the PWMOUT duty cycle is not allowed to go to zero. There is a minimum on-time that ensures the LED string is not allowed to become a continuos open circuit.

Aside from tracking the main control loop reference, the PWM dimming control is open loop, but is nevertheless self regulating. There is no closed loop feedback to regulate the load current during PWM conduction as is the case with most PWM dimming methods. If the average current into and out of the output capacitor is not equal, the output voltage will change, increasing or decreasing with the polarity of the charge imbalance. The forward voltage characteristic of the LEDs will cause the current to increase or decrease with the change in output voltage until the average capacitor current returns to zero. Figures 24 and 25 show a simulation schematic and results, respectively, illustrating the PWM dimming behavior for a 50% loaded condition. The converter output is idealized and represented as a 50mA DC current source and the PWM is operating at 50% duty cycle.

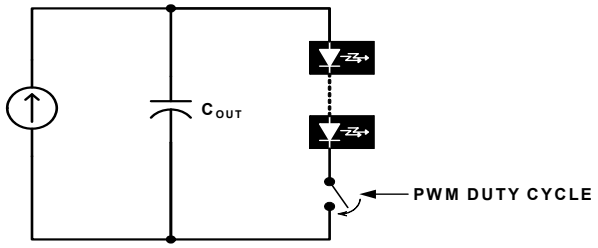


FIGURE 24. PWM DIMMING SIMULATION SCHEMATIC

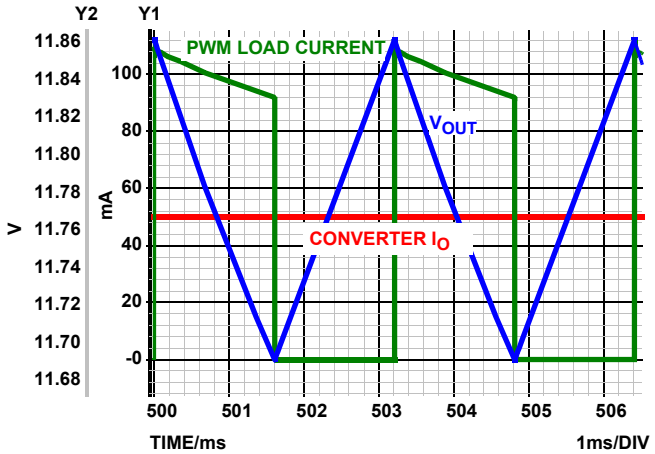


FIGURE 25. PWM DIMMING RESULTS

The red trace is the current source supplying the output. The blue trace is the output capacitor voltage. The green trace is the LED current. When the PWM signal is off, the 50mA current source charges C_{OUT} and the output voltage increases. When the PWM turns on, 100mA of current flows through the LEDs, with the initial current slightly higher and the final current slightly lower as C_{OUT} discharges. The peak-to-peak ripple voltage on C_{OUT} is ~160mV. The decrease in the LED current during conduction is determined by the size of the output capacitor and the LED current.

Linear Amplifier

The linear amplifier block is a fully accessible uncommitted operational amplifier. It may be used for a variety of purposes, such as interfacing sensors, direct sensing of LED current, or a pre-load amplifier. Examples of using the linear amplifier as a sensor interface are shown in Figures 20 through 23.

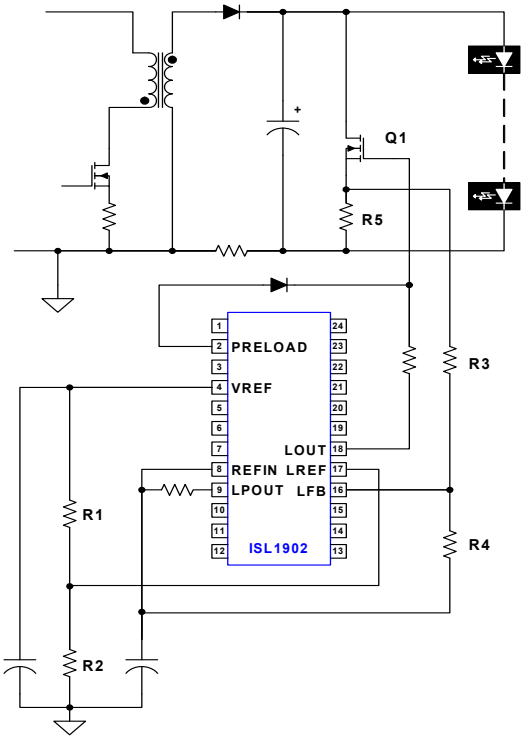


FIGURE 26. LINEAR AMPLIFIER CONFIGURED AS PRE-LOAD

The linear amplifier may be used as a pre-load control to provide a larger dynamic dimming range as well as providing additional holding current for applications using triac-based dimmers. As shown in Figure 26, the pre-load can be configured as an active load that increases linearly as the control loop reference level (REFIN) decreases. The result is not only is the total load current decreased as REFIN is lowered, but an increasing portion of the load current is shunted to the pre-load. At some point, the preload conducts all of the load current while allowing zero LED current. This allows the converter to continue operation to maintain circuit bias with zero LED current. Very high levels of LED dimming resolution become achievable. Both the maximum pre-load current and turn-on threshold are adjustable.

Again referring to FIgure 26, the voltage across R5 represents the current flowing in the pre-load. The maximum level of this signal is limited by the VOH of the linear amplifier and the gate threshold voltage of the pre-load FET, Q1. A reasonable maximum voltage for this signal is 3.0V. Therefore, the maximum pre-load current, I_{PL}, is 3.0/R5.

$$V_O = V_{R5} = LREF \cdot \left(1 + \frac{R3}{R4}\right) - \left(\frac{R3}{R4} \cdot REFIN\right) \quad V \qquad \text{(EQ. 25)}$$

where LREF and REFIN are the voltages at the LREF and REFIN pins, respectively. For purposes of illustration, if R3 and R4 are equal, Equation 25 simplifies to:

$$V_O = V_{R5} = 2 \cdot LREF - REFIN \quad V \qquad \text{(EQ. 26)}$$

Equation 26 shows that if REFIN is greater than 2x LREF, V_O is non-positive and the pre-load is not conducting. With proper selection of LREF and R3/R4, the pre-load turn-on threshold and gain characteristics can be matched to the application requirements.

$$\frac{R3}{R4} = \frac{3 - (0.5 \cdot \%H) \pm \sqrt{(0.5 \cdot \%H - 3)^2 + 6 \cdot \%H}}{\%H} \qquad \text{(EQ. 27)}$$

where%H is the selected fraction of maximum load when the pre-load begins to conduct.

$$LREF = \frac{\frac{R3}{R4} \cdot 0.5 \cdot \%H}{1 + \frac{R3}{R4}} = VREF \cdot \frac{R2}{R1 + R2} \quad V \qquad \text{(EQ. 28)}$$

As an example, assume the pre-load should begin to operate at 75% of full load, and that the maximum pre-load current, I_{PL}, is 50mA. Using Equation 27 to solve for the ratio of R3/R4 yields a result of 8. Equation 28 yields a value of 0.333V for LREF. Remembering the maximum allowed voltage across R5 is 3.0V yields R5 = 3.0V/50mA = 60Ω at 150mW. V_O is plotted in Figure 27.

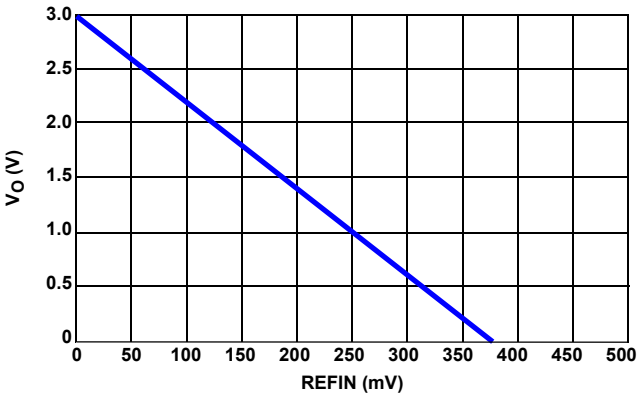


FIGURE 27. PRE-LOAD EXAMPLE

Alternatively, the linear amplifier may be used to control a second LED string, either to force current sharing, or to control a colored LED string for color correction. The second string can be controlled from the same reference as the first LED string allowing the string currents to track, or it can be controlled from a separate reference that allows the two strings to work in opposition, sharing the load current in proportion to each reference. Figure 28 shows the tracking configuration.

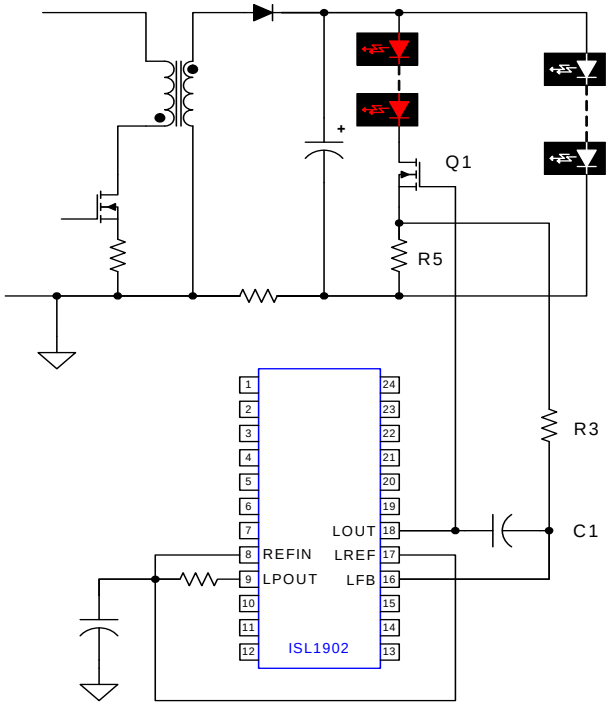


FIGURE 28. SECOND LED STRING CONTROL

The linear amplifier may also be used to measure and scale the LED current directly rather than using the differential current sensing inputs, CS+ and CS-, that measure the switching current. Amplifying the signal allows a smaller sensing resistor value for improved efficiency. As shown in Figure 29, the voltage across R4 is scaled by the linear amplifier with a gain of 1 + R2/R1.

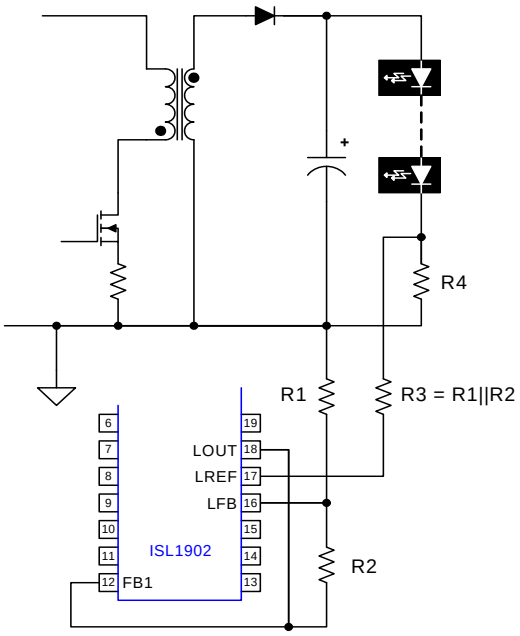


FIGURE 29. DIRECT LED CURRENT SENSING

Control Loop

The control loop configuration is user adjustable with selection of the external compensation components. For applications requiring power factor correction (PFC), a very low bandwidth integrator is used, typically 20Hz or less. In other applications, the control loop bandwidth can be increased as required, like any other externally compensated voltage mode PWM controller.

The ISL1902 has two error amplifiers that share a common non-inverting input and a common output. Each EA can sink current, but has negligible sourcing capability. An external pull-up resistor to VREF is required. This configuration causes the EA with lowest output to be dominant. EA1 is the principal error amplifier and is compensated externally for low bandwidth for PFC applications. The downside to a low bandwidth amplifier is that it cannot respond to input transients quickly. This is where the second EA comes in. It can be configured for a much higher bandwidth so that transient response is greatly improved. Under normal operating conditions EA2 is not active. Its feedback network is set for a higher output than EA1. When an input surge occurs, EA1 cannot respond rapidly and the surge propagates to the output. EA2 becomes active when its feedback voltage exceeds the reference setpoint and acts to reduce the output transient. The difference in setpoint is accomplished by weighting the feedback networks to the EAs appropriately.

The voltage on IOUT is a scaled version of the CS+/CS- differential signal, having been amplified by 4x. When averaged, it is a scaled representation of the converter output current, I_O. By measuring IOUT in this manner, both average and instantaneous inductor currents are known. The instantaneous inductor current information informs the critical conduction mode (CrCM) oscillator when the switching current has decayed to zero.

Figure 30 shows a typical configuration for the control loop. The sensing resistor R_S determines the amplitude of the CS+ signal. At maximum load this signal must be scaled to match the 0.5V maximum reference. Since IOUT is 4x the amplitude of the CS+ signal, a simple resistor divider with filtering is required to scale IOUT prior to connecting to the FB input.

$$R_S = \frac{V_{REF}}{A_{IOUT} \cdot A_{DIVIDER} \cdot I_O} \quad \Omega \qquad \text{(EQ. 29)}$$

where A_{IOUT} is the IOUT buffer gain (nominally 4x), $A_{DIVIDER}$ is the gain of the external resistor divider on IOUT ($R2/(R1 + R2)$), V_{REF} is the maximum reference level (0.5V), and I_O is the maximum output current. In most applications, R_S will be sized to minimize power dissipation while providing adequate signal level. The minimum value of the $I_O R_S$ product is 125mV, required to achieve 0.5V on IOUT.

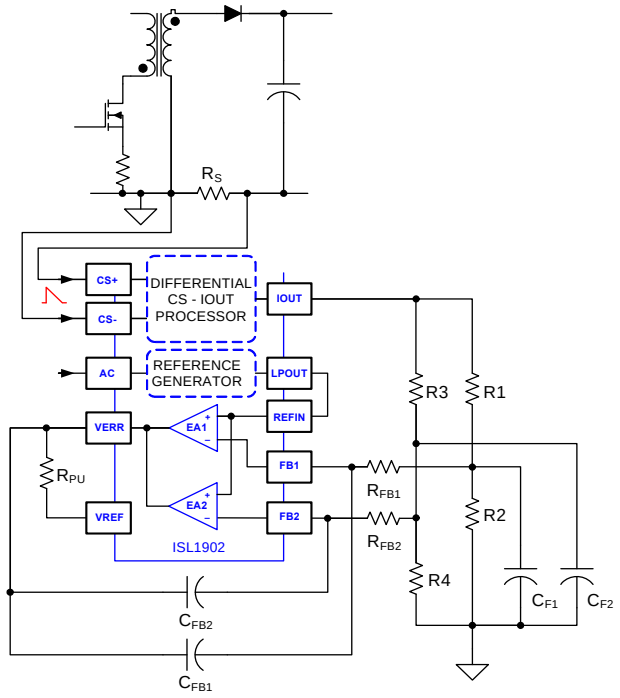


FIGURE 30. CONTROL LOOP CONFIGURATION

In applications requiring PFC, the fast loop bandwidth can be set to react to line transients without affecting steady state operation. For example, the slow loop requires IOUT to be filtered with a time constant of 50ms to 100ms. The fast loop (to be effective), requires less filtering on IOUT and requires a bandwidth three orders of magnitude (1000x) higher with a 60% divider weighting compared to the slow loop (taking into account the peak-to-average ratio of a sinusoid).

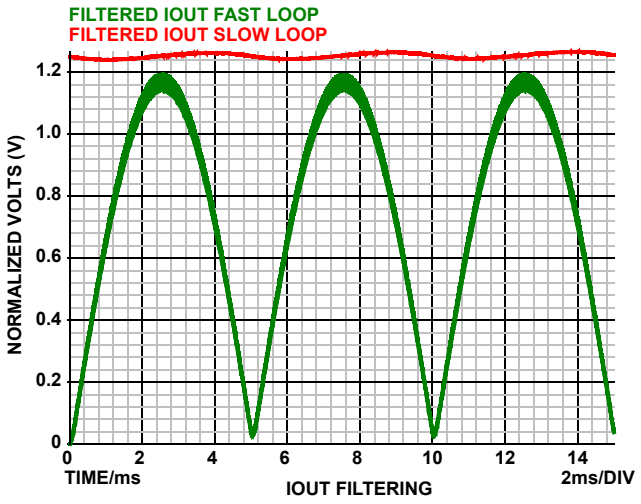


FIGURE 31. IOUT FILTERED WAVEFORMS (100Hz)

OVP

The ISL1902 has independent overvoltage protection accessed through the OV pin. There is a nominal 20µA switched current source used to create hysteresis. The current source is active only during an OV fault; otherwise, it is inactive and does not affect the node voltage. The magnitude of the hysteresis voltage is a function of the external resistor divider impedance.

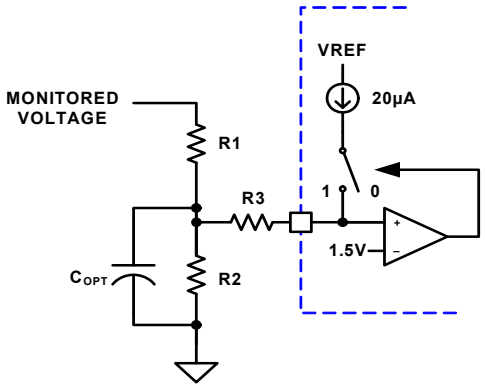


FIGURE 32. OV HYSTERESIS

$$V_{ov(rising)} = 1.5 \cdot \frac{(R1 + R2)}{R2} \quad V \qquad \text{(EQ. 30)}$$

If the divider formed by R1 and R2 is sufficiently high impedance, R3 is not required, and the hysteresis is:

$$\Delta V = 20 \cdot 10^{-6} \cdot R1 \quad V \qquad \text{(EQ. 31)}$$

If that does not result in the desired hysteresis then R3 is needed, and the hysteresis is:

$$\Delta V = 20 \cdot 10^{-6} \cdot \left(R1 + R3 \cdot \frac{(R1 + R2)}{R2}\right) \quad V \qquad \text{(EQ. 32)}$$

If the OV signal requires filtering, the filter capacitor, C_{OPT}, should be placed as shown in Figure 17. The current hysteresis provides great flexibility in setting the magnitude of the hysteresis voltage, but it is susceptible to noise due to its high impedance. If the hysteresis was implemented as a fixed voltage instead, the signal could be filtered with a small capacitor placed between the OV pin and signal ground. This technique does not work well when the hysteresis is a current source because a current source takes time to charge the filter capacitor. There is no instantaneous change in the threshold level rendering the current hysteresis ineffective. To remedy the situation, the filter capacitor must be separated from the OV pin by R3. The capacitor and R3 must be physically close to the OV pin.

OFFREF Control

The ISL1902 provides the ability to disable the output based on the level of the control loop reference, REFIN. Setting OFFREF to a voltage between 0 and 0.6V determines the threshold voltage that disables the output.

$$REFIN(off) = OFFREF - 0.100 \quad V \qquad \text{(EQ. 33)}$$

OFFREF allows the designer to disable the output at a predetermined load current to prevent undesirable behavior, such as at light loading conditions when there may be insufficient current to maintain the holding current in a triac-based dimmer. Setting OFFREF to less than 100mV disables this feature. OFFREF has a nominal hysteresis of 50mV.

PRELOAD Signal

PRELOAD is a digital signal used to control an external FET that discharges the output capacitance if AC is low for more than ~30ms, or if REFIN drops below the OFFREF threshold. This feature prevents the output capacitor from providing load current for an extended period of time after the converter is disabled. Otherwise, the output will dim as the output capacitance slowly discharges through the LEDs. This process can take a significant amount of time, resulting in “afterglow”, unless supplemental discharge methods are used. The advantage of PRELOAD over a non-switched resistive load is efficiency improvement. Examples of PRELOAD usage may be found on pages 5 through 7 in the “Typical Applications”.

In-rush Control

The ISL1902 features a AC half-cycle-by-half-cycle in-rush control signal. Due to the capacitive input of DC/DC converters operating with a leading edge modulated AC line dimmer, there is an input current spike every half-cycle when the AC line dimmer turns on, particularly so when conduction begins near the AC peak. The current spike is normally attenuated with a resistor in series with the AC line. The resistor is always present and dissipates power even at full dimmer conduction.

The ISL1902 provides a control signal, INRUSH, which may be used to gate an external switch, such as a triac to bypass the in-rush limiting resistor after the in-rush event is over. The signal is low when the IC detects the absence of AC line voltage. When enabled, approximately 150µs after AC voltage is detected, IN-RUSH outputs an 80kHz square wave. This may be coupled through a pulse transformer or other isolation device to allow control of a level shifted device. Examples of using INRUSH can be found in the “Typical Applications” on pages 5 and 7. Another example is shown in Figure 33.

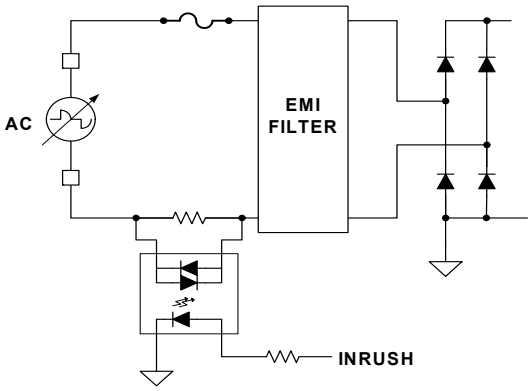


FIGURE 33. INRUSH EXAMPLE USING A PHOTO-TRIAC

Gate Drive

The ISL1902 output is capable of sourcing and sinking 1.5A. The typical ON-resistance of the outputs is 12Ω. The OUT high level is limited to the OUT clamp voltage or V_{DD}, whichever is lower.

Thermal Protection

Internal die over-temperature protection is provided. An integrated temperature sensor protects the device should the junction temperature exceed +150°C. There is approximately +25°C of hysteresis.

Ground Plane Requirements

Careful layout is essential for satisfactory operation of the device. A good ground plane must be employed. V_{DD} and VREF should be bypassed directly to GND with good high frequency capacitance.

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please go to web to make sure you have the latest revision.

DATE	REVISION	CHANGE
March 20, 2013	FN7981.2	Initial Release.

About Intersil

Intersil Corporation is a leader in the design and manufacture of high-performance analog, mixed-signal and power management semiconductors. The company's products address some of the fastest growing markets within the industrial and infrastructure, personal computing and high-end consumer markets. For more information about Intersil or to find out how to become a member of our winning team, visit our website and career page at www.intersil.com.

For a complete listing of Applications, Related Documentation and Related Parts, please see the respective product information page. Also, please check the product information page to ensure that you have the most updated datasheet: ISL1902

To report errors or suggestions for this datasheet, please go to: www.intersil.com/askourstaff

Reliability reports are available from our website at: http://rel.intersil.com/reports/search.php

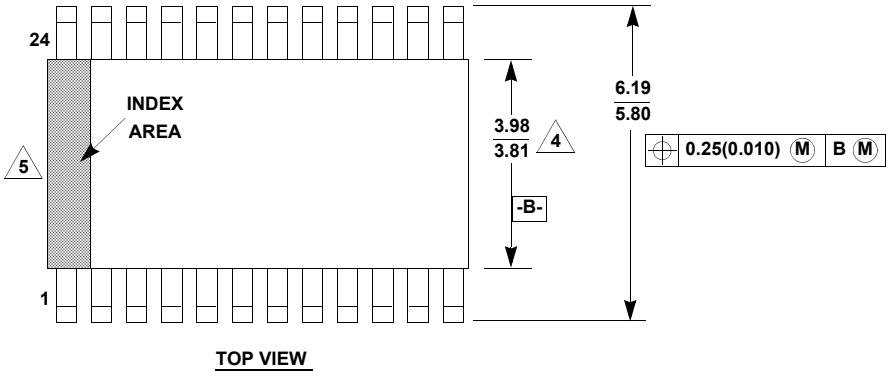
Package Outline Drawing

M24.15

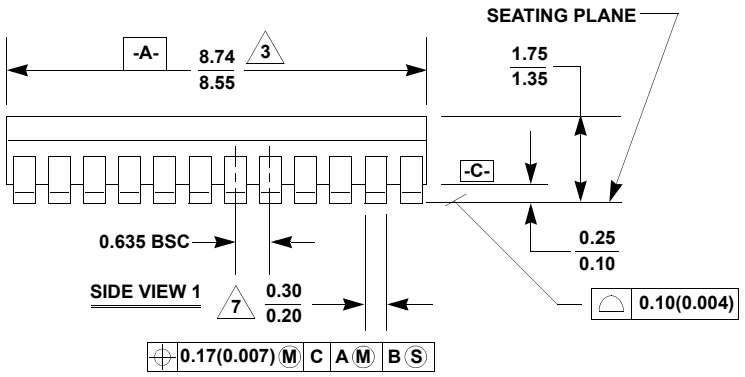
24 LEAD SHRINK SMALL OUTLINE PLASTIC PACKAGE (QSOP/SSOP)

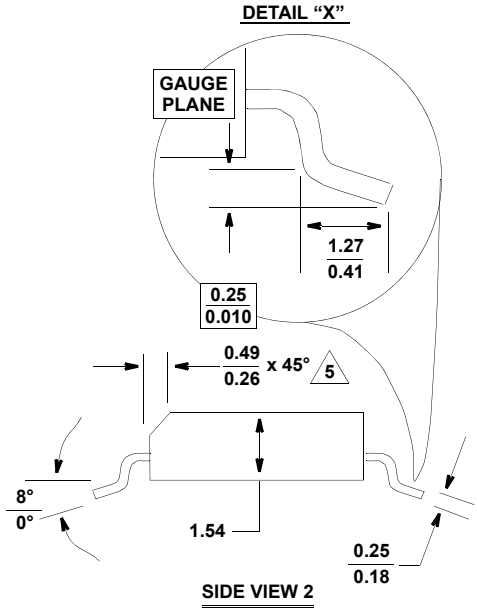
0.150" WIDE BODY

Rev 3, 2/13

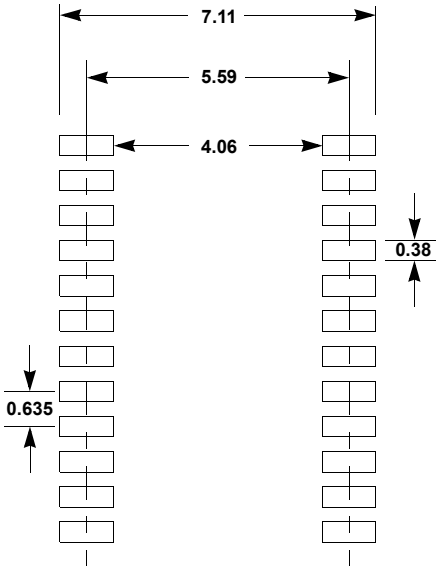


TOP VIEW





SIDE VIEW 2



TYPICAL RECOMMENDED LAND PATTERN

NOTES:

1. Symbols are defined in the "MO Series Symbol List" in Section 2.2 of Publication Number 95.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Package length does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Package width does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. Terminal numbers are shown for reference only.
7. Lead width does not include dambar protrusion. Allowable dambar protrusion shall be 0.10mm (0.004 inch) total in excess of "B" dimension at maximum material condition.
8. Controlling dimension: MILLIMETER.