

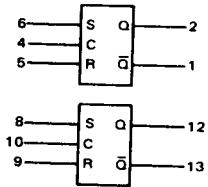
DUAL R-S FLIP-FLOPS
WITH POSITIVE CLOCK

MECL II MC1000/1200 series

MC1014
MC1214

Two dc Set-Reset flip-flops with a positive clock input provided for each flip-flop. This device is useful as a dual storage element and may be teamed with the MC1015/MC1215 for shift register functions with a minimum number of packages.

POSITIVE LOGIC



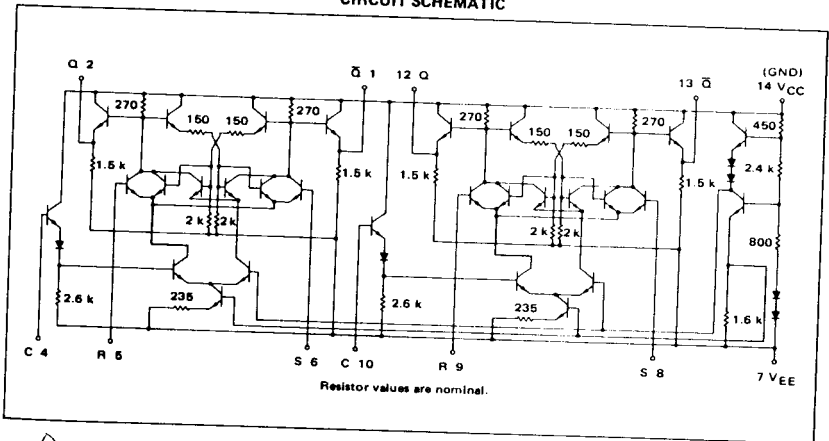
TRUTH TABLE

R	S	C	Q ⁿ⁺¹
0	1	1	1
1	0	1	0
0	0	1	Q ⁿ
1	1	1	N.D.
*	*	0	Q ⁿ

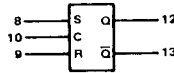
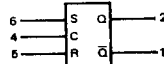
* Either State
N.D. = Not Defined

DC Input Loading Factor: C = 1; S, R = 1.5
DC Output Loading Factor = 25
Power Dissipation = 140 mW typical

CIRCUIT SCHEMATIC



MC1014, MC1214 (continued)



ELECTRICAL CHARACTERISTICS

Test procedures are shown for only one flip-flop. The other flip-flop is tested in the same manner.

Characteristic	Symbol	Pin Under Test	MC1214 Test Limits						Unit	MC1014 Test Limits							
			-55°C		+25°C		+125°C			0°C		+25°C		+75°C		Unit	
			Min	Max	Min	Max	Min	Max		Min	Max	Min	Max	Min	Max		
Power Supply Drain Current	I_E	7	-	-	-	-	-	-	-	-	-	-	-	-	-	-	mAdc
Input Current	I_{in}	4	-	-	-	100	-	-	-	-	-	-	100	-	-	-	μ Adc
		5	-	-	-	150	-	-	-	-	-	-	150	-	-	-	μ Adc
		6	-	-	-	150	-	-	-	-	-	-	150	-	-	-	μ Adc
Input Leakage Current	I_R	Inputs*	-	-	-	0.2	-	1.0	-	-	-	0.2	-	1.0	-	-	μ Adc
Q Logical "1" Output Voltage	V_{OH}^1	2	-0.990	-0.825	-0.850	-0.700	-0.700	-0.530	Vdc	-0.895	-0.740	-0.850	-0.700	-0.775	-0.615	-	Vdc
Q Logical "0" Output Voltage	V_{OL}	2	-1.890	-1.580	-1.800	-1.500	-1.720	-1.380	Vdc	-1.830	-1.525	-1.800	-1.500	-1.760	-1.435	-	Vdc
Q-bar Logical "1" Output Voltage	V_{OH}^1	1	-0.990	-0.825	-0.850	-0.700	-0.700	-0.530	Vdc	-0.895	-0.740	-0.850	-0.700	-0.775	-0.615	-	Vdc
Q-bar Logical "0" Output Voltage	V_{OL}	1	-1.890	-1.580	-1.800	-1.500	-1.720	-1.380	Vdc	-1.830	-1.525	-1.800	-1.500	-1.760	-1.435	-	Vdc
Switching Times (Fan-Out \times 3)																	
Clock Inputs Propagation Delay	t_{4-1}	1	6.0	9.0	6.0	9.0	7.0	10.5	ns	6.0	9.0	6.0	9.0	6.0	9.5	9.5	ns
		1	5.0	8.5	5.0	8.5				5.0	8.5	5.0	8.5				
		2	5.0	8.5	5.0	8.5				5.0	8.5	5.0	8.5				
		2	6.0	9.0	6.0	9.0				6.0	9.0	6.0	9.0				
Rise Time	t_{1-}	1						10.0							7.0	10.0	
		2						10.0									
Fall Time	t_{1-}	1	5.0	8.5			8.0	11.5									
		2	5.0	8.5			8.0	11.5									
Set-Reset Inputs Propagation Delay	t_{6-1}	1	5.0	8.0	5.0	8.0	7.0	10.5	ns	5.0	8.0	5.0	8.0	6.0	9.0	9.0	ns
		1															
		2															
		2															
Rise Time	t_{1-}	1	6.0	9.0	6.0	9.0	8.0	10.0		6.0	9.0	6.0	9.0	7.0	9.5		
		2	6.0	9.0	6.0	9.0	8.0	10.0		6.0	9.0	6.0	9.0	7.0	9.5		
Fall Time	t_{1-}	1	5.0	8.5	5.0	8.5	7.0	11.5		5.0	8.5	5.0	8.5	6.0	10.0		
		2	5.0	8.5	5.0	8.5	7.0	11.5		5.0	8.5	5.0	8.5	6.0	10.0		

* Individually test each input using the pin connections shown.
 $1V_{OH}$ limits apply from no load (0 mA) to full load (-2.5 mA).

APPLICATIONS INFORMATION

The MC1014/MC1214 is a dual R-S flip-flop with a positive clock input for each flip-flop. An extra level of gating is accomplished with only 2.0 ns increase in propagation delay. This device may be used with the MC1015/MC1215 negative-clock R-S flip-flop in a single-phase clocked master-slave type of shift register as shown in Figure 1.

@Test Temperature
 MC1214 { -55°C
 +25°C
 +125°C
 MC1014 { 0°C
 +25°C
 +75°C

TEST VOLTAGE/CURRENT VALUES									
Vdc ± 1.0%									
V _{IL min} to V _{IL max}	V _{IH min} to V _{IH max}	V _{IH max}	V _{EE}	V _{BB}	I _L				
-5.2 to -1.405	-1.165 to -0.825	-	-5.2	-1.270	-2.5				
-5.2 to -1.325	-1.025 to -0.700	-0.700	-5.2	-1.175	-2.5				
-5.2 to -1.205	-0.875 to -0.530	-	-5.2	-1.025	-2.5				
-5.2 to -1.350	-1.070 to -0.740	-	-5.2	-1.210	-2.5				
-5.2 to -1.325	-1.025 to -0.700	-0.700	-5.2	-1.175	-2.5				
-5.2 to -1.280	-0.950 to -0.615	-	-5.2	-1.115	-2.5				

TEST VOLTAGE/CURRENT APPLIED TO PINS LISTED BELOW:									
Characteristic	Symbol	Pin Under Test	V _{IL min} to V _{IL max}	V _{IH min} to V _{IH max}	V _{IH max}	V _{EE}	V _{BB}	I _L	V _{CC} (Gnd)
Power Supply Drain Current	I _E	7	-	4, 10	-	5, 6, 7, 8, 9	-	-	14
Input Current	I _{In}	4, 5, 6	-	-	4, 4.5, 4.6	5, 6, 7, 8, 9, 10	-	-	14
Input Leakage Current	I _R	Inputs*	-	-	-	5, 7, 8, 9, 10	-	-	14
"Q" Logical "1" Output Voltage	V _{OH} [†]	2	-	4.6	-	4.5, 6, 7, 8, 9, 10	-	-	14
"Q" Logical "0" Output Voltage	V _{OL}	2	-	4.5	-	5, 7, 8, 9, 10	5	2	14
"Q" Logical "1" Output Voltage	V _{OH} [†]	1	-	4.5	-	4, 7, 8, 9, 10	6	-	14
"Q" Logical "0" Output Voltage	V _{OL}	1	-	4.6	-	4, 7, 8, 9, 10	6	1	14
Switching Times (Fan-Out = 3) Clock Inputs			Pulse In	V _{IH min} + 1.2 Vdc	Pulse Out	V _{EE} = -4.0 Vdc			(+12V)
Propagation Delay	t ₄₊₁₋ , t ₄₊₁₊ , t ₄₊₂₊	1, 1, 2	4	-	1, 1, 2	5, 6, 7, 8, 9, 10	-	-	14
Rise Time	t ₁₊ , t ₂₊	1, 2	-	-	1, 2	-	-	-	-
Fall Time	t ₁₋ , t ₂₋	1, 2	-	-	1, 2	-	-	-	-
Set-Reset Inputs Propagation Delay	t ₆₊₁₋ , t ₅₊₁₊ , t ₆₊₂₊ , t ₅₊₂₋	1, 1, 2, 2	6, 5, 6, 5	4	-	7, 8, 9, 10	-	-	14
Rise Time	t ₁₊ , t ₂₊	1, 2	6	-	2, 2	-	-	-	-
Fall Time	t ₁₋ , t ₂₋	1, 2	-	-	1, 2	-	-	-	-

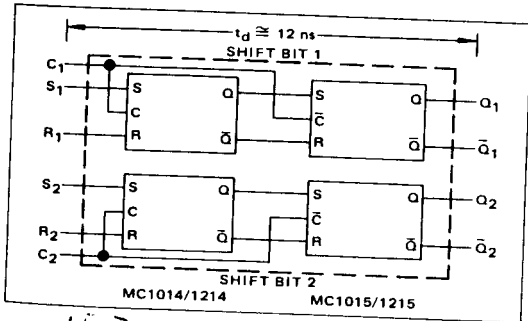
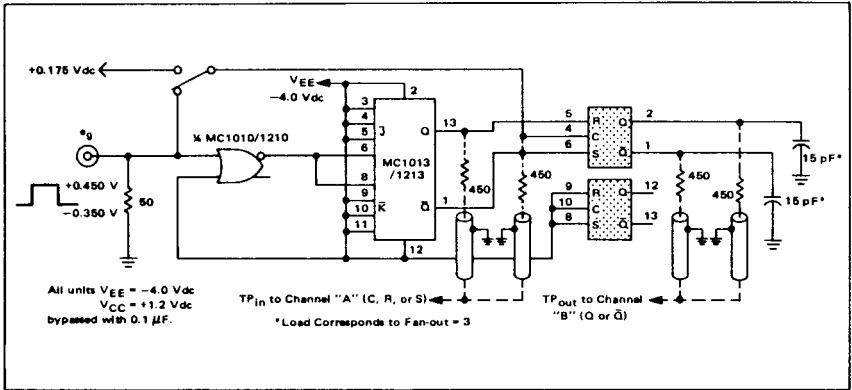


FIGURE 1 - MC1014/MC1214 AND MC1015/MC1215 CONNECTED TO MAKE TWO MASTER-SLAVE SHIFT REGISTER ELEMENTS

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MC1014, MC1214 (continued)

SWITCHING TIME TEST CIRCUIT
 $T_A = 25^\circ\text{C}$



SWITCHING TIME DEFINITIONS AND TIMING DIAGRAM

