3.3V 1K/4K/16K x36 x2 Bidirectional Synchronous FIFO with Bus Matching

Features

- 3.3V high-speed, low-power, bidirectional, First-In First-Out (FIFO) memories w/ bus matching capabilities
- 1K × 36 × 2 (CY7C43644AV)
- 4K × 36 × 2 (CY7C43664AV)
- 16K × 36 × 2 (CY7C43684AV)
- 0.25-micron CMOS for optimum speed/power
- High-speed 133-MHz operation (7.5-ns Read/Write cycle times)
- Low power
  - I_{CC}= 60 mA
  - I_{SB}= 10 mA
- Fully asynchronous and simultaneous Read and Write operation permitted
- Mailbox bypass register for each FIFO
- Parallel and Serial Programmable Almost Full and Almost Empty flags
- Retransmit function
- Standard or FWFT user selectable mode
- Partial Reset
- Big or Little Endian format for word or byte bus sizes
- 128-pin TQFP packaging
- Easily expandable in width and depth

Table 1.

Logic Block Diagram

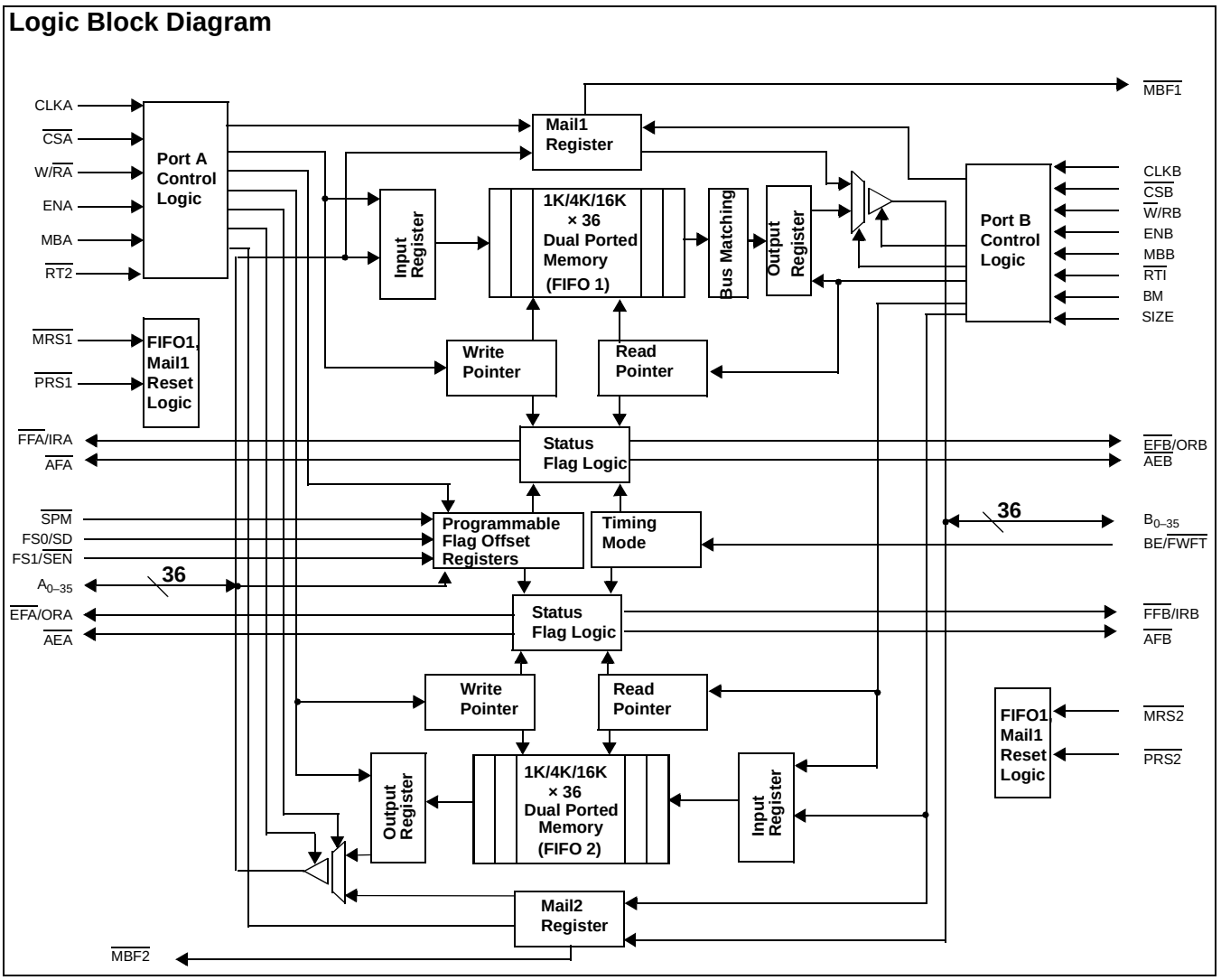
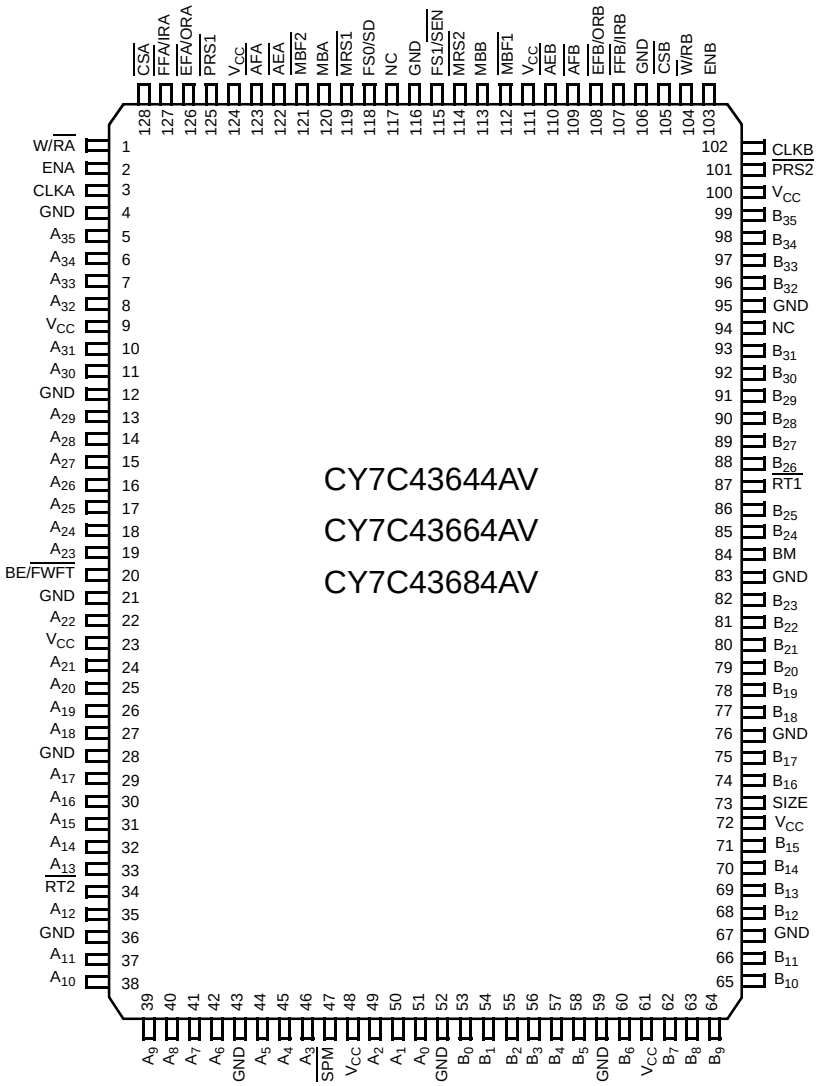


Table 1.

Pin Configuration[1]

TQFP

Top View



Note:

1. Pin-compatible to IDT7236X4 family.

Functional Description

The CY7C436X4AV is a monolithic, high-speed, low-power, CMOS Bidirectional Synchronous FIFO memory which supports clock frequencies up to 133 MHz and has Read access times as fast as 6 ns. Two independent 1K/4K/16K × 36 dual-port SRAM FIFOs on board each chip buffer data in opposite directions. FIFO data on Port B can be input and output in 36-bit, 18-bit, or 9-bit formats with a choice of Big or Little Endian configurations.

The CY7C436X4AV is a synchronous (clocked) FIFO, meaning each port employs a synchronous interface. All data transfers through a port are gated to the LOW-to-HIGH transition of a port clock by enable signals. The clocks for each port are independent of one another and can be asynchronous or coincident. The enables for each port are arranged to provide a simple bidirectional interface between microprocessors and/or buses with synchronous control.

Communication between each port may bypass the FIFOs via two mailbox registers. The mailbox registers' width matches the selected Port B bus width. Each mailbox register has a flag ($\overline{MBF1}$ and $\overline{MBF2}$) to signal when new mail has been stored.

Two kinds of reset are available on the CY7C436X4AV: Master Reset and Partial Reset. Master Reset initializes the Read and Write pointers to the first location of the memory array, configures the FIFO for Big or Little Endian byte arrangement and selects serial flag programming, parallel flag programming, or one of the three possible default flag offset settings, 8, 16, or 64. Each FIFO has its own independent Master Reset pin, $\overline{MRS1}$ and $\overline{MRS2}$.

Partial Reset also sets the Read and Write pointers to the first location of the memory. Unlike Master Reset, any settings existing prior to Partial Reset (i.e., programming method and partial flag default offsets) are retained. Partial Reset is useful since it permits flushing of the FIFO memory without changing any configuration settings. Each FIFO has its own, independent Partial Reset pin, $\overline{PRS1}$ and $\overline{PRS2}$.

The CY7C436X4AV have two modes of operation: In the CY Standard mode, the first word written to an empty FIFO is deposited into the memory array. A Read operation is required to access that word (along with all other words residing in memory). In the First-Word Fall-Through mode (FWFT), the first long-word (36-bit wide) written to an empty FIFO appears automatically on the outputs, no Read operation required (nevertheless, accessing subsequent words does necessitate a formal Read request). The state of the BE/$\overline{FWFT}$ pin during FIFO operation determines the mode in use.

Each FIFO has a combined Empty/Output Ready flag ($\overline{EFA}$/ORA and $\overline{EFB}$/ORB) and a combined Full/Input Ready flag ($\overline{FFA}$/IRA and $\overline{FFB}$/IRB). The $\overline{EF}$ and $\overline{FF}$ functions are selected in the CY Standard mode. $\overline{EF}$ indicates whether the memory is empty and $\overline{FF}$ indicates whether the FIFO memory is full. The IR and OR functions are selected in the First-Word Fall-Through mode. IR indicates whether or not the FIFO has available memory locations. OR shows whether the FIFO has data available for reading or not. It marks the presence of valid data on the outputs.

Each FIFO has a programmable Almost Empty flag ($\overline{AEA}$ and $\overline{AEB}$) and a programmable Almost Full flag ($\overline{AFA}$ and $\overline{AFB}$). $\overline{AEA}$ and $\overline{AEB}$ are asserted when a selected number of words written to FIFO memory achieve a predetermined "almost empty state." $\overline{AFA}$ and $\overline{AFB}$ are asserted when a selected number of words written to the memory achieve a predetermined "almost full state." [2]

IRA, IRB, $\overline{AFA}$, and $\overline{AFB}$ are synchronized to the port clock that writes data into its array. ORA, ORB, $\overline{AEA}$, and $\overline{AEB}$ are synchronized to the port clock that reads data from its array. Programmable offset for $\overline{AEA}$, $\overline{AEB}$, $\overline{AFA}$, and $\overline{AFB}$ are loaded in parallel using Port A or in serial via the SD input. Three default offset settings are also provided. The $\overline{AEA}$ and $\overline{AEB}$ threshold can be set at 8, 16, or 64 locations from the empty boundary and $\overline{AFA}$ and $\overline{AFB}$ threshold can be set at 8, 16, or 64 locations from the full boundary. All these choices are made using the FS0 and FS1 inputs during Master Reset.

Two or more devices may be used in parallel to create wider data paths. A Retransmit feature is available on these devices.

The CY7C436X4AV FIFOs are characterized for operation from 0°C to 70°C commercial, and from –40°C to 85°C industrial. Input ESD protection is greater than 2001V, and latch-up is prevented by the use of guard rings.

Selection Guide

		CY7C43644/64/84AV –7	CY7C43644/64/84AV –10	CY7C43644/64/84AV –15	Unit
Maximum Frequency		133	100	66.7	MHz
Maximum Access Time		6	8	10	ns
Minimum Cycle Time		7.5	10	15	ns
Minimum Data or Enable Set-Up		3	4	5	ns
Minimum Data or Enable Hold		0	0	0	ns
Maximum Flag Delay		6	8	10	ns
Active Power Supply Current (I_{CC1})	Commercial	60	60	60	mA
	Industrial			60	

Note:

2. When FIFO is operated at the almost empty/full boundary, there may be an uncertainty of up to two clock cycles for flag deassertion, but the flag will always be asserted exactly when the FIFO content reaches the programmed value. Use the assertion edge for trigger if flag accuracy is required. Refer to Cypress's application note entitled "Designing with CY7C436xx Synchronous FIFOs" for more details on flag uncertainties.

	CY7C43644AV	CY7C43664AV	CY7C43684AV
Density	1K × 36 × 2	4K × 36 × 2	16K × 36 × 2
Package	128 TQFP	128 TQFP	128 TQFP

Pin Definitions

Signal Name	Description	I/O	Function
$A_{0–35}$	Port A Data	I/O	36-bit bidirectional data port for side A.
$\overline{AEA}$	Port A Almost Empty Flag	O	**Programmable Almost Empty flag synchronized to CLKA**. It is LOW when the number of words in FIFO2 is less than or equal to the value in the Almost Empty A offset register, X2.[2]
$\overline{AEB}$	Port B Almost Empty Flag	O	**Programmable Almost Empty flag synchronized to CLKB**. It is LOW when the number of words in FIFO1 is less than or equal to the value in the Almost Empty B offset register, X1.[2]
$\overline{AFA}$	Port A Almost Full Flag	O	**Programmable Almost Full flag synchronized to CLKA (MHz)**. It is LOW when the number of empty locations in FIFO1 is less than or equal to the value in the Almost Full A offset register, Y1.[2]
$\overline{AFB}$	Port B Almost Full Flag	O	**Programmable Almost Full flag synchronized to CLKB**. It is LOW when the number of empty locations in FIFO2 is less than or equal to the value in the Almost Full B offset register, Y2.[2]
$B_{0–35}$	Port B Data	I/O	36-bit bidirectional data port for side B.
BE/$\overline{FWFT}$	Big Endian/ First-Word Fall-Through Select	I	**This is a dual-purpose pin**. During Master Reset, a HIGH on BE will select Big Endian operation. In this case, depending on the bus size, the most significant byte or word on Port A is transferred to Port B first for A-to-B data flow. For data flowing from port B to Port A, the first word/byte written to Port B will come out as the most significant word/ byte on port A. On the other hand, a LOW on BE will select Little Endian operation. In this case, the least significant byte or word on Port A is transferred to Port B first for A-to-B data flow. Similarly, the first word/byte written into port B will come out as the least significant word/byte on Port A for B-to-A data flow. After Master Reset, this pin selects the timing mode. A HIGH on BE/$\overline{FWFT}$ selects CY Standard mode, a LOW selects First-Word Fall-Through mode. Once the timing mode has been selected, the level on this pin must be static throughout device operation.
BM	Bus Match Select (Port A)	I	**A HIGH on this pin enables either byte or word bus width on Port B**, depending on the state of SIZE. A LOW selects long word operation. BM works with SIZE and BE to select the bus size and endian arrangement for Port B. The level of BM must be static throughout device operation.
CLKA	Port A Clock	I	**CLKA is a continuous clock that synchronizes all data transfers through Port A** and can be asynchronous or coincident to CLKB. $\overline{FFA}$/IRA, $\overline{EFA}$/ORA, $\overline{AFA}$, and $\overline{AEA}$ are all synchronized to the LOW-to-HIGH transition of CLKA.
CLKB	Port B Clock	I	**CLKB is a continuous clock that synchronizes all data transfers through Port B** and can be asynchronous or coincident to CLKA. $\overline{FFB}$/IRB, $\overline{EFB}$/ORB, $\overline{AFB}$, and $\overline{AEB}$ are all synchronized to the LOW-to-HIGH transition of CLKB.
$\overline{CSA}$	Port A Chip Select	I	**CSA must be LOW to enable a LOW-to HIGH transition of CLKA** to Read or Write on Port A. The $A_{0–35}$ are in the high-impedance state when $\overline{CSA}$ is HIGH.
$\overline{CSB}$	Port B Chip Select	I	**CSB must be LOW to enable a LOW-to HIGH transition of CLKB** to Read or Write on Port B. The $B_{0–35}$ are in the high-impedance state when $\overline{CSB}$ is HIGH.
$\overline{EFA}$/ORA	Port A Empty/ Output Ready Flag	O	**This is a dual-function pin**. In the CY Standard mode, the $\overline{EFA}$ function is selected. $\overline{EFA}$ indicates whether or not the FIFO2 memory is empty. In the FWFT mode, the ORA function is selected. ORA indicates the presence of valid data on $A_{0–35}$ outputs available for reading. $\overline{EFA}$/ORA is synchronized to the LOW-to-HIGH transition of CLKA.

Pin Definitions (continued)

Signal Name	Description	I/O	Function
$\overline{EFB}$/ORB	Port B Empty/ Output Ready Flag	O	**This is a dual-function pin**. In the CY Standard mode, the $\overline{EFB}$ function is selected. $\overline{EFB}$ indicates whether or not the FIFO1 memory is empty. In the FWFT mode, the ORB function is selected. ORB indicates the presence of valid data on $B_{0–35}$ outputs available for reading. $\overline{EFB}$/ORB is synchronized to the LOW-to-HIGH transition of CLKB.
ENA	Port A Enable	I	**ENA must be HIGH to enable a LOW-to-HIGH transition of CLKA** to Read or Write data on Port A.
ENB	Port B Enable	I	**ENB must be HIGH to enable a LOW-to-HIGH transition of CLKB** to Read or Write data on Port B.
$\overline{FFA}$/IRA	Port A Full/Input Ready Flag	O	**This is a dual-function pin**. In the CY Standard mode, the $\overline{FFA}$ function is selected. $\overline{FFA}$ indicates whether or not the FIFO1 memory is full. In the FWFT mode, the IRA function is selected. IRA indicates whether or not there is space available for writing to the FIFO1 memory. $\overline{FFA}$/IRA is synchronized to the LOW-to-HIGH transition of CLKA.
$\overline{FFB}$/IRB	Port B Full/Input Ready Flag	O	**This is a dual-function pin**. In the CY Standard mode, the $\overline{FFB}$ function is selected. $\overline{FFB}$ indicates whether or not the FIFO2 memory is full. In the FWFT mode, the IRB function is selected. IRB indicates whether or not there is space available for writing to the FIFO2 memory. $\overline{FFB}$/IRB is synchronized to the LOW-to-HIGH transition of CLKB.
FS1/$\overline{SEN}$	Flag Offset Select 1/Serial Enable	I	**FS1/$\overline{SEN}$ and FS0/SD are dual-purpose inputs used for flag offset register programming**. During Master Reset, FS1/$\overline{SEN}$ and FS0/SD, together with SPM, select the flag offset programming method. Three offset register programming methods are available: automatically load one of three preset values (8, 16, or 64), parallel load from Port A, and serial load. When serial load is selected for flag offset register programming, FS1/$\overline{SEN}$ is used as an enable synchronous to the LOW-to-HIGH transition of CLKA. When FS1/$\overline{SEN}$ is LOW, a rising edge on CLKA loads the bit present on FS0/SD into the X and Y registers. The number of bit Writes required to program the offset registers is 40 for the CY7C43644AV, 48 for the CY7C43664AV, and 56 for the CY7C43684AV. The first bit Write stores the Y-register MSB and the last bit Write stores the X-register LSB.
FS0/SD	Flag Offset Select 0/Serial Data	I	
MBA	Port A Mailbox Select	I	**A HIGH level on MBA chooses a mailbox register for a Port A Read or Write operation**. When a Read operation is performed on Port A, a HIGH level on MBA selects data from the Mail2 register for output and a LOW level selects FIFO2 output register data for output. When a Write operation is performed on port A, a HIGH level on MBA will write the data into Mail1 register, while a LOW level will write the data into FIFO1.
MBB	Port B Mailbox Select	I	**A HIGH level on MBB chooses a mailbox register for a Port B Read or Write operation**. When a Read operation is performed on Port B, a HIGH level on MBB selects data from the Mail1 register for output and a LOW level selects FIFO1 output register data for output. When a Write operation is performed on port B, a HIGH level on MBB will write the data into Mail2 register, while a LOW level will write the data into FIFO2.
$\overline{MBF1}$	Mail1 Register Flag	O	**$\overline{MBF1}$ is set LOW by a LOW-to-HIGH transition of CLKA that writes data to the Mail1 register**. Writes to the Mail1 register are inhibited while $\overline{MBF1}$ is LOW. $\overline{MBF1}$ is set HIGH by a LOW-to-HIGH transition of CLKB when a Port B Read is selected and MBB is HIGH. $\overline{MBF1}$ is set HIGH following either a Master or Partial Reset of FIFO1.
$\overline{MBF2}$	Mail2 Register Flag	O	**$\overline{MBF2}$ is set LOW by a LOW-to-HIGH transition of CLKB** that writes data to the Mail2 register. Writes to the Mail2 register are inhibited while $\overline{MBF2}$ is LOW. $\overline{MBF2}$ is set HIGH by a LOW-to-HIGH transition of CLKA when a Port A Read is selected and MBA is HIGH. $\overline{MBF2}$ is set HIGH following either a Master or Partial Reset of FIFO2.
$\overline{MRS1}$	FIFO1 Master Reset	I	**A LOW on this pin initializes the FIFO1 Read and Write pointers** to the first location of memory and sets the Port B output register to all zeroes. A LOW pulse on $\overline{MRS1}$ selects the programming method (serial or parallel) and one of three programmable flag default offsets for FIFO1. It also configures Port B for bus size and endian arrangement. Four LOW-to-HIGH transitions of CLKA and four LOW-to-HIGH transitions of CLKB must occur while $\overline{MRS1}$ is LOW.

Pin Definitions (continued)

Signal Name	Description	I/O	Function
$\overline{MRS2}$	FIFO2 Master Reset	I	**A LOW on this pin initializes the FIFO2 Read and Write pointers** to the first location of memory and sets the Port A output register to all zeroes. A LOW pulse on $\overline{MRS2}$ selects one of three programmable flag default offsets for FIFO2. Four LOW-to-HIGH transitions of CLKA and four LOW-to-HIGH transitions of CLKB must occur while $\overline{MRS2}$ is LOW.
$\overline{PRS1}$	FIFO1 Partial Reset	I	**A LOW on this pin initializes the FIFO1 Read and Write pointers** to the first location of memory and sets the Port B output register to all zeroes. During Partial Reset, the currently selected bus size, endian arrangement, programming method (serial or parallel), and programmable flag settings are all retained.
$\overline{PRS2}$	FIFO2 Partial Reset	I	**A LOW on this pin initializes the FIFO2 Read and Write pointers** to the first location of memory and sets the Port A output register to all zeroes. During Partial Reset, the currently selected bus size, endian arrangement, programming method (serial or parallel), and programmable flag settings are all retained.
$\overline{RT1}$	Retransmit FIFO1	I	**A LOW strobe on this pin will retransmit the data on FIFO1**. This is achieved by bringing the Read pointer back to location zero. The user will still need to perform Read operations to retransmit the data. Retransmit function applies to CY standard mode only.
$\overline{RT2}$	Retransmit FIFO2	I	**A LOW strobe on this pin will retransmit the data on FIFO2**. This is achieved by bringing the Read pointer back to location zero. The user will still need to perform Read operations to retransmit the data. Retransmit function applies to CY standard mode only.
SIZE	Bus Size Select	I	**A HIGH on this pin when BM is HIGH selects byte bus (9-bit) size on Port B**. A LOW on this pin when BM is HIGH selects word (18-bit) bus size. SIZE works with BM and BE to select the bus size and endian arrangement for Port B. The level of SIZE must be static throughout device operation.
$\overline{SPM}$	Serial Programming	I	**A LOW on this pin selects serial programming of partial flag offsets**. A HIGH on this pin selects parallel programming or default offsets (8, 16, or 64).
W/$\overline{RA}$	Port A Write/ Read Select	I	**A HIGH selects a Write operation and a LOW selects a Read operation on Port A** for a LOW-to-HIGH transition of CLKA. The $A_{0–35}$ outputs are in the high-impedance state when W/$\overline{RA}$ is HIGH.
$\overline{W}$/RB	Port B Write/ Read Select	I	**A LOW selects a Write operation and a HIGH selects a Read operation on Port B** for a LOW-to-HIGH transition of CLKB. The $B_{0–35}$ outputs are in the high-impedance state when $\overline{W}$/RB is LOW.

Signal Description

Master Reset ($\overline{MRS1}$, $\overline{MRS2}$)

Each of the two FIFO memories of the CY7C436X4AV undergoes a complete reset by taking its associated Master Reset ($\overline{MRS1}$, $\overline{MRS2}$) input LOW for at least four Port A clock (CLKA) and four Port B clock (CLKB) LOW-to-HIGH transitions. The Master Reset inputs can switch asynchronously to the clocks. A Master Reset initializes the internal Read and Write pointers and forces the Full/Input Ready flag ($\overline{FFA}$/IRA, $\overline{FFB}$/IRB) LOW, the Empty/Output Ready flag ($\overline{EFA}$/ORA, $\overline{EFB}$/ORB) LOW, the Almost Empty flag ($\overline{AEA}$, $\overline{AEB}$) LOW, and the Almost Full flag ($\overline{AFA}$, $\overline{AFB}$) HIGH. A Master Reset also forces the Mailbox flag ($\overline{MBF1}$, $\overline{MBF2}$) of the parallel mailbox register HIGH. After a Master Reset, the FIFO's Full/Input Ready flag is set HIGH after two clock cycles to begin normal operation. A Master Reset must be performed on the FIFO after power up, before data is written to its memory.

A LOW-to-HIGH transition on a FIFO Master Reset ($\overline{MRS1}$, $\overline{MRS2}$) input latches the value of the Big Endian (BE) input or determining the order by which bytes are transferred through Port B.

A LOW-to-HIGH transition on a FIFO reset ($\overline{MRS1}$, $\overline{MRS2}$) input latches the values of the Flag select (FS0, FS1) and Serial Programming Mode ($\overline{SPM}$) inputs for choosing the Almost Full and Almost Empty offset programming method (see Almost Empty and Almost Full flag offset programming below).

Partial Reset ($\overline{PRS1}$, $\overline{PRS2}$)

Each of the two FIFO memories of the CY7C436X4AV undergoes a limited reset by taking its associated Partial Reset ($\overline{PRS1}$, $\overline{PRS2}$) input LOW for at least four Port A clock (CLKA) and four Port B clock (CLKB) LOW-to-HIGH transitions. The Partial Reset inputs can switch asynchronously to the clocks. A Partial Reset initializes the internal Read and Write pointers and forces the Full/Input Ready flag ($\overline{FFA}$/IRA, $\overline{FFB}$/IRB) LOW, the Empty/Output Ready flag ($\overline{EFA}$/ORA, $\overline{EFB}$/ORB) LOW, the Almost Empty flag ($\overline{AEA}$, $\overline{AEB}$) LOW, and the Almost Full flag ($\overline{AFA}$, $\overline{AFB}$) HIGH. A Partial Reset also forces the Mailbox flag ($\overline{MBF1}$, $\overline{MBF2}$) of the parallel mailbox register HIGH. After a Partial Reset, the FIFO's Full/Input Ready flag is set HIGH after two clock cycles to begin normal operation.

Whatever flag offsets, programming method (parallel or serial), and timing mode (FWFT or CY Standard mode) are currently selected at the time a Partial Reset is initiated, those settings will remain unchanged upon completion of the reset operation. A Partial Reset may be useful in the case where reprogramming a FIFO following a Master Reset would be inconvenient.

Big Endian/First Word Fall Through (BE/$\overline{FWFT}$)

This is a dual-purpose pin. At the time of Master Reset, the BE select function is active, permitting a choice of Big or Little Endian byte arrangement for data written to or read from Port B. This selection determines the order by which bytes (or words) of data are transferred through this port. For the following illustrations, assume that a byte (or word) bus size has been selected for Port B. (Note that when Port B is configured for a long word size, the Big Endian function has no application and the BE input is a "Don't Care.")

A HIGH on the BE/$\overline{FWFT}$ input when the Master Reset ($\overline{MRS1}$ and $\overline{MRS2}$) inputs go from LOW to HIGH will select a Big Endian arrangement. When data is moving in the direction from Port A to Port B, the most significant byte (word) of the long-word written to Port A will be transferred to Port B first; the least significant byte (word) of the long word written to Port A will be transferred to Port B last. When data is moving in the direction from Port B to Port A, the byte (word) written to Port B first will be transferred to Port A as the most significant byte (word) of the long-word; the byte (word) written to Port B last will be transferred to Port A as the least significant byte (word) of the long-word.

A LOW on the BE/$\overline{FWFT}$ input when the Master Reset ($\overline{MRS1}$ and $\overline{MRS2}$) inputs go from LOW to HIGH will select a Little Endian arrangement. When data is moving in the direction from Port A to Port B, the least significant byte (word) of the long word written to Port A will be transferred to Port B first; the most significant byte (word) of the long-word written to Port A will be transferred to Port B last. When data is moving in the direction from Port B to Port A, the byte (word) written to Port B first will be transferred to port A as the least significant byte (word) of the long-word; the byte (word) written to Port B last will be transferred to Port A as the most significant byte (word) of the long-word.

After Master Reset, the FWFT select function is active, permitting a choice between two possible timing modes: CY Standard mode or First-Word Fall-Through (FWFT) mode. Once the Master Reset ($\overline{MRS1}$, $\overline{MRS2}$) input is HIGH, a HIGH on the BE/$\overline{FWFT}$ input at the second LOW-to-HIGH transition of CLKA (for FIFO1) and CLKB (for FIFO2) will select CY Standard mode. This mode uses the Empty Flag function ($\overline{EFA}$, $\overline{EFB}$) to indicate whether or not there are any words present in the FIFO memory. It uses the Full Flag function ($\overline{FFA}$, $\overline{FFB}$) to indicate whether or not the FIFO memory has any free space for writing. In CY Standard mode, every word read from the FIFO, including the first, must be requested using a formal Read operation.

Once the Master Reset ($\overline{MRS1}$, $\overline{MRS2}$) input is HIGH, a LOW on the BE/$\overline{FWFT}$ input at the second LOW-to-HIGH transition of CLKA (for FIFO1) and CLKB (for FIFO2) will select FWFT mode. This mode uses the Output Ready function (ORA, ORB) to indicate whether or not there is valid data at the data outputs ($A_{0–35}$ or $B_{0–35}$). It also uses the Input Ready function (IRA, IRB) to indicate whether or not the FIFO memory has any free space for writing. In the FWFT mode, the first word written to an empty FIFO goes directly to data outputs, no Read request necessary. Subsequent words must be accessed by performing a formal Read operation.

Following Master Reset, the level applied to the BE/$\overline{FWFT}$ input to choose the desired timing mode must remain static throughout the FIFO operation.

Programming the Almost Empty and Almost Full Flags

Four registers in the CY7C436X4AV are used to hold the offset values for the Almost Empty and Almost Full flags. The Port B Almost Empty flag ($\overline{AEB}$) offset register is labeled X1 and the Port A Almost Empty flag ($\overline{AEA}$) offset register is labeled X2. The Port A Almost Full flag ($\overline{AFA}$) offset register is labeled Y1 and the Port B Almost Full flag ($\overline{AFB}$) offset register is labeled Y2. The index of each register name corresponds with preset values during the reset of a FIFO, programmed in parallel using the FIFO's Port A data inputs, or programmed in serial using the Serial Data (SD) input (see *Table 3*). To load a FIFO's

Almost Empty flag and Almost Full flag offset registers with one of the three preset values listed in *Table 3*, the Serial Program Mode (SPM) and at least one of the flag-select inputs must be HIGH during the LOW-to-HIGH transition of its Master Reset input (MRS1 and MRS2). For example, to load the preset value of 64 into X1 and Y1, SPM, FS0, and FS1 must be HIGH when FIFO1 reset (MRS1) returns HIGH. Flag-offset registers associated with FIFO2 are loaded with one of the preset values in the same way with Master Reset (MRS2). When using one of the preset values for the flag offsets, the FIFOs can be reset simultaneously or at different times.

To program the X1, X2, Y1, and Y2 registers in parallel from Port A, perform a Master Reset on both FIFOs simultaneously with SPM HIGH and FS0 and FS1 LOW during the LOW-to-HIGH transition of MRS1 and MRS2. After this reset is complete, the first four Writes to FIFO1 do not store data in RAM but load the offset registers in the order Y1, X1, Y2, X2. The Port A data inputs used by the offset registers are ($A_{0–9}$), ($A_{0–11}$), or ($A_{0–13}$), for the CY7C436X4AV, respectively. The highest numbered input is used as the most significant bit of the binary number in each case. Valid programming values for the registers range from 0 to 1023 for the CY7C43644AV; 0 to 4095 for the CY7C43664AV; 0 to 16383 for the CY7C43684AV.[2] After all the offset registers are programmed from Port A, the Port B Full/Input Ready ($\overline{FFB}$/IRB) is set HIGH and both FIFOs begin normal operation.

To program the X1, X2, Y1, and Y2 registers serially, initiate a Master Reset with SPM LOW, FS0/SD LOW, and FS1/$\overline{SEN}$ HIGH during the LOW-to-HIGH transition of MRS1 and MRS2. After this reset is complete, the X and Y register values are loaded bit-wise through the FS0/SD input on each LOW-to-HIGH transition of CLKA that the FS1/$\overline{SEN}$ input is LOW. Forty, forty-eight, or fifty-six bit Writes are needed to complete the programming for the CY7C436X4AV, respectively. The four registers are written in the order Y1, X1, Y2, and, finally, X2. The first-bit Write stores the most significant bit of the Y1 register and the last-bit Write stores the least significant bit of the X2 register.

When the option to program the offset registers serially is chosen, the Port A Full/Input Ready ($\overline{FFA}$/IRA) flag remains LOW until all register bits are written. $\overline{FFA}$/IRA is set HIGH by the LOW-to-HIGH transition of CLKA after the last bit is loaded to allow normal FIFO1 operation. The Port B Full/Input ready ($\overline{FFB}$/IRB) flag also remains LOW throughout the serial programming process, until all register bits are written. $\overline{FFB}$/IRB is set HIGH by the LOW-to-HIGH transition of CLKB after the last bit is loaded to allow normal FIFO2 operation.

$\overline{SPM}$, FS0/SD, and FS1/$\overline{SEN}$ function the same way in both CY Standard and FWFT modes.

FIFO Write/Read Operation

The state of the Port A data ($A_{0–35}$) lines is controlled by Port A Chip Select ($\overline{CSA}$) and Port A Write/Read Select (W/$\overline{RA}$). The $A_{0–35}$ lines are in the high-impedance state when either $\overline{CSA}$ or W/$\overline{RA}$ is HIGH. The $A_{0–35}$ lines are active outputs when both $\overline{CSA}$ and W/$\overline{RA}$ are LOW.

Data is loaded into FIFO1 from the $A_{0–35}$ inputs on a LOW-to-HIGH transition of CLKA when $\overline{CSA}$ is LOW, W/$\overline{RA}$ is HIGH, ENA is HIGH, MBA is LOW, and $\overline{FFA}$/IRA is HIGH. Data is read from FIFO2 to the $A_{0–35}$ outputs by a LOW-to-HIGH transition of CLKA when $\overline{CSA}$ is LOW, W/$\overline{RA}$ is LOW, ENA is HIGH, MBA is LOW, and $\overline{EFA}$/ORA is HIGH (see *Table 4*). FIFO Reads and Writes on Port A are independent of any concurrent Port B operation.

The Port B control signals are identical to those of Port A with the exception that the Port B Write/Read select (W/$\overline{RB}$) is the inverse of the Port A Write/Read select (W/$\overline{RA}$). The state of the Port B data ($B_{0–35}$) lines is controlled by the Port B Chip Select ($\overline{CSB}$) and Port B Write/Read select (W/$\overline{RB}$). The $B_{0–35}$ lines are in the high-impedance state when either $\overline{CSB}$ is HIGH or W/$\overline{RB}$ is LOW. The $B_{0–35}$ lines are active outputs when $\overline{CSB}$ is LOW and W/$\overline{RB}$ is HIGH.

Data is loaded into FIFO2 from the $B_{0–35}$ inputs on a LOW-to-HIGH transition of CLKB when $\overline{CSB}$ is LOW, W/$\overline{RB}$ is LOW, ENB is HIGH, MBB is LOW, and $\overline{FFB}$/IRB is HIGH. Data is read from FIFO1 to the $B_{0–35}$ outputs by a LOW-to-HIGH transition of CLKB when $\overline{CSB}$ is LOW, W/$\overline{RB}$ is HIGH, ENB is HIGH, MBB is LOW, and $\overline{EFB}$/ORB is HIGH (see *Table 5*). FIFO Reads and Writes on Port B are independent of any concurrent Port A operation.

The set-up and hold time constraints to the port clocks for the port Chip Selects and Write/Read selects are only for enabling Write and Read operations and are not related to high-impedance control of the data outputs. If a port enable is LOW during a clock cycle, the port's Chip Select and Write/Read select may change states during the set-up and hold time window of the cycle.

When operating the FIFO in FWFT mode and the Output Ready flag is LOW, the next word written is automatically sent to the FIFO's output register by the LOW-to-HIGH transition of the port clock that sets the Output Ready flag HIGH, data residing in the FIFO's memory array is clocked to the output register only when a Read is selected using the port's Chip Select, Write/Read select, Enable, and Mailbox select.

When operating the FIFO in CY Standard mode, data residing in the FIFO's memory array is clocked to the output register only when a Read is selected using the port's Chip Select, Write/Read select, Enable, and Mailbox select.

Synchronized FIFO Flags

Each FIFO is synchronized to its port clock through at least two flip-flop stages. This is done to improve flag-signal reliability by reducing the probability of the metastable events when CLKA and CLKB operate asynchronously to one another. $\overline{EFA}$/$\overline{ORA}$, $\overline{AEA}$, $\overline{FFA}$/IRA, and $\overline{AFA}$ are synchronized to CLKA. $\overline{EFB}$/ORB, $\overline{AEB}$, $\overline{FFB}$/IRB, and $\overline{AFB}$ are synchronized to CLKB. *Table 6* and *Table 7* show the relationship of each port flag to FIFO1 and FIFO2.

Empty/Output Ready Flags ($\overline{EFA}$/ORA, $\overline{EFB}$/ORB)

These are dual-purpose flags. In the FWFT mode, the Output Ready (ORA, ORB) function is selected. When the Output Ready flag is HIGH, new data is present in the FIFO output register. When the Output Ready flag is LOW, the previous data word remains in the FIFO output register and any FIFO reads are ignored.

In the CY Standard mode, the Empty Flag ($\overline{EFA}$, $\overline{EFB}$) function is selected. When the Empty Flag is HIGH, data is available in the FIFO's RAM memory for reading to the output register. When Empty Flag is LOW, the previous data word remains in the FIFO output register and any FIFO reads are ignored.

The Empty/Output Ready flag of a FIFO is synchronized to the port clock that reads data from its array. For both the FWFT

and CY Standard modes, the FIFO Read pointer is incremented each time a new word is clocked to its output register. The state machine that controls an Output Ready flag monitors a Write pointer and Read pointer comparator that indicates when the FIFO SRAM status is empty, empty + 1, or empty + 2.

In FWFT Mode, from the time a word is written to a FIFO, it can be shifted to the FIFO output register in a minimum of three cycles of the Output Ready flag synchronizing clock. Therefore, an Output Ready flag is LOW if a word in memory is the next data to be sent to the FIFO output register and three cycles have not elapsed since the time the word was written. The Output Ready flag of the FIFO remains LOW until the third LOW-to-HIGH transition of the synchronizing clock occurs, simultaneously forcing the Output Ready flag HIGH and shifting the word to the FIFO output register.

In the CY Standard mode, from the time a word is written to a FIFO, the Empty Flag will indicate the presence of data available for reading in a minimum of two cycles of the Empty Flag synchronizing clock. Therefore, an Empty Flag is LOW if a word in memory is the next data to be sent to the FIFO output register and two cycles have not elapsed since the time the word was written. The Empty Flag of the FIFO remains LOW until the second LOW-to-HIGH transition of the synchronizing clock occurs, forcing the Empty Flag HIGH; only then will data be read.

A LOW-to-HIGH transition on an Empty/Output Ready flag synchronizing clock begins the first synchronization cycle of a Write if the clock transition occurs at time t_{SKEW1} or greater after the Write. Otherwise, the subsequent clock cycle can be the first synchronization cycle.

Full/Input Ready Flags ($\overline{FFA}$/IRA, $\overline{FFB}$/IRB)

This is a dual-purpose flag. In FWFT mode, the Input Ready (IRA and IRB) function is selected. In CY Standard mode, the Full Flag ($\overline{FFA}$ and $\overline{FFB}$) function is selected. For both timing modes, when the Full/Input Ready flag is HIGH, a memory location is free in the SRAM to receive new data. No memory locations are free when the Full/Input Ready flag is LOW and any Writes to the FIFO are ignored.

The Full/Input Ready flag of a FIFO is synchronized to the port clock that writes data to its array. For both FWFT and CY Standard modes, each time a word is written to a FIFO, its Write pointer is incremented. The state machine that controls a Full/Input Ready flag monitors a Write pointer and read pointer comparator that indicates when the FIFO SRAM status is full, full – 1, or full – 2. From the time a word is read from a FIFO, its previous memory location is ready to be written to in a minimum of two cycles of the Full/Input Ready flag synchronizing clock. Therefore, a Full/Input Ready flag is LOW if less than two cycles of the Full/Input Ready flag synchronizing clock have elapsed since the next memory Write location has been read. The second LOW-to-HIGH transition on the Full/Input Ready flag synchronizing clock after the Read sets the Full/Input Ready flag HIGH.

A LOW-to-HIGH transition on a Full/Input Ready flag synchronizing clock begins the first synchronization cycle of a Read if the clock transition occurs at time t_{SKEW1} or greater after the Read. Otherwise, the subsequent clock cycle will be the first synchronization cycle.

Almost Empty Flags ($\overline{AEA}$, $\overline{AEB}$)

The Almost Empty flag of a FIFO is synchronized to the port clock that reads data from its array. The state machine that controls an Almost Empty flag monitors a Write pointer and Read pointer comparator that indicates when the FIFO SRAM status is almost empty, almost empty + 1, or almost empty + 2. The Almost Empty state is defined by the contents of register X1 for $\overline{AEB}$ and register X2 for $\overline{AEA}$. These registers are loaded with preset values during a FIFO reset, programmed from Port A, or programmed serially (see Almost Empty flag and Almost Full flag offset programming above). An Almost Empty flag is LOW when its FIFO contains X or less words and is HIGH when its FIFO contains (X + 2) or more words.[2]

The Almost Empty flag is set HIGH by the first LOW-to-HIGH transition of its synchronizing clock after two FIFO Writes that fills memory to the (X + 2) level. A LOW-to-HIGH transition of an Almost Empty flag synchronizing clock begins the first synchronization cycle if it occurs at time t_{SKEW2} or greater after the Write that fills the FIFO to (X + 2) words. Otherwise, the subsequent synchronizing clock cycle will be the first synchronization cycle.

Almost Full Flags ($\overline{AFA}$, $\overline{AFB}$)

The Almost Full flag of a FIFO is synchronized to the port clock that writes data to its array. The state machine that controls an Almost Full flag monitors a Write pointer and Read pointer comparator that indicates when the FIFO SRAM status is almost full, almost full – 1, or almost full – 2. The Almost Full state is defined by the contents of register Y1 for AFA and register Y2 for AFB. These registers are loaded with preset values during a FIFO reset, programmed from Port A, or programmed serially (see Almost Empty flag and Almost Full flag offset programming above). An Almost Full flag is LOW when the number of words in its FIFO is greater than or equal to (1024 – Y), (4096 – Y), or (16384 – Y) for the CY7C436X4AV respectively. An Almost Full flag is HIGH when the number of words in its FIFO is less than or equal to [1024 – (Y + 2)], [4096 – (Y + 2)], or [16384 – (Y + 2)], for the CY7C436X4AV respectively.[2]

The Almost Full flag is set HIGH by the first LOW-to-HIGH transition of its synchronizing clock after two FIFO reads that reduces the number of words in memory to [1024/4096/16384 – (Y + 2)]. A LOW-to-HIGH transition of an Almost Full flag synchronizing clock begins the first synchronization cycle if it occurs at time t_{SKEW2} or greater after the Read that reduces the number of words in memory to [1024/4096/16384 – (Y + 2)]. Otherwise, the subsequent synchronizing clock cycle will be the first synchronization cycle.

Mailbox Registers

Each FIFO has a 36-bit bypass register to pass command and control information between Port A and Port B without putting it in queue. The Mailbox Select (MBA, MBB) inputs choose between a mail register and a FIFO for a port data transfer operation. The usable width of both the Mail1 and Mail2 registers matches the selected bus size for Port B.

A LOW-to-HIGH transition on CLKA writes $A_{0<35}$ data to the Mail1 Register when a Port A Write is selected by $\overline{CSA}$ LOW, W/$\overline{RA}$ HIGH, ENA HIGH, and MBA HIGH. If the selected Port A bus size is also 36 bits, then the usable width of the Mail1 Register employs data lines $A_{0<35}$. If the selected Port A bus size is 18 bits, then the usable width of the Mail1 Register

employs data lines $A_{0<17}$. (In this case, $A_{18<35}$ are "Don't Care" inputs.) If the selected Port A bus size is 9 bits, then the usable width of the Mail1 Register employs data lines $A_{0<8}$. (In this case, $A_{9<35}$ are "Don't Care" inputs.)

A LOW-to-HIGH transition on CLKB writes $B_{0<35}$ data to the Mail2 Register when a Port B Write is selected by CSB LOW, W/RB LOW, ENB HIGH and MBB HIGH. If the selected Port B bus size is also 36 bits, then the usable width of the Mail2 Register employs data lines $B_{0–35}$. If the selected Port B bus size is 18 bits, then the usable width of the Mail2 Register employs data lines $B_{0–17}$. (In this case, $B_{18–35}$ are "Don't Care" inputs.) If the selected Port B bus size is 9 bits, then the usable width of the Mail2 Register employs data lines $B_{0<8}$. (In this case, $B_{9<35}$ are "Don't Care" inputs.)

Writing data to a mail register sets its corresponding flag ($\overline{MBF1}$ or $\overline{MBF2}$) LOW. Any Attempt to write to a mail register are ignored while the mail flag is LOW.

When data outputs of a port are active, the data on the bus comes from the FIFO output register when the port Mailbox Select input is LOW and from the mail register when the port Mailbox Select input is HIGH.

The Mail1 Register Flag ($\overline{MBF1}$) is set HIGH by a LOW-to-HIGH transition on CLKB when a Port B Read is selected by CSB LOW, W/RB HIGH, ENB HIGH AND MBB HIGH. For a 36-bit bus size, 36 bits of mailbox data are placed on $B_{0–35}$. For an 18-bit bus size, 18 bits of mailbox data are placed on $B_{0–17}$. (In this case, $B_{18–35}$ are indeterminate.) For a 9-bit bus size, 9 bits of mailbox data are placed on $B_{0–8}$. (In this case, $B_{9–35}$ are indeterminate.)

The Mail2 register Flag ($\overline{MBF2}$) is set HIGH by a LOW-to-HIGH transition on CLKA when a Port A Read is selected by CSA LOW, W/RA LOW, ENA HIGH, MBA HIGH.

For a 36-bit bus size, 36 bits of mailbox data are placed on $A_{0–35}$. For an 18-bit bus size, 18 bits of mailbox data are placed on $A_{0–17}$. (In this case, $A_{18–35}$ are indeterminate.) For a 9-bit bus size, 9 bits of mailbox data are placed on $A_{0–8}$. (In this case, $A_{9–35}$ are indeterminate.)

The data in a mail register remains intact after it is read and changes only when new data is written to the register. The Endian Select feature has no effect on the mailbox data.

Bus Sizing

The Port B bus can be configured in a 36-bit long-word, 18-bit word, or 9-bit byte format for data read from FIFO1 or written to FIFO2. The levels applied to the Port B Bus Size Select (SIZE) and the Bus Match Select (BM) determine the Port B bus size. These levels should be static throughout FIFO operation. Both bus size selections are implemented at the completion of Master Reset, by the time the Full/Input Ready flag is set HIGH.

Two different methods for sequencing data transfer are available for Port B when the bus size selection is either byte- or word-size. They are referred to as Big Endian (most significant byte first) and Little Endian (least significant byte first). The level applied to the Big Endian Select (BE) input during the LOW-to-HIGH transition of $\overline{MRS1}$ and $\overline{MRS2}$ selects the endian method that will be active during FIFO operation. BE is a "Don't Care" input when the bus size selected for Port B is long word. The endian method is implemented at the completion of Master Reset, by the time the Full/Input Ready flag is set HIGH.

Bus-Matching operations are not available when transferring data via mailbox registers. Furthermore, both the word- and byte-size bus selections limit the width of the data bus that can be used for mail register operations. In this case, only those byte lanes belonging to the selected word- or byte-size bus can carry mailbox data. The remaining data outputs will be indeterminate. The remaining data inputs will be don't care inputs. For example, when a word-size bus is selected, then mailbox data can be transmitted only between $A_{0–17}$ and $B_{0–17}$. When a byte-size bus is selected, then mailbox data can be transmitted only between $A_{0–8}$ and $B_{0–8}$.

Bus-Matching FIFO1 Reads

Data is read from the FIFO1 RAM in 36-bit long-word increments. If a long-word bus size is implemented, the entire long-word immediately shifts to the FIFO1 output register. If byte or word size is implemented on Port B, only the first one or two bytes appear on the selected portion of the FIFO1 output register, with the rest of the long-word stored in auxiliary registers. In this case, subsequent FIFO1 reads output the rest of the long word to the FIFO1 output register.

When reading data from FIFO1 in the byte or word format, the unused $B_{0–35}$ outputs are indeterminate.

Bus-Matching FIFO2 Writes

Data is written to the FIFO2 RAM in 36-bit long-word increments. Data written to FIFO2 with a byte or word bus size stores the initial bytes or words in auxiliary registers. The CLKB rising edge that writes the fourth byte or the second word of long-word to FIFO2 also stores the entire long word in FIFO2 RAM.

Reading from FIFO2 on Port A can only be in 36-bit format

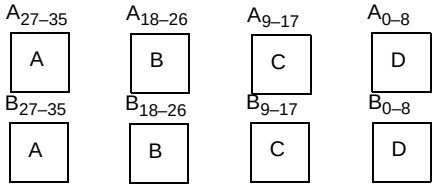
Retransmit ($\overline{RT1}$, $\overline{RT2}$)

The retransmit feature is beneficial when transferring packets of data. It enables the receipt of data to be acknowledged by the receiver and retransmitted if necessary. The retransmit function applies to CY Standard mode only.

The number of 36-/18-/9-bit words written into the FIFO should be less than full depth minus 2/4/8 words between the reset of the FIFO (master or partial) and Retransmit setup. A LOW pulse on $\overline{RT1}$, ($\overline{RT2}$) resets the internal Read pointer to the first physical location of the FIFO. CLKA and CLKB may be free running but ENB (ENA) must be disabled during and t_{RTR} after the retransmit pulse. With every valid Read cycle after retransmit, previously accessed data is read and the Read pointer is incremented until it is equal to the Write pointer. Flags are governed by the relative locations of the Read and Write pointers and are updated during a retransmit cycle. Data written to the FIFO after activation of $\overline{RT1}$, ($\overline{RT2}$) are transmitted also. The full depth of the FIFO can be repeatedly retransmitted.

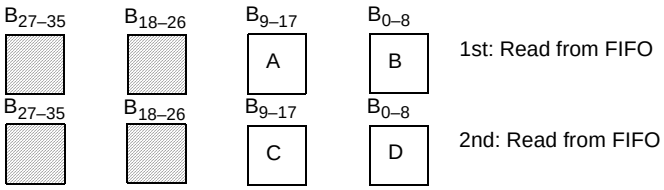
Table 2.

BYTE ORDER ON PORT A:



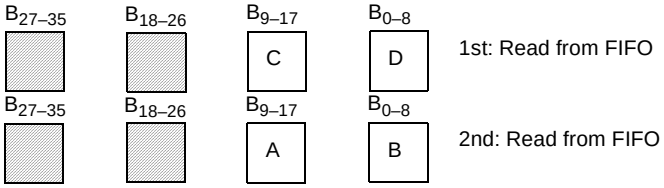
BE	BM	SIZE
X	L	X

(a) LONG-WORD SIZE



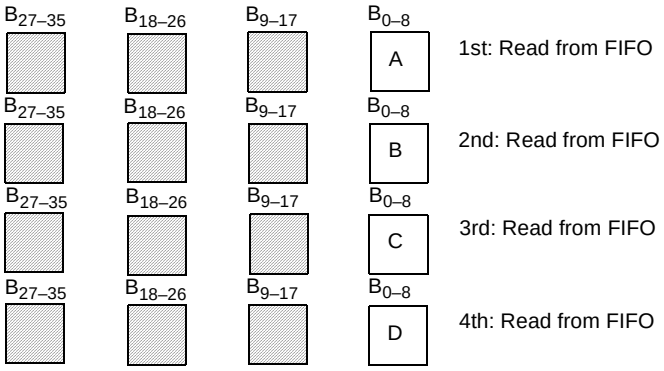
BE	BM	SIZE
H	H	L

(b) WORD SIZE – BIG ENDIAN



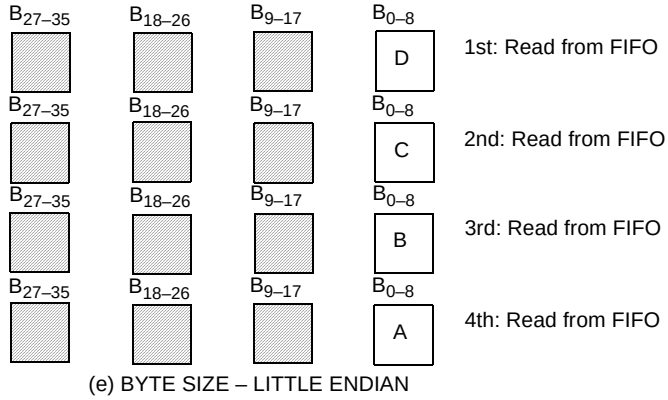
BE	BM	SIZE
L	H	L

(c) WORD SIZE – LITTLE ENDIAN



BE	BM	SIZE
H	H	H

(d) BYTE SIZE – BIG ENDIAN



BE	BM	SIZE
L	H	H

(e) BYTE SIZE – LITTLE ENDIAN

Table 3. Flag Programming

$\overline{SPM}$	FS1/ SEN	FS0/ SD	MRS1	MRS2	X1 and Y1 Registers[3]	X2 andY2 Registers[4]
H	H	H	↑	X	64	X
H	H	H	X	↑	X	64
H	H	L	↑	X	16	X
H	H	L	X	↑	X	16
H	L	H	↑	X	8	X
H	L	H	X	↑	X	8
H	L	L	↑	↑	Parallel programming via Port A	Parallel programming via Port A
L	H	L	↑	↑	Serial programming via SD	Serial programming via SD
L	H	H	↑	↑	Reserved	Reserved
L	L	H	↑	↑	Reserved	Reserved
L	L	L	↑	↑	Reserved	Reserved

Table 4. Port A Enable Function

$\overline{CSA}$	W/$\overline{RA}$	ENA	MBA	CLKA	$A_{0–35}$	Port Function
H	X	X	X	X	In high-impedance state	None
L	H	L	X	X	In high-impedance state	None
L	H	H	L	↑	In high-impedance state	FIFO1 Write
L	H	H	H	↑	In high-impedance state	Mail1 Write
L	L	L	L	X	Active, FIFO2 output register	None
L	L	H	L	↑	Active, FIFO2 output register	FIFO2 Read
L	L	L	H	X	Active, Mail2 register	None
L	L	H	H	↑	Active, Mail2 register	Mail2 Read (set $\overline{MBF2}$ HIGH)

Table 5. Port B Enable Function

$\overline{CSB}$	W/$\overline{RB}$	ENB	MBB	CLKB	$B_{0–35}$	Port Function
H	X	X	X	X	In high-impedance state	None
L	L	L	X	X	In high-impedance state	None
L	L	H	L	↑	In high-impedance state	FIFO2 Write
L	L	H	H	↑	In high-impedance state	Mail2 Write
L	H	L	L	X	Active, FIFO1 output register	None
L	H	H	L	↑	Active, FIFO1 output register	FIFO1 Read
L	H	L	H	X	Active, Mail1 register	None
L	H	H	H	↑	Active, Mail1 register	Mail1 Read (set $\overline{MBF1}$ HIGH)

Notes:
3. X1 register holds the offset for $\overline{AEB}$; Y1 register holds the offset for $\overline{AFA}$.
4. X2 register holds the offset for AEA; Y2 register holds the offset for AFB.

Table 6. FIFO1 Flag Operation (CY Standard and FWFT modes)

Number of Words in FIFO Memory[2, 5, 6, 7, 8]			Synchronized to CLKB		Synchronized to CLKA	
CY7C43644AV	CY7C43664AV	CY7C43684AV	$\overline{\text{EFB}}$/$\overline{\text{ORB}}$	$\overline{\text{AEB}}$	$\overline{\text{AFA}}$	$\overline{\text{FFA}}$/$\overline{\text{IRA}}$
0	0	0	L	L	H	H
1 to X1	1 to X1	1 to X1	H	L	H	H
(X1 + 1) to [1024 – (Y1 + 1)]	(X1 + 1) to [4096 – (Y1 + 1)]	(X1 + 1) to [16384 – (Y1 + 1)]	H	H	H	H
(1024 – Y1) to 1023	(4096 – Y1) to 4095	(16384 – Y1) to 16383	H	H	L	H
1024	4096	16384	H	H	L	L

Table 7. FIFO2 Flag Operation (CY Standard and FWFT modes)

Number of Words in FIFO Memory[2, 6, 7, 9, 10]			Synchronized to CLKA		Synchronized to CLKB	
CY7C43644AV	CY7C43664AV	CY7C43684AV	$\overline{\text{EFA}}$/$\overline{\text{ORA}}$	$\overline{\text{AEA}}$	$\overline{\text{AFB}}$	$\overline{\text{FFB}}$/$\overline{\text{IRB}}$
0	0	0	L	L	H	H
1 to X2	1 to X2	1 to X2	H	L	H	H
(X2 + 1) to [1024 – (Y2 + 1)]	(X2 + 1) to [4096 – (Y2 + 1)]	(X2 + 1) to [16384 – (Y2 + 1)]	H	H	H	H
(1024 – Y2) to 1023	(4096 – Y2) to 4095	(16384 – Y2) to 16383	H	H	L	H
1024	4096	16384	H	H	L	L

Table 8. Data Size for Long-Word Writes to FIFO2

Size Mode[11]			Data Written to FIFO2				Data Read From FIFO2			
BM	SIZE	BE	$B_{27–35}$	$B_{18–26}$	$B_{9–17}$	$B_{0–8}$	$A_{27–35}$	$A_{18–26}$	$A_{9–17}$	$A_{0–8}$
L	X	X	A	B	C	D	A	B	C	D

Table 9. Data Size for Word Writes to FIFO2

Size Mode[11]			Write No.	Data Written to FIFO2		Data Read From FIFO2			
BM	SIZE	BE		$B_{9–17}$	$B_{0–8}$	$A_{27–35}$	$A_{18–26}$	$A_{9–17}$	$A_{0–8}$
H	L	H	1	A	B	A	B	C	D
			2	C	D				
H	L	L	1	C	D	A	B	C	D
			2	A	B				

Notes:

5. X1 is the almost-empty offset for FIFO1 used by AEB. Y1 is the almost-full offset for FIFO1 used by AFA. Both X1 and Y1 are selected during a FIFO1 reset or port A programming.
6. When a word loaded to an empty FIFO is shifted to the output register, its previous FIFO memory location is free.
7. Data in the output register does not count as a “word in FIFO memory”. Since in FWFT mode, the first word written to an empty FIFO goes unrequested to the output register (no Read operation necessary), it is not included in the FIFO memory count.
8. The ORB and IRA functions are active during FWFT mode; the EFB and FFA functions are active in CY Standard mode.
9. X2 is the almost-empty offset for FIFO2 used by AEA. Y2 is the almost-full offset for FIFO2 used by AFB. Both X2 and Y2 are selected during a FIFO2 reset or port A programming.
10. The ORA and IRB functions are active during FWFT mode; the EFA and FFB functions are active in CY Standard mode.quested to the output register (no Read operation necessary), it is not included in the FIFO memory count.
11. BE is selected at Master Reset; BM and SIZE must be static throughout device operation.

Table 10. Data Size for Byte Writes to FIFO2

Size Mode[11]			Write No.	Data Written to FIFO2	Data Read From FIFO2			
BM	SIZE	BE		$B_{0–8}$	$A_{27–35}$	$A_{18–26}$	$A_{9–17}$	$A_{0–8}$
H	H	H	1	A	A	B	C	D
			2	B				
			3	C				
			4	D				
H	H	L	1	D	A	B	C	D
			2	C				
			3	B				
			4	A				

Table 11. Data Size for FIFO Long-Word Reads from FIFO1

Size Mode[11]			Data Written to FIFO1				Data Read From FIFO1			
BM	SIZE	BE	$A_{27–35}$	$A_{18–26}$	$A_{9–17}$	$A_{0–8}$	$B_{27–35}$	$B_{18–26}$	$B_{9–17}$	$B_{0–8}$
L	X	X	A	B	C	D	A	B	C	D

Table 12. Data Size for Word Reads from FIFO1

Size Mode[11]			Data Written to FIFO1				Read No.	Data Read From FIFO1	
BM	SIZE	BE	$A_{27–35}$	$A_{18–26}$	$A_{9–17}$	$A_{0–8}$		$B_{9–17}$	$B_{0–8}$
H	L	H	A	B	C	D	1	A	B
							2	C	D
H	L	L	A	B	C	D	1	C	D
							2	A	B

Table 13. Data Size for Byte Reads from FIFO1

Size Mode[11]			Data Written to FIFO1				Read No.	Data Read From FIFO1
BM	SIZE	BE	$A_{27–35}$	$A_{18–26}$	$A_{9–17}$	$A_{0–8}$		$B_{0–8}$
H	H	H	A	B	C	D	1	A
							2	B
							3	C
							4	D
H	H	L	A	B	C	D	1	D
							2	C
							3	B
							4	A

Maximum Ratings[12, 14]

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature .....< 65°C to +150°C

Ambient Temperature with Power Applied.....< 55°C to +125°C

Supply Voltage to Ground Potential..... < 0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State[13].....< 0.5V to V_{CC}+0.5V

DC Input Voltage[13].....< 0.5V to V_{CC}+0.5V

Output Current into Outputs (LOW)..... 20 mA

Static Discharge Voltage..... >2001V (per MIL-STD-883, Method 3015)

Latch-Up Current..... >200 mA

Operating Range

Range	Ambient Temperature	V_{CC}[15]
Commercial	0°C to +70°C	3.3V ± 10%
Industrial	<40°C to +85°C	3.3V ± 10%

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions		CY7C43644/64/84AV Min.	CY7C43644/64/84AV Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = 3.0V, I_{OH} = <2.0 mA		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = 3.0V, I_{OL} = 8.0 mA			0.5	V
V_{IH}	Input HIGH Voltage			2.0	V_{CC}	V
V_{IL}	Input LOW Voltage			<0.5	0.8	V
I_{IX}	Input Leakage Current	V_{CC} = Max.		<10	+10	µA
I_{OZL} I_{OZH}	Output OFF, High Z Current	V_{SS} < V_O< V_{CC}		<10	+10	µA
I_{CC1}[16]	Active Power Supply Current		Commercial		60	mA
			Industrial		60	mA
I_{SB}[17]	Average Standby Current		Commercial		10	mA
			Industrial		10	mA

Capacitance[18]

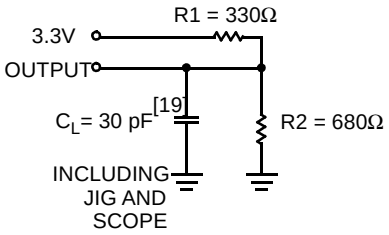
Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 3.3V	4	pF
C_{OUT}	Output Capacitance		8	pF

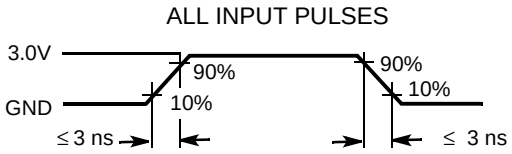
Note:

12. Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
13. The input and output voltage ratings may be exceeded provided the input and output current ratings are observed.
14. The Voltage on any input or I/O pin cannot exceed the power pin during power-up.
15. Operating V_{CC} Range for –7 speed is 3.3V ± 5%.
16. Input signals switch from 0V to 3V with a rise/fall time of less than 3 ns, clocks and clock enables switch at 20 MHz, while data inputs switch at 10 MHz. Outputs are unloaded.
17. All inputs = V_{CC} – 0.2V, except RCLK and WCLK (which are at frequency = 0 MHz). All outputs are unloaded.
18. Tested initially and after any design or process changes that may affect these parameters.

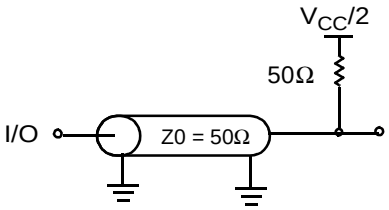
Table 14.

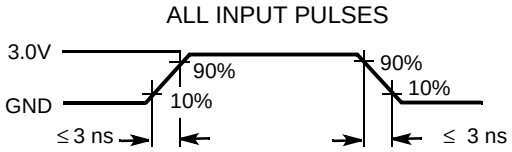
AC Test Loads and Waveforms (–10 and –15)





AC Test Loads and Waveforms (–7)





Switching Characteristics Over the Operating Range

Parameter	Description	CY7C43644/64/84AV –7		CY7C43644/64/84AV –10		CY7C43644/64/84AV –15		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
f_S	Clock Frequency, CLKA or CLKB		133		100		67	MHz
t_{CLK}	Clock Cycle Time, CLKA or CLKB	7.5		10		15		ns
t_{CLKH}	Pulse Duration, CLKA or CLKB HIGH	3.5		4		6		ns
t_{CLKL}	Pulse Duration, CLKA or CLKB LOW	3.5		4		6		ns
t_{DS}	Set-Up Time, $A_{0–35}$ before CLKA↑ and $B_{0–35}$ before CLKB↑	3		4		5		ns
t_{ENS}	Set-Up Time, $\overline{CSA}$, W/$\overline{RA}$, ENA, and MBA before CLKA↑; $\overline{CSB}$, W/$\overline{RB}$, ENB, and MBB before CLKB↑	3		4		5		ns
t_{RSTS}	Set-Up Time, $\overline{MRS1}$, $\overline{MRS2}$, $\overline{PRS1}$, $\overline{PRS2}$, $\overline{RT1}$ or $\overline{RT2}$ LOW before CLKA↑ or CLKB↑[20]	2.5		4		5		ns
t_{FSS}	Set-Up Time, FS0 and FS1 before $\overline{MRS1}$ and $\overline{MRS2}$ HIGH	5		7		7.5		ns
t_{BES}	Set-Up Time, BE/$\overline{FWFT}$ before $\overline{MRS1}$ and $\overline{MRS2}$ HIGH	5		7		7.5		ns
t_{SPMS}	Set-Up Time, $\overline{SPM}$ before $\overline{MRS1}$ and $\overline{MRS2}$ HIGH	5		7		7.5		ns
t_{SDS}	Set-Up Time, FS0/SD before CLKA↑	3		4		5		ns
t_{SENS}	Set-Up Time, FS1/$\overline{SEN}$ before CLKA↑	3		4		5		ns
t_{FWS}	Set-Up Time, BE/$\overline{FWFT}$ before CLKA↑	0		0		0		ns
t_{DH}	Hold Time, $A_{0–35}$ after CLKA↑ and $B_{0–35}$ after CLKB↑	0		0		0		ns
t_{ENH}	Hold Time, $\overline{CSA}$, W/$\overline{RA}$, ENA, and MBA after CLKA↑; $\overline{CSB}$, W/$\overline{RB}$, ENB, and MBB after CLKB↑	0		0		0		ns

Notes:
19. C_L = 5 pF for t_{DIS}.
20. Requirement to count the clock edge as one of at least four needed to reset a FIFO.

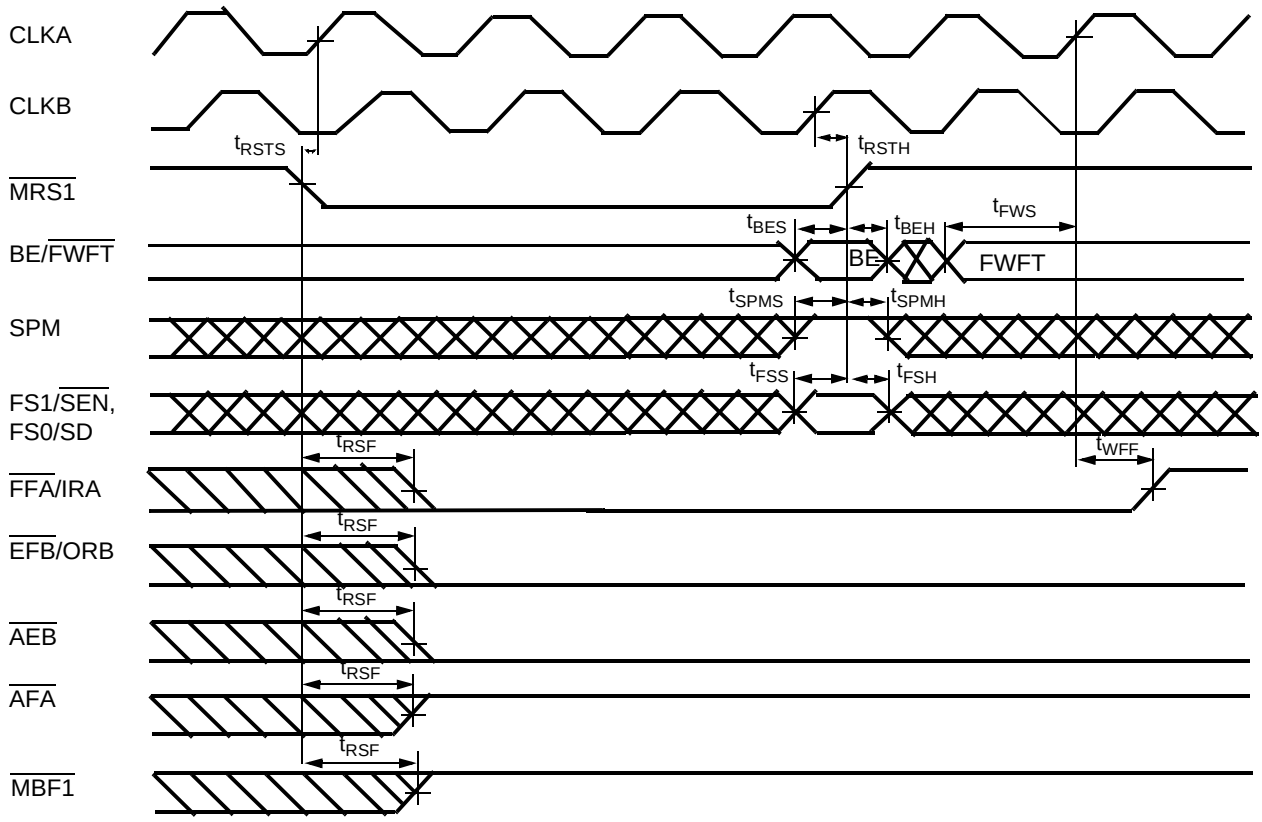
Switching Characteristics Over the Operating Range (continued)

Parameter	Description	CY7C43644/64/84AV –7		CY7C43644/64/84AV –10		CY7C43644/64/84AV –15		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{RSTH}	Hold Time, $\overline{MRS1}$, $\overline{MRS2}$, $\overline{PRS1}$, $\overline{PRS2}$, $\overline{RT1}$ or $\overline{RT2}$ LOW after CLKA↑ or CLKB↑[20]	1		2		2		ns
t_{FSH}	Hold Time, FS0 and FS1 after $\overline{MRS1}$ and $\overline{MRS2}$ HIGH	1		1		2		ns
t_{BEH}	Hold Time, BE/FWFT after $\overline{MRS1}$ and $\overline{MRS2}$ HIGH	1		1		2		ns
t_{SPMH}	Hold Time, $\overline{SPM}$ after $\overline{MRS1}$ and $\overline{MRS2}$ HIGH	1		1		2		ns
t_{SDH}	Hold Time, FS0/SD after CLKA↑	0		0		0		ns
t_{SENH}	Hold Time, FS1/$\overline{SEN}$ after CLKA↑	0		0		0		ns
t_{SPH}	Hold Time, FS1/$\overline{SEN}$ HIGH after $\overline{MRS1}$ and $\overline{MRS2}$ HIGH	1		1		2		ns
t_{SKEW1}[21]	Skew Time between CLKA↑ and CLKB↑ for $\overline{EFA}$/ORA, $\overline{EFB}$/ORB, $\overline{FFA}$/IRA, and $\overline{FFB}$/IRB	5		5		7.5		ns
t_{SKEW2}[21]	Skew Time between CLKA↑ and CLKB↑ for $\overline{AEA}$, $\overline{AEB}$, $\overline{AFA}$, $\overline{AFB}$	7		8		12		ns
t_A	Access Time, CLKA↑ to $A_{0–35}$ and CLKB↑ to $B_{0–35}$	1	6	1	8	3	10	ns
t_{WFF}	Propagation Delay Time, CLKA↑ to $\overline{FFA}$/IRA and CLKB↑ to $\overline{FFB}$/IRB	1	6	1	8	2	10	ns
t_{REF}	Propagation Delay Time, CLKA↑ to $\overline{EFA}$/ORA and CLKB↑ to $\overline{EFB}$/ORB	1	6	1	8	2	10	ns
t_{PAE}	Propagation Delay Time, CLKA↑ to $\overline{AEA}$ and CLKB↑ to $\overline{AEB}$	1	6	1	8	1	10	ns
t_{PAF}	Propagation Delay Time, CLKA↑ to $\overline{AFA}$ and CLKB↑ to $\overline{AFB}$	1	6	1	8	1	10	ns
t_{PMF}	Propagation Delay Time, CLKA↑ to $\overline{MBF1}$ LOW or $\overline{MBF2}$ HIGH and CLKB↑ to $\overline{MBF2}$ LOW or $\overline{MBF1}$ HIGH	0	6	0	8	0	12	ns
t_{PMR}	Propagation Delay Time, CLKA↑ to $B_{0–35}$[22] and CLKB↑ to $A_{0–35}$[23]	1	7	2	11	3	12	ns
t_{MDV}	Propagation Delay Time, MBA to $A_{0–35}$ Valid and MBB to $B_{0–35}$ Valid	1	6	2	9	3	11	ns
t_{RSF}	Propagation Delay Time, $\overline{MRS1}$ or $\overline{PRS1}$ LOW to $\overline{AEB}$ LOW, $\overline{AFA}$ HIGH, $\overline{FFA}$ / IRA LOW, $\overline{EFB}$ /ORB LOW and $\overline{MBF1}$ HIGH and $\overline{MRS2}$ or $\overline{PRS2}$ LOW to $\overline{AEA}$ LOW, $\overline{AFB}$ HIGH, $\overline{FFB}$ / IRB LOW, $\overline{EFA}$ /ORA LOW and $\overline{MBF2}$ HIGH	1	6	1	10	1	15	ns
t_{EN}	Enable Time, $\overline{CSA}$ or W/$\overline{RA}$ LOW to $A_{0–35}$ Active and $\overline{CSB}$ LOW and W/$\overline{RB}$ HIGH to $B_{0–35}$ Active	1	6	2	8	2	10	ns
t_{DIS}[19]	Disable Time, $\overline{CSA}$ or W/$\overline{RA}$ HIGH to $A_{0–35}$ at High Impedance and $\overline{CSB}$ HIGH or W/$\overline{RB}$ LOW to $B_{0–35}$ at High Impedance	1	5	1	6	1	8	ns
t_{RTR}	Retransmit Recovery Time	90		90		90		ns

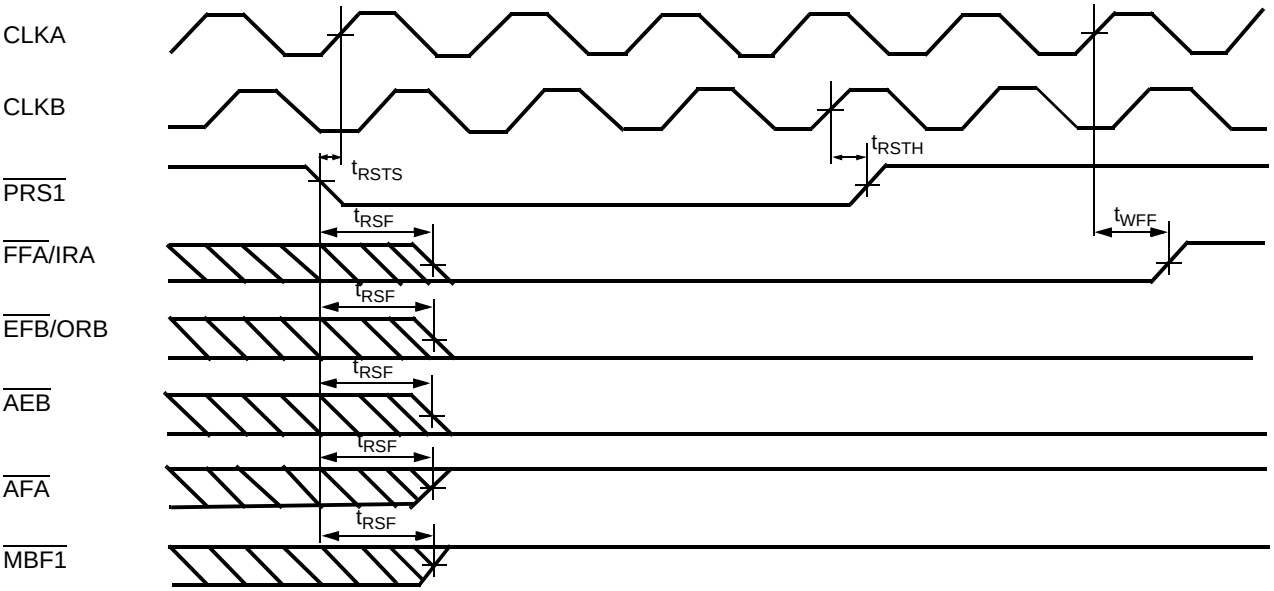
Notes:
21. Skew time is not a timing constraint for proper device operation and is only included to illustrate the timing relationship between the CLKA cycle and the CLKB cycle.
22. Writing data to the Mail1 register when the $B_{0–35}$ outputs are active and MBB is HIGH.
23. Writing data to the Mail2 register when the $A_{0–35}$ outputs are active and MBA is HIGH

Switching Waveforms

FIFO1 Master Reset Loading X1 and Y1 with a Preset Value of Eight [24, 25]



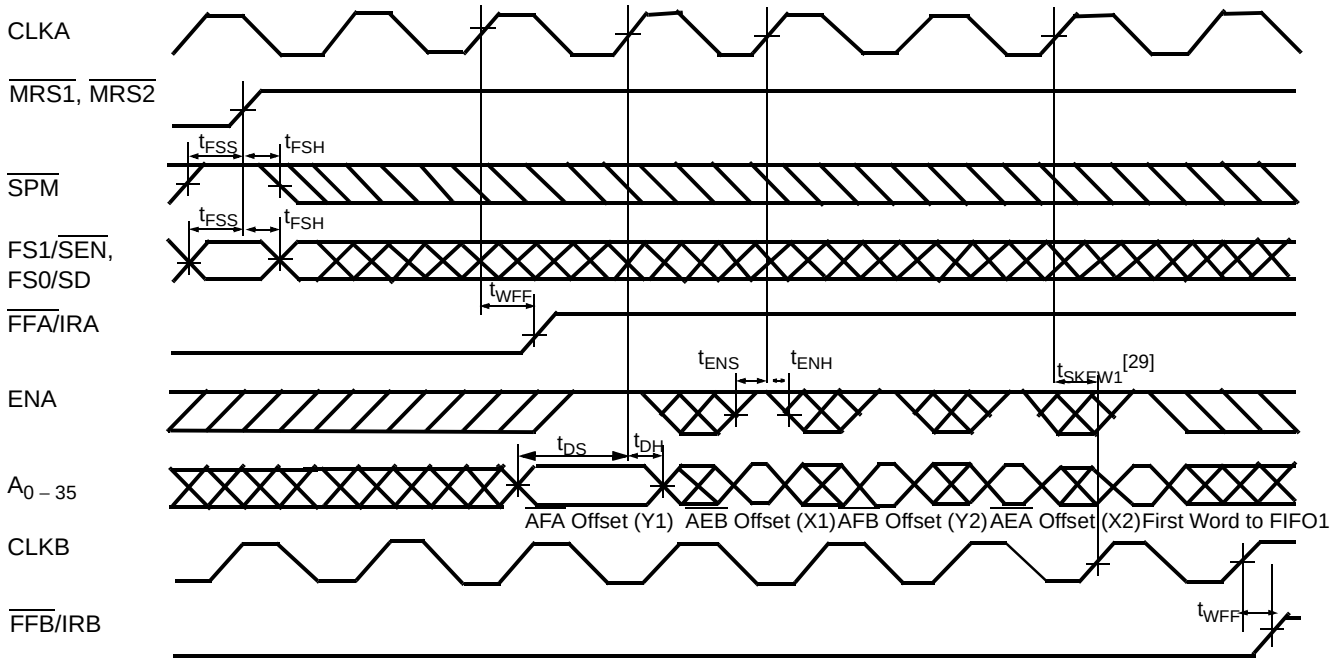
FIFO1 Partial Reset (CY Standard and FWFT Modes)[26, 27]



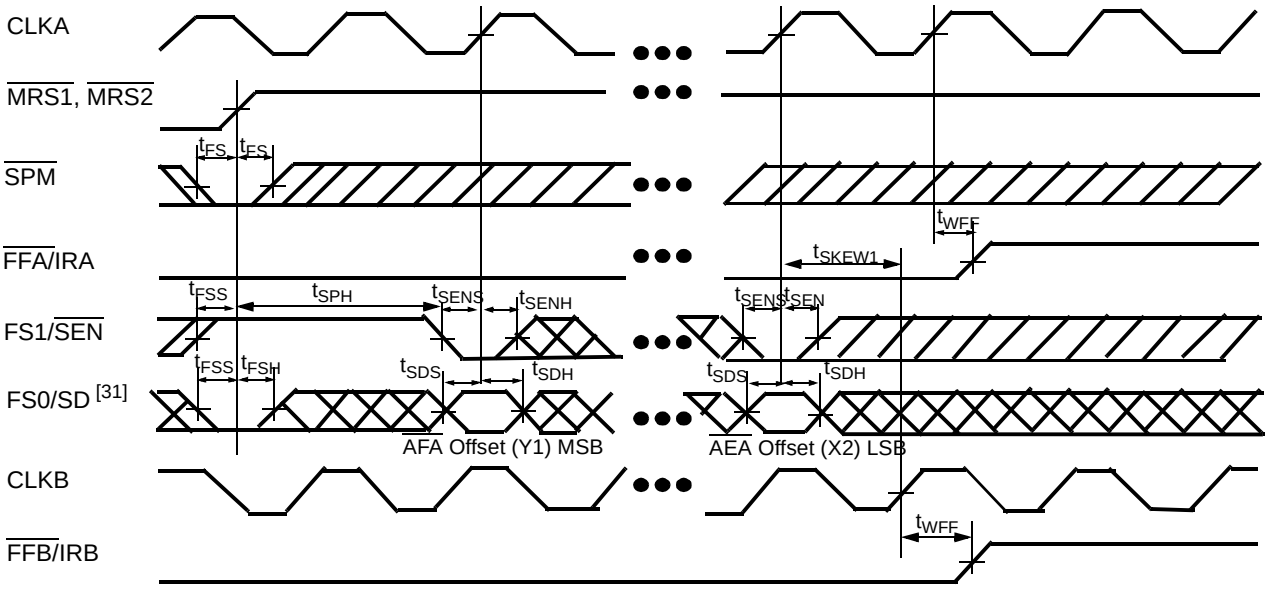
Notes:
24. Master Reset is performed in the same manner for FIFO2 to load X2 and Y2 with a preset value.
25. PRS1 must be HIGH during Master Reset.

Switching Waveforms (continued)

Parallel Programming of the Almost-Full Flag and Almost-Empty Flag Offset Values after Reset (CY Standard and FWFT Modes) [28]



Serial Programming of the Almost-Full Flag and Almost-Empty Flag Offset Values (CY Standard and FWFT Modes) [30, 31]

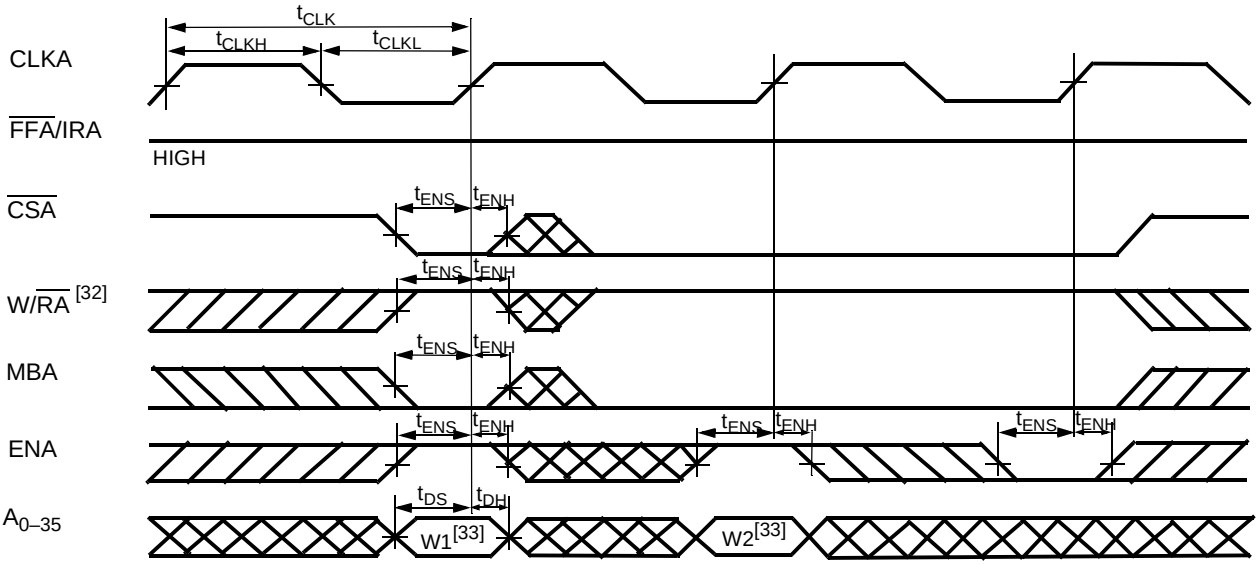


Notes:

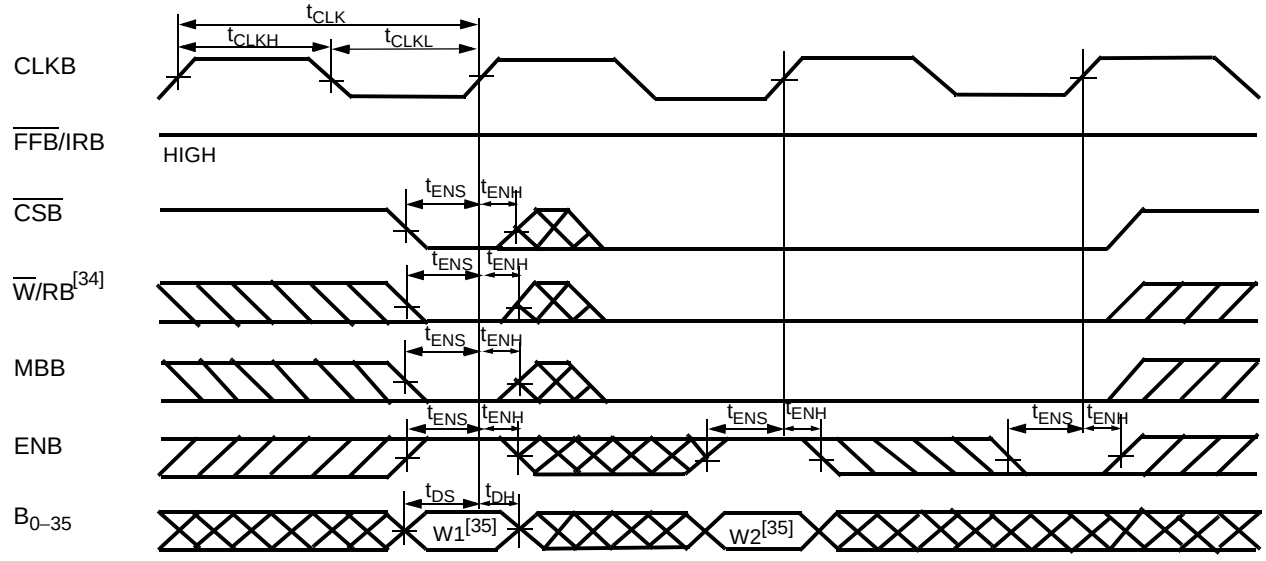
26. Partial Reset is performed in the same manner for FIFO2.
27. MRS1 must be HIGH during Partial Reset.
28. CSAU = LOW, W/RA = HIGH, MBA = LOW. It is not necessary to program offset register on consecutive clock cycles. FIFO can only be programmed in parallel when FFA/IRA is HIGH.
29. t_{SKEW1} is the minimum time between the rising CLKA edge and a rising CLKB for FFB/IRB to transition HIGH in the next cycle. If the time between the rising edge of CLKA and rising edge of CLKB is less than t_{SKEW1}, then FFB/IRB may transition HIGH one cycle later than shown.

Switching Waveforms (continued)

Port A Write Cycle Timing for FIFO1 (CY Standard and FWFT Modes)



Port B Long-Word Write Cycle Timing for FIFO2 (CY Standard and FWFT Modes)

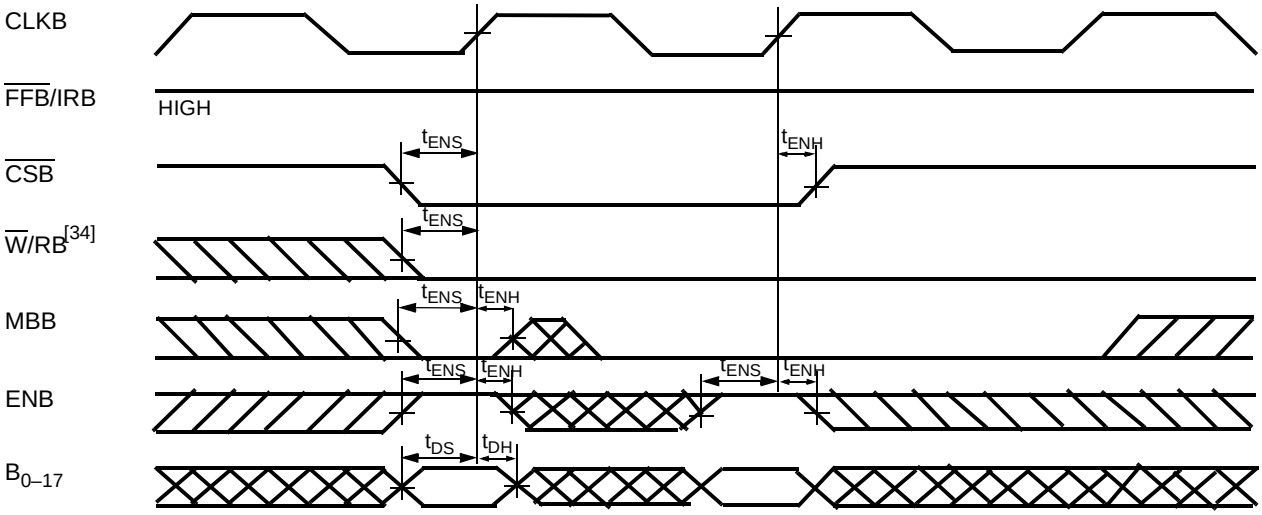


Notes:

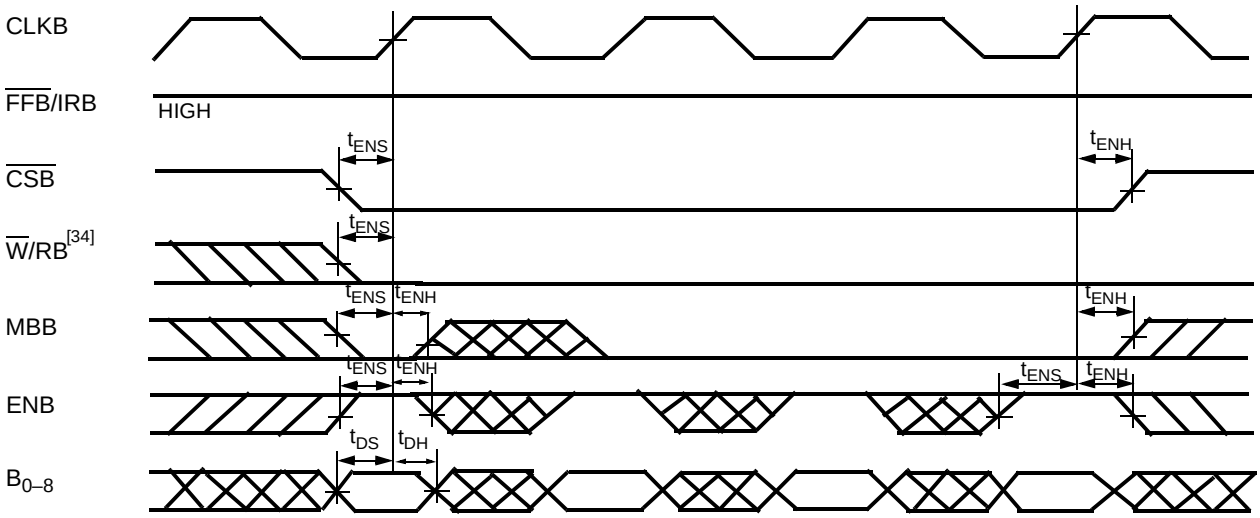
30. It is not necessary to program offset register bits on consecutive clock cycles. Attempts to write into FIFO memory are ignored until FFA/IRA is set HIGH.
31. Programmable offsets are written serially to the SD input in the order AFA offset (Y1), AEB offset (X1), AFB offset (Y2), and AEA offset (X2).
32. If W/RA switches from Read to Write before the assertion of CSA, $t_{ENS} = t_{DIS} + t_{ENS}$.
33. Written to FIFO1.

Switching Waveforms (continued)

Port B Word Write Cycle Timing for FIFO2 (CY Standard and FWFT Modes)



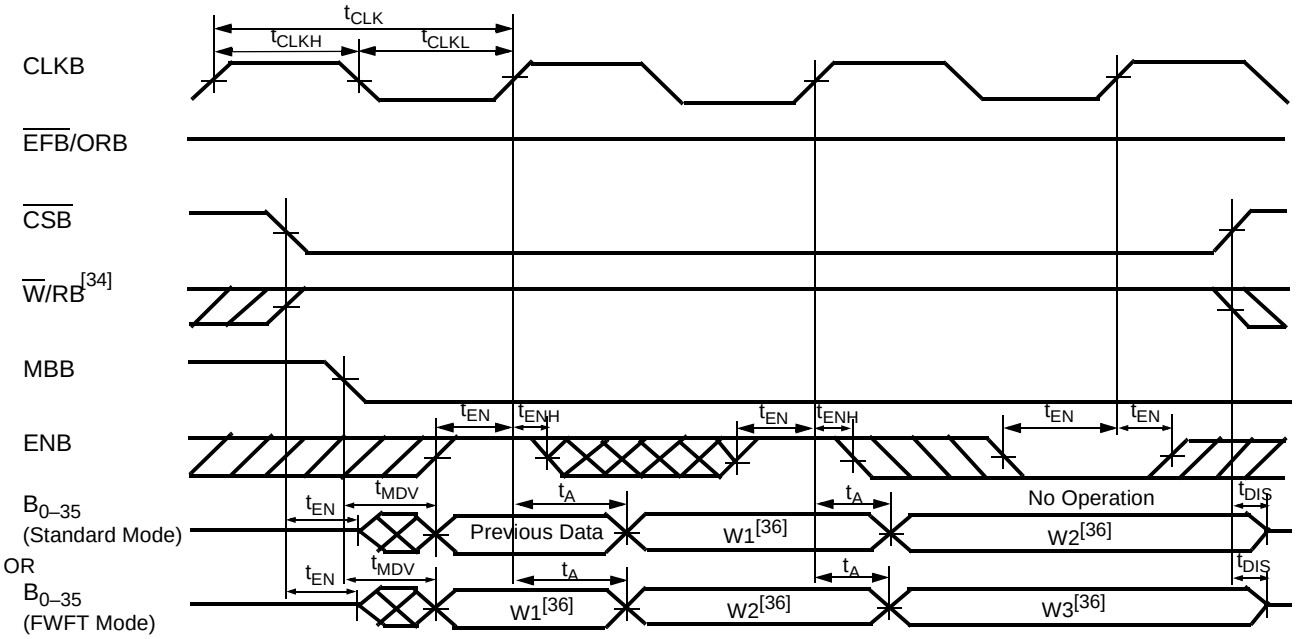
Port B Byte Write Cycle Timing for FIFO2 (CY Standard and FWFT Modes)



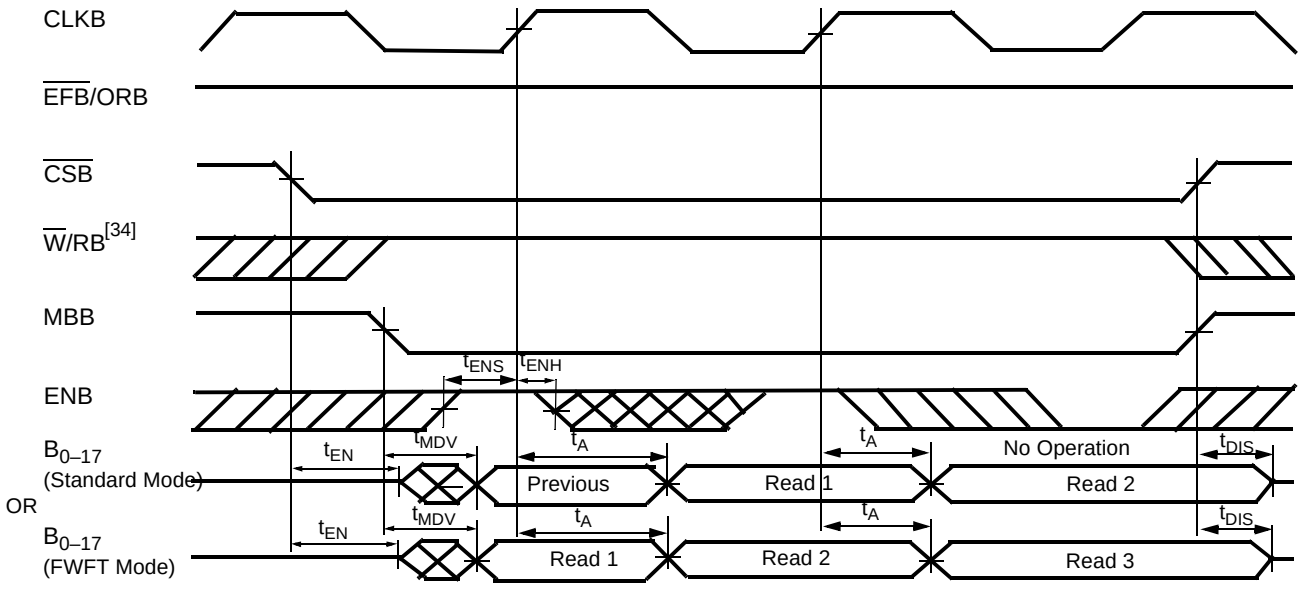
Note:
34. If W/RB switches from Read to Write before the assertion of CSB, $t_{ENS} = t_{DIS} + t_{ENS}$.
35. Written to FIFO2.

Switching Waveforms (continued)

Port B Long-Word Read Cycle Timing for FIFO1 (CY Standard and FWFT Modes)



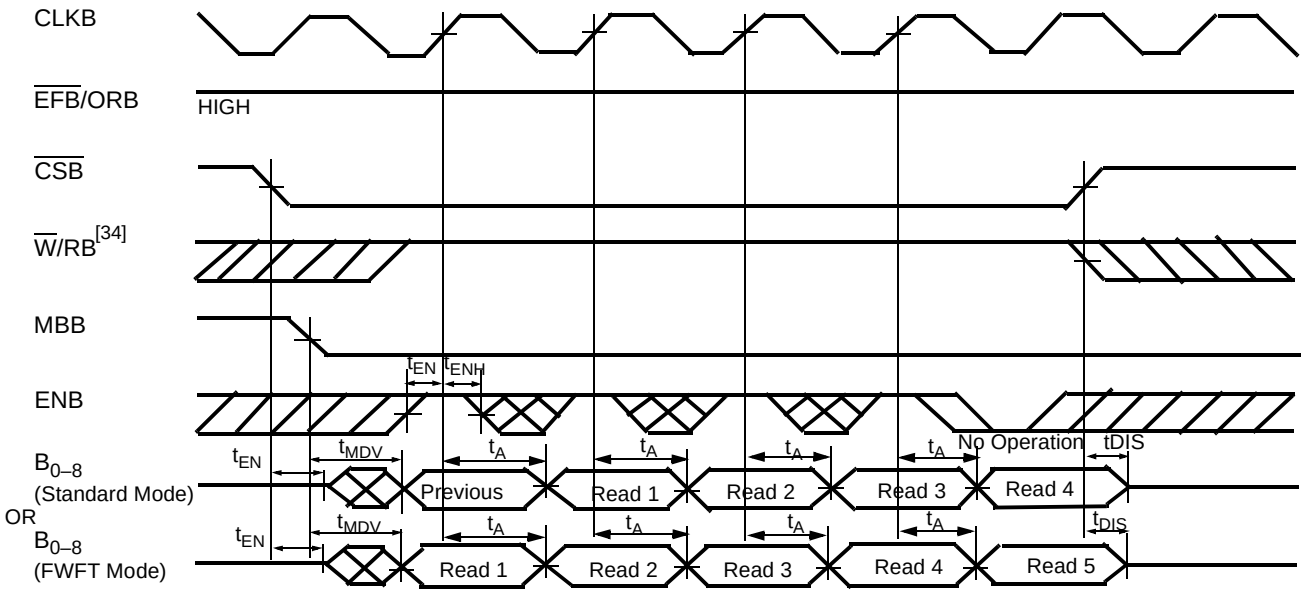
Port B Word Read Cycle Timing for FIFO1 (CY Standard and FWFT Modes)[37]



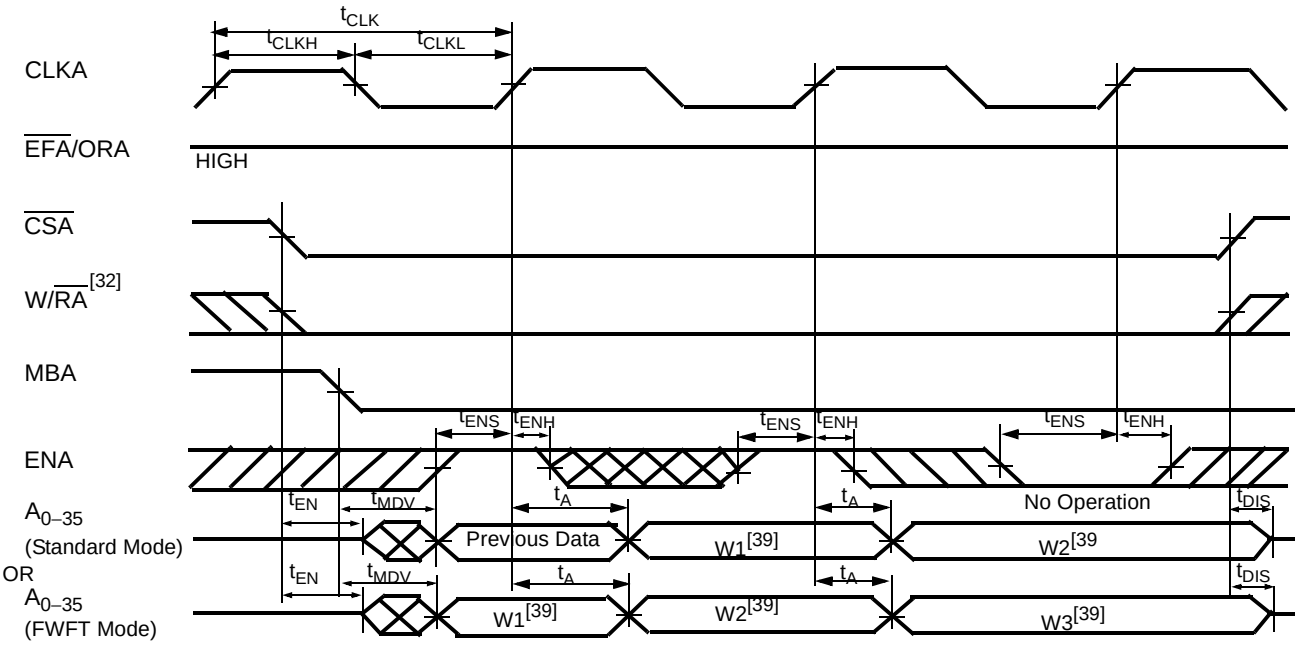
Note:
36. Read From FIFO1.

Switching Waveforms (continued)

Port B Byte Read Cycle Timing for FIFO1 (CY Standard and FWFT Modes)[38]



Port A Read Cycle Timing for FIFO2 (CY Standard and FWFT Modes)

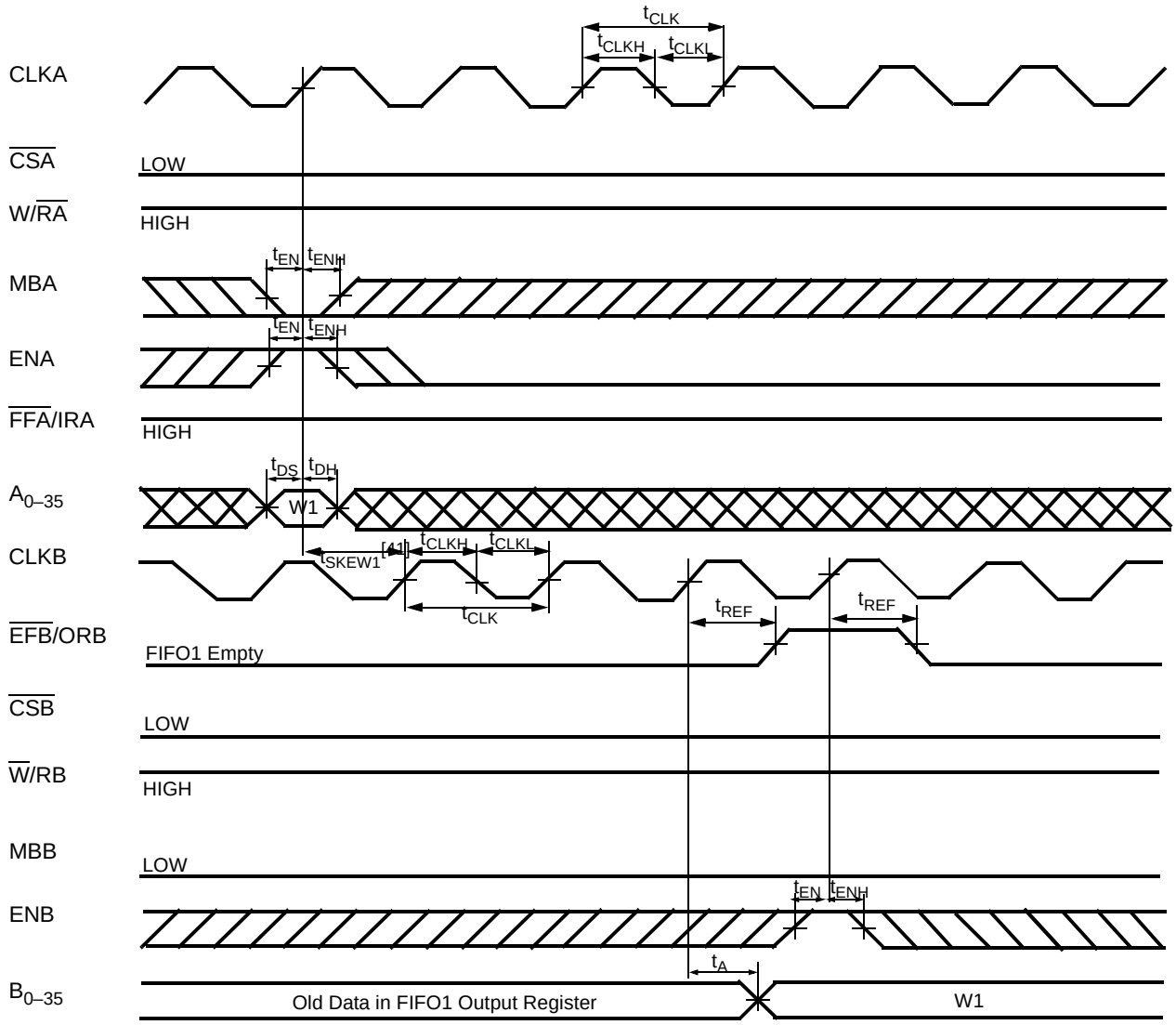


Notes:

37. Unused word $B_{18–35}$ contains all zeroes for word-size reads.
38. Unused bytes $B_{9–17}$, $B_{18–26}$, and $B_{27–35}$ contain all zeroes for byte-size reads.
39. Read From FIFO2.

Switching Waveforms (continued)

ORB Flag Timing and First Data Word Fall Through when FIFO1 is Empty (FWFT Mode)[40]

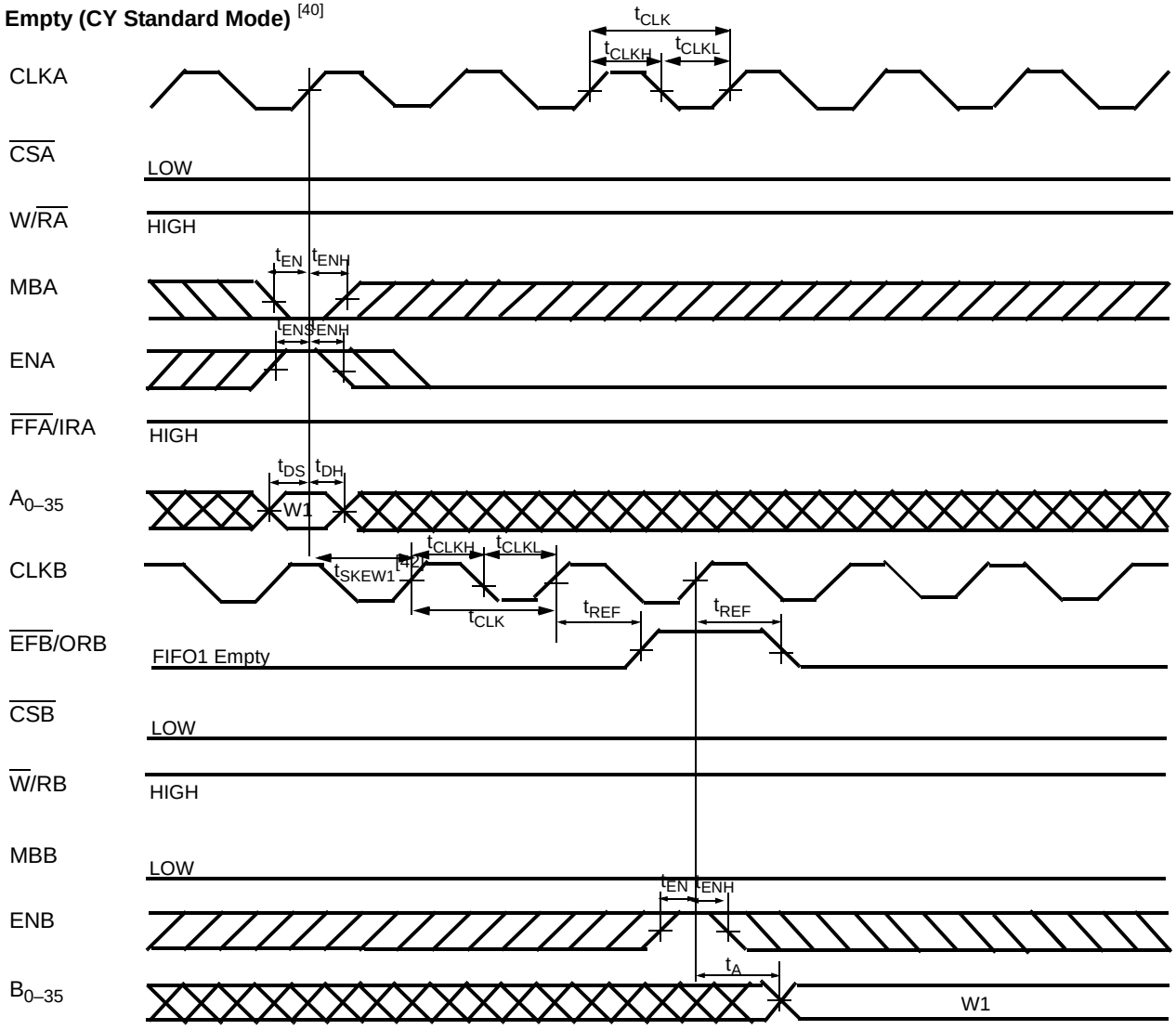


Notes:

40. If Port B size is word or byte, $\overline{EFB}$ is set LOW by the last word or byte Read from FIFO1, respectively.
41. t_{SKEW1} is the minimum time between a rising CLKA edge and a rising CLKB edge for ORB to transition HIGH and to clock the next word to the FIFO1 output register in three CLKB cycles. If the time between the rising CLKA edge and rising CLKB edge is less than t_{SKEW1}, then the transition of ORB HIGH and load of the first word to the output register may occur one CLKB cycle later than shown.

Switching Waveforms (continued)

$\overline{EFB}$ Flag Timing and First Data Read Fall Through when FIFO1 is Empty (CY Standard Mode) [40]

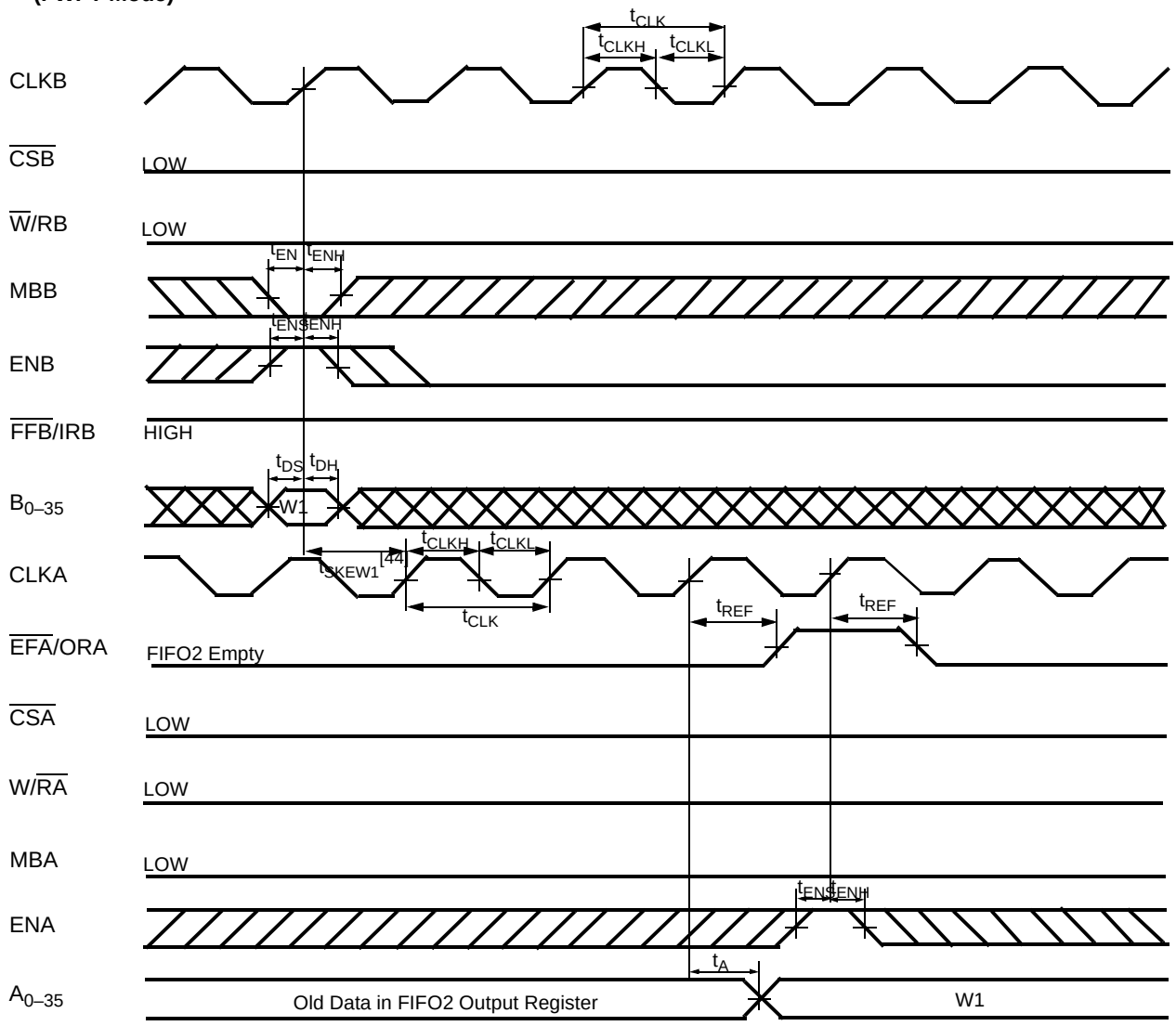


Note:

42. t_{SKEW1} is the minimum time between a rising CLKA edge and a rising CLKB edge for $\overline{EFB}$ to transition HIGH in the next CLKB cycle. If the time between the rising CLKA edge and rising CLKB edge is less than t_{SKEW1}, then the transition of $\overline{EFB}$ HIGH may occur one CLKB cycle later than shown.

Switching Waveforms (continued)

ORA Flag Timing and First Data Word Fall Through when FIFO2 is Empty (FWFT Mode) [43]

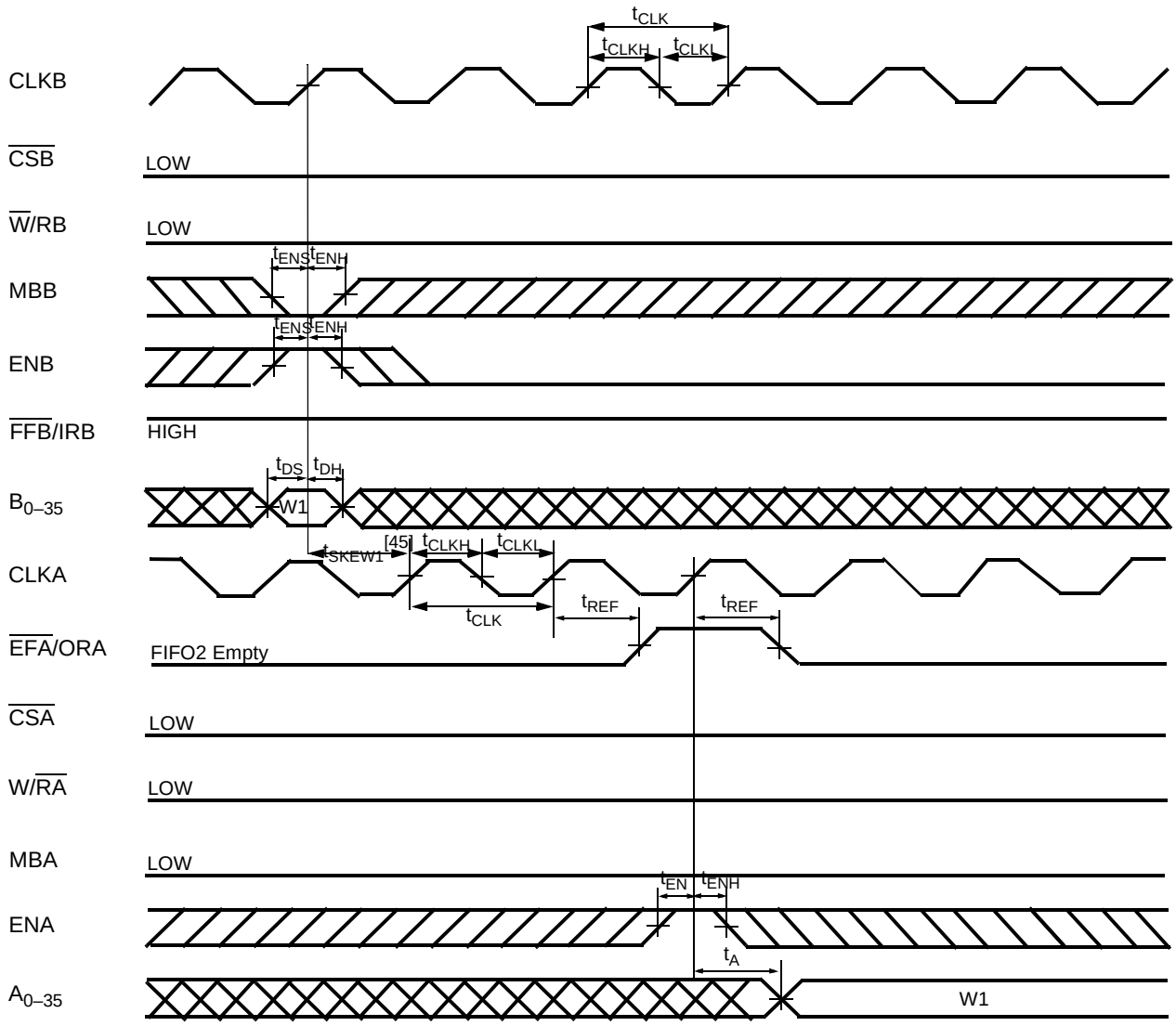


Notes:

43. If Port B size is word or byte, t_{SKEW1} is referenced to the rising CLKB edge that writes the last word or byte of the long word, respectively.
44. t_{SKEW1} is the minimum time between a rising CLKB edge and a rising CLKA edge for ORA to transition HIGH and to clock the next word to the FIFO2 output register in three CLKA cycles. If the time between the rising CLKB edge and rising CLKA edge is less than t_{SKEW1}, then the transition of ORA HIGH and load of the first word to the output register may occur one CLKA cycle later than shown.

Switching Waveforms (continued)

$\overline{EFA}$ Flag Timing and First Data Read when FIFO2 is Empty (CY Standard Mode) [43]

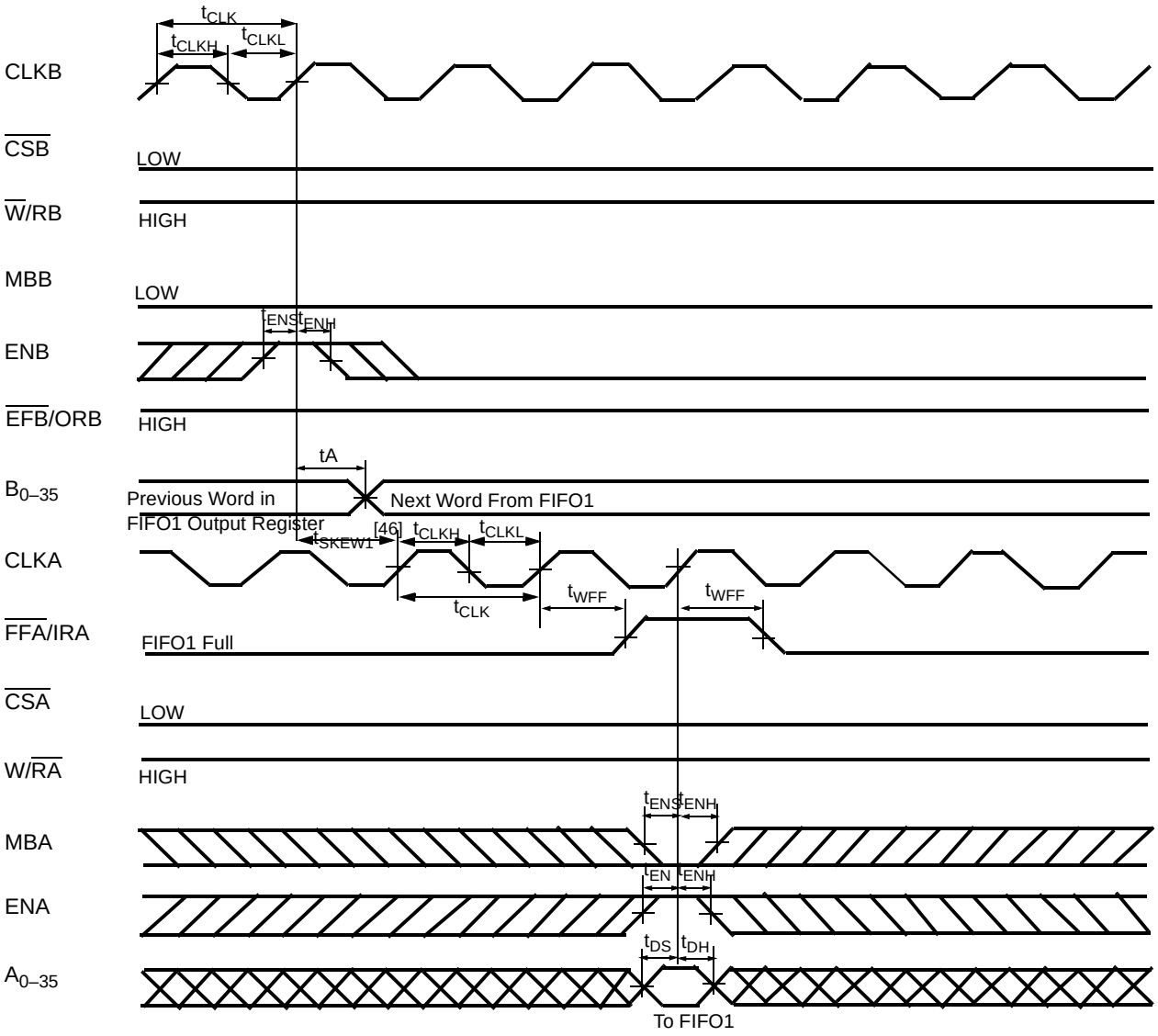


Note:

45. t_{SKEW1} is the minimum time between a rising CLKB edge and a rising CLKA edge for $\overline{EFA}$ to transition HIGH in the next CLKA cycle. If the time between the rising CLKB edge and rising CLKA edge is less than t_{SKEW1}, then the transition of $\overline{EFA}$ HIGH may occur one CLKA cycle later than shown.

Switching Waveforms (continued)

IRA Flag Timing and First Available Write when FIFO1 is Full (FWFT Mode) [43]

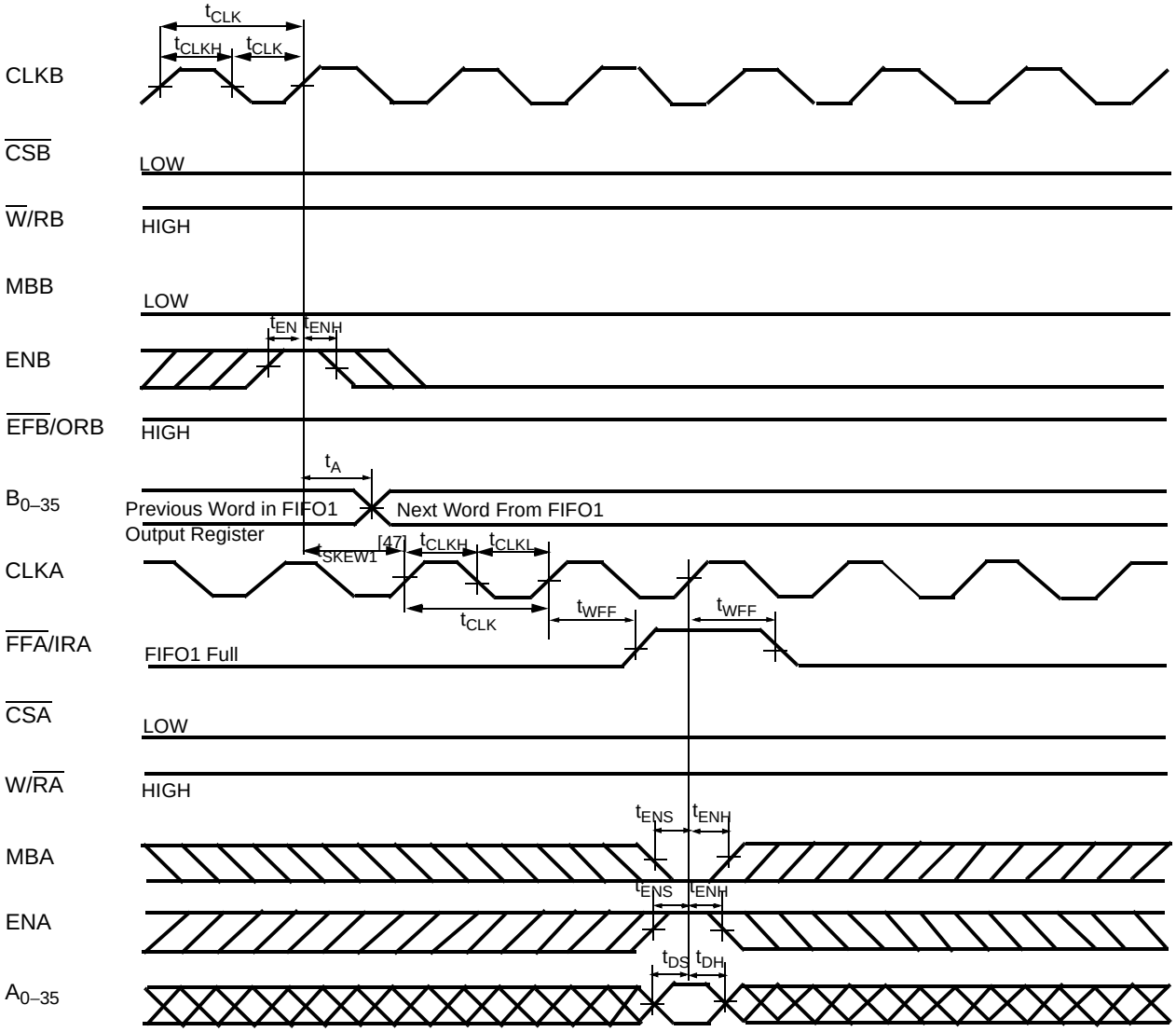


Note:

46. t_{SKEW1} is the minimum time between a rising CLKB edge and a rising CLKA edge for IRA to transition HIGH in the next CLKA cycle. If the time between the rising CLKB edge and rising CLKA edge is less than t_{SKEW1}, then IRA may transition HIGH one CLKA cycle later than shown.

Switching Waveforms (continued)

$\overline{\text{FFA}}$ Flag Timing and First Available Write when FIFO1 is Full (CY Standard Mode) [43]

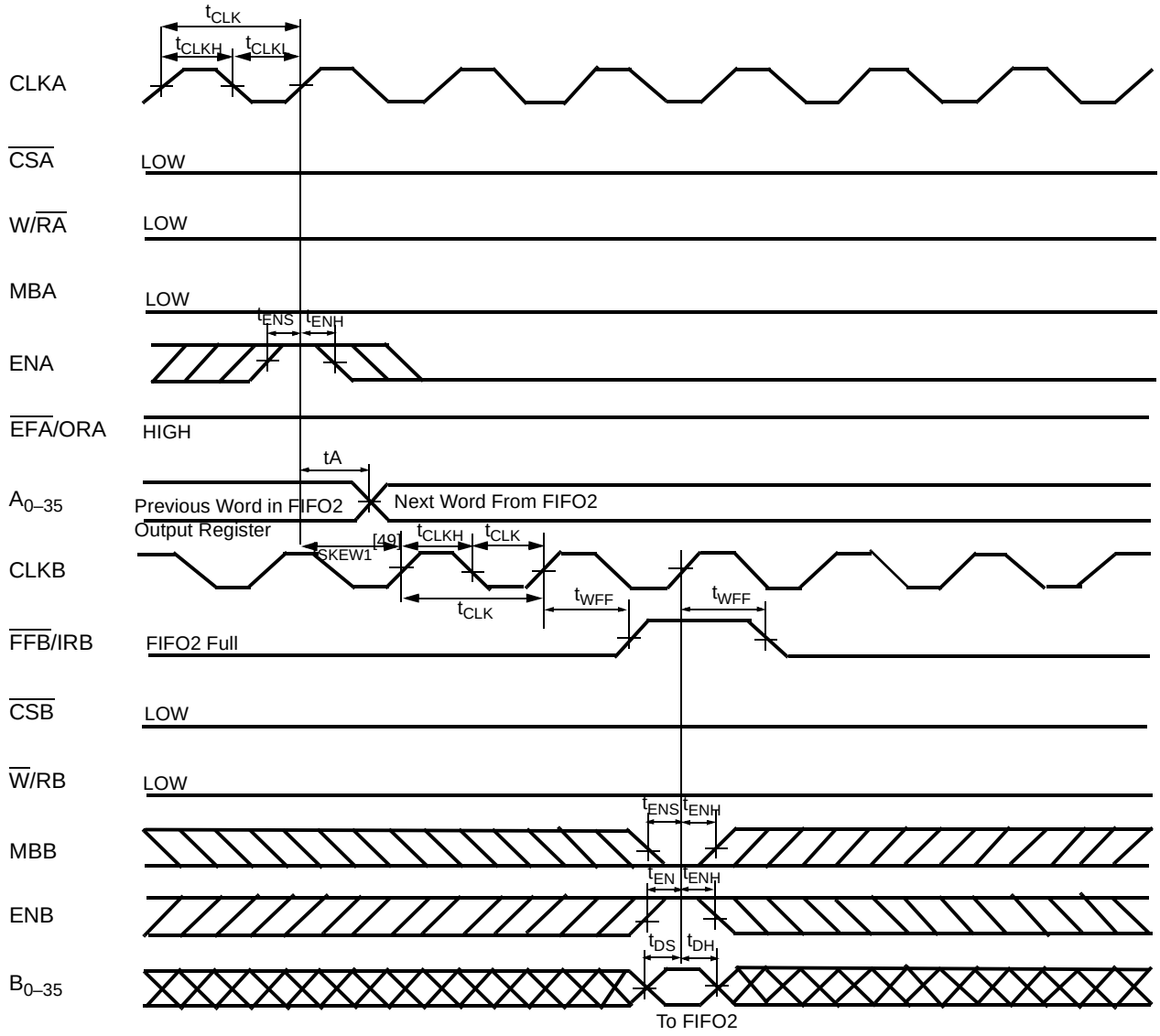


Note:

47. t_{SKEW1} is the minimum time between a rising CLKB edge and a rising CLKA edge for $\overline{\text{FFA}}$ to transition HIGH in the next CLKA cycle. If the time between the rising CLKB edge and rising CLKA edge is less than t_{SKEW1}, then the transition of FFA HIGH may occur one CLKA cycle later than shown.

Switching Waveforms (continued)

IRB Flag Timing and First Available Write when FIFO2 is Full (FWFT Mode)[48]

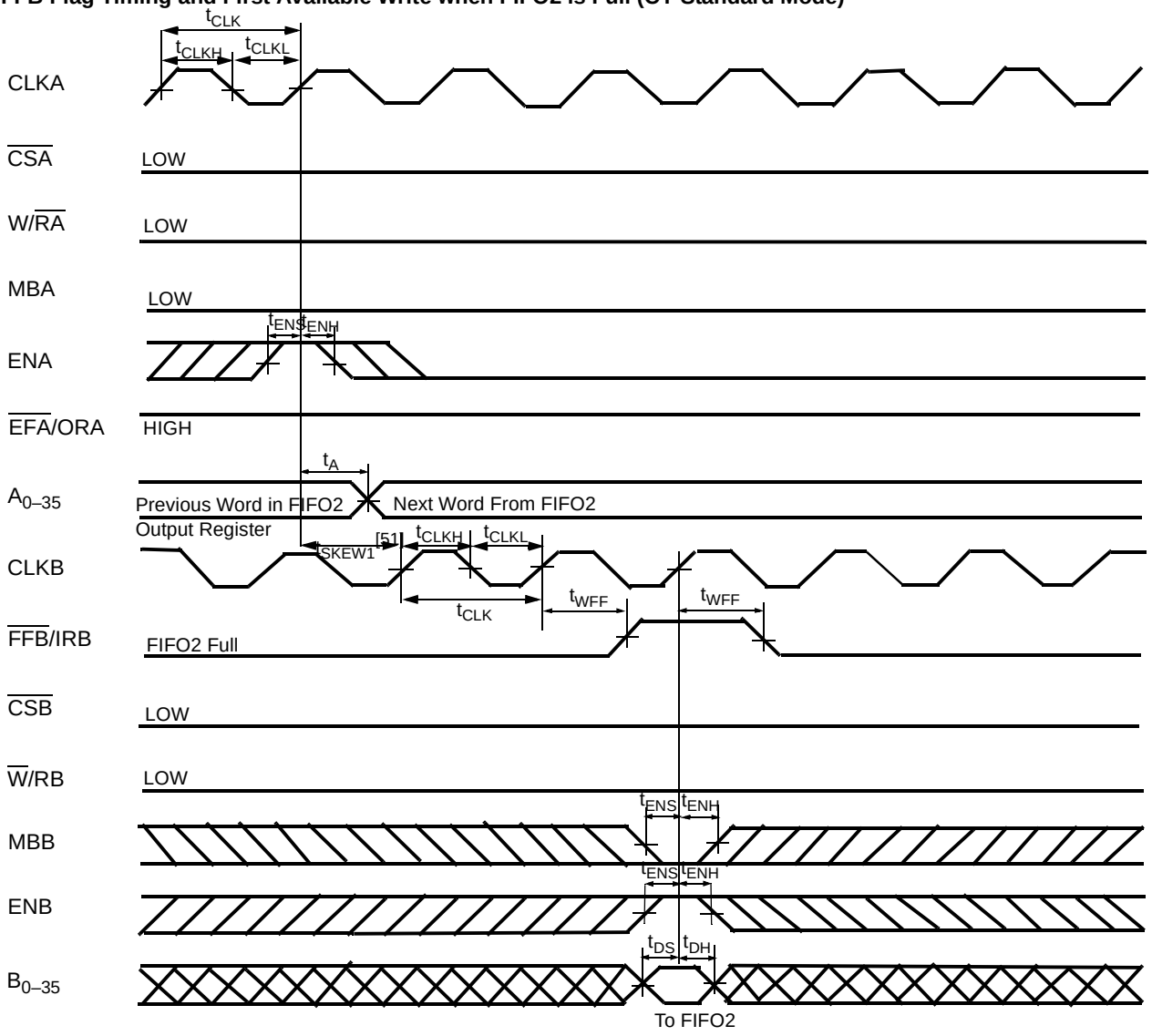


Notes:

48. If Port B size is word or byte, IRB is set LOW by the last word or byte Write of the long-word, respectively.
49. t_{SKEW1} is the minimum time between a rising CLKA edge and a rising CLKB edge for IRB to transition HIGH in the next CLKB cycle. If the time between the rising CLKA edge and rising CLKB edge is less than t_{SKEW1}, then the transition of IRB HIGH may occur one CLKB cycle later than shown.

Switching Waveforms (continued)

$\overline{\text{FFB}}$ Flag Timing and First Available Write when FIFO2 is Full (CY Standard Mode)[50]

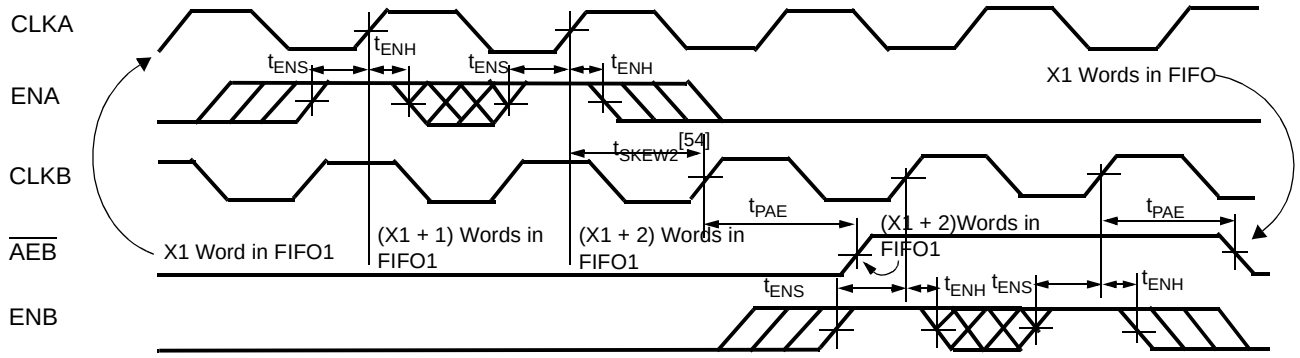


Notes:

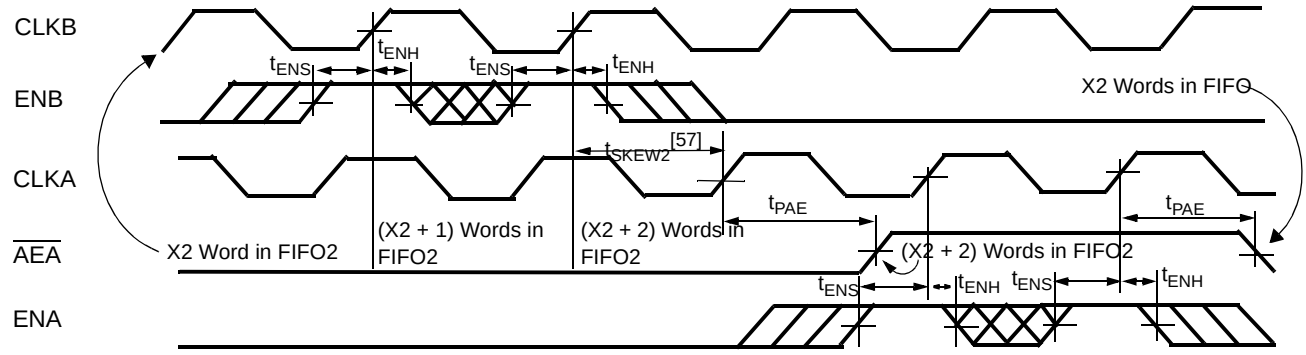
50. If Port B size is word or byte, $\overline{\text{FFB}}$ is set LOW by the last word or byte Write of the long-word, respectively.
51. t_{SKEW1} is the minimum time between a rising CLKA edge and a rising CLKB edge for $\overline{\text{FFB}}$ to transition HIGH in the next CLKB cycle. If the time between the rising CLKA edge and rising CLKB edge is less than t_{SKEW1}, then the transition of FFB HIGH may occur one CLKB cycle later than shown.

Switching Waveforms (continued)

Timing for $\overline{AEB}$ when FIFO1 is Almost Empty (CY Standard and FWFT Modes) [52, 53]



Timing for $\overline{AEA}$ when FIFO2 is Almost Empty (CY Standard and FWFT Modes) [55, 56]

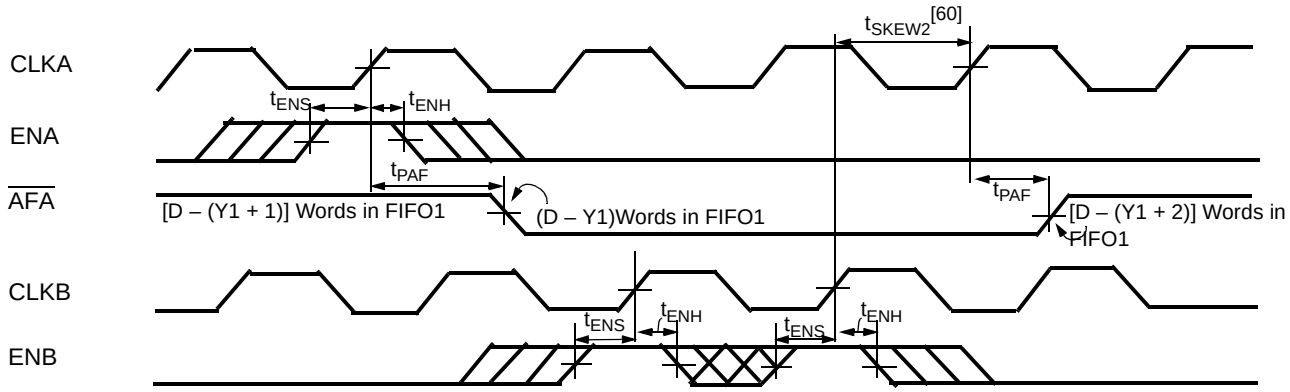


Notes:

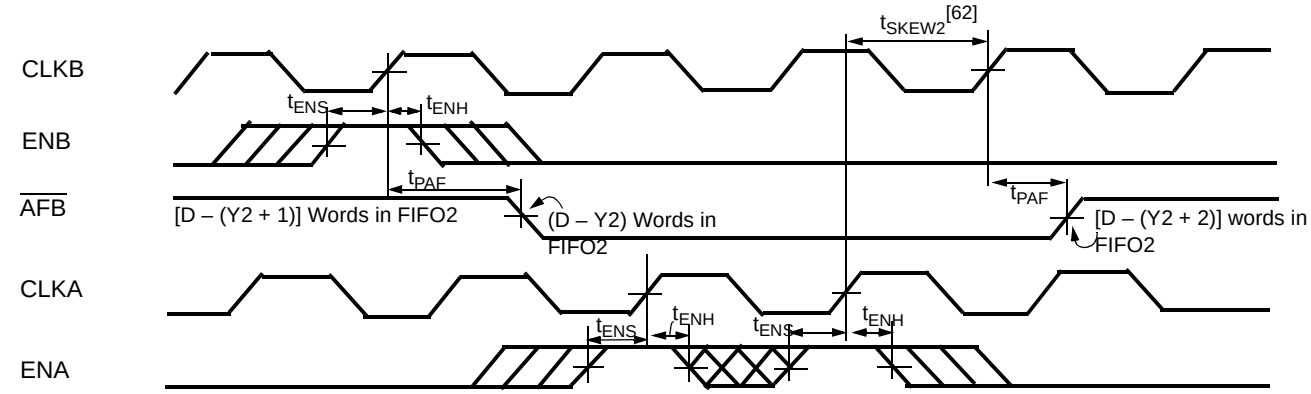
52. FIFO1 Write ($\overline{CSA}$ = LOW, W/$\overline{RA}$ = HIGH, MBA = LOW), FIFO1 Read ($\overline{CSB}$ = LOW, $\overline{W}$/RB = HIGH, MBB = LOW). Data in the FIFO1 output register has been Read from the FIFO.
53. If Port B size is word or byte, $\overline{AEB}$ is set LOW by the last word or byte Read from FIFO1, respectively.
54. t_{SKEW2} is the minimum time between a rising CLKA edge and a rising CLKB edge for AEB to transition HIGH in the next CLKB cycle. If the time between the rising CLKA edge and rising CLKB edge is less than t_{SKEW2}, then AEB may transition HIGH one CLKB cycle later than shown.
55. FIFO2 Write ($\overline{CSB}$ = LOW, W/RB = LOW, MBB = LOW), FIFO2 Read ($\overline{CSA}$ = LOW, W/RA = LOW, MBA = LOW). Data in the FIFO2 output register has been Read from the FIFO.
56. If Port B size is word or byte, t_{SKEW2} is referenced to the rising CLKB edge that writes the last word or byte of the long-word, respectively.
57. t_{SKEW2} is the minimum time between a rising CLKB edge and a rising CLKA edge for AEA to transition HIGH in the next CLKA cycle. If the time between the rising CLKB edge and rising CLKA edge is less than t_{SKEW2}, then AEA may transition HIGH one CLKA cycle later than shown.

Switching Waveforms (continued)

Timing for $\overline{AFA}$ when FIFO1 is Almost Full (CY Standard and FWFT Modes)[2, 56, 58, 59]



Timing for $\overline{AFB}$ when FIFO2 is Almost Full (CY Standard and FWFT Modes)[2, 55, 59, 61]

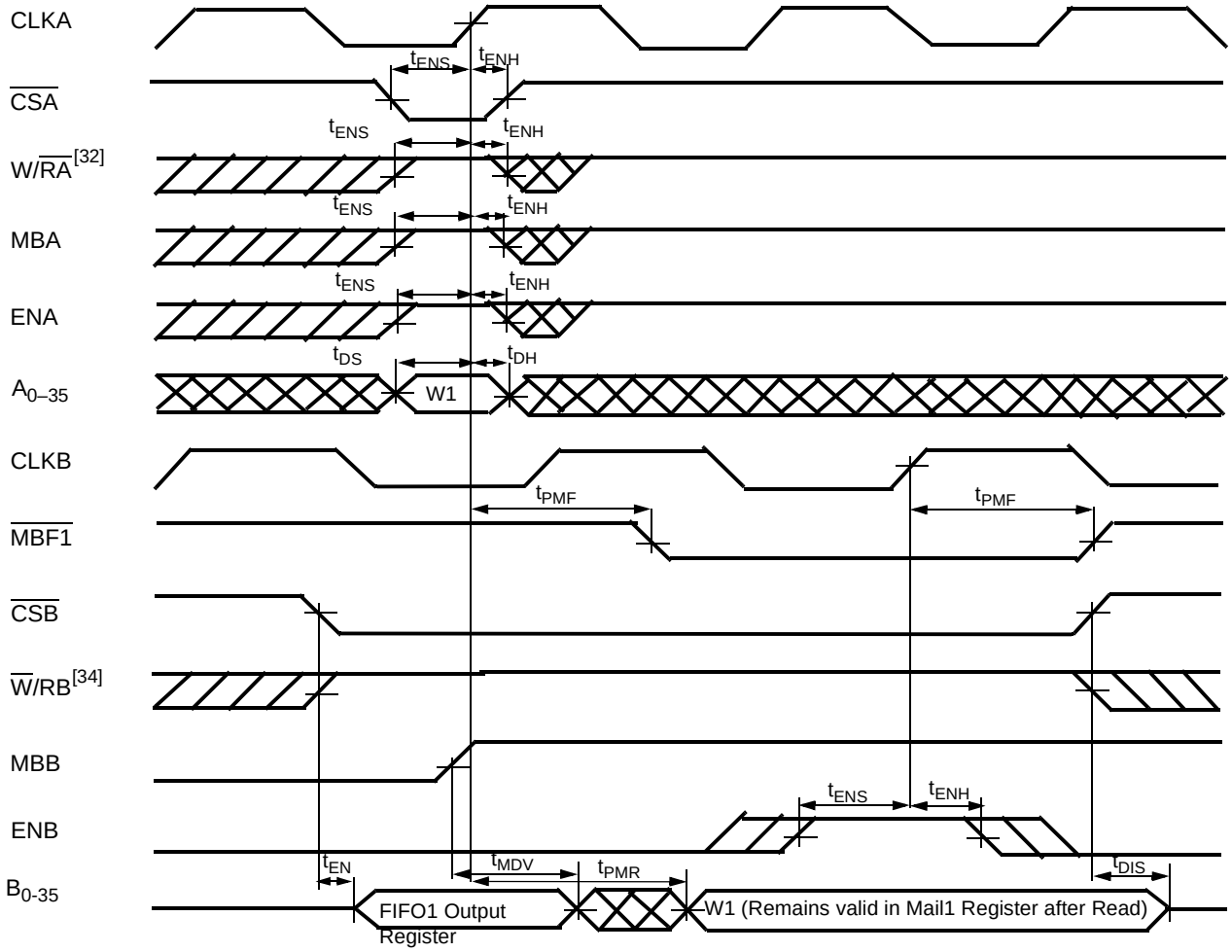


Notes:

58. FIFO1 Write ($\overline{CSA}$ = LOW, W/$\overline{RA}$ = HIGH, MBA = LOW), FIFO1 Read ($\overline{CSB}$ = LOW, $\overline{W}$/RB = HIGH, MBB = LOW). Data in the FIFO1 output register has been Read from the FIFO.
59. D = Maximum FIFO Depth = 1K for the CY7C43644AV, 4K for the CY7C43664AV, and 16K for the CY7C43684AV.
60. t_{SKEW2} is the minimum time between a rising CLKA edge and a rising CLKB edge for $\overline{AFA}$ to transition HIGH in the next CLKA cycle. If the time between the rising CLKA edge and rising CLKB edge is less than t_{SKEW2}, then $\overline{AFA}$ may transition HIGH one CLKB cycle later than shown.
61. If Port B size is word or byte, $\overline{AFB}$ is set LOW by the last word or byte Write of the long-word, respectively.
62. t_{SKEW2} is the minimum time between a rising CLKB edge and a rising CLKA edge for $\overline{AFB}$ to transition HIGH in the next CLKB cycle. If the time between the rising CLKB edge and rising CLKA edge is less than t_{SKEW2}, then $\overline{AFB}$ may transition HIGH one CLKA cycle later than shown.

Switching Waveforms (continued)

Timing for Mail1 Register and $\overline{MBF1}$ Flag (CY Standard and FWFT Modes)[63]

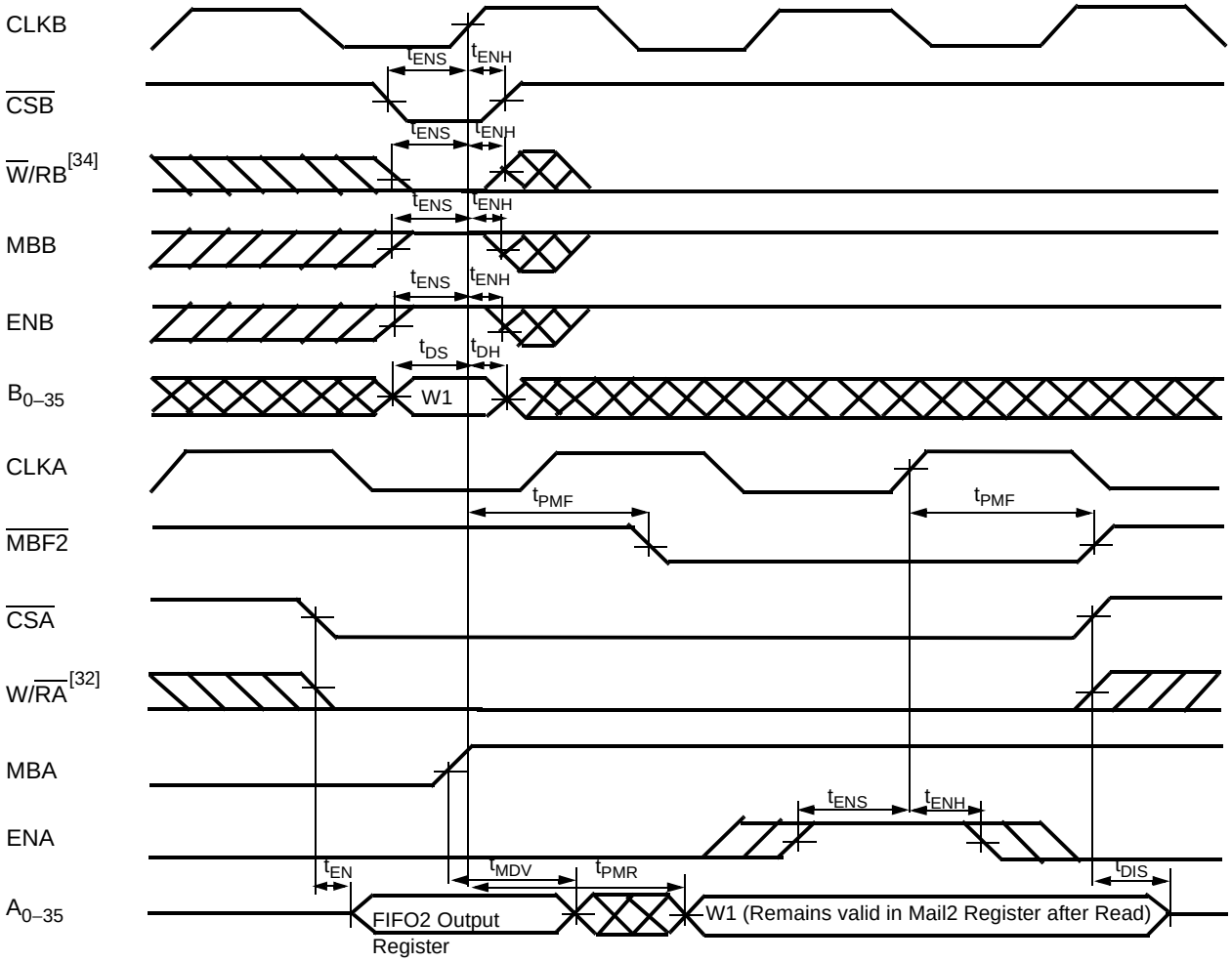


Note:

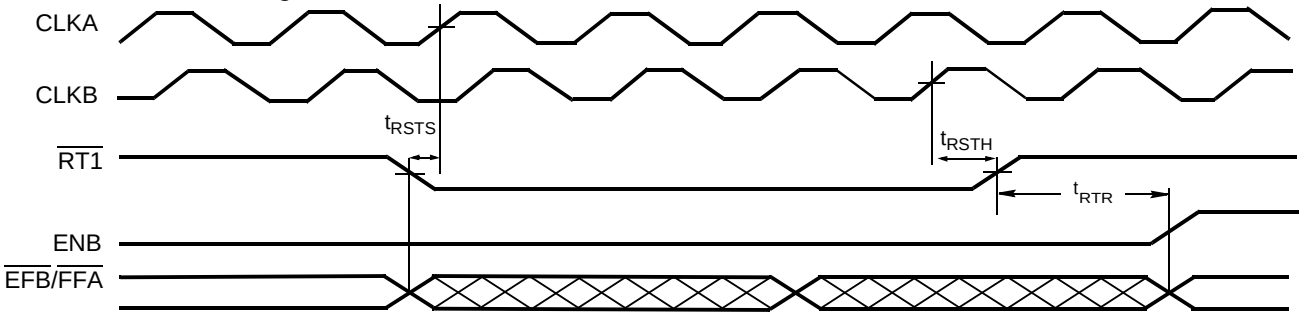
63. If Port B is configured for word size, data can be written to the Mail1 register using $A_{0–17}$ ($A_{18–35}$ are "Don't Care" inputs). In this first case $B_{0–17}$ will have valid data ($B_{18–35}$ will be indeterminate). If Port B is configured for byte size, data can be written to the Mail1 Register using $A_{0–8}$ ($A_{9–35}$ are "Don't Care" inputs). In this second case, $B_{0–8}$ will have valid data ($B_{9–35}$ will be indeterminate).

Switching Waveforms (continued)

Timing for Mail2 Register and $\overline{MBF2}$ Flag (CY Standard and FWFT Modes)[64]



FIFO1 Retransmit Timing [65, 66, 67, 68,69]



Notes:

64. If Port B is configured for word size, data can be written to the Mail2 register using $B_{0–17}$ ($B_{18–35}$ are "Don't Care" inputs). In this first case $A_{0–17}$ will have valid data ($A_{18–35}$ will be indeterminate). If Port B is configured for byte size, data can be written to the Mail2 Register using $B_{0–8}$ ($B_{9–35}$ are "Don't Care" inputs). In this second case, $A_{0–8}$ will have valid data ($A_{9–35}$ will be indeterminate).
65. Retransmit is performed in the same manner for FIFO2.
66. Clocks are free running in this case. CY standard mode only. Write operation should be prohibited one Write clock cycle before the falling edge of $\overline{RT1}$, and during the retransmit operation, i.e, when RT1 is LOW and t_{RTR} after the RT1 rising edge.
67. The Empty and Full flags may change state during Retransmit as a result of the offset of the Read and Write pointers, but the Empty and Full flags will be valid at t_{RTR}.
68. For the $\overline{AEA}$, $\overline{AEB}$, $\overline{AFA}$,and $\overline{AFB}$ flags, two clock cycle are necessary after t_{RTR} to update these flags.
69. The number of 36-/18-/9-bit words written into the FIFO should be less than full depth minus 2/4/8 words between the reset of the FIFO (master or partial) and the Retransmit setup.

Ordering Information

3.3V 1K ×36 ×2 Bidirectional Synchronous FIFO with Bus Matching

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
7	CY7C43644AV–7AC	A128	128-lead Thin Quad Flat Package	Commercial
10	CY7C43644AV–10AC	A128	128-lead Thin Quad Flat Package	Commercial
15	CY7C43644AV–15AC	A128	128-lead Thin Quad Flat Package	Commercial

3.3V 4K ×36 ×2 Bidirectional Synchronous FIFO with Bus Matching

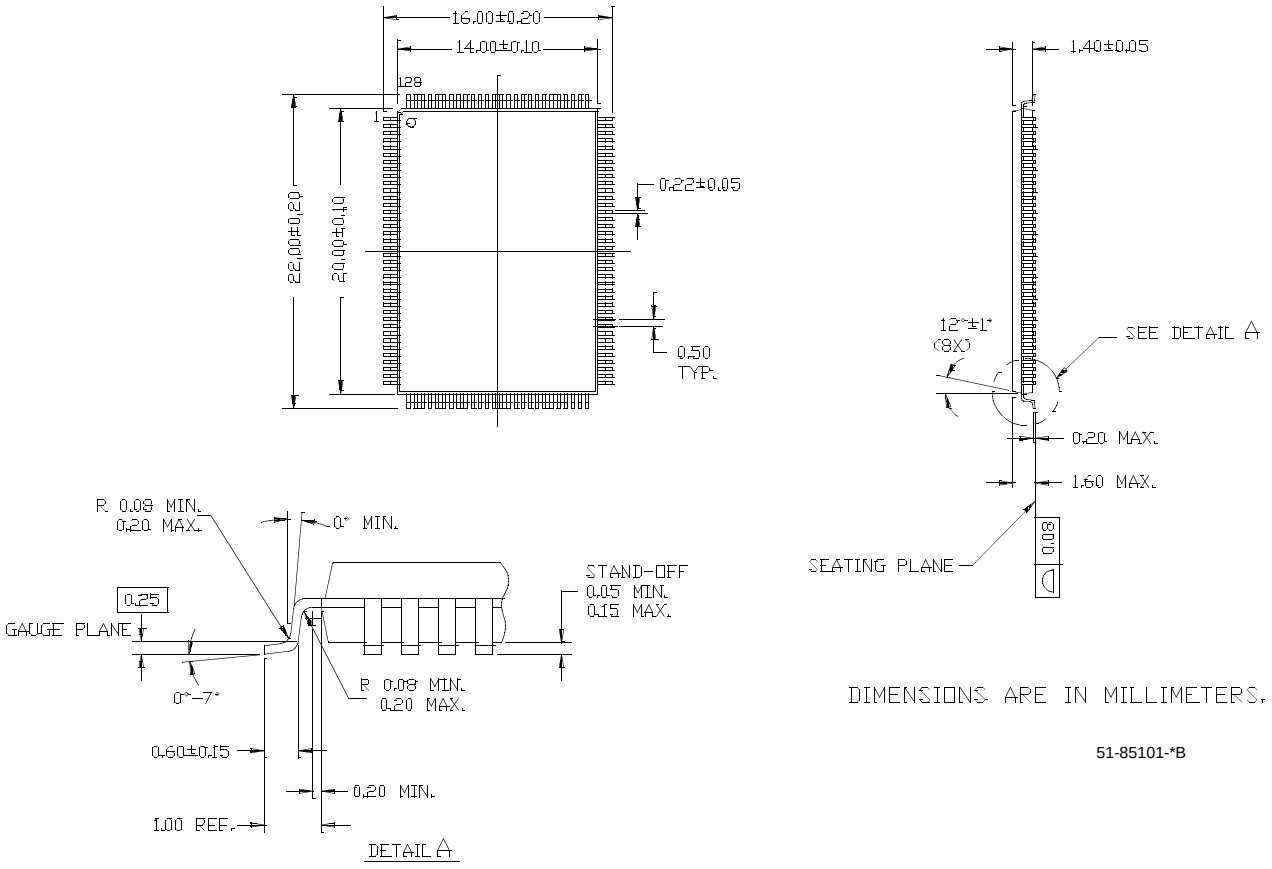
Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
7	CY7C43664AV–7AC	A128	128-lead Thin Quad Flat Package	Commercial
10	CY7C43664AV–10AC	A128	128-lead Thin Quad Flat Package	Commercial
15	CY7C43664AV–15AC	A128	128-lead Thin Quad Flat Package	Commercial

3.3V 16K ×36 ×2 Bidirectional Synchronous FIFO with Bus Matching

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
7	CY7C43684AV–7AC	A128	128-lead Thin Quad Flat Package	Commercial
10	CY7C43684AV–10AC	A128	128-lead Thin Quad Flat Package	Commercial
15	CY7C43684AV–15AC	A128	128-lead Thin Quad Flat Package	Commercial
10	CY7C43684AV–10AI	A128	128-lead Thin Quad Flat Package	Industrial

Package Diagram

128-lead Thin Plastic Quad Flatpack (14 x 20 x 1.4 mm) A128



Document Title: CY7C43644AV/CY7C43664AV/CY7C43684AV 3.3V 1K/4K/16K x36 x2 Bidirectional Synchronous FIFO with Bus Matching Document Number: 38-06025				
REV.	**ECN NO.**	**Issue Date**	**Orig. of Change**	**Description of Change**
**	107506	05/24/01	KTM	Change from Spec #: 38-00777 to 38-06025
*A	109943	02/06/02	FSG	Preliminary to final
*B	117209	08/22/02	OOR	Added footnote to retransmit timing, and added note to retransmit section
*C	122277	12/26/02	RBI	Power up requirements added to Maximum Ratings Information