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NTE4006B
Integrated Circuit
CMOS, 18−Stage Static Shift Register

Description:

The NTE4006B is a shift register in a 14−Lead DIP type package and is comprised of four separate shift register sections sharing a common clock: two sections have four stages, and two sections have five stages with an output tap on both the fourth and fifth stages. This makes it possible to obtain a shift register of 4, 5, 8, 9, 10, 12, 13, 14, 16, 17, or 18 bits by appropriate selection of inputs and outputs. This part is particularly useful in serial shift registers and time delay circuits.

Features:

- Output Transitions Occur on the Falling Edge of the Clock Pulse
- Supply Voltage Range: 3Vdc to 18Vdc
- Can be Cascaded to Provide Longer Shift Register Lengths
- Capable of Driving Two Low−Power TTL Loads or One Low−Power Schottky TTL Load Over the Rated Temperature Range

Absolute Maximum Ratings: (Voltages referenced to V_{SS}, Note 1)

DC Supply Voltage, V_{DD} . . . . −0.5 to +18.0V
Input Voltage (DC or Transient), V_{in} . . . . −0.5 to V_{DD} to +0.5V
Output Voltage (DC or Transient), V_{out} . . . . −0.5 to V_{DD} to +0.5V
Input Current (DC or Transient, Per Pin), I_{in} . . . . ±10mA
Output Current (DC or Transient, Per Pin), I_{out} . . . . ±10mA
Power Dissipation (Per Package), P_D 500mW
Temperature Derating (from +65° to +125°C) . . . . −7.0mW/°C
Storage Temperature, T_{stg} . . . . −65° to +150°C
Lead Temperature (During Soldering, 8sec max), T_L . . . . +260°C

Note 1. Maximum Ratings are those values beyond which damage to the device may occur.

Electrical Characteristics: (Voltages referenced to V_{SS}, Note 2)

Parameter		Symbol	V_{DD} Vdc	–55°C Min	–55°C Max	+25°C Min	+25°C Typ	+25°C Max	+125°C Min	+125°C Max	Unit
Output Voltage	"0" Level	V_{OL}	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
$V_{in} = V_{DD}$ or 0			10	–	0.05	–	0	0.05	–	0.05	Vdc
			15	–	0.05	–	0	0.05	–	0.05	Vdc
	"1" Level	V_{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
$V_{in} = 0$ or V_{DD}			10	9.95	–	9.95	10	–	9.95	–	Vdc
			15	14.95	–	14.95	15	–	14.95	–	Vdc
Input Voltage (V_O = 4.5 or 0.5Vdc)	"0" Level	V_{IL}	5.0	–	1.5	–	2.25	1.5	–	1.5	Vdc
(V_O = 9.0 or 1.0Vdc)			10	–	3.0	–	4.50	3.0	–	3.0	Vdc
(V_O = 13.5 or 1.5Vdc)			15	–	4.0	–	6.75	4.0	–	4.0	Vdc
(V_O = 0.5 or 4.5Vdc)	"1" Level	V_{IH}	5.0	3.5	–	3.5	2.75	–	3.5	–	Vdc
(V_O = 1.0 or 9.0Vdc)			10	7.0	–	7.0	5.50	–	7.0	–	Vdc
(V_O = 1.5 or 13.5Vdc)			15	11.0	–	11.0	8.25	–	11.0	–	Vdc
Output Drive Current (V_{OH} = 2.5Vdc)	Source	I_{OH}	5.0	–3.0	–	–2.4	–4.2	–	–1.7	–	mAdc
(V_{OH} = 4.6Vdc)			5.0	–0.64	–	–0.51	–0.88	–	–0.36	–	mAdc
(V_{OH} = 9.5Vdc)			10	–1.6	–	–1.3	–2.25	–	–0.9	–	mAdc
(V_{OH} = 13.5Vdc)			15	–4.2	–	–3.4	–8.8	–	–2.4	–	mAdc
(V_{OL} = 0.4Vdc)	Sink	I_{OL}	5.0	0.64	–	0.51	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5Vdc)			10	1.6	–	1.3	2.25	–	0.9	–	mAdc
(V_{OL} = 1.5Vdc)			15	4.2	–	3.4	8.8	–	2.4	–	mAdc
Input Current		I_{in}	15	–	±0.1	–	±0.00001	±0.1	–	±0.1	µAdc
Input Capacitance (V_{IN} = 0)		C_{in}	–	–	–	–	5.0	7.5	–	–	pF
Quiescent Current (Per Package)		I_{DD}	5.0	–	5.0	–	0.005	5.0	–	150	µAdc
			10	–	10	–	0.010	10	–	300	µAdc
			15	–	20	–	0.015	20	–	600	µAdc
Total Supply Current (Dynamic plus Quiescent, Per Package, C_L = 50pF on all buffers switching Note 3, Note 4)		I_T	5.0	I_T = (1.3µA/kHz) f + I_{DD}							µAdc
			10	I_T = (2.6µA/kHz) f + I_{DD}							µAdc
			15	I_T = (3.9µA/kHz) f + I_{DD}							µAdc

Note 2. Data labeled "Typ" is not to be used for design purposes but is intended as an indication of the device's potential performance.

Note 3. The formulas given are for the typical characteristics only at +25°C.

Note 4. To calculate total supply current at loads other than 50pF:

$$I_T(C_L) = I_T(50pF) + (C_L - 50)\, V_{fk}$$

where: I_T is in µA (per package), C_L in pF, $V = (V_{DD} - V_{SS})$ in volts, f in kHz is input frequency, and k = 0.001.

Switching Characteristics: (C_L = 50pF, T_A = +25°C, Note 2)

Parameter	Symbol	V_{DD} Vdc	Min	Typ	Max	Unit
Output Rise and Fall Time t_{TLH}, t_{THL} = (1.5ns/pf) C_L + 33ns	t_{TLH}, t_{THL}	5.0	–	100	200	ns
T_{TLH}, t_{THL} = (0.75ns/pf) C_L + 12.5ns		10	–	50	100	ns
T_{TLH}, t_{THL} = (0.55ns/pf) C_L + 9.5ns		15	–	40	80	ns
Propagation Delay Time t_{PLH}, t_{PHL} = (1.7ns/pf) C_L + 220ns	t_{PLH}· t_{PHL}	5.0	–	300	600	ns
t_{PLH}, t_{PHL} = (0.66ns/pf) C_L + 77ns		10	–	110	220	ns
t_{PLH}, t_{PHL} = (0.5ns/pf) C_L + 55ns		15	–	80	160	ns
Clock Pulse Width	t_{WH}	5.0	200	100	–	ns
		10	120	60	–	ns
		15	80	40	–	ns
Clock Pulse Frequency	f_{cl}	5.0	–	5.0	2.5	MHz
		10	–	8.3	4.2	MHz
		15	–	12	6.0	MHz
Clock Pulse Rise and Fall Time (Note 5)	t_{TLH}, t_{THL}	5.0	–	–	15	µs
		10	–	–	5	µs
		15	–	–	4	µs
Setup Time	t_{su}	5.0	0	–50	–	ns
		10	0	–15	–	ns
		15	0	–8.0	–	ns
Hold Time	t_h	5.0	180	75	–	ns
		10	90	25	–	ns
		15	75	20	–	ns

Note 2. Data labeled "Typ" is not to be used for design purposes but is intended as an indication of the device's potential performance.

Note 3. The formulas given are for the typical characteristics only at +25°C.

Note 5. When shift register sections are cascaded, the maximum rise and fall times of the clock input should be equal to or less than the rise and fall times of the data outputs driving data inputs, plus the propagation delay of the output driving stage for the output capacitance load.

Truth Table (Single Stage):

D_n	C	Q_{n+1}
0	$\searrow$	0
1	$\searrow$	1
X	$\nearrow$	Q_n

X = Don't Care

Pin Connection Diagram