



80960CA-33, -25, -16

32-BIT HIGH-PERFORMANCE EMBEDDED PROCESSOR

- *Two Instructions/Clock Sustained Execution*
- *Four 59 Mbytes/s DMA Channels with Data Chaining*
- *Demultiplexed 32-bit Burst Bus with Pipelining*

- **32-bit Parallel Architecture**
 - Two Instructions/clock Execution
 - Load/Store Architecture
 - Sixteen 32-bit Global Registers
 - Sixteen 32-bit Local Registers
 - Manipulates 64-bit Bit Fields
 - 11 Addressing Modes
 - Full Parallel Fault Model
 - Supervisor Protection Model
 - **Fast Procedure Call/Return Model**
 - Full Procedure Call in 4 Cycles
 - **On-Chip Register Cache**
 - Caches Registers on Call/Ret
 - Minimum of 6 Frames Provided
 - Up to 15 Programmable Frames
 - **On-Chip Instruction Cache**
 - 1 Kbyte Two-Way Set Associative
 - 128-bit Path to Instruction Sequencer
 - Cache-Lock Modes
 - Cache-Off Mode
 - **High Bandwidth On-Chip Data RAM**
 - 1 Kbyte On-Chip Data RAM
 - Sustains 128 bits per Clock Access
 - **Four On-Chip DMA Channels**
 - 59 Mbytes/s Fly-by Transfers
 - 32 Mbytes/s Two-Cycle Transfers
 - Data Chaining
 - Data Packing/Unpacking
 - Programmable Priority Method
 - **32-Bit Demultiplexed Burst Bus**
 - 128-bit Internal Data Paths to and from Registers
 - Burst Bus for DRAM Interfacing
 - Address Pipelining Option
 - Fully Programmable Wait States
 - Supports 8-, 16- or 32-bit Bus Widths
 - Supports Unaligned Accesses
 - Supervisor Protection Pin
 - **Selectable Big or Little Endian Byte Ordering**
 - **High-Speed Interrupt Controller**
 - Up to 248 External Interrupts
 - 32 Fully Programmable Priorities
 - Multi-mode 8-bit Interrupt Port
 - Four Internal DMA Interrupts
 - Separate, Non-maskable Interrupt Pin
 - Context Switch in 750 ns Typical
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