19-0509; Rev 0; 4/06

Stereo 3W Audio Power Amplifiers with Headphone Drive and Input Mux

General Description

The MAX9777/MAX9778 combine a stereo 3W bridge-tied load (BTL) audio power amplifier, stereo single-ended (SE) headphone amplifier, headphone sensing, and a 2:1 input multiplexer all in a tiny 28-pin thin QFN package. These devices operate from a single 4.5V to 5.5V supply and feature an industry-leading 100dB PSRR, allowing these devices to operate from noisy supplies without the addition of a linear regulator. An ultra-low 0.002% THD+N ensures clean, low-distortion amplification of the audio signal. Click-and-pop suppression minimizes audible transients on power and shutdown cycles. Power-saving features include low 4mV V_{OS} (minimizes DC current drain through the speakers), low 13mA supply current, and a 10µA shutdown mode. A MUTE function allows the outputs to be quickly enabled or disabled.

A headphone sense input detects the presence of a headphone jack and automatically configures the amplifiers for either speaker or headphone mode. In speaker mode, the amplifiers can deliver up to 3W of continuous average power into a 3Ω load. In headphone mode, the amplifier can deliver up to 200mW of continuous average power into a 16Ω load. The gain of the amplifiers is externally set, allowing maximum flexibility in optimizing output levels for a given load. The amplifiers also feature a 2:1 input multiplexer, allowing multiple audio sources to be selected. The multiplexer can also be used to compensate for limitations in the frequency response of the loud speakers by selecting an external equalizer network. The various functions are controlled by either an I²C-compatible (MAX9777) or simple parallel control interface (MAX9778).

The MAX9777/MAX9778 are available in a thermally efficient 28-pin thin QFN package (5mm x 5mm x 0.8mm). These devices have thermal-overload protection (OVP) and are specified over the extended -40°C to +85°C temperature range.

Applications

Notebooks	PC Audio Peripherals
Portable DVD Players	Camcorders
Tablet PCs	Multimedia Monitor

Features

- **Industry-Leading, Ultra-High 100dB PSRR**
- **3W BTL Stereo Speaker Amplifier**
- **200mW Stereo Headphone Amplifier**
- **Low 0.002% THD+N**
- **Click-and-Pop Suppression**
- **ESD-Protected Outputs**
- **Low Quiescent Current: 13mA**
- **Low-Power Shutdown Mode: 10µA**
- **MUTE Function**
- **Headphone Sense Input**
- **Stereo 2:1 Input Multiplexer**
- **Optional 2-Wire, I²C-Compatible or Parallel Interface**
- **Tiny 28-Pin Thin QFN (5mm x 5mm x 0.8mm) Package**

Ordering Information

PART	CONTROL INTERFACE	PIN-PACKAGE	PKG CODE
MAX9777ETI+	I²C Compatible	28 Thin QFN-EP*	T2855-6
MAX9778ETI+	Parallel	28 Thin QFN-EP*	T2855-6

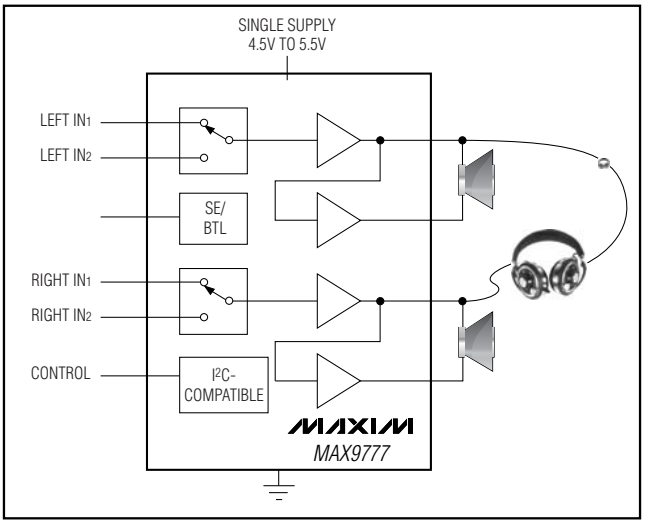
Note: All devices are specified over the -40°C to +85°C operating temperature range.

+Denotes lead-free package.

**EP = Exposed paddle.*

Pin Configurations and Functional Diagrams appear at end of data sheet.

Simplified Block Diagram



Stereo 3W Audio Power Amplifiers with Headphone Drive and Input Mux

ABSOLUTE MAXIMUM RATINGS

V_{DD} to GND .....+6V
PV_{DD} to V_{DD} .....±0.3V
PGND to GND.....±0.3V
All Other Pins to GND.....-0.3V to (V_{DD} + 0.3V)
Continuous Input Current (into any pin except power-supply and output pins) .....±20mA
OUT__ Short Circuit to GND, V_{DD} 10s
Short Circuit Between OUT_+ and OUT_- .....Continuous

Continuous Power Dissipation (T_A = +70°C)
28-Pin TQFN, Multilayer Board
(derate 34.5mW/°C above +70°C).....2758.6mW
Operating Temperature Range .....-40°C to +85°C
Storage Temperature Range .....-65°C to +150°C
Junction Temperature.....+150°C
Lead Temperature (soldering, 10s) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{DD} = PV_{DD} = 5.0V, GND = PGND = 0V, $V_{\overline{SHDN}}$ = 5V, C_{BIAS} = 1µF, R_{IN} = R_F = 15kΩ, R_L = ∞. T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Supply Voltage Range	V_{DD}/PV_{DD}	Inferred from PSRR test		4.5		5.5	V
Quiescent Supply Current (I_{VDD} + I_{PVDD})	I_{DD}	BTL mode, HPS = 0V, MAX9777/MAX9778			13	32	mA
		Single-ended mode, HPS = V_{DD}			7	18	
Shutdown Current	$I_{\overline{SHDN}}$	$\overline{SHDN}$ = GND			10	50	µA
Switching Time	t_{SW}	Gain or input switching			10		µs
Turn-On Time	t_{ON}	C_{BIAS} = 1µF			300		ms
		C_{BIAS} = 0.1µF			30		
Thermal Shutdown Threshold					+160		°C
Thermal Shutdown Hysteresis					15		°C
OUTPUT AMPLIFIERS (SPEAKER MODE, HPS = GND)							
Output Offset Voltage	V_{OS}	OUT_+ - OUT_-, A_V = 1V/V			±4	±32	mV
Power-Supply Rejection Ratio (Note 2)	PSRR	V_{DD} = 4.5V to 5.5V		75	100		dB
		f = 1kHz, V_{RIPPLE} = 200mV_{P-P}			82		
		f = 20kHz, V_{RIPPLE} = 200mV_{P-P}			70		
Output Power	P_{OUT}	f_{IN} = 1kHz, THD+N < 1%, T_A = +25°C	R_L = 8Ω		1.4		W
			R_L = 4Ω		2.6		
			R_L = 3Ω		3		
Total Harmonic Distortion Plus Noise	THD+N	f_{IN} = 1kHz, BW = 22Hz to 22kHz	P_{OUT} = 1W, R_L = 8Ω		0.005		%
			P_{OUT} = 2W, R_L = 4Ω		0.01		
Signal-to-Noise Ratio	SNR	R_L = 8Ω, P_{OUT} = 1W, BW = 22Hz to 22kHz			95		dB
Slew Rate	SR				1.6		V/µs
Maximum Capacitive Load Drive	C_L	No sustained oscillations			1		nF
Crosstalk		f_{IN} = 10kHz			73		dB
Click/Pop Level	K_{CP}	Peak voltage, A-weighted, 32 samples per second (Notes 2, 6)	Into shutdown		-50		dBV
			Out of shutdown		-65		

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = PV_{DD} = 5.0V, GND = PGND = 0V, $V_{\overline{SHDN}}$ = 5V, C_{BIAS} = 1µF, R_{IN} = R_F = 15kΩ, R_L = ∞. T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
OUTPUT AMPLIFIERS (HEADPHONE MODE, HPS = V_{DD})							
Power-Supply Rejection Ratio (Note 2)	PSRR	V_{DD} = 4.5V to 5.5V		75	106		dB
		f = 1kHz, V_{RIPPLE} = 200mV_{P-P}			88		
		f = 20kHz, V_{RIPPLE} = 200mV_{P-P}			76		
Output Power	P_{OUT}	f_{IN} = 1kHz, THD+N < 1%, T_A = +25°C	R_L = 32Ω		88		mW
			R_L = 16Ω		200		
Total Harmonic Distortion Plus Noise	THD+N	f_{IN} = 1kHz, BW = 22Hz to 22kHz	P_{OUT} = 60mW, R_L = 32Ω		0.002		%
			P_{OUT} = 125mW, R_L = 16Ω		0.002		
Signal-to-Noise Ratio	SNR	R_L = 32Ω, BW = 22Hz to 22kHz, V_{OUT} = 1V_{RMS}			92		dB
Slew Rate	SR				1.8		V/µs
Maximum Capacitive Load Drive	C_L	No sustained oscillations			2		nF
Crosstalk		f_{IN} = 10kHz			78		dB
BIAS VOLTAGE (BIAS)							
BIAS Voltage	V_{BIAS}			2.35	2.5	2.65	V
Output Resistance	R_{BIAS}				50		kΩ
DIGITAL INPUTS (MUTE, $\overline{SHDN}$, HPS_EN, GAIN$\overline{A}$/B, IN$\overline{1}$/2)							
Input-Voltage High	V_{IH}			2			V
Input-Voltage Low	V_{IL}					0.8	V
Input Leakage Current	I_{IN}					±1	µA
HEADPHONE SENSE INPUT (HPS)							
Input-Voltage High	V_{IH}			0.9 x V_{DD}			V
Input-Voltage Low	V_{IL}					0.7 x V_{DD}	V
Input Leakage Current	I_{IN}					±1	µA
Click/Pop Level	K_{CP}	Peak voltage, A-weighted, 32 samples per second (Notes 2, 4)	Into shutdown		-70		dBV
			Out of shutdown		-52		

Stereo 3W Audio Power Amplifiers with Headphone Drive and Input Mux

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = PV_{DD} = 5.0V, GND = PGND = 0V, $V_{\overline{SHDN}}$ = 5V, C_{BIAS} = 1µF, R_{IN} = R_F = 15kΩ, R_L = ∞. T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
2-WIRE SERIAL INTERFACE (SCL, SDA, ADD, $\overline{INT}$) (MAX9777)						
Input-Voltage High	V_{IH}		2.6			V
Input-Voltage Low	V_{IL}				0.8	V
Input Hysteresis				0.2		V
Input High Leakage Current	I_{IH}	V_{IN} = 5V			±1	µA
Input Low Leakage Current	I_{IL}	V_{IN} = 0V			±1	µA
Input Capacitance	C_{IN}			10		pF
Output-Voltage Low	V_{OL}	I_{OL} = 3mA			0.4	V
Output Current High	I_{OH}	V_{OH} = 5V			1	µA
TIMING CHARACTERISTICS (MAX9777)						
Serial Clock Frequency	f_{SCL}				400	kHz
Bus Free Time Between STOP and START Conditions	t_{BUF}		1.3			µs
START Condition Hold Time	$t_{HD:STA}$		0.6			µs
START Condition Setup Time	$t_{SU:STA}$		0.6			µs
Clock Period Low	t_{LOW}		1.3			µs
Clock Period High	t_{HIGH}		0.6			µs
Data Setup Time	$t_{SU:DAT}$		100			ns
Data Hold Time	$t_{HD:DAT}$	(Note 3)	0		0.9	µs
Receive SCL/SDA Rise Time	t_r	(Note 4)	20 + 0.1C_B		300	ns
Receive SCL/SDA Fall Time	t_f	(Note 4)	20 + 0.1C_B		300	ns
Transmit SDA Fall Time	t_f	(Note 4)	20 + 0.1C_B		250	ns
Pulse Width of Suppressed Spike	t_{SP}	(Note 5)		50		ns

Note 1: All devices are 100% production tested at +25°C. All temperature limits are guaranteed by design.

Note 2: Inputs AC-coupled to GND.

Note 3: A master device must provide a hold time of at least 300ns for the SDA signal to bridge the undefined region of SCL's falling edge.

Note 4: C_B = total capacitance of one of the bus lines in picofarads. Device tested with C_B = 400pF. 1kΩ pullup resistors connected from SDA/SCL to V_{DD}.

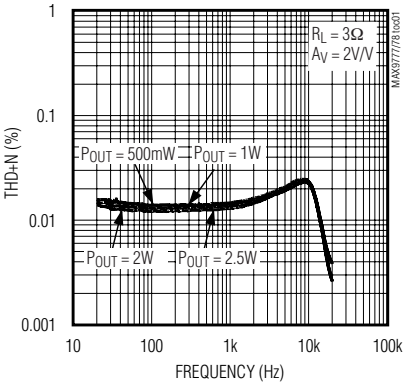
Note 5: Input filters on SDA, SCL, and ADD suppress noise spikes of less than 50ns.

Note 6: Headphone mode testing performed with 32Ω resistive load connected to GND. Speaker mode testing performed with 8Ω resistive load connected to GND. Mode transitions are controlled by $\overline{SHDN}$. KCP level is calculated as 20log[(peak voltage during mode transition, no input signal)/1V_{RMS}]. Units are expressed in dBV.

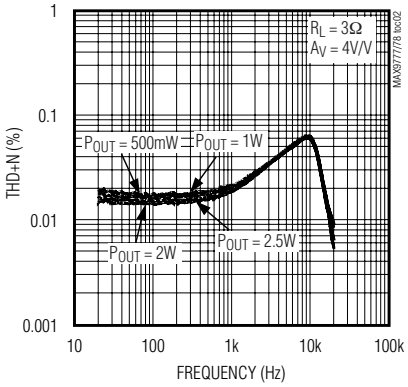
Typical Operating Characteristics

(V_{DD} = PV_{DD} = 5V, GND = PGND = 0V, $V_{\overline{SHDN}}$ = 5V, C_{BIAS} = 1µF, T_A = +25°C, unless otherwise noted.)

TOTAL HARMONIC DISTORTION PLUS NOISE vs. FREQUENCY (SPEAKER MODE)



TOTAL HARMONIC DISTORTION PLUS NOISE vs. FREQUENCY (SPEAKER MODE)



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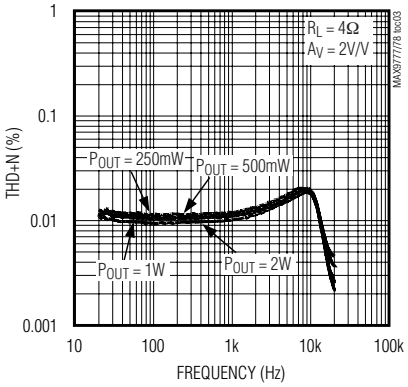

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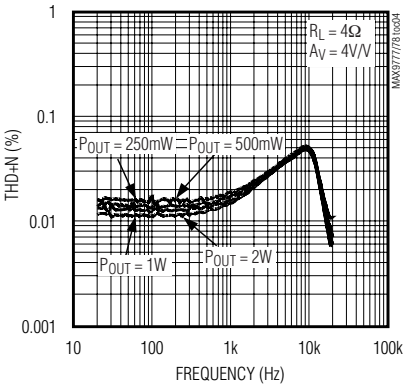

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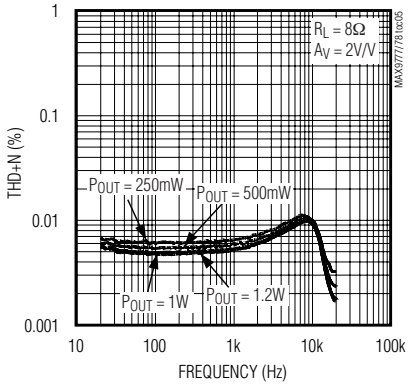

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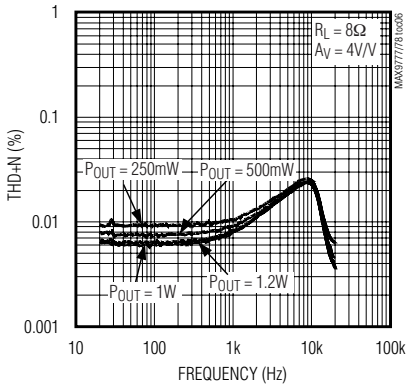
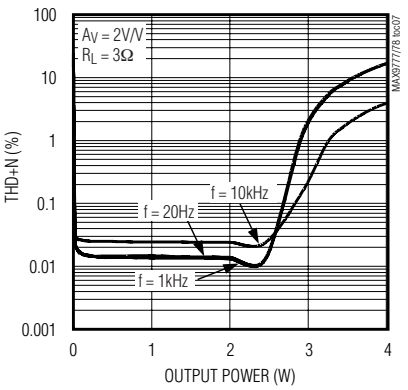


TOTAL HARMONIC DISTORTION PLUS NOISE vs. OUTPUT POWER (SPEAKER MODE)



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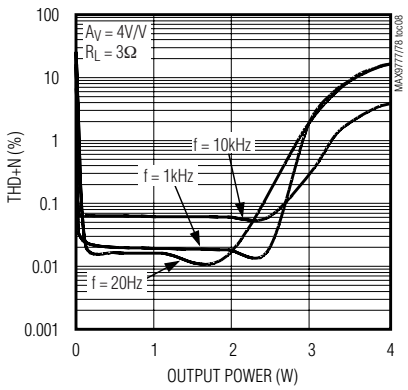

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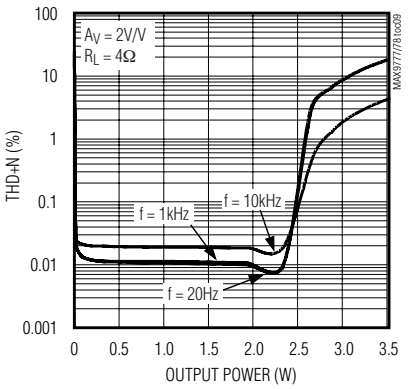
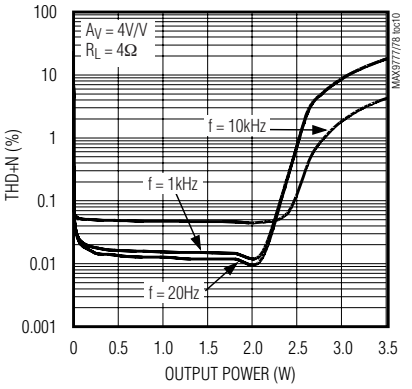


Stereo 3W Audio Power Amplifiers with Headphone Drive and Input Mux

Typical Operating Characteristics (continued)

(V_{DD} = PV_{DD} = 5V, GND = PGND = 0V, $V_{\overline{SHDN}}$ = 5V, C_{BIAS} = 1µF, T_A = +25°C, unless otherwise noted.)

TOTAL HARMONIC DISTORTION PLUS NOISE vs. OUTPUT POWER (SPEAKER MODE)



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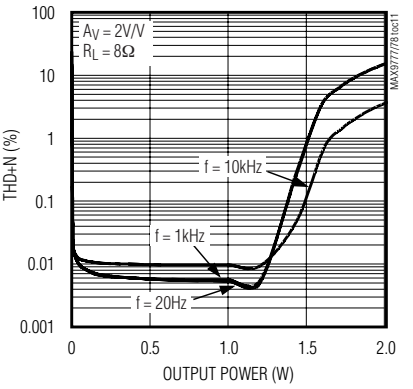
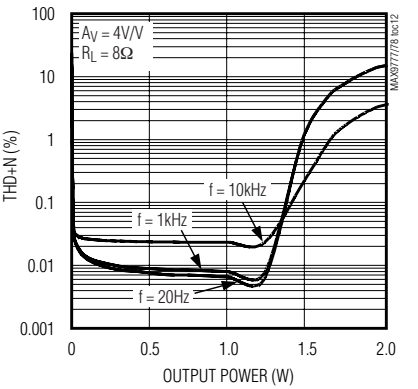
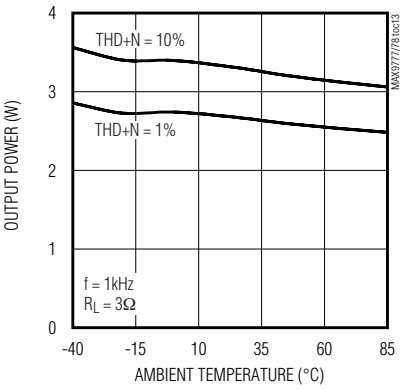


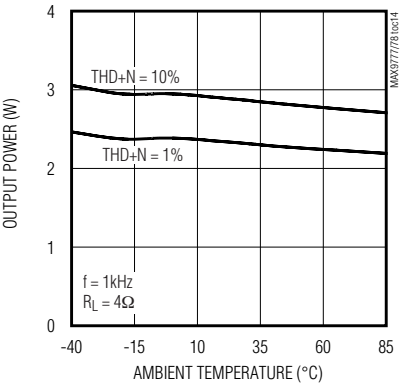
TOTAL HARMONIC DISTORTION PLUS NOISE vs. OUTPUT POWER (SPEAKER MODE)



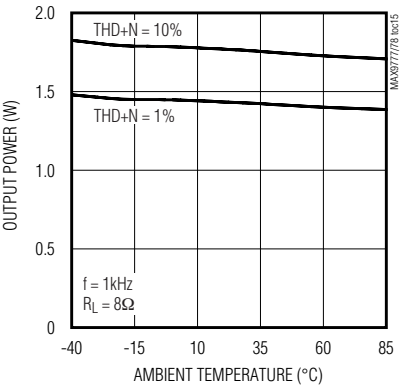
OUTPUT POWER vs. AMBIENT TEMPERATURE (SPEAKER MODE)



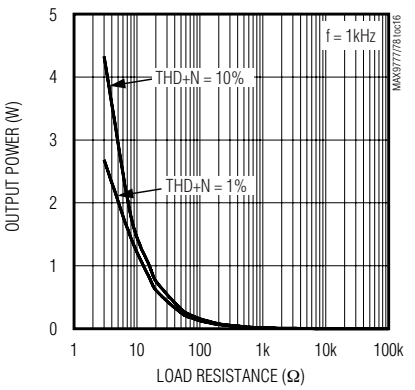
OUTPUT POWER vs. AMBIENT TEMPERATURE (SPEAKER MODE)



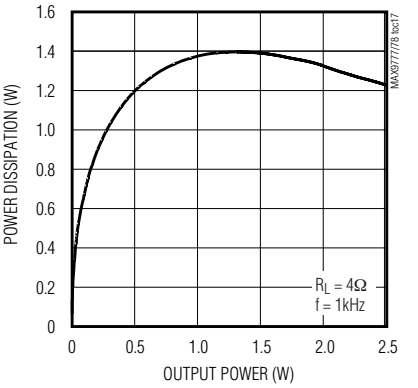
OUTPUT POWER vs. AMBIENT TEMPERATURE (SPEAKER MODE)



OUTPUT POWER vs. LOAD RESISTANCE (SPEAKER MODE)



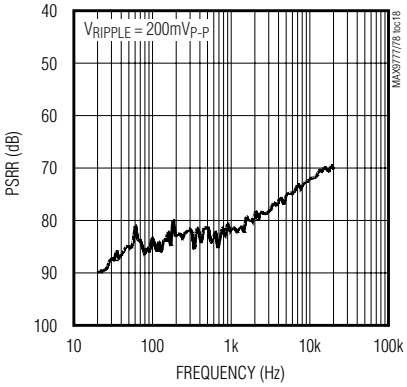
POWER DISSIPATION vs. OUTPUT POWER (SPEAKER MODE)



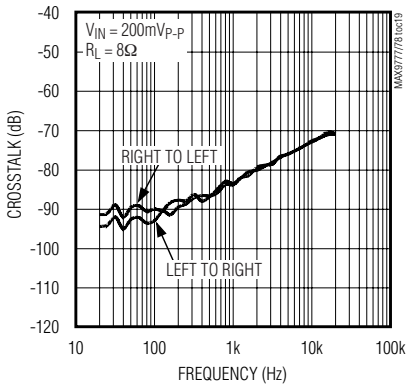
Typical Operating Characteristics (continued)

(V_{DD} = PV_{DD} = 5V, GND = PGND = 0V, $V_{\overline{SHDN}}$ = 5V, C_{BIAS} = 1µF, T_A = +25°C, unless otherwise noted.)

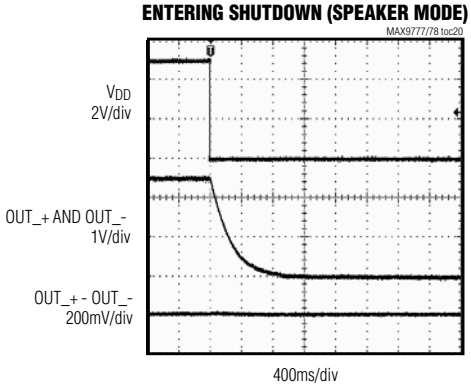
POWER-SUPPLY REJECTION RATIO vs. FREQUENCY (SPEAKER MODE)



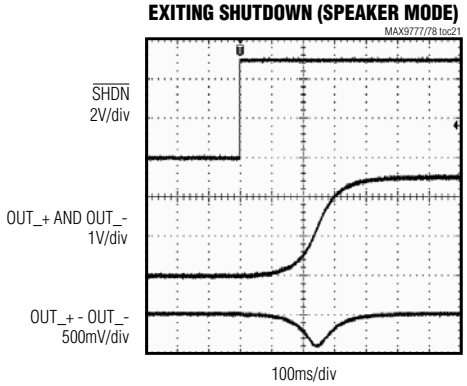
CROSSTALK vs. FREQUENCY (SPEAKER MODE)



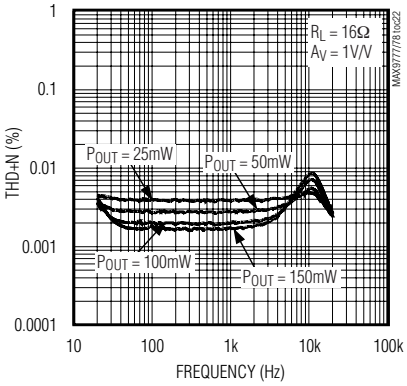
ENTERING SHUTDOWN (SPEAKER MODE)



EXITING SHUTDOWN (SPEAKER MODE)



TOTAL HARMONIC DISTORTION PLUS NOISE vs. FREQUENCY (HEADPHONE MODE)



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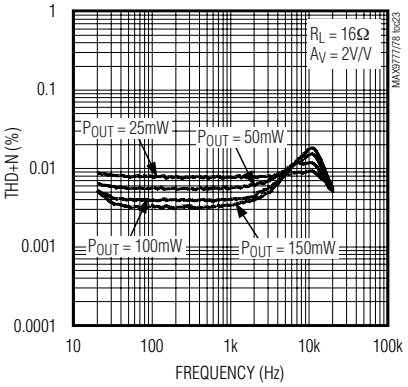

Stereo 3W Audio Power Amplifiers with Headphone Drive and Input Mux

Typical Operating Characteristics (continued)

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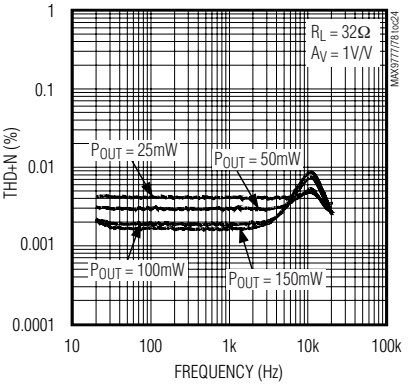

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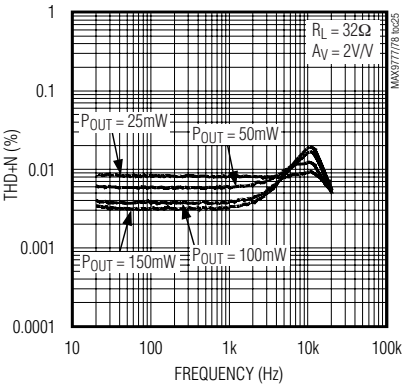
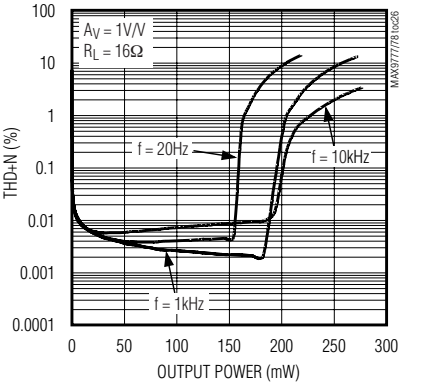
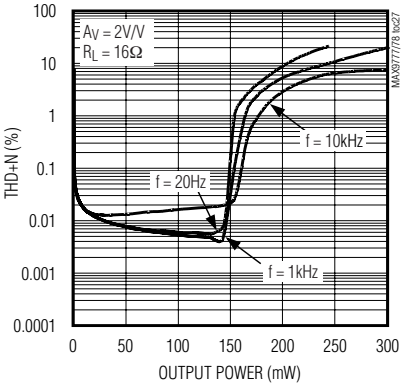


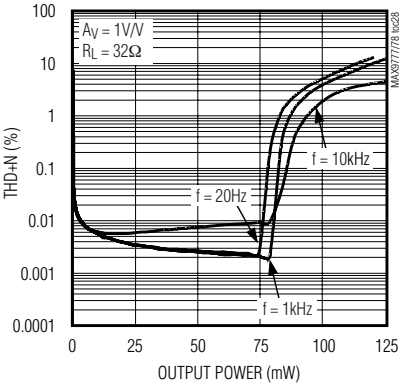
TOTAL HARMONIC DISTORTION PLUS NOISE vs. OUTPUT POWER (HEADPHONE MODE)



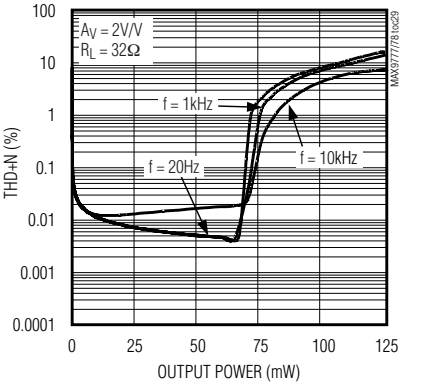
TOTAL HARMONIC DISTORTION PLUS NOISE vs. OUTPUT POWER (HEADPHONE MODE)



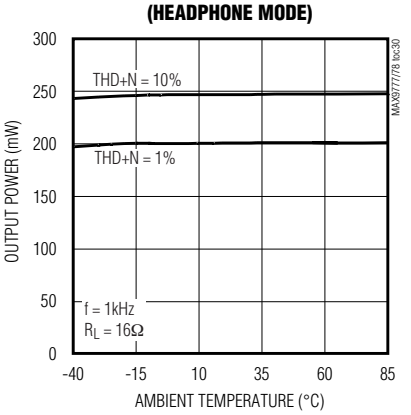
TOTAL HARMONIC DISTORTION PLUS NOISE vs. OUTPUT POWER (HEADPHONE MODE)



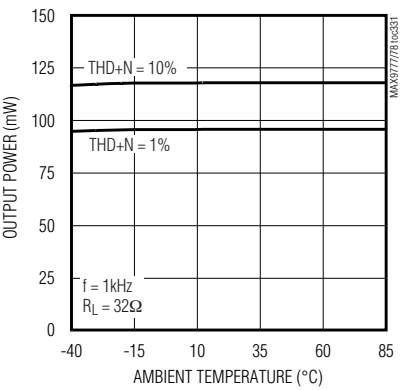
TOTAL HARMONIC DISTORTION PLUS NOISE vs. OUTPUT POWER (HEADPHONE MODE)



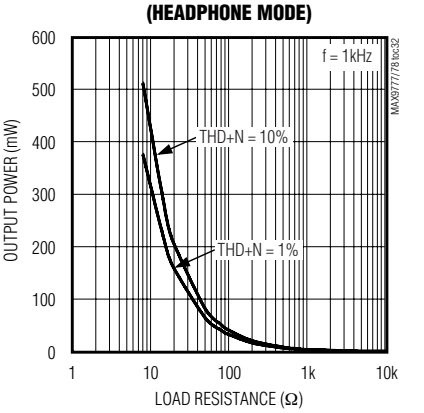
OUTPUT POWER vs. AMBIENT TEMPERATURE (HEADPHONE MODE)



OUTPUT POWER vs. AMBIENT TEMPERATURE (HEADPHONE MODE)



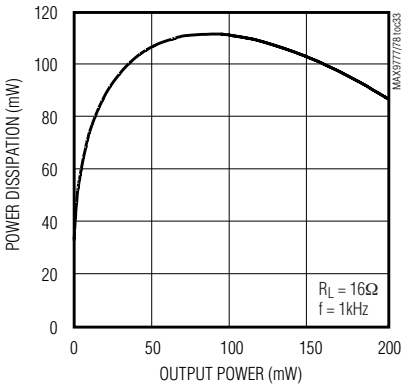
OUTPUT POWER vs. LOAD RESISTANCE (HEADPHONE MODE)



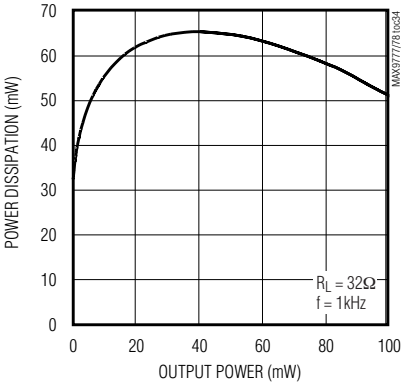
Typical Operating Characteristics (continued)

(V_{DD} = PV_{DD} = 5V, GND = PGND = 0V, $V_{\overline{SHDN}}$ = 5V, C_{BIAS} = 1µF, T_A = +25°C, unless otherwise noted.)

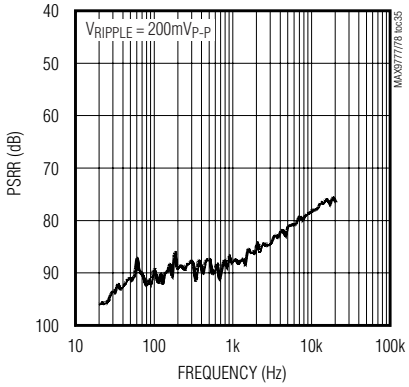
POWER DISSIPATION vs. OUTPUT POWER (HEADPHONE MODE)



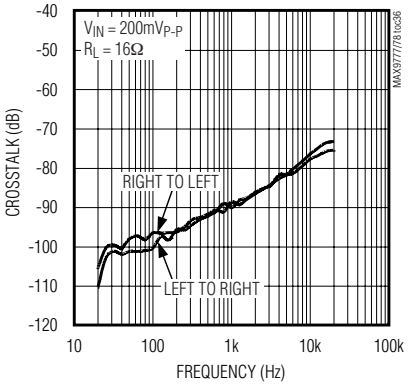
POWER DISSIPATION vs. OUTPUT POWER (HEADPHONE MODE)



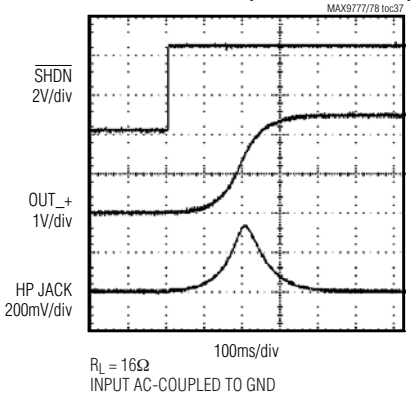
POWER-SUPPLY REJECTION RATIO vs. FREQUENCY (HEADPHONE MODE)



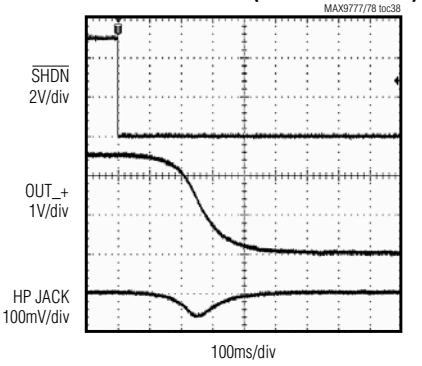
CROSSTALK vs. FREQUENCY (HEADPHONE MODE)



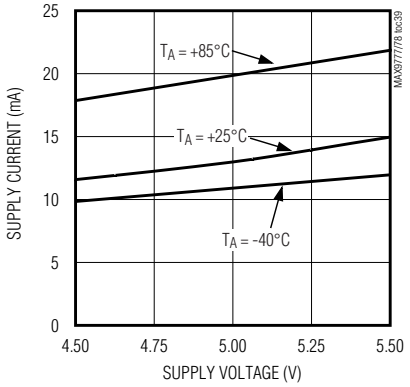
EXITING SHUTDOWN (HEADPHONE MODE)



ENTERING SHUTDOWN (HEADPHONE MODE)



SUPPLY CURRENT vs. SUPPLY VOLTAGE (SPEAKER MODE)

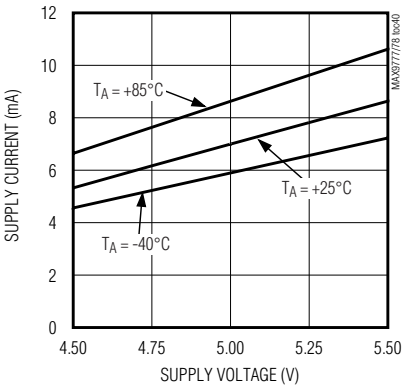


Stereo 3W Audio Power Amplifiers with Headphone Drive and Input Mux

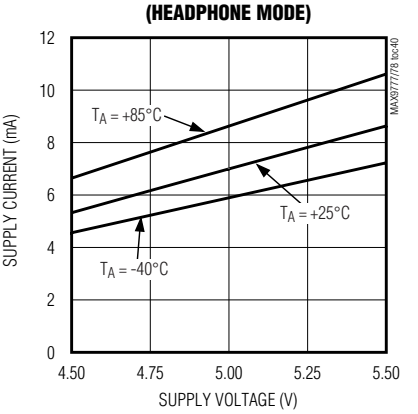
Typical Operating Characteristics (continued)

(V_{DD} = PV_{DD} = 5V, GND = PGND = 0V, $V_{\overline{SHDN}}$ = 5V, C_{BIAS} = 1µF, T_A = +25°C, unless otherwise noted.)

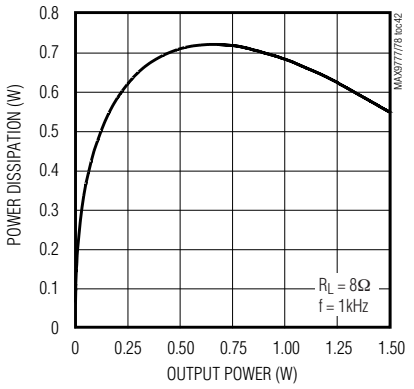
SUPPLY CURRENT vs. SUPPLY VOLTAGE (HEADPHONE MODE)



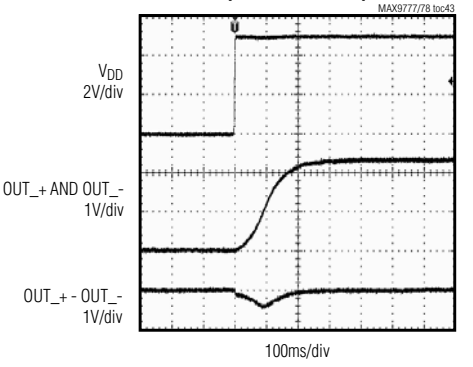
SUPPLY CURRENT vs. SUPPLY VOLTAGE (HEADPHONE MODE)



POWER DISSIPATION vs. OUTPUT POWER (SPEAKER MODE)



EXITING POWER-DOWN (SPEAKER MODE)



Pin Description

PIN		NAME	FUNCTION
MAX9777	MAX9778		
1	—	SDA	Serial Data I/O
2	—	$\overline{INT}$	Interrupt Output
3, 4	3, 4	V_{DD}	Power-Supply Input
5	5	INL1	Left-Channel Input 1
6	6	INL2	Left-Channel Input 2
7	7	GAINLA	Left-Channel Gain Set A
8	8	GAINLB	Left-Channel Gain Set B
9, 13, 23, 27	9, 13, 23, 27	PGND	Power Ground. Connect to GND.
10	10	OUTL+	Left-Channel Bridged Amplifier Positive Output. OUTL+ also serves as the left-channel headphone amplifier output.
11, 25	11, 25	PV_{DD}	Output Amplifier Power Supply
12	12	OUTL-	Left-Channel Bridged Amplifier Negative Output
14	14	$\overline{SHDN}$	Active-Low Shutdown Input. Connect $\overline{SHDN}$ to V_{DD} for normal operation.
15	—	ADD	Address Select. A logic-high sets the address LSB to 1, a logic-low sets the address LSB to zero.
16	16	HPS	Headphone Sense Input. A logic-high configures the device as a single-ended headphone amp. A logic-low configures the device as a BTL speaker amp.
17	17	BIAS	DC Bias Bypass Terminal. See the *BIAS Capacitor* section for capacitor selection. Connect C_{BIAS} from BIAS to GND.
18	18	GND	Ground. Connect to PGND.
19	19	INR1	Right-Channel Input 1
20	20	INR2	Right-Channel Input 2
21	21	GAINRA	Right-Channel Gain Set A
22	22	GAINRB	Right-Channel Gain Set B
24	24	OUTR+	Right-Channel Bridged Amplifier Positive Output. OUTR+ also serves as the right-channel headphone amplifier output.
26	26	OUTR-	Right-Channel Bridged Amplifier Negative Output
28	—	SCL	Serial Clock Line
—	1	MUTE	Active-High Mute Input
—	2	HPS_EN	Headphone Enable. A logic-high enables HPS. A logic-low disables HPS and the device is always configured as a BTL speaker amplifier.
—	15	GAIN$\overline{A}$/B	Gain Select. A logic-low selects the gain set by GAIN_A. A logic-high selects the gain set by GAIN_B.
—	28	IN$\overline{1}$/2	Input Select. A logic-low selects amplifier input 1. A logic-high selects amplifier input 2.
EP	EP	EP	Exposed Paddle. Connect to GND.

Stereo 3W Audio Power Amplifiers with Headphone Drive and Input Mux

Detailed Description

The MAX9777/MAX9778 feature 3W BTL speaker amplifiers, 200mW headphone amplifiers, input multiplexers, headphone sensing, and comprehensive click-and-pop suppression. The MAX9777/MAX9778 are stereo BTL/headphone amplifiers. The MAX9777 is controlled through an I²C-compatible, 2-wire serial interface. The MAX9778 is controlled through five logic inputs: MUTE, $\overline{SHDN}$, HPS_EN, GAIN$\overline{A}$/B, and IN$\overline{1}$/2 (see the *Selector Guide*). The MAX9777/MAX97778 feature exceptional PSRR (100dB at 1kHz), allowing these devices to operate from noisy digital supplies without the need for a linear regulator.

The speaker amplifiers use a BTL configuration. The signal path is composed of an input amplifier and an output amplifier. Resistor R_{IN} sets the input amplifier's gain, and resistor R_F sets the output amplifier's gain. The output of these two amplifiers serves as the input to a slave amplifier configured as an inverting unity-gain follower. This results in two outputs, identical in magnitude, but 180° out of phase. The overall gain of the speaker amplifiers is twice the product of the two amplifier gains (see the *Gain-Setting Resistors* section). A feature of this architecture is that there is no phase inversion from input to output.

When configured as a headphone (single-ended) amplifier, the slave amplifier is disabled, muting the speaker and the main amplifier drives the headphone. The MAX9777/MAX9778 can deliver 3W of continuous power into a 3Ω load with less than 1% THD+N in speaker mode, and 200mW of continuous average power into a 16Ω load with less than 1% THD+N in headphone mode. These devices also feature thermal-overload protection.

BIAS

These devices operate from a single 5V supply, and feature an internally generated, power-supply independent, common-mode bias voltage of 2.5V referenced to GND. BIAS provides both click-and-pop suppression and sets the DC bias level for the audio outputs. BIAS is internally connected to the noninverting input of each speaker amplifier (see the *Typical Application Circuits* and *Functional Diagrams*). Choose the value of the bypass capacitor as described in the *BIAS Capacitor* section. No external load should be applied to BIAS. Any load lowers the BIAS voltage, affecting the overall performance of the device.

Input Multiplexer

Each amplifier features a 2:1 input multiplexer, allowing input selection between two stereo sources. Both multiplexers are controlled by bit 1 in the control register (MAX9777) or by the IN$\overline{1}$/2 pin (MAX9778). A logic-low selects input IN_1 and a logic-high selects input IN_2.

The input multiplexer can also be used to further expand the number of gain options available from the MAX9777/MAX9778 family. Connecting the audio source to the device through two different input resistors (Figure 1) increases the number of gain options from two to four. Additionally, the input multiplexer allows a speaker equalization network to be switched into the speaker signal path. This is typically useful in optimizing acoustic response from speakers with small physical dimensions.

Headphone Sense Enable

The HPS input is enabled by HPS_EN (MAX9778) or the HPS_D bit (MAX9777). HPS_D or HPS_EN determines whether the device is in automatic detection mode or fixed-mode operation (see Tables 1a and 1b).

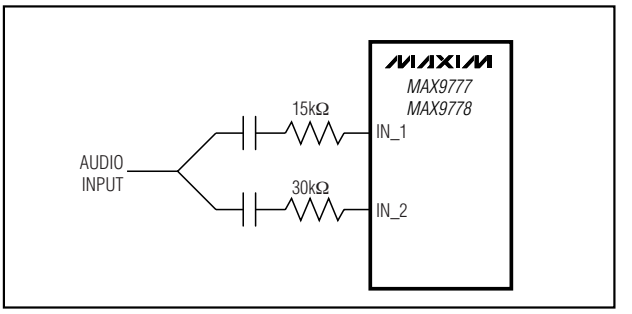


Figure 1. Using the Input Multiplexer for Gain Setting

Table 1a. MAX9777 HPS Setting

INPUTS			MODE	GAIN PATH*
HPS_D BIT	HPS	SPKR/HP BIT		
0	0	X	BTL	A
0	1	X	SE	B
1	X	0	BTL	A or B
1	X	1	SE	A or B

***Note:**

A—GAINA path selected

B—GAINB path selected

A or B—Gain path selected by GAINAB control bit in register 02h

Table 1b. MAX9778 HPS Setting

INPUTS		MODE	GAIN PATH*
HPS_EN	HPS		
0	X	BTL	A or B
1	0	BTL	A or B
1	1	SE	A or B

Note:

A or B—Gain path selected by external GAINAB

Headphone Sense Input (HPS)

With headphone sense enabled, a voltage on HPS less than 0.7 x V_{DD} sets the device to speaker mode. A voltage greater than 0.9 x V_{DD} disables the inverting bridge amplifier (OUT_-), which mutes the speaker amplifier and sets the device into headphone mode.

For automatic headphone detection, enable headphone sense and connect HPS to the control pin of a 3-wire headphone jack as shown in Figure 2. With no headphone present, the resistive voltage-divider created by R1 and R2 sets the voltage on HPS to be less than 0.7 x V_{DD}, setting the device to speaker mode and the gain setting defaults to GAINA (MAX9777). When a headphone plug is inserted into the jack, the control pin is disconnected from the tip contact, and HPS is pulled to V_{DD} through R1, setting the device into headphone mode and the gain-setting defaults to GAINB (MAX9777) (see the *Gain Select* section). Place a resistor in series with the control pin and HPS (R3) to prevent any audio signal from coupling into HPS when the device is in speaker mode.

Shutdown

The MAX9777/MAX9778 feature a 10µA, low-power shutdown mode that reduces quiescent current consumption and extends battery life. The drive amplifiers and bias circuitry are disabled, the amplifier outputs (OUT_) go high impedance, and BIAS is driven to GND. Driving $\overline{SHDN}$ low places the devices into shutdown mode, disables the interface, and resets the I^2C registers to a default state. A logic-high on $\overline{SHDN}$ enables the devices.

MAX9777 Software Shutdown

A logic-high on bit 0 of the SHDN register places the MAX9777 in shutdown mode. A logic-low enables the device. The digital section of the MAX9777 remains active when the device is shut down through the interface. All devices feature a logic-low on the $\overline{SHDN}$ input.

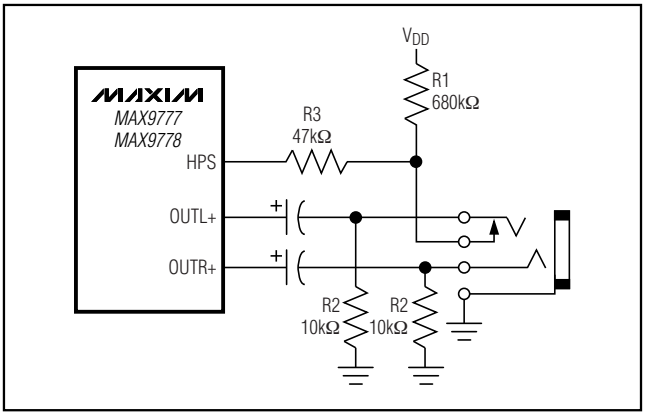


Figure 2. HPS Configuration Circuit

MUTE

The MAX9777/MAX9778 feature a mute mode. When the device is muted, the input is disconnected from the amplifiers. MUTE does not shut down the device.

MAX9777 MUTE

The MAX9777 MUTE mode is selected by writing to the MUTE register (see the *Mute Register* section). The left and right channels can be independently muted.

MAX9778 MUTE

The MAX9778 features an active-high MUTE input that mutes all channels.

Click-and-Pop Suppression

The MAX9777/MAX9778 feature Maxim's comprehensive click-and-pop suppression. When entering or exiting shutdown, the common-mode bias voltage of the amplifiers is slowly ramped to and from the DC bias point using an S-shaped waveform. In headphone mode, this waveform shapes the frequency spectrum, minimizing the amount of audible components present at the headphone. In speaker mode, the BTL amplifiers start up in the same fashion as in headphone mode. When entering shutdown, both amplifier outputs ramp to GND quickly and simultaneously. To maximize click-and-pop suppression, drive $\overline{SHDN}$ to 0V before power-up or power-down transitions.

Stereo 3W Audio Power Amplifiers with Headphone Drive and Input Mux

Digital Interface

The MAX9777 features an I²C/SMBus™-compatible 2-wire serial interface consisting of a serial data line (SDA) and a serial clock line (SCL). SDA and SCL facilitate bidirectional communication between the MAX9777 and the master at clock rates up to 400kHz. Figure 3 shows the 2-wire interface timing diagram. The MAX9777 is a transmit/receive slave-only device, relying upon a master to generate a clock signal. The master (typically a microcontroller) initiates data transfer on the bus and generates SCL to permit that transfer.

A master device communicates to the MAX9777 by transmitting the proper address followed by a command and/or data words. Each transmit sequence is framed by a START (S) or REPEATED START (S_r) condition and a STOP (P) condition. Each word transmitted over the bus is 8 bits long and is always followed by an acknowledge clock pulse.

SDA and SCL are open-drain outputs requiring a pullup resistor (500Ω or greater) to generate a logic-high voltage. Series resistors in line with SDA and SCL are optional. These series resistors protect the input stages of the devices from high-voltage spikes on the bus lines, and minimize crosstalk and undershoot of the bus signals.

SMBus is a trademark of Intel Corp.

Bit Transfer

One data bit is transferred during each SCL clock cycle. The data on SDA must remain stable during the high period of the SCL clock pulse. Changes in SDA while SCL is high are control signals (see the *START and STOP Conditions* section). SDA and SCL idle high when the I²C bus is not busy.

START and STOP Conditions

When the serial interface is inactive, SDA and SCL idle high. A master device initiates communication by issuing a START condition. A START condition is a high-to-low transition on SDA with SCL high. A STOP condition is a low-to-high transition on SDA while SCL is high (Figure 4). A START condition from the master signals the beginning of a transmission to the MAX9777. The master terminates transmission by issuing the STOP condition; this frees the bus. If a REPEATED START condition is generated instead of a STOP condition, the bus remains active.

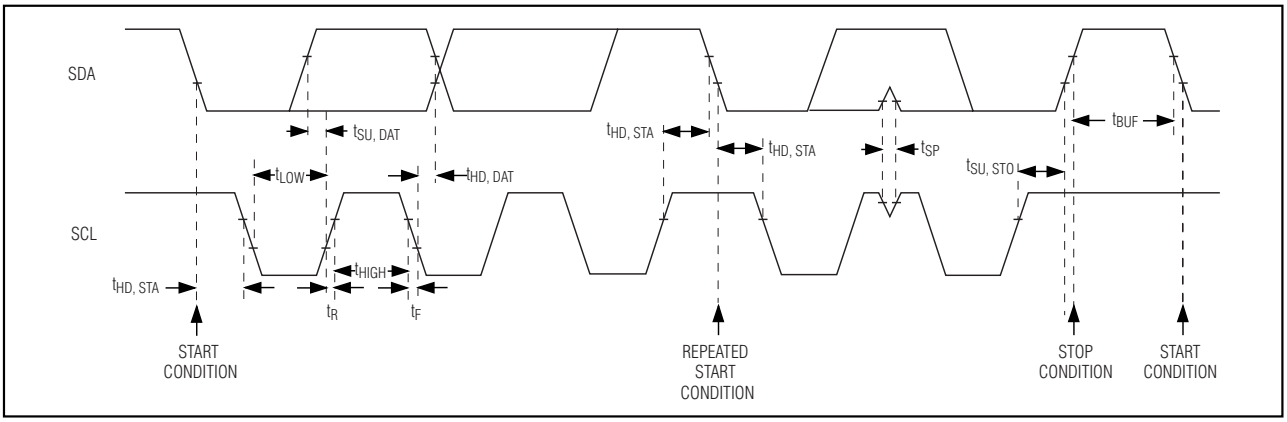


Figure 3. 2-Wire Serial-Interface Timing Diagram

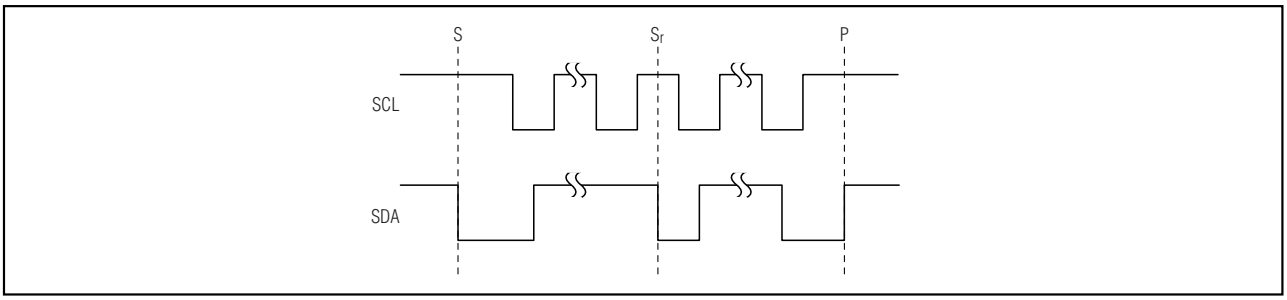


Figure 4. START/STOP Conditions

Early STOP Conditions

The MAX9777 recognizes a STOP condition at any point during the transmission except if a STOP condition occurs in the same high pulse as a START condition (Figure 5). This condition is not a legal I²C format; at least one clock pulse must separate any START and STOP condition.

REPEATED START Conditions

A REPEATED START (S_r) condition may indicate a change of data direction on the bus. Such a change occurs when a command word is required to initiate a read operation. S_r may also be used when the bus master is writing to several I²C devices and does not want to relinquish control of the bus. The MAX9777 serial interface supports continuous write operations with or without an S_r condition separating them. Continuous read operations require S_r conditions because of the change in direction of data flow.

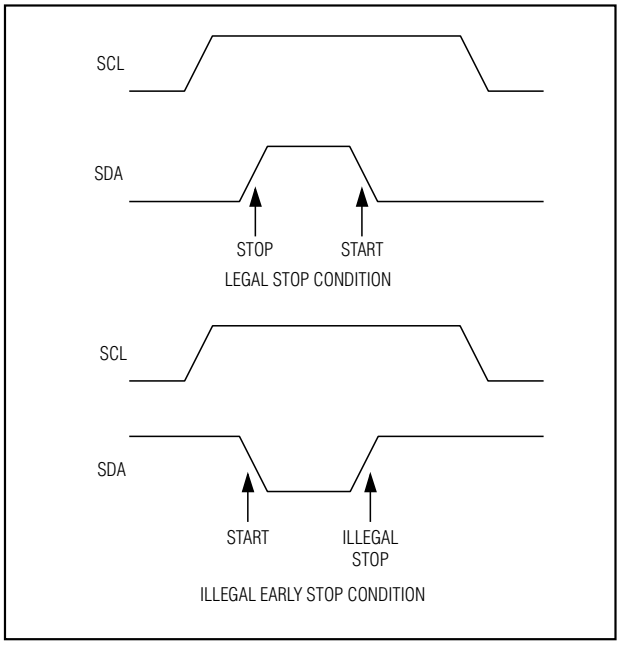


Figure 5. Early STOP Condition

Acknowledge Bit (ACK)

The acknowledge bit (ACK) is the ninth bit attached to any 8-bit data word. The receiving device always generates ACK. The MAX9777 generates an ACK when receiving an address or data by pulling SDA low during the night clock period. When transmitting data, the MAX9777 waits for the receiving device to generate an ACK. Monitoring ACK allows for detection of unsuccessful data transfers. An unsuccessful data transfer occurs if a receiving device is busy or if a system fault has occurred. In the event of an unsuccessful data transfer, the bus master should reattempt communication at a later time.

Slave Address

The bus master initiates communication with a slave device by issuing a START condition followed by a 7-bit slave address (Figure 6). When idle, the MAX9777 waits for a START condition followed by its slave address. The LSB of the address word is the Read/$\overline{\text{Write}}$ (R/$\overline{W}$) bit. R/$\overline{W}$ indicates whether the master is writing to or reading from the MAX9777 (R/$\overline{W}$ = 0 selects the write condition, R/$\overline{W}$ = 1 selects the read condition). After receiving the proper address, the MAX9777 issues an ACK by pulling SDA low for one clock cycle.

The MAX9777 has a factory-/user-programmed address. Address bits A6–A2 are preset, while A0 and A1 is set by ADD. Connect ADD to either V_{DD}, GND, SCL, or SDA to change the last 2 bits of the slave address (Table 2).

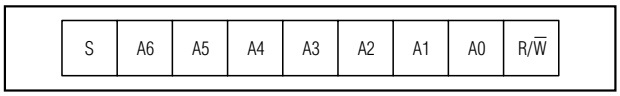


Figure 6. Slave Address Byte Definition

Table 2. MAX9777 I²C Slave Addresses

ADD CONNECTION	I²C ADDRESS
GND	100 1000
V_{DD}	100 1001
SDA	100 1010
SCL	100 1011

Stereo 3W Audio Power Amplifiers with Headphone Drive and Input Mux

Write Data Format

There are three registers that configure the MAX9777: the MUTE register, SHDN register, and control register. In write data mode (R/$\overline{W}$ = 0), the register address and data byte follow the device address (Figure 7).

MUTE Register

The MUTE register (01hex) is a read/write register that sets the MUTE status of the device. Bit 3 (MUTEL) of the MUTE register controls the left channel; bit 4 (MUTER) controls the right channel. A logic-high mutes the respective channel; a logic-low brings the channel out of mute.

SHDN Register

The SHDN register (02hex) is a read/write register that controls the power-up state of the device. A logic-high in bit 0 of the SHDN register shuts down the device; a logic-low turns on the device. A logic-high is required in bits 2 to 7 to reset all registers to their default settings.

Control Register

The control register (03hex) is a read/write register that determines the device configuration. Bit 1 (IN1/IN2) controls the input multiplexer, a logic-high selects input 1; a logic-low selects input 2. Bit 2 (HPS_D) controls the headphone sensing. A logic-low configures the device in automatic headphone detection mode. A logic-high disables the HPS input. Bit 3 (GAINA/B) controls the gain-select multiplexer. A logic-low selects GAINA. A logic-high selects GAINB. GAINA/B is ignored when HPS_D = 0. Bit 4 (SPKR/HP) selects the amplifier operating mode when HPS_D = 1. A logic-high selects speaker mode, and a logic-low selects headphone mode.

S	ADDRESS	WR	ACK	COMMAND	ACK	DATA	ACK	P
	7 BITS			8 BITS		8 BITS		1
	I^2C SLAVE ADDRESS. SELECTS DEVICE.			REGISTER ADDRESS. SELECTS REGISTER TO BE WRITTEN TO.		REGISTER DATA		

S	ADDRESS	WR	ACK	COMMAND	ACK	S	ADDRESS	WR	ACK	DATA	P
	7 BITS			8 BITS			7 BITS			8 BITS	1
	I^2C SLAVE ADDRESS. SELECTS DEVICE.			REGISTER ADDRESS. SELECTS REGISTER TO BE READ.			I^2C SLAVE ADDRESS. SELECTS DEVICE.			DATA FROM SELECTED REGISTER	

Figure 7. Write/Read Data Format Example

Table 3. MAX9777 MUTE Register Format

REGISTER ADDRESS		0000 0001	
BIT	**NAME**	**VALUE**	**DESCRIPTION**
7	X	Don't Care	—
6	X	Don't Care	—
5	X	Don't Care	—
4	MUTER	0*	Unmute right channel
		1	Mute right channel
3	MUTEL	0*	Unmute left channel
		1	Mute left channel
2	X	Don't Care	—
1	X	Don't Care	—
0	X	Don't Care	—

**Default state.*

Table 4. MAX9777 SHDN Register Format

REGISTER ADDRESS		0000 0010	
BIT	**NAME**	**VALUE**	**DESCRIPTION**
7	RESET	0*	—
		1	Reset device
6	RESET	0*	—
		1	Reset device
5	RESET	0*	—
		1	Reset device
4	RESET	0*	—
		1	Reset device
3	RESET	0*	—
		1	Reset device
2	RESET	0*	—
		1	Reset device
1	X	Don't Care	—
0	SHDN	0*	Normal operation
		1	Shutdown

**Default state.*

Table 5. MAX9777 Control Register Format

REGISTER ADDRESS		0000 0011	
BIT	**NAME**	**VALUE**	**DESCRIPTION**
7	X	Don't Care	—
6	X	Don't Care	—
5	X	Don't Care	—
4	SPKR/HP	0*	Speaker mode selected
		1	Headphone mode selected
3	GAINA/B	0*	Gain-setting A selected
		1	Gain-setting B selected
2	HPS_D	0*	Automatic headphone detection enabled
		1	Automatic headphone detection disabled (HPS ignored)
1	IN1/IN2	0*	Input 1 selected
		1	Input 2 selected
0	X	Don't Care	—

**Default*

Read Data Format

In read mode (R/$\overline{W}$ = 1), the MAX9777 writes the contents of the selected register to the bus. The direction of the data flow reverses following the address acknowledge by the MAX9777. The master device reads the contents of all registers, including the read-only status register. Table 6 shows the status register format.

Interrupt Output ($\overline{INT}$)

The MAX9777 includes an interrupt output ($\overline{INT}$) that can indicate to a master device that an event has occurred. $\overline{INT}$ is triggered when the state of HPS changes. During normal operation, $\overline{INT}$ idles high. If a headphone is inserted/removed from the jack and that action is detected by HPS, $\overline{INT}$ pulls the line low. $\overline{INT}$ remains low until a read data operation is executed.

I²C Compatibility

The MAX9777 is compatible with existing I²C systems. SCL and SDA are high-impedance inputs; SDA has an open drain that pulls the data line low during the ninth clock pulse. The communication protocol supports the standard I²C 8-bit communications. The general call address is ignored. The MAX9777 slave addresses are compatible with the 7-bit I²C addressing protocol only.

Table 6. MAX9777 Status Register Format

REGISTER ADDRESS		0000 0000	
BIT	**NAME**	**VALUE**	**DESCRIPTION**
7	THRM	0	Device temperature below thermal limit
		1	Device temperature exceeding thermal limit
6	AMPR-	0	OUTR- current below current limit
		1	OUTR- current exceeding current limit
5	AMPR+	0	OUTR+ current below current limit
		1	OUTR+ current exceeding current limit
4	AMPL-	0	OUTL- current below current limit
		1	OUTL- current exceeding current limit
3	AMPL+	0	OUTL+ current below current limit
		1	OUTL+ current exceeding current limit
2	HPSTS	0	Device in speaker mode
		1	Device in headphone mode
1	X	Don't Care	—
0	X	Don't Care	—

Stereo 3W Audio Power Amplifiers with Headphone Drive and Input Mux

Applications Information

BTL Speaker Amplifiers

The MAX9777/MAX9778 feature speaker amplifiers designed to drive a load differentially, a configuration referred to as bridge-tied load (BTL). The BTL configuration (Figure 8) offers advantages over the single-ended configuration, where one side of the load is connected to ground. Driving the load differentially doubles the output voltage compared to a single-ended amplifier under similar conditions. Thus, the devices' differential gain is twice the closed-loop gain of the input amplifier. The effective gain is given by:

$$A_{VD} = 2 \times \frac{R_F}{R_{IN}}$$

Substituting 2 x $V_{OUT(P-P)}$ for $V_{OUT(P-P)}$ into the following equations yields four times the output power due to doubling of the output voltage:

$$V_{RMS} = \frac{V_{OUT(P-P)}}{2\sqrt{2}}$$

$$P_{OUT} = \frac{V_{RMS}^2}{R_L}$$

Since the differential outputs are biased at midsupply, there is no net DC voltage across the load. This eliminates the need for DC-blocking capacitors required for single-ended amplifiers. These capacitors can be large and expensive, consume board space, and degrade low-frequency performance.

When the MAX9777 is configured to automatically detect the presence of a headphone jack, the device defaults to gain setting A when the device is in speaker mode.

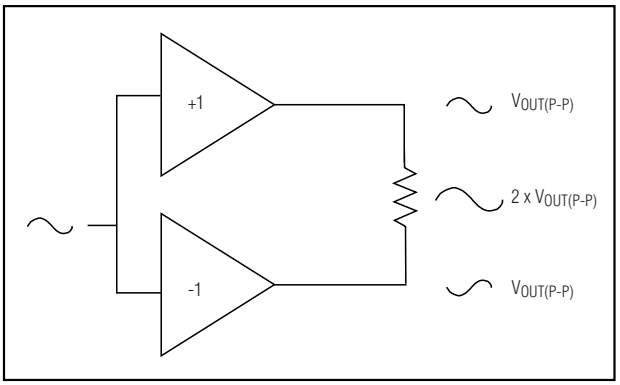


Figure 8. Bridge-Tied Load Configuration

Single-Ended Headphone Amplifier

The MAX9777/MAX9778 can be configured as single-ended headphone amplifiers through software or by sensing the presence of a headphone plug (HPS). In headphone mode, the inverting output of the BTL amplifier is disabled, muting the speaker. The gain is 1/2 that of the device in speaker mode, and the output power is reduced by a factor of 4.

In headphone mode, the load must be capacitively coupled to the device, blocking the DC bias voltage from the load (see the *Typical Application Circuits*).

Power Dissipation and Heat Sinking

Under normal operating conditions, the MAX9777/MAX9778 can dissipate a significant amount of power. The maximum power dissipation for each package is given in the *Absolute Maximum Ratings* section under Continuous Power Dissipation or can be calculated by the following equation:

$$P_{DISSPKG(MAX)} = \frac{T_{J(MAX)} - T_A}{\theta_{JA}}$$

where $T_{J(MAX)}$ is +150°C, T_A is the ambient temperature, and θ_{JA} is the reciprocal of the derating factor in °C/W as specified in the *Absolute Maximum Ratings* section. For example, θ_{JA} of the TQFN package is +29°C/W.

The increase in power delivered by the BTL configuration directly results in an increase in internal power dissipation over the single-ended configuration. The maximum power dissipation for a given V_{DD} and load is given by the following equation:

$$P_{DISS(MAX)} = \frac{2V_{DD}^2}{\pi^2 R_L}$$

If the power dissipation for a given application exceeds the maximum allowed for a given package, either reduce V_{DD}, increase load impedance, decrease the ambient temperature, or add heatsinking to the device. Large output, supply, and ground PC board traces improve the maximum power dissipation in the package.

Thermal-overload protection limits total power dissipation in these devices. When the junction temperature exceeds +160°C, the thermal-protection circuitry disables the amplifier output stage. The amplifiers are enabled once the junction temperature cools by 15°C. This results in a pulsing output under continuous thermal-overload conditions as the device heats and cools.

Component Selection

Gain-Setting Resistors

External feedback components set the gain of the MAX9777/MAX9778. Resistor R_{IN} sets the gain of the input amplifier (A_{VIN}), and resistor R_F sets the gain of the second stage amplifier (A_{VOUT}):

$$A_{VIN} = -\left(\frac{10k\Omega}{R_{IN}}\right),\ A_{VOUT} = -\left(\frac{R_F}{10k\Omega}\right)$$

Combining A_{VIN} and A_{VOUT}, R_{IN} and R_F set the single-ended gain of the device as follows:

$$A_V = A_{VIN} \times A_{VOUT} = -\left(\frac{10k\Omega}{R_{IN}}\right) \times -\left(\frac{R_F}{10k\Omega}\right) = +\left(\frac{R_F}{R_{IN}}\right)$$

As shown, the two-stage amplifier architecture results in a noninverting gain configuration, preserving absolute phase through the MAX9777/MAX9778. The gain of the device in BTL mode is twice that of the single-ended mode. Choose R_{IN} between 10kΩ and 15kΩ and R_F between 15kΩ and 100kΩ.

Input Filter

The input capacitor (C_{IN}), in conjunction with R_{IN}, forms a highpass filter that removes the DC bias from an incoming signal. The AC-coupling capacitor allows the amplifier to bias the signal to an optimum DC level. Assuming zero-source impedance, the -3dB point of the highpass filter is given by:

$$f_{-3dB} = \frac{1}{2\pi R_{IN} C_{IN}}$$

Choose R_{IN} according to the *Gain-Setting Resistors* section. Choose the C_{IN} such that f_{-3dB} is well below the lowest frequency of interest. Setting f_{-3dB} too high affects the amplifier's low-frequency response. Use capacitors whose dielectrics have low-voltage coefficients, such as tantalum or aluminum electrolytic. Capacitors with high-voltage coefficients, such as ceramics, may result in an increased distortion at low frequencies.

Other considerations when designing the input filter include the constraints of the overall system, the actual frequency band of interest, and click-and-pop suppression.

Output-Coupling Capacitor

The MAX9777/MAX9778 require output-coupling capacitors to operate in single-ended (headphone) mode. The output-coupling capacitor blocks the DC component of the amplifier output, preventing DC current from flowing to the load. The output capacitor and the load impedance form a highpass filter with a -3dB point determined by:

$$f_{-3dB} = \frac{1}{2\pi R_L C_{OUT}}$$

As with the input capacitor, choose C_{OUT} such that f_{-3dB} is well below the lowest frequency of interest. Setting f_{-3dB} too high affects the amplifier's low-frequency response.

Load impedance is a concern when choosing C_{OUT}. Load impedance can vary, changing the -3dB point of the output filter. A lower impedance increases the corner frequency, degrading low-frequency response. Select C_{OUT} such that the worst-case load/C_{OUT} combination yields an adequate response. Select capacitors with low ESR to minimize resistive losses and optimize power transfer to the load.

If layout constraints require a physically smaller output-coupling capacitor, decrease the value of C_{OUT} and add series resistance to the output of the MAX9777/MAX9778 (see Figure 9). With the added series resistance at the output, the cutoff frequency of the highpass filter is:

$$f_{-3dB} = \frac{1}{2\pi(R_L + R_{SERIES})C_{OUT}}$$

Since the cutoff frequency of the output highpass filter is inversely proportional to the product of the total load resistance seen by the outputs (R_L + R_{SERIES}) and C_{OUT}, increase the total resistance seen by the MAX9777/MAX9778 outputs by the same amount C_{OUT} is decreased to maintain low-frequency performance. Since the added series resistance forms a voltage-divider with the headphone speaker resistance for frequencies within the passband of the highpass filter, there is a loss in voltage gain. To compensate for this loss, increase the voltage gain setting by an amount equal to the attenuation due to the added series resistance. Use the following equation to approximate the required voltage gain compensation:

$$A_{V\_COMP} = 20\log\left(\frac{R_L + R_{SERIES}}{R_L}\right)$$

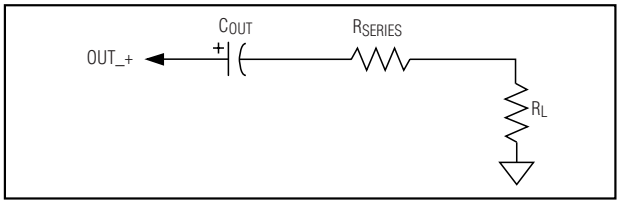


Figure 9. Reducing C_{OUT} by Adding R_{SERIES}

Stereo 3W Audio Power Amplifiers with Headphone Drive and Input Mux

BIAS Capacitor

BIAS is the output of the internally generated 2.5VDC bias voltage. The BIAS bypass capacitor, C_{BIAS}, improves PSRR and THD+N by reducing power supply and other noise sources at the common-mode bias node, and also generates the clickless/popless, start-up/shutdown DC bias waveforms for the speaker amplifiers. Bypass BIAS with a 1µF capacitor to GND.

Supply Bypassing

Proper power-supply bypassing ensures low-noise, low-distortion performance. Place a 0.1µF ceramic capacitor from V_{DD} to GND. Add additional bulk capacitance as required by the application, typically 100µF. Bypass PV_{DD} with a 100µF capacitor to GND. Locate bypass capacitors as close to the device as possible.

Gain Select

The MAX9777/MAX9778 feature multiple gain settings on each channel, making available different gain and feedback configurations. The gain-setting resistor (R_F) is connected between the amplifier output (OUT_+) and the gain set point (GAIN_). An internal multiplexer switches between the different feedback resistors depending on the status of the gain control input. The stereo MAX9777/MAX9778 feature two gain options per channel. See Tables 1a and 1b for the gain-setting options.

Bass Boost Circuit

Headphones typically have a poor low-frequency response due to speaker and enclosure size limitations. A bass boost circuit compensates the poor low-frequency response (Figure 10). At low frequencies, the capacitor C_F is an open circuit, and the effective impedance in the feedback loop ($R_{F(EFF)}$) is $R_{F(EFF)} = R_{F1}$.

At the frequency:

$$\frac{1}{2\pi R_{F2} C_F}$$

where the impedance, C_F, begins to decrease, and at high frequencies, the C_F is a short circuit. Here the impedance of the feedback loop is:

$$R_{F(EFF)} = \frac{R_{F1} \times R_{F2}}{R_{F1} + R_{F2}}$$

Assuming $R_{F1} = R_{F2}$, then $R_{F(EFF)}$ at low frequencies is twice that of $R_{F(EFF)}$ at high frequencies (Figure 11). Thus, the amplifier has more gain at lower frequencies, boosting the system's bass response. Set the gain roll-off frequency based upon the response of the speaker and enclosure.

To minimize distortion at low frequencies, use capacitors with low-voltage coefficient dielectrics when selecting C_F. Film or C0G dielectric capacitors are good choices for C_F. Capacitors with high-voltage coefficients, such as ceramics (non-C0G dielectrics), can result in increased distortion at low frequencies.

Layout and Grounding

Good PC board layout is essential for optimizing performance. Use large traces for the power-supply inputs and amplifier outputs to minimize losses due to parasitic trace resistance, as well as route heat away from the device. Good grounding improves audio performance, minimizes crosstalk between channels, and prevents any digital switching noise from coupling into the audio signal. If digital signal lines must cross over or under audio signal lines, ensure that they cross perpendicular to each other.

The MAX9777/MAX9778 TQFN package features an exposed thermal pad. This pad lowers the package's thermal resistance by providing a direct heat conduction path from the die to the PC board. Connect the pad to signal ground (0V) by using a large pad or multiple vias to the ground plane.

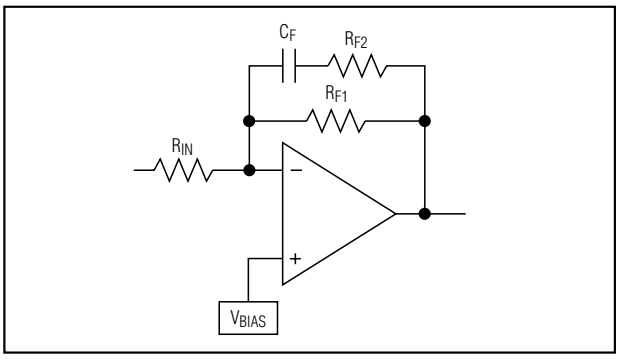


Figure 10. Bass Boost Circuit

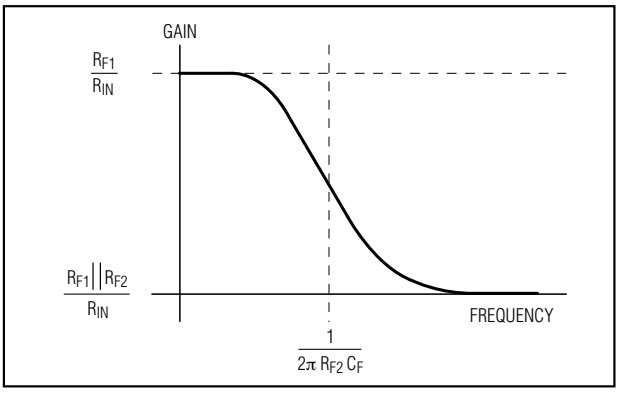
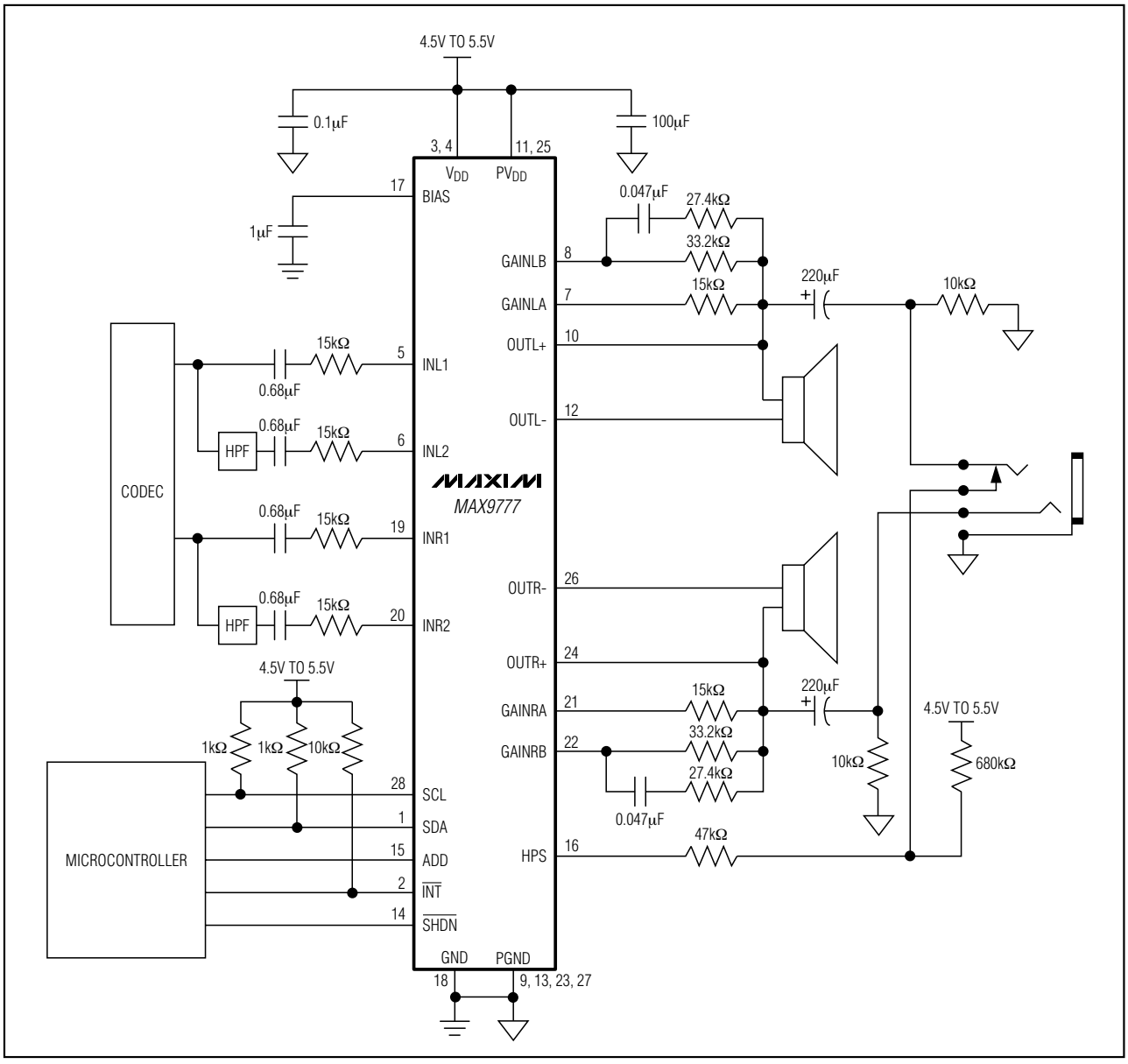


Figure 11. Bass Boost Response

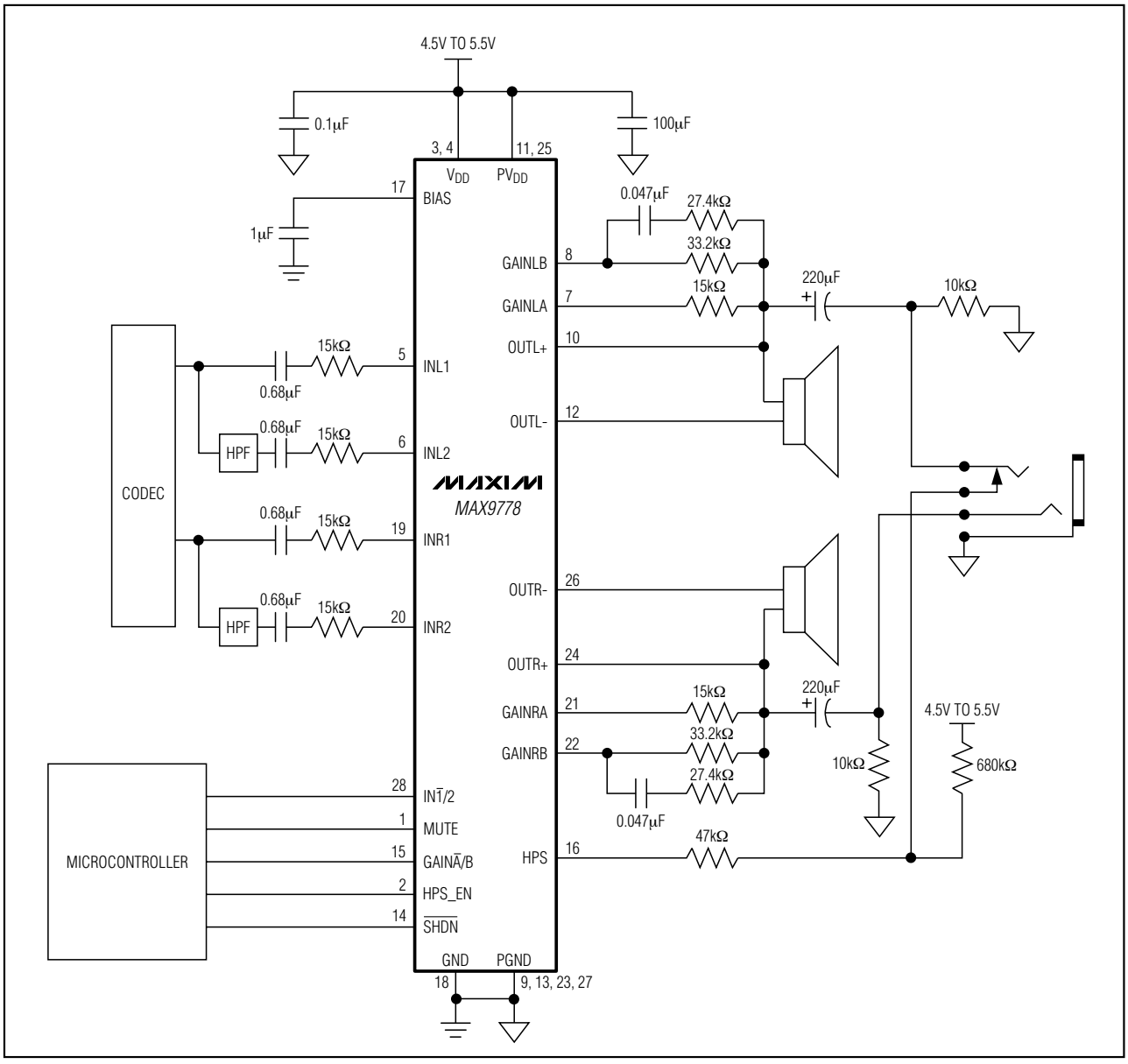
Stereo 3W Audio Power Amplifiers with Headphone Drive and Input Mux

Typical Application Circuits



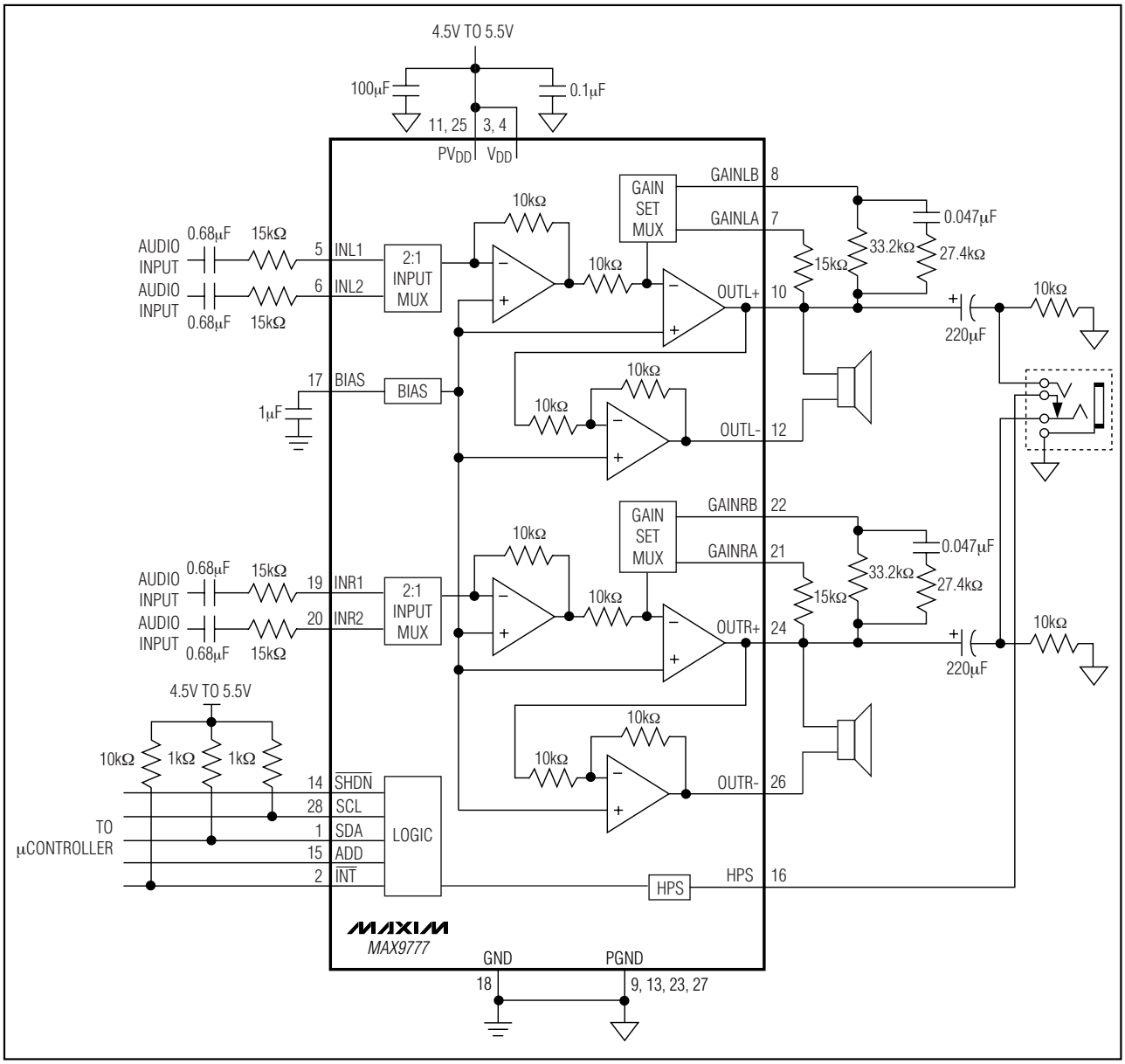
Stereo 3W Audio Power Amplifiers with Headphone Drive and Input Mux

Typical Application Circuits (continued)



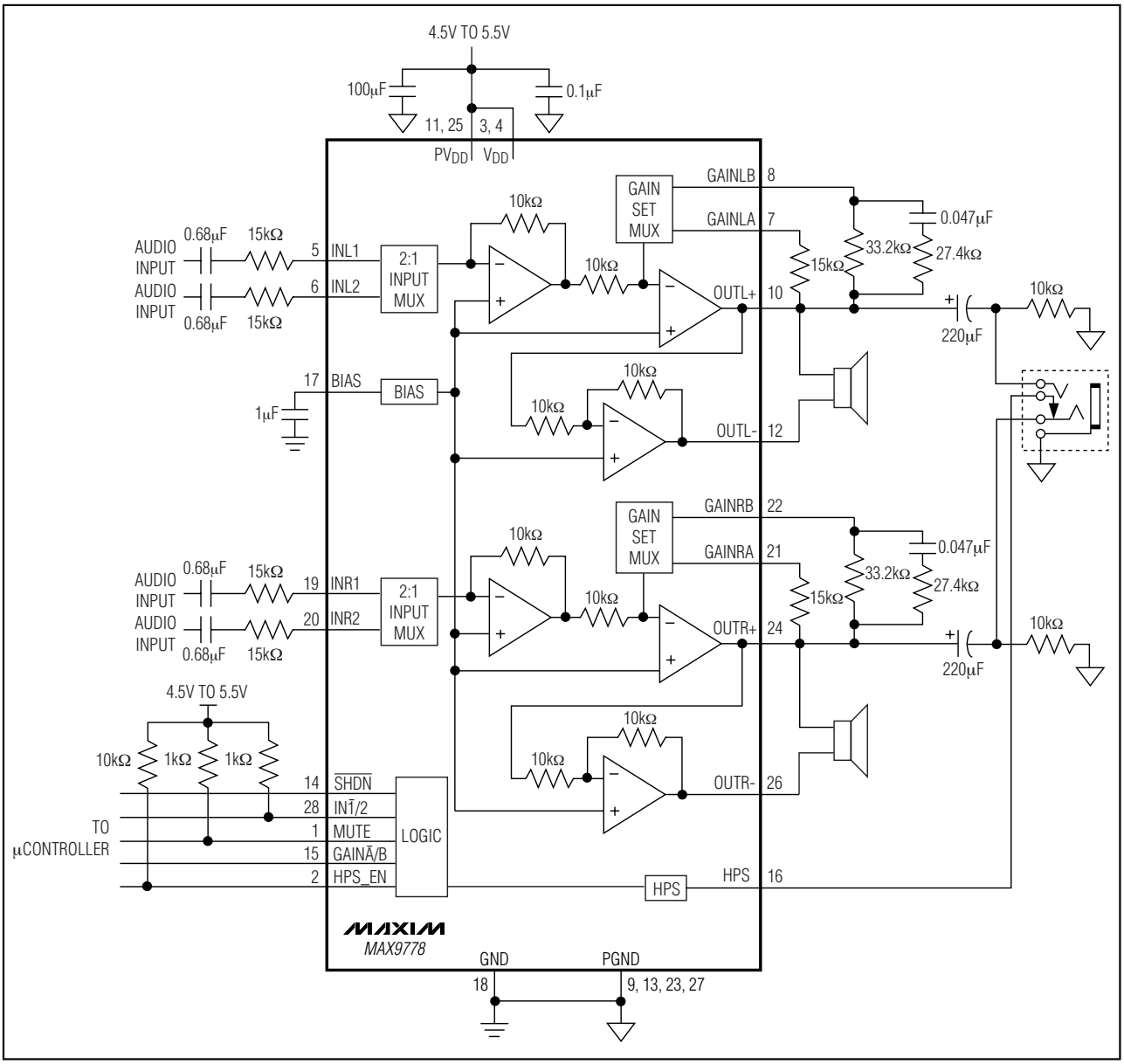
Stereo 3W Audio Power Amplifiers with Headphone Drive and Input Mux

Functional Diagrams



Stereo 3W Audio Power Amplifiers with Headphone Drive and Input Mux

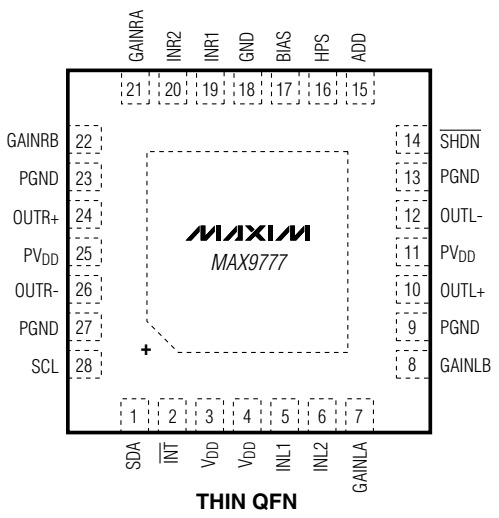
Functional Diagrams (continued)



Stereo 3W Audio Power Amplifiers with Headphone Drive and Input Mux

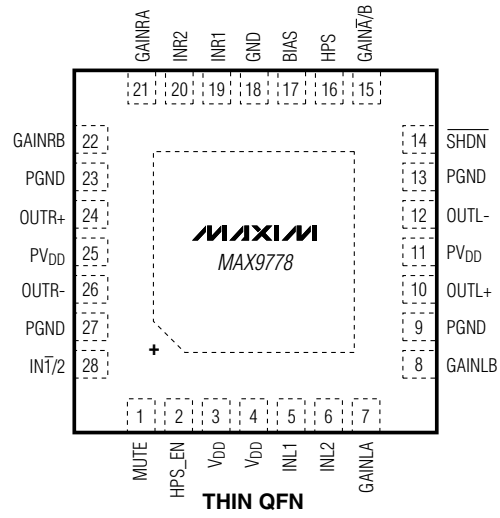
Pin Configurations

TOP VIEW



THIN QFN

TOP VIEW

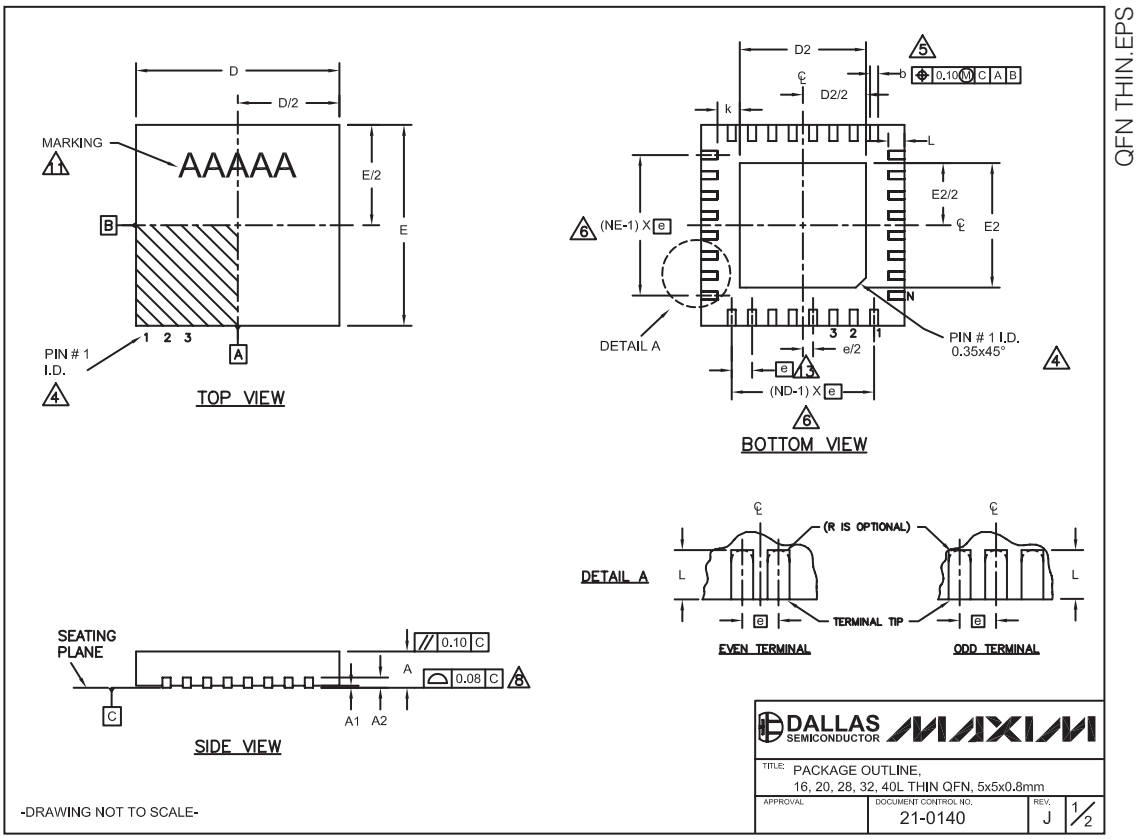


THIN QFN

Stereo 3W Audio Power Amplifiers with Headphone Drive and Input Mux

Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)



Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)

COMMON DIMENSIONS															
PKG.	16L 5x5			20L 5x5			28L 5x5			32L 5x5			40L 5x5		
SYMBOL	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80
A1	0	0.02	0.05	0	0.02	0.05	0	0.02	0.05	0	0.02	0.05	0	0.02	0.05
A2	0.20 REF.			0.20 REF.			0.20 REF.			0.20 REF.			0.20 REF.		
b	0.25	0.30	0.35	0.25	0.30	0.35	0.20	0.25	0.30	0.20	0.25	0.30	0.15	0.20	0.25
D	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10
E	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10
e	0.80 BSC.			0.65 BSC.			0.50 BSC.			0.50 BSC.			0.40 BSC.		
k	0.25	-	-	0.25	-	-	0.25	-	-	0.25	-	-	0.25	-	-
L	0.30	0.40	0.50	0.45	0.55	0.65	0.45	0.55	0.65	0.30	0.40	0.50	0.30	0.40	0.50
N	16			20			28			32			40		
ND	4			5			7			8			10		
NE	4			5			7			8			10		
JEDEC	WHHB			WHHC			WHHD-1			WHHD-2			---		

EXPOSED PAD VARIATIONS						
PKG. CODES	D2			E2		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
T1655-2	3.00	3.10	3.20	3.00	3.10	3.20
T1655-3	3.00	3.10	3.20	3.00	3.10	3.20
T1655N-1	3.00	3.10	3.20	3.00	3.10	3.20
T2055-3	3.00	3.10	3.20	3.00	3.10	3.20
T2055-4	3.00	3.10	3.20	3.00	3.10	3.20
T2055-5	3.15	3.25	3.35	3.15	3.25	3.35
T2855-3	3.15	3.25	3.35	3.15	3.25	3.35
T2855-4	2.60	2.70	2.80	2.60	2.70	2.80
T2855-5	2.60	2.70	2.80	2.60	2.70	2.80
T2855-6	3.15	3.25	3.35	3.15	3.25	3.35
T2855-7	2.60	2.70	2.80	2.60	2.70	2.80
T2855-8	3.15	3.25	3.35	3.15	3.25	3.35
T2855N-1	3.15	3.25	3.35	3.15	3.25	3.35
T3255-3	3.00	3.10	3.20	3.00	3.10	3.20
T3255-4	3.00	3.10	3.20	3.00	3.10	3.20
T3255-5	3.00	3.10	3.20	3.00	3.10	3.20
T3255N-1	3.00	3.10	3.20	3.00	3.10	3.20
T4055-1	3.40	3.50	3.60	3.40	3.50	3.60
T4055-2	3.40	3.50	3.60	3.40	3.50	3.60

**SEE COMMON DIMENSIONS TABLE

NOTES:

1. DIMENSIONING & TOLERANCING CONFORM TO ASME Y14.5M-1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS. ANGLES ARE IN DEGREES.
3. N IS THE TOTAL NUMBER OF TERMINALS.
4. THE TERMINAL #1 IDENTIFIER AND TERMINAL NUMBERING CONVENTION SHALL CONFORM TO JESD 95-1 SPP-012. DETAILS OF TERMINAL #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE TERMINAL #1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE.
5. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.25 mm AND 0.30 mm FROM TERMINAL TIP.
6. ND AND NE REFER TO THE NUMBER OF TERMINALS ON EACH D AND E SIDE RESPECTIVELY.
7. DEPOPULATION IS POSSIBLE IN A SYMMETRICAL FASHION.
8. COPLANARITY APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.
9. DRAWING CONFORMS TO JEDEC MO220, EXCEPT EXPOSED PAD DIMENSION FOR T2855-3 AND T2855-6.
10. WARPAGE SHALL NOT EXCEED 0.10 mm.
11. MARKING IS FOR PACKAGE ORIENTATION REFERENCE ONLY.
12. NUMBER OF LEADS SHOWN ARE FOR REFERENCE ONLY.
13. LEAD CENTERLINES TO BE AT TRUE POSITION AS DEFINED BY BASIC DIMENSION "e", ±0.05.

-DRAWING NOT TO SCALE-

DALLAS SEMICONDUCTOR MAXIM

TITLE: PACKAGE OUTLINE, 16, 20, 28, 32, 40L THIN QFN, 5x5x0.8mm

APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-0140	J	2/2