

# 9344

## BINARY (4-BIT BY 2-BIT) FULL MULTIPLIER

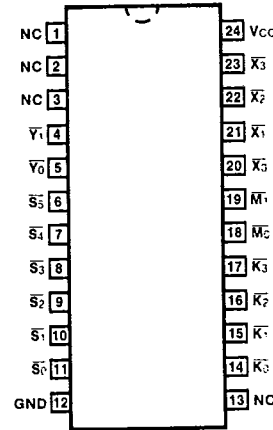
**DESCRIPTION**—The '44 is a 4-bit by 2-bit full multiplier building block. It multiplies two binary numbers and simultaneously adds two other binary numbers to the product. '44 devices can be interconnected to form a high speed multiplier array of any size. The device is constructed with TTL compatible inputs and outputs. Inputs are buffered to reduce loading.

- PERFORMS DIRECT MULTIPLICATION
- EXPANDS TO ANY SIZE ARRAY WITHOUT ADDITIONAL COMPONENTS
- MULTIPLIES AND ADDS SIMULTANEOUSLY

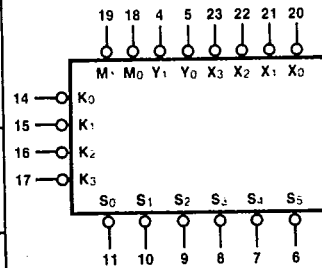
**ORDERING CODE:** See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE	MILITARY GRADE	PKG TYPE
		$V_{CC} = +5.0\text{ V} \pm 5\%$ , $T_A = 0^\circ\text{ C to } +70^\circ\text{ C}$	$V_{CC} = +5.0\text{ V} \pm 10\%$ , $T_A = -55^\circ\text{ C to } +125^\circ\text{ C}$	
Plastic DIP (P)	A	9344PC		9N
Ceramic DIP (D)	A	9344DC	9344DM	6N
Flatpak (F)	A	9344FC	9344FM	4M

### CONNECTION DIAGRAM PINOUT A



### LOGIC SYMBOL



$V_{CC} = \text{Pin } 24$   
 $GND = \text{Pin } 12$

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**INPUT LOADING/FAN-OUT:** See Section 3 for U.L. definitions

PIN NAMES	DESCRIPTION	93XX (U.L.) HIGH/LOW
$\bar{X}_0 - \bar{X}_3$	Multiplicand Inputs (Active LOW)	0.66/0.66
$\bar{Y}_0, \bar{Y}_1$	Multiplier Inputs (Active LOW)	0.66/0.66
$\bar{M}_1$	Additive Carry Inputs (Active LOW)	1.0/1.0
$\bar{K}_0, \bar{M}_0$		4.0/4.0
$\bar{K}_1 - \bar{K}_3$	Outputs	2.0/2.0
$\bar{S}_0 - \bar{S}_5$		20/10

**FUNCTIONAL DESCRIPTION** — The '44 is a binary full multiplier for 4-bit by 2-bit words. It is easily expandable in an array to form a high speed parallel multiplier of any length. The functional equation is illustrated below:

$$S(6\text{-bits}) = \overline{X}(4\text{-bits}) \text{ times } \overline{Y}(2\text{-bits}) \text{ plus } \overline{M}(2\text{-bits}) \text{ plus } \overline{K}(4\text{-bits})$$

Functionally the '44 multiplies a 4-bit word ( $\overline{X}_0 - \overline{X}_3$ ) by a two bit word ( $\overline{Y}_0 - \overline{Y}_1$ ), generating eight partial products. Two other words,  $\overline{K}_0 - \overline{K}_3$  and  $\overline{M}_0 - \overline{M}_1$ , are added to these partial products through a lookahead carry adder, generating a 6-bit product/sum. The function can be described by the following equation (note that "+" means arithmetic addition):

$$S = 2^0 (\overline{X}_0 \overline{Y}_0 + \overline{M}_0 + \overline{K}_0) + 2^1 (\overline{X}_1 \overline{Y}_0 + \overline{X}_0 \overline{Y}_1 + \overline{M}_1 + \overline{K}_1) + 2^2 (\overline{X}_2 \overline{Y}_0 + \overline{X}_1 \overline{Y}_1 + \overline{K}_2) + 2^3 (\overline{X}_3 \overline{Y}_0 + \overline{X}_2 \overline{Y}_1 + \overline{K}_3) + 2^4 (\overline{X}_3 \overline{Y}_1)$$

All inputs and outputs are active LOW;  $\overline{X}$  and  $\overline{Y}$  inputs are buffered to present only one TTL unit load. The device operates only on positive numbers. If two's complement multiplication is required, then the numbers must be changed to sign magnitude before multiplication, or else the product must be corrected following multiplication of the two's complement numbers. The correction algorithm depends on whether  $\overline{X}$  or  $\overline{Y}$  or both are negative.

If  $\overline{X}$  is negative:  
Subtract  $\overline{Y}$  from most significant half of product.

If  $\overline{Y}$  is negative:  
Subtract  $\overline{X}$  from most significant half of product.

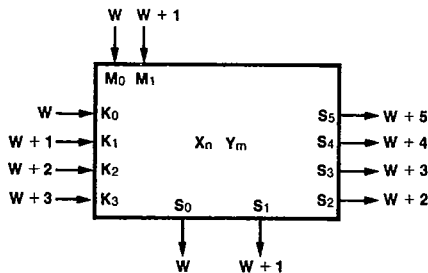
If both  $\overline{X}$  and  $\overline{Y}$  are negative:  
Add  $\overline{X}$  plus  $\overline{Y}$  to most significant half of product.

The result will be the correct two's complement product.

**MULTIPLICATION TIME**

NUMBER OF BITS	PACKAGES	TIME (ns)
8 x 8	8	150
12 x 12	18	260
16 x 16	32	350
24 x 24	72	550

**WEIGHTING FACTORS OF THE BASIC MULTIPLIER**



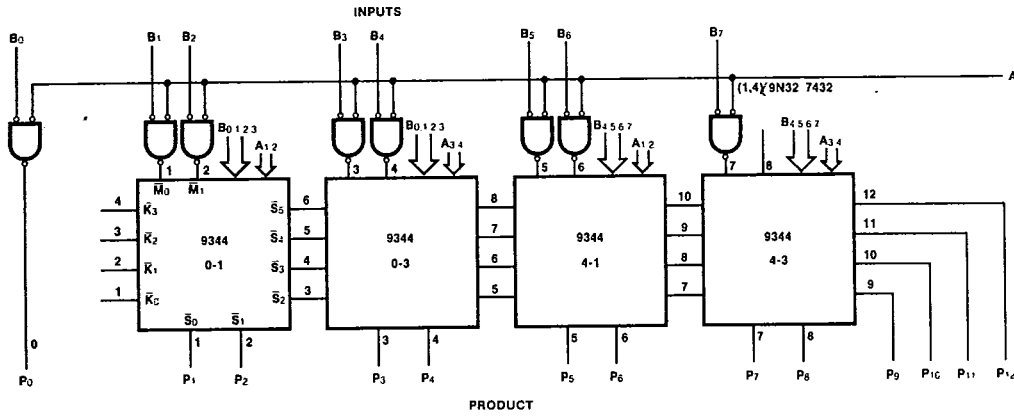
This block represents the basic 4-bit by 2-bit multiplier, and indicates the weighting factors (power of two) attached to each of the inputs and outputs.

**TYPICAL MULTIPLICATION ARRAYS**

The '44 can be assembled in an iterative structure to perform multi-bit multiplication. The blocks are interconnected so that partial product sums generated in a particular '44 are applied, if necessary, to equal weight carry inputs ( $\bar{K}_0 - \bar{K}_3$  or  $M_0, \bar{M}_1$ ) of succeeding stages.

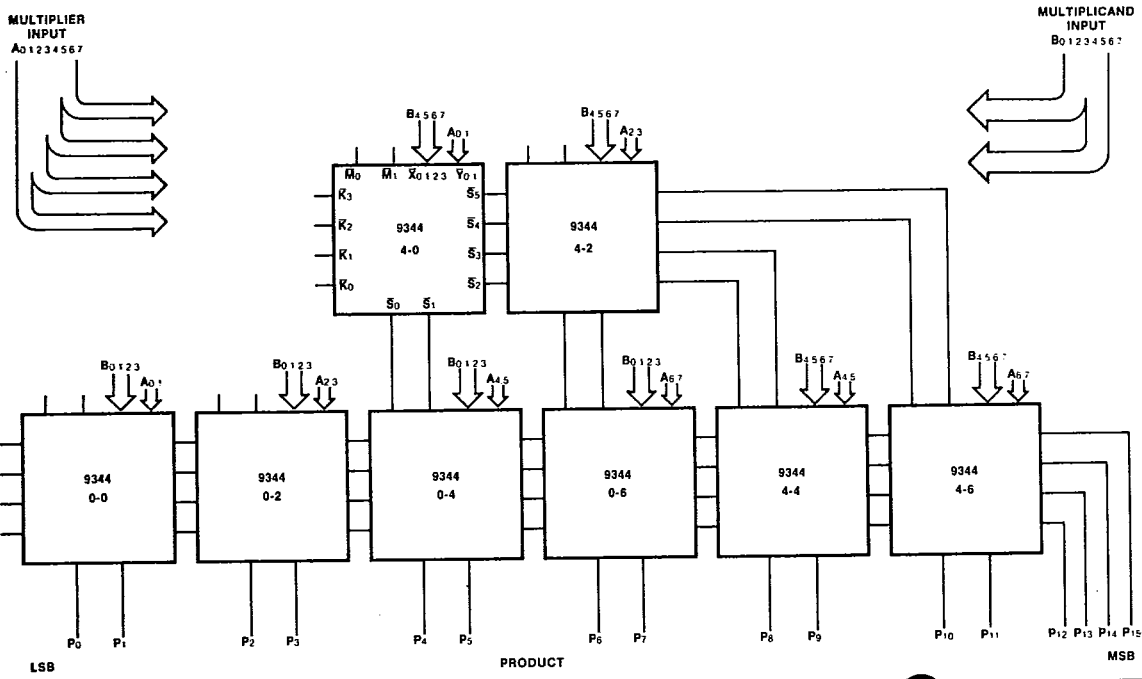
In the active iterative multiplication arrays shown, weighting factors of the carry and sums between '44's are indicated (i.e., 0 = 20, 1 = 21, 2 = 22, etc.). Labels inside the blocks identify bits multiplied in that block. For instance 0-0 refers to multiplicand bits  $B_{0,1,2,3}$  and multiplier bits  $A_{0,1}$ , while 4-2 would represent multiplicand bits  $B_{4,5,6,7}$  and multiplier bits  $A_{2,3}$ .

**8-BIT BY 5-BIT MULTIPLICATION ARRAY**

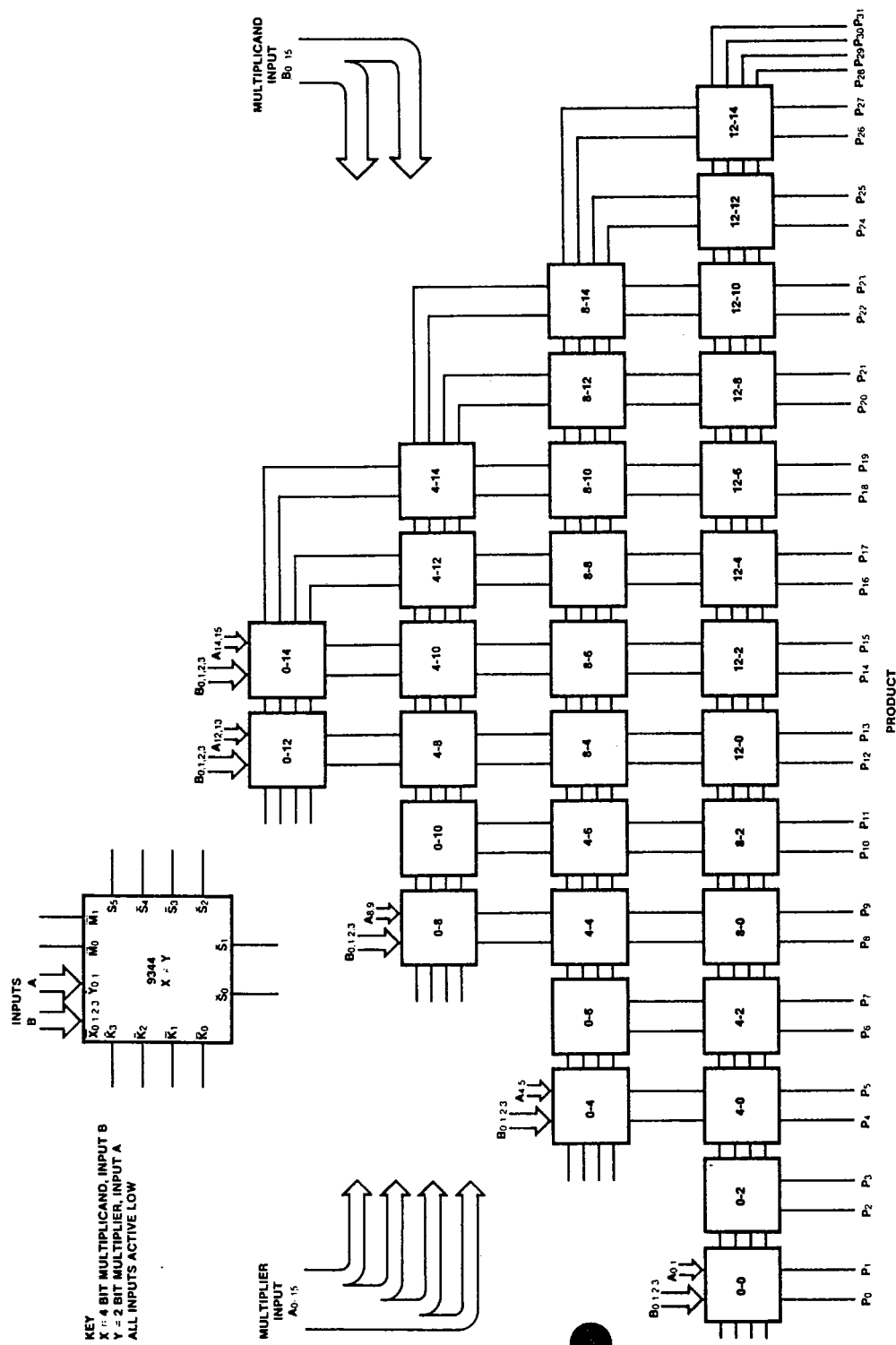


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**8-BIT BY 8-BIT MULTIPLICATION ARRAY**



16-BIT BY 16-BIT MULTIPLICATION ARRAY

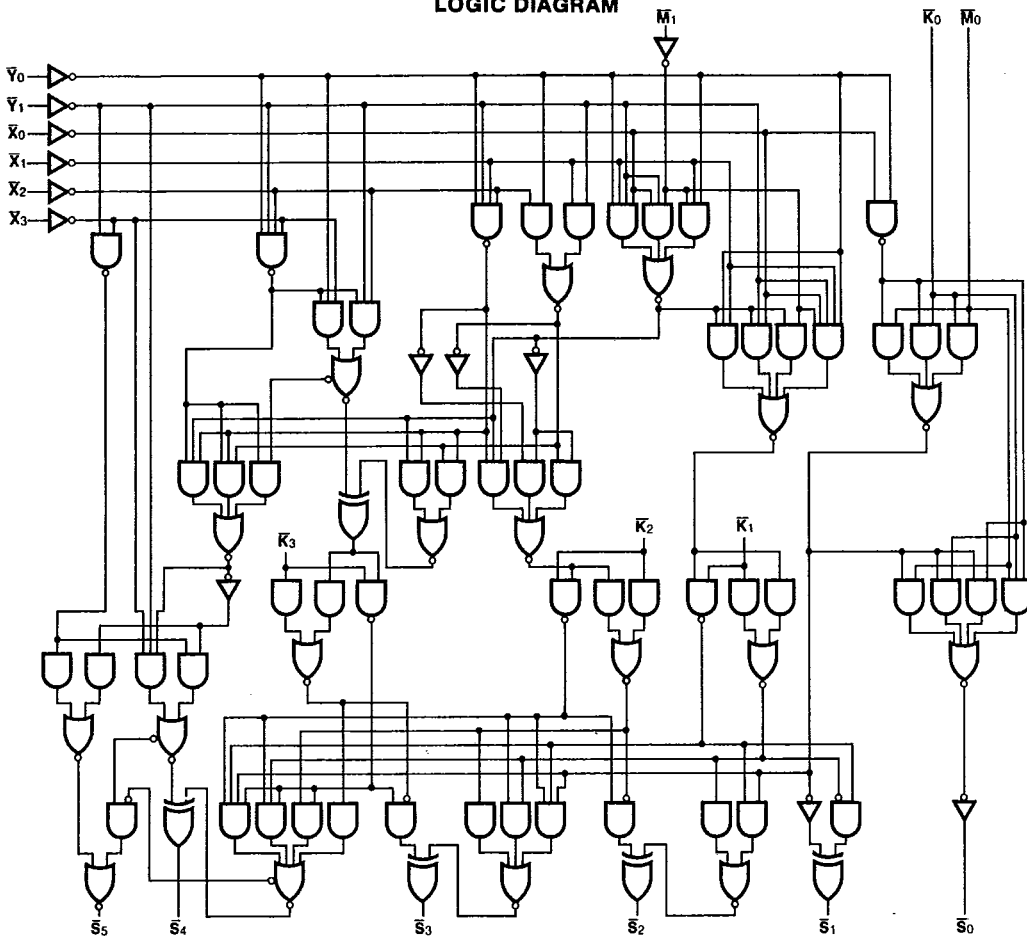


KEY  
 X = 4 BIT MULTIPLICAND, INPUT B  
 Y = 2 BIT MULTIPLIER, INPUT A  
 ALL INPUTS ACTIVE LOW

NOTE:  
 Each block represents one 9344. Labels inside the blocks identify bits multiplied in that block. The first number is the 4-bit B input, and the second number is the 2-bit A input. For instance, 12-0 refers to multiplicand bits B12,13,14,15 and multiplier bits A0,1.

T-45-07

LOGIC DIAGRAM



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DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER	93XX		UNITS	CONDITIONS
		Min	Max		
I <sub>CC</sub>	Power Supply Current		150	mA	V <sub>CC</sub> = Max

AC CHARACTERISTICS: V<sub>CC</sub> = +5.0 V, T<sub>A</sub> = +25° C (See Section 3 for waveforms and load configurations)

SYMBOL	PARAMETER	93XX		UNITS	CONDITIONS
		C <sub>L</sub> = 15 pF R <sub>L</sub> = 400 Ω			
		Min	Max		
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay M <sub>1</sub> to S <sub>3</sub>		51 52	ns	Figs. 3-1, 3-4
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay K <sub>0</sub> to S <sub>5</sub>		22 39	ns	Figs. 3-1, 3-5