

High-Speed, Low R_{ON} , SPDT Analog Switch (2:1 Multiplexer/Demultiplexer Bus Switch)

DESCRIPTION

The DG3157 is a high-speed single-pole double-throw, low power, TTL-Compatible bus switch. Using sub-micro CMOS technology, the DG3157 achieves low on-resistance and negligible propagation delay.

The DG3157 can handle both analog and digital signals and permits signals with amplitudes of up to V_{CC} to be transmitted in either direction.

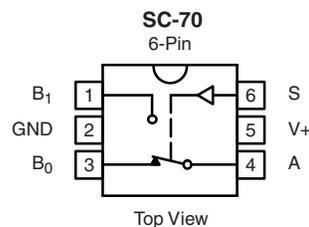
When the Select pin is low, B_0 is connected to the output A pin. When the Select pin is high, B_1 is connected to the output A pin. The path that is open will have a high-impedance state with respect to the output. Make-before-break is guaranteed. An epitaxial layer prevents latch-up.

FEATURES

- Halogen-free According to IEC 61249-2-21
- Direct cross to industry standard *SN74LVC1G3157*, *NC7SB3157*, *NLASB3175*, *PI5A3157*, and *STG3157*
- SC-70 6-lead package
- 1.65 V to 5.5 V V_{CC} operation
- 5 Ω connection between ports
- Minimal propagation delay
- Break-before-make switching
- Zero bounce in flow-through mode



RoHS
COMPLIANT
HALOGEN
FREE

FUNCTIONAL BLOCK DIAGRAM AND PIN CONFIGURATION


Device Marking: G1

TRUTH TABLE	
Logic Input (S)	Function
0	B_0 Connected to A
1	B_1 Connected to A

ORDERING INFORMATION		
Temp. Range	Package	Part Number
- 40 °C to 85 °C	SC-70-6	DG3157DL-T1-E3 DG3157DL-T1-GE3 (Halogen-free)



ABSOLUTE MAXIMUM RATINGS		
Parameter	Limit	Unit
Reference V+ to GND	- 0.3 to + 6	V
S, A, B ^a	- 0.3 to (V+ + 0.3)	
Continuous Current (Any terminal)	± 50	mA
Peak Current (Pulsed at 1 ms, 10 % duty cycle)	± 200	
Storage Temperature	D Suffix	°C
Power Dissipation (Packages) ^b	6-Pin SC-70 ^c	mW

Notes:

- a. Signals on A, or B or S exceeding V+ will be clamped by internal diodes. Limit forward diode current to maximum current ratings.
- b. All leads welded or soldered to PC board.
- c. Derate 3.1 mW/°C above 70 °C.

SPECIFICATIONS								
Parameter	Symbol	Test Conditions Unless Otherwise Specified V+ = 3.0 V, V _S = 0.25 V to 0.7 V+ ^e	Temp. ^a	Limits - 40 °C to 85 °C			Unit	
				Min. ^b	Typ. ^c	Max. ^b		
DC Characteristics								
High Level Input Voltage	V _{SH}	V+ = 1.65 to 1.95 V	Full	0.75 V+			V	
		V+ = 2.3 to 5.5 V	Full	0.7 V+				
Low Level Input Voltage	V _{SL}	V+ = 1.65 to 1.95 V	Full			0.25 V+	V	
		V+ = 2.3 to 5.5 V	Full			0.3 V+		
On Resistance	R _{ON}	V+ = 4.5 V	V _{BN} = 0 V, I _A = 30 mA	Full		6	7	Ω
			V _{BN} = 2.3 V, I _A = - 30 mA	Full		6	12	
			V _{BN} = 4.5 V, I _A = - 30 mA	Full		9	15	
		V+ = 3.0 V	V _{BN} = 0 V, I _A = 24 mA	Full		8	9	
			V _{BN} = 3.0 V, I _A = - 24 mA	Full		12	20	
		V+ = 2.3 V	V _{BN} = 0 V, I _A = 8 mA	Full		9	12	
			V _{BN} = 2.3 V, I _A = - 8 mA	Full		13	30	
		V+ = 1.65 V	V _{BN} = 0 V, I _A = 4 mA	Full		12	20	
V _{BN} = 1.8 V, I _A = - 4 mA	Full			18	50			
On Resistance Flatness	R _{FLAT}	0 < V _{BN} < V+	V+ = 4.5 V, I _A = - 30 mA	Room		6		
			V+ = 3.0 V, I _A = - 24 mA	Room		12		
			V+ = 2.3 V, I _A = - 8 mA	Room		22		
			V+ = 1.65 V, I _A = - 4 mA	Room		90		
On Resistance Matching Between Channels	ΔR _{ON}		V+ = 4.5 V, V _{BN} = 3.15 V, I _A = - 30 mA	Room		0.32		
			V+ = 3.0 V, V _{BN} = 2.1 V, I _A = - 24 mA	Room		0.31		
			V+ = 2.3 V, V _{BN} = 1.6 V, I _A = - 8 mA	Room		0.30		
			V+ = 1.65 V, V _{BN} = 1.15 V, I _A = - 4 mA	Room		0.29		
Input Leakage Current	I _S	V+ = 5.5 V, V _A = 5.5 V	Room Full	- 0.1 - 1.0		0.1 - 1.0	μA	
Off Stage Switch Leakage	I _{BN(off)}	V+ = 5.5 V, V _A /V _B = 0 V/5.5 V	Room Full	- 0.1 - 1.0		0.1 - 1.0		
On State Switch Leakage	I _{BN(on)}	V+ = 5.5 V, V _A /V _B = 0 V/5.5 V	Room Full	- 0.1 - 1.0		0.1 - 1.0		



SPECIFICATIONS								
Parameter	Symbol	Test Conditions Unless Otherwise Specified $V_+ = 3.0\text{ V}$, $V_S = 0.25\text{ V}$ to 0.7 V ^e		Temp. ^a	Limits - 40 °C to 85 °C			Unit
					Min. ^b	Typ. ^c	Max. ^b	
Power Supply								
Power Supply Range	V_+			Full	1.65		5.5	V
Quiescent Supply Current	I_+	$V_+ = 5.5\text{ V}$, $V_A = V_B = V_+$ or GND		Room Full			1 10	μA
AC Electrical Characteristic								
Prop Delay Time ^f	t_{PHL}/t_{PLH}	$V_A = 0\text{ V}$	$V_+ = 1.65\text{ to }1.95\text{ V}$	Full				ns
			$V_+ = 2.3\text{ to }2.7\text{ V}$	Full		1.2		
			$V_+ = 3.0\text{ to }3.6\text{ V}$	Full		0.8		
			$V_+ = 4.5\text{ to }5.5\text{ V}$	Full		0.3		
Output Enable Time ^f	t_{PZL}/t_{PZH}	$V_{LOAD} = 2 \times V_+$ for t_{PZL} $V_{LOAD} = 0\text{ V}$ for t_{PZH}	$V_+ = 1.65\text{ to }1.95\text{ V}$	Room Full		10.2 10.4		ns
			$V_+ = 2.3\text{ to }2.7\text{ V}$	Room Full		5.9 6.2		
			$V_+ = 3.0\text{ to }3.6\text{ V}$	Room Full		4.1 4.5		
			$V_+ = 4.5\text{ to }5.5\text{ V}$	Room Full		2.6 2.9		
Output Disable Time ^f	t_{PLZ}/t_{PHZ}	$V_{LOAD} = 2 \times V_+$ for t_{PLZ} $V_{LOAD} = 0\text{ V}$ for t_{PHZ}	$V_+ = 1.65\text{ to }1.95\text{ V}$	Room Full		10.2 10.4		ns
			$V_+ = 2.3\text{ to }2.7\text{ V}$	Room Full		5.9 6.2		
			$V_+ = 3.0\text{ to }3.6\text{ V}$	Room Full		4.1 4.5		
			$V_+ = 4.5\text{ to }5.5\text{ V}$	Room Full		2.6 2.9		
Break-Before-Make Time ^d	t_{BBM}	$V_+ = 1.65\text{ to }1.95\text{ V}$		Full	0.5			ns
		$V_+ = 2.3\text{ to }2.7\text{ V}$		Full	0.5			
		$V_+ = 3.0\text{ to }3.65\text{ V}$		Full	0.5			
		$V_+ = 4.5\text{ to }5.5\text{ V}$		Full	0.5			
Charge Injection ^d	Q	$C_L = 0.1\text{ nF}$, $V_{GEN} = 0\text{ V}$ $R_{GEN} = 0\ \Omega$	$V_+ = 5\text{ V}$	Room		7		μC
			$V_+ = 3.3\text{ V}$	Room		3		
Analog Switch Characteristics								
Off Isolation ^d	OIRR	$R_L = 50\ \Omega$, $f = 10\text{ MHz}$		Room		- 57.6		dB
Crosstalk ^d	X_{TALK}			Room		- 58.7		
- 3 db Bandwidth ^d	BW	$R_L = 50\ \Omega$		Room		> 250		MHz
Capacitance								
Control Pin Capacitance ^d	C_{IN}	$V_+ = 0\text{ V}$		Room		4.9		μF
B Port Off Capacitance ^d	C_{IO-B}	$V_+ = 5\text{ V}$		Room		< 6.5		
A Port Capacitance When Switch Enable ^d	$C_{IO-A(on)}$			Room		< 18.5		

Notes:

- a. Room = 25 °C, Full = as determined by the operating suffix.
- b. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
- c. Typical values are for design aid only, not guaranteed nor subject to production testing.
- d. Guarantee by design, nor subjected to production test.
- e. V_{IN} = input voltage to perform proper function.
- f. Guaranteed by design and not production tested. The bus switch propagation delay is a function of the RC time constant contributed by the on-resistance and the specified load capacitance with an ideal voltage source (zero output impedance) driving the switch.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

LOGIC DIAGRAM Positive Logic

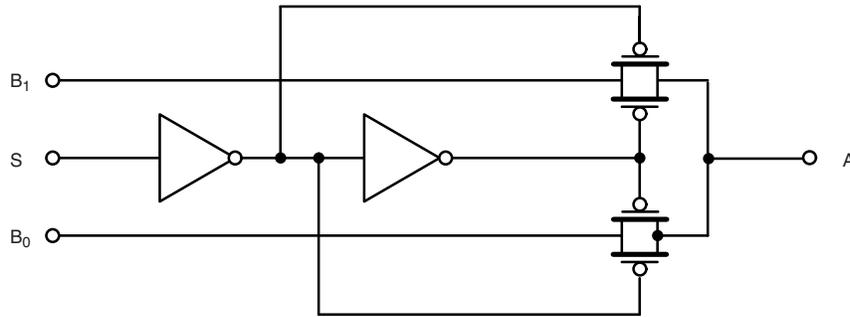
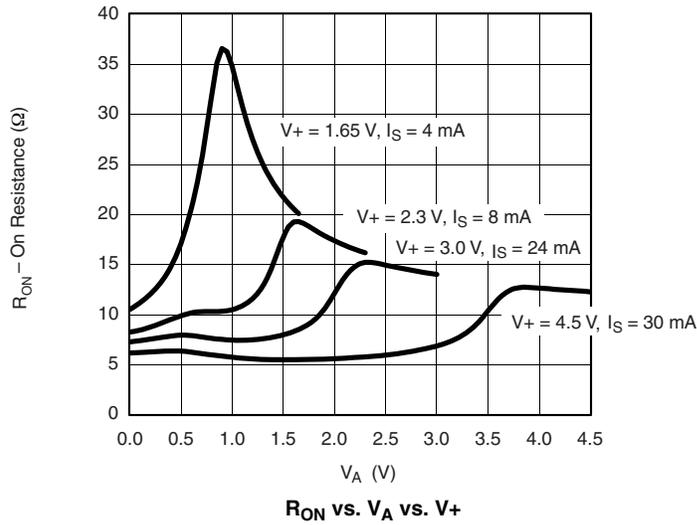


Figure 1.

TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



AC LOADING AND WAVEFORMS

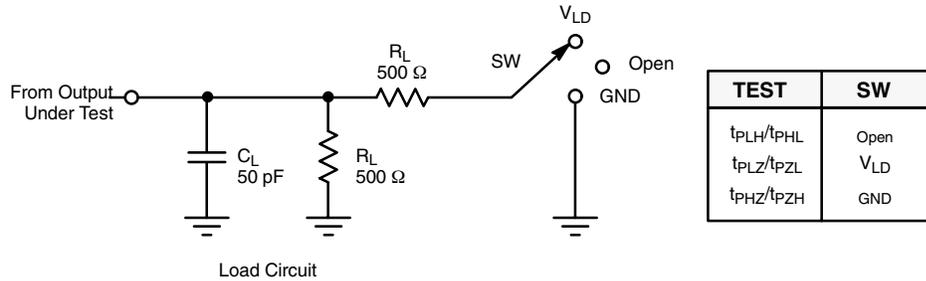


Figure 2. AC Test Circuit

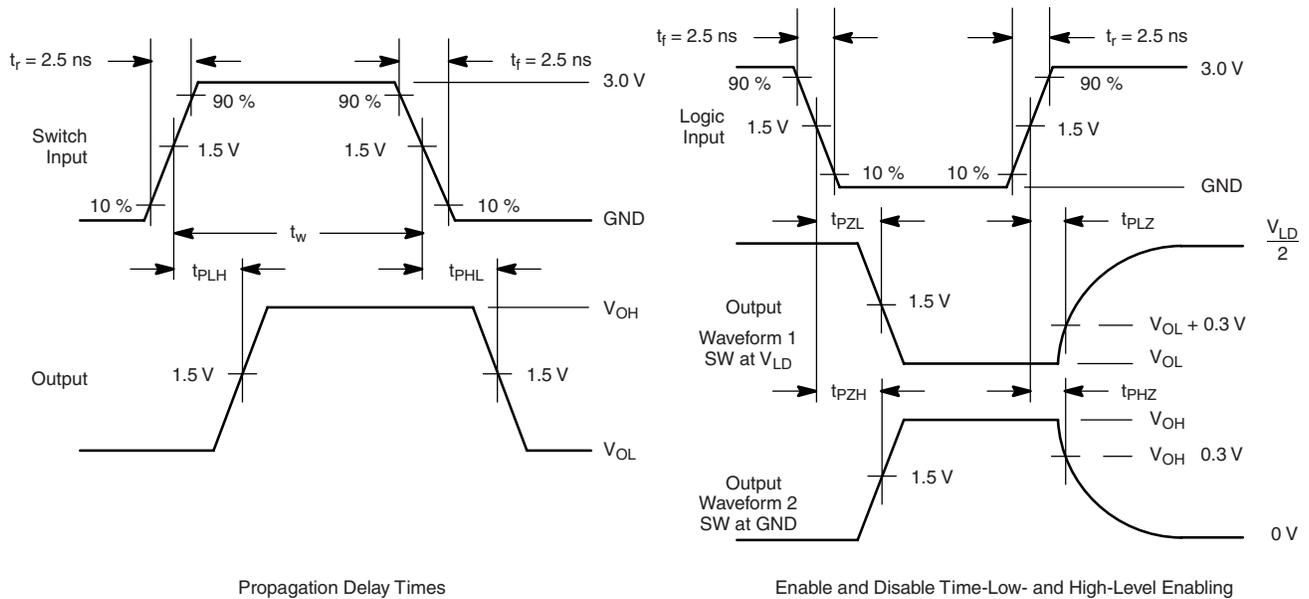
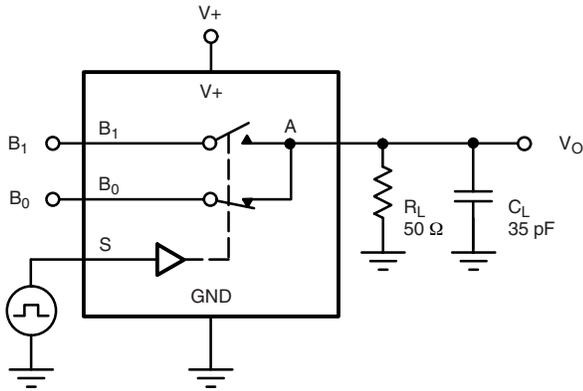


Figure 3. AC Waveforms

Notes:

- C_L includes probe and jig capacitance.
- Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.
- Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- All input pulses are supplied by generators having the following characteristics: $PRR \leq 10$ MHz, $Z_O = 50 \Omega$.
- The outputs are measured one at a time with one transition per measurement.
- t_{PLZ} and t_{PHZ} are the same as t_{dis} .
- t_{PZL} and t_{PZH} are the same as t_{dis} .
- t_{PLH} and t_{PHL} are the same as t_{dis} .
- $V_{LD} = 2$ V+.

TEST CIRCUITS



C_L (includes fixture and stray capacitance)

Figure 4. Break-Before-Make Interval

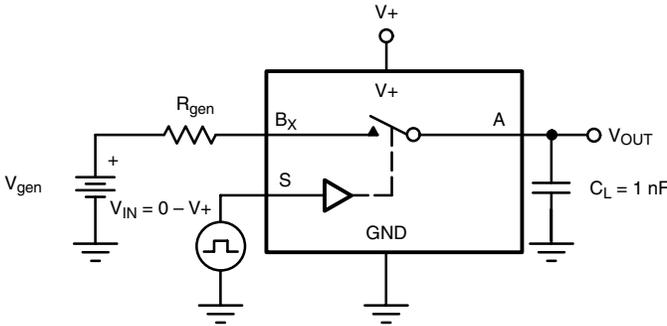
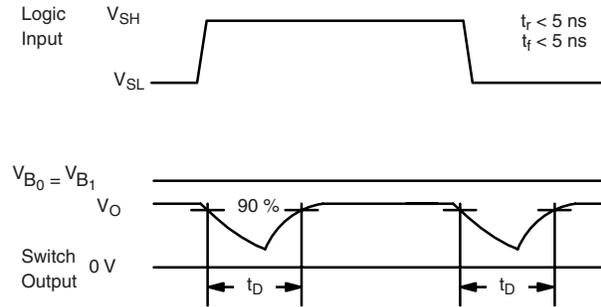
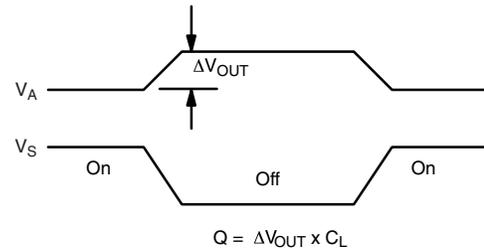


Figure 5. Charge Injection



IN depends on switch configuration: input polarity determined by sense of switch.

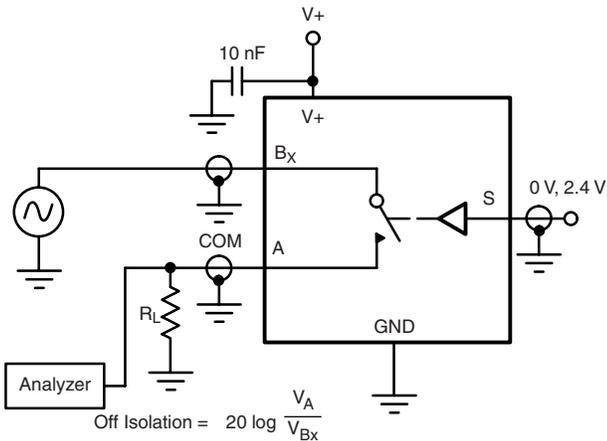


Figure 6. Off-Isolation

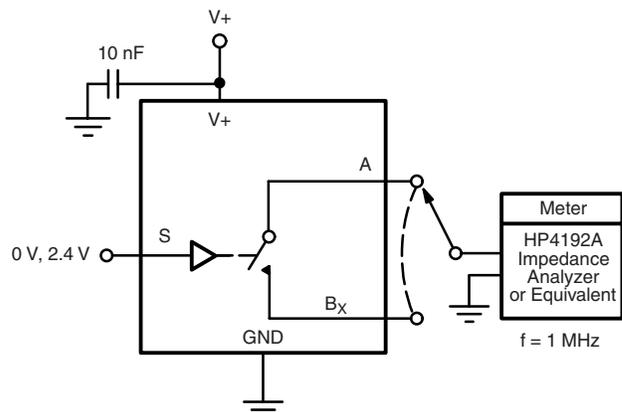
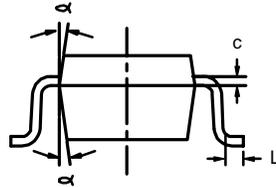
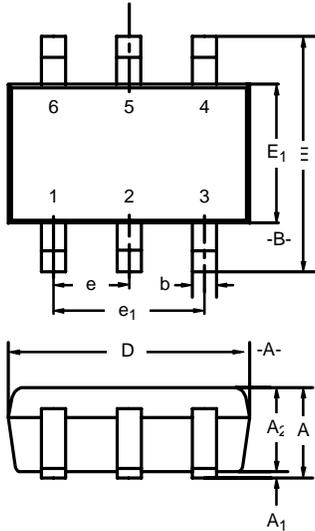


Figure 7. Channel Off/On Capacitance

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SC-70: 6-LEADS



Dim	MILLIMETERS			INCHES		
	Min	Nom	Max	Min	Nom	Max
A	0.90	-	1.10	0.035	-	0.043
A ₁	-	-	0.10	-	-	0.004
A ₂	0.80	-	1.00	0.031	-	0.039
b	0.15	-	0.30	0.006	-	0.012
c	0.10	-	0.25	0.004	-	0.010
D	1.80	2.00	2.20	0.071	0.079	0.087
E	1.80	2.10	2.40	0.071	0.083	0.094
E ₁	1.15	1.25	1.35	0.045	0.049	0.053
e	0.65BSC			0.026BSC		
e ₁	1.20	1.30	1.40	0.047	0.051	0.055
L	0.10	0.20	0.30	0.004	0.008	0.012
α	7°Nom			7°Nom		

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