

# M62342P/FP, M62343P/FP

8-Bit D/A Converter (Buffered)

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#### **Description**

The M62342 and M62343 are CMOS-structure semiconductor integrated circuits incorporating two or three 8-bit D/A converter channels with output buffer op-amps.

Serial data transfer type input can easily be used through a combination of three lines: DI, CLK, and LD.

Outputs incorporate buffer op-amps that have a drive capacity of 1 mA or above for both sink and source, and can operate over the entire voltage range from almost ground to  $V_{CC}$  (0 to 5 V), making peripheral elements unnecessary and enabling configuration of a system with few component parts.

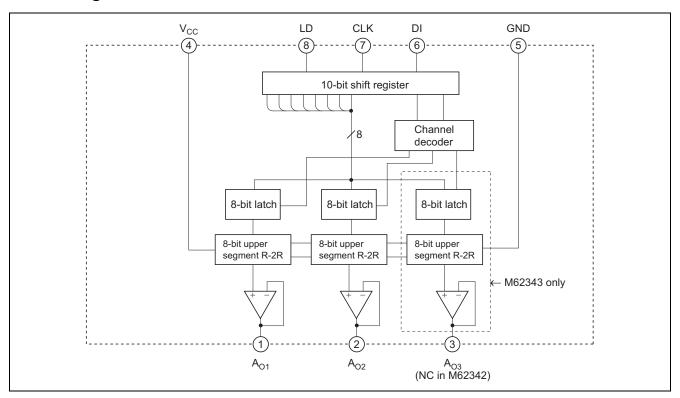
#### **Features**

- Data transfer format
   10-bit serial data input type
- Output buffer op-amps Operable over entire voltage range from almost ground to  $V_{CC}$  (0 to 5 V)
- High output current capacity ±1 mA or higher

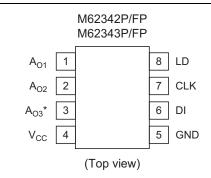
### **Application**

Signal gain setting and automatic adjustment in CTV, and display monitors, conversion from digital data to analog data in consumer and industrial products

### **Block Diagram**



### **Pin Arrangement**



Outline: PRDP0008AA-A (8P4) [P] (not recommend for new design) PRSP0008DE-C [FP] (recommend)

PRSP0008DA-A (8P2S-A) [FP] (not recommend for new design)

Note: Pin 3 of the M62342 is a NC pin.

# **Pin Description**

Pin No.	Symbol	Function
6	DI	Serial data input pin. Inputs serial data with a 10-bit data length.
7	CLK	Serial clock input pin. Input signal from DI pin is input to 10-bit shift register at rise of shift clock.
8	LD	Load pin. When "H" level is input to LD pin, value in 10-bit shift register is loaded into decoder and D/A output register.
1	A <sub>O1</sub>	8-bit resolution D/A converter output pins
2	A <sub>O2</sub>	(After power-on, all channels are reset and DAC data 00h is output.)
3	A <sub>O3</sub> (M62343 only)	
4	V <sub>CC</sub>	Power supply voltage pin
5	GND	GND pin

# **Absolute Maximum Ratings**

Item	Symbol	Rated Value	Unit
Power supply voltage	V <sub>CC</sub>	-0.3 to 7.0	V
Input voltage	Vin	$-0.3$ to $V_{CC} + 0.3 \le 7.0$	V
Output voltage	Vo	$-0.3$ to $V_{CC} + 0.3 \le 7.0$	V
Internal power consumption	Pd	417 (P) / 272 (FP)	mW
Operating ambient temperature	Topr	-20 to +85	°C
Storage temperature	Tstg	-40 to +125	°C

# **Electrical Characteristics**

(Unless specified otherwise,  $V_{CC}$  = +5 V ±10%, GND = 0 V, Ta = -20°C to 85°C)

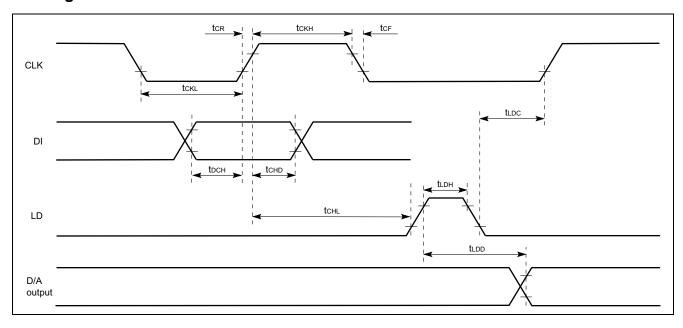
		Specification Values						
Item	Symbol	Min	Тур	Max	Unit	Test Conditions		
Power supply voltage	V <sub>CC</sub>	2.7	5.0	5.5	V			
Power supply current	I <sub>CC</sub>	0	0.7 (M62342) 0.8 (M62343)	2.5 (M62342) 2.7 (M62343)	mA	At CLK = 1 MHz operation, $I_{AO}$ = 0 $\mu A$ D/A data: 6 Ah (at maximum current)		
		0	0.5 (M62342) 0.6 (M62343)	1.6 (M62342) 1.8 (M62343)		DI = CLK = LD = GND, $I_{AO} = 0 \mu A$		
Input leakage current	I <sub>ILK</sub>	-10	_	10	μΑ	$V_{IN} = 0$ to $V_{CC}$		
Input voltage "L"	V <sub>IL</sub>	0	_	0.2V <sub>CC</sub>	V			
Input voltage "H"	V <sub>IH</sub>	0.5V <sub>CC</sub>	_	V <sub>CC</sub>	V			
Buffer amp output	V <sub>AO</sub>	0.1	_	V <sub>CC</sub> -0.1	V	$I_{AO} = \pm 100 \mu A$		
voltage range		0.2	_	V <sub>CC</sub> -0.2		$I_{AO} = \pm 500 \mu\text{A}$		
Buffer amp output drive range	I <sub>AO</sub>	-1.0	_	1.0	mA	Upper saturation voltage = 0.3 V Lower saturation voltage = 0.2 V		
Differential nonlinearity error	S <sub>DL</sub>	-1.0	_	1.0	LSB	$V_{CC} = 5.12 \text{ V } (20 \text{ mV/LSB})$ No load (I <sub>AO</sub> = 0)		
Nonlinearity error	S <sub>L</sub>	-1.5	_	1.5	LSB			
Zero point error	S <sub>ZERO</sub>	-2.0	_	2.0	LSB			
Full-scale error	S <sub>FULL</sub>	-2.0	_	2.0	LSB			
Oscillation limit output capacitance	Co	_	_	0.1	μF			
Buffer amp output impedance	Ro	_	5.0	_	Ω			

# **AC Characteristics**

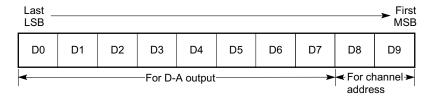
(Unless specified otherwise,  $V_{CC}$  = +5 V ±10%, GND = 0 V, Ta = -20°C to 85°C)

		Specification Values				
Item	Symbol	Min	Тур	Max	Unit	Test Conditions
Clock "L" pulse width	t <sub>CKL</sub>	200	_		ns	
Clock "H" pulse width	t <sub>CKH</sub>	200	_		ns	
Clock rise time	t <sub>CR</sub>	1	_	200	ns	
Clock fall time	t <sub>CF</sub>	1	_	200	ns	
Data setup time	t <sub>DCH</sub>	30	_	_	ns	
Data hold time	t <sub>CHD</sub>	60	_	_	ns	
Load setup time	t <sub>CHL</sub>	200	_	_	ns	
Load hold time	t <sub>LDC</sub>	100	_	_	ns	
Load "H" pulse width	t <sub>LDH</sub>	100	_	_	ns	
D-A output settling time	t <sub>LDD</sub>	_	_	300	μS	Until output reaches last 1/2 LSB

# **Timing Chart**



# **Digital Data Format**



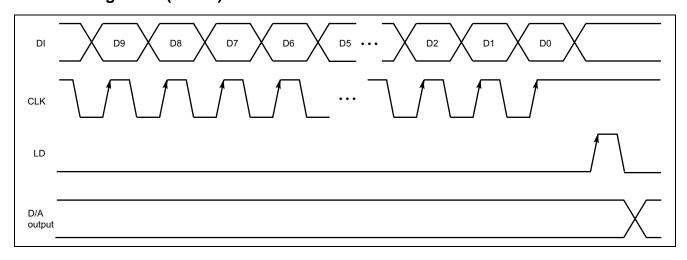
#### **Channel Select Data**

D8	D9	Channel Selection			
0	0	AO1 selected			
1	0	AO2 selected			
0	1	M62343 : AO3 selected			
		M62343 Don't care			
1	1	Don't care			

#### **DAC Data**

D0	D1	D2	D3	D4	D5	D6	D7	DAC output
0	0	0	0	0	0	0	0	V <sub>CC</sub> /256×1
1	0	0	0	0	0	0	0	V <sub>CC</sub> /256×2
0	1	0	0	0	0	0	0	V <sub>CC</sub> /256×3
1	1	0	0	0	0	0	0	V <sub>CC</sub> /256×4
•	•	•	•	•	•	•	•	•
	:	•	•	:	:	•	•	:
	•	•	-	•	,	-	•	-
0	1	1	1	1	1	1	1	V <sub>CC</sub> /256×255
1	1	1	1	1	1	1	1	V <sub>CC</sub> /256×256

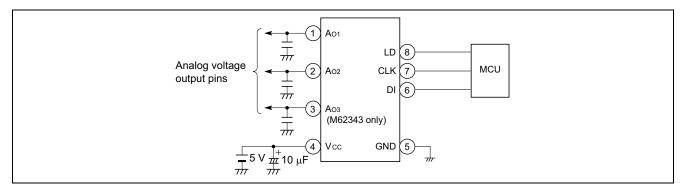
# **Data Timing Chart (Model)**



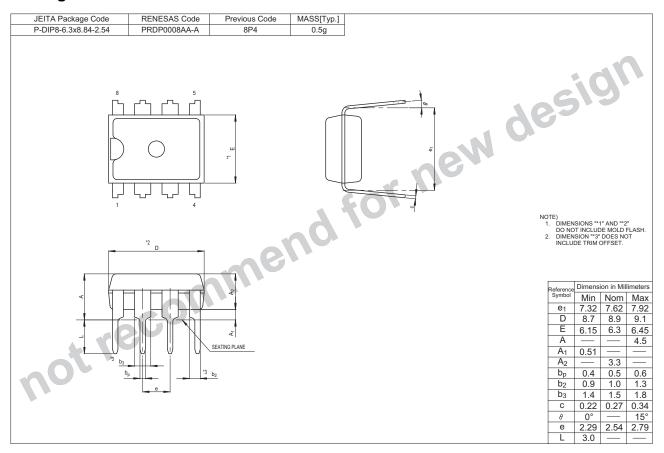
### **Usage Notes**

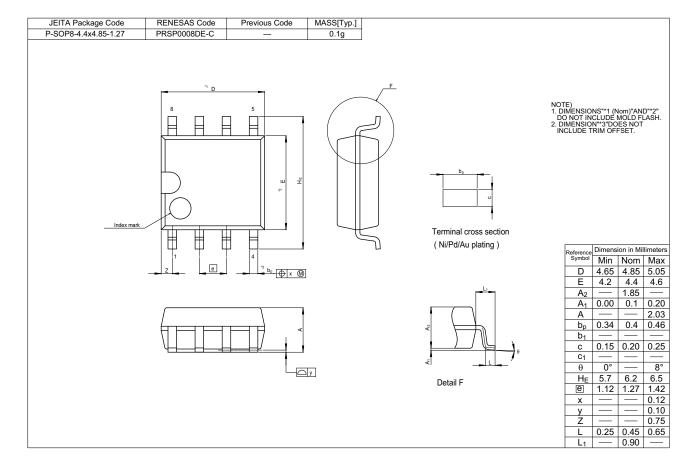
- 1. With this IC, D/A converter upper reference voltage setting is performed by means of the power supply voltage. If ripples or spikes are imposed on this pin, conversion accuracy may fall. When using this IC, a capacitor must be inserted between the power supply pin and GND in order to ensure stable D/A conversion.
- 2. The output buffer amps of this IC are highly tolerant of capacitive loads. Therefore, connecting capacitors (0.1  $\mu$ F max.) between the output pins and ground in order to eliminate jitter or noise due to output line wiring presents no problems whatever in terms of operation.

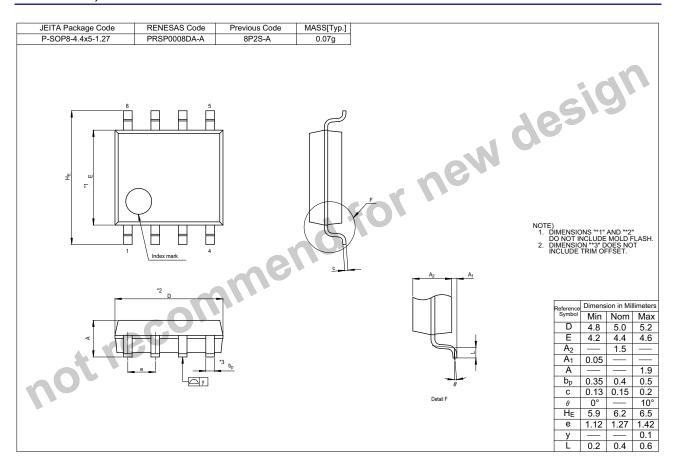
### **Sample Standard Application Circuit**



### **Package Dimensions**







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