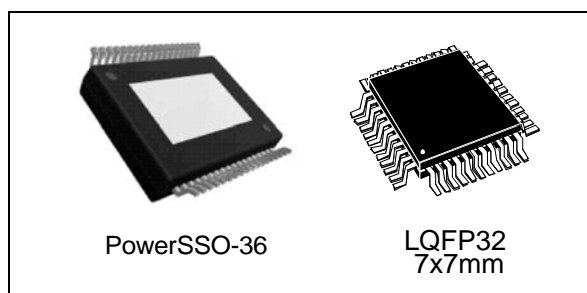


## Motor bridge driver for automotive applications

Datasheet - production data



### Applications

- Wiper
- Power door
- Seat belt tensioner
- Seat positioning
- Valve tronic
- Park break
- 2H motors

### Features

- Operating supply voltage 6 V to 28 V
- Central 2 stage charge pump
- 100% duty cycle
- Full  $R_{DS(on)}$  down to 6 V (normal level MOSFETs)
- Control of reverse battery protection MOSFET
- Charge pump current limited
- PWM operation up to 30 kHz
- SPI interface
- Current sense amplifier / free configurable
- Zero adjust for end of line trimming
- Power management: programmable free wheeling
- Sensing circuitry of external MOSFETs with embedded thermal sensors

### Description

The L99H01 is designed to control 4 external N-channel MOS transistors in bridge configuration for DC-motor driving in automotive applications. A free configurable current sense amplifier is integrated. The integrated standard serial peripheral interface (SPI) controls all outputs and provides diagnostic information. An interface pin for the thermal sensors of the external MOSFETs is implemented.

Table 1. Device summary

Package	Order codes		
	Part number (tube)	Part number (tape and reel)	Part number (tray)
PowerSSO-36	L99H01XP	L99H01XPTR	—
LQFP32	—	L99H01QFTR	L99H01QF

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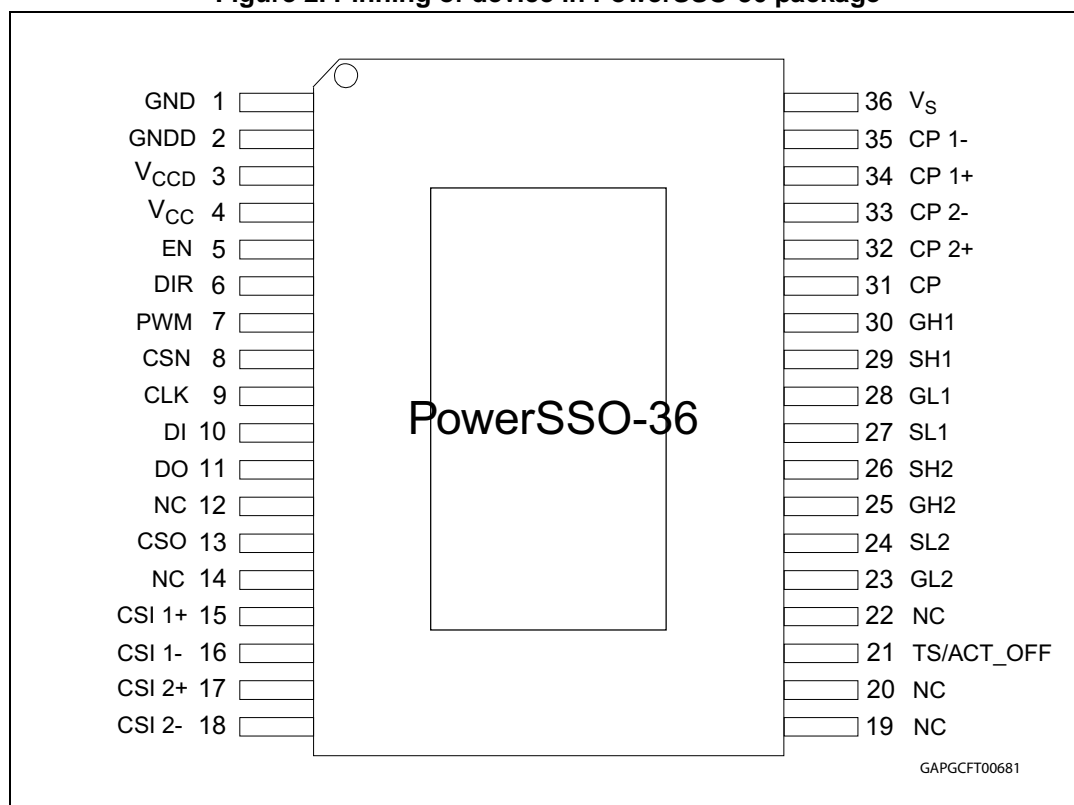


Table 2. Pin definitions and functions (continued)

Pin	Symbol	Function
9	CLK	Serial clock input: this input controls the internal shift register of the SPI and requires CMOS logic levels. This input has a pull-down current.
10	DI	Serial data in: the input requires CMOS logic levels and receives serial data from the microcontroller. The data is an 8-bit control word and the most significant bit (MSB, bit 7) is transferred first. This input has a pull-down current.
11	DO	Serial data out: the diagnosis data is available via the SPI and this tristate-output. The output remains in tristate, if the chip is not selected by the input CSN (CSN = high).
12, 14, 19, 20, 22	NC	Not connected.
13	CSO	Current sense amplifier output: $V_{CC}$ compatible.
15	CSI1+	Current sense amplifier input: positive input 1, multiplexible.
16	CSI1-	Current sense amplifier input: negative input 1, multiplexible.
17	CSI2+	Current sense amplifier input: positive input 2, multiplexible.
18	CSI2-	Current sense amplifier input: negative input 2, multiplexible.
21	TS/ ACT_OFF	Thermal sensor interface or input to switch all driver active off.
23	GL2	Gate driver for PowerMOS low-side switch in halfbridge 2.
24	SL2	Source of low-side switch in halfbridge 2.
25	GH2	Gate driver for PowerMOS high-side switch in halfbridge 2.
26	SH2	Source/drain of halfbridge 2.
27	SL1	Source of low-side switch in halfbridge 1.
28	GL1	Gate driver for PowerMOS low-side switch in halfbridge 1.
29	SH1	Source/drain of halfbridge 1.
30	GH1	Gate driver for PowerMOS high-side switch in halfbridge 1.
31	CP	Charge pump output.
32	CP2+	Charge pump pin for capacitor 2, positive side.
33	CP2-	Charge pump pin for capacitor 2, negative side.
34	CP1+	Charge pump pin for capacitor 1, positive side.
35	CP1-	Charge pump pin for capacitor 1, negative side.
36	$V_S$	Power supply voltage (external reverse protection required). For EMI reason a ceramic capacitor as close as possible to GND is recommended.



Figure 2. Pinning of device in PowerSSO-36 package



1. The slug is connected to pin 1.

## 1.2 Pinout LQFP32

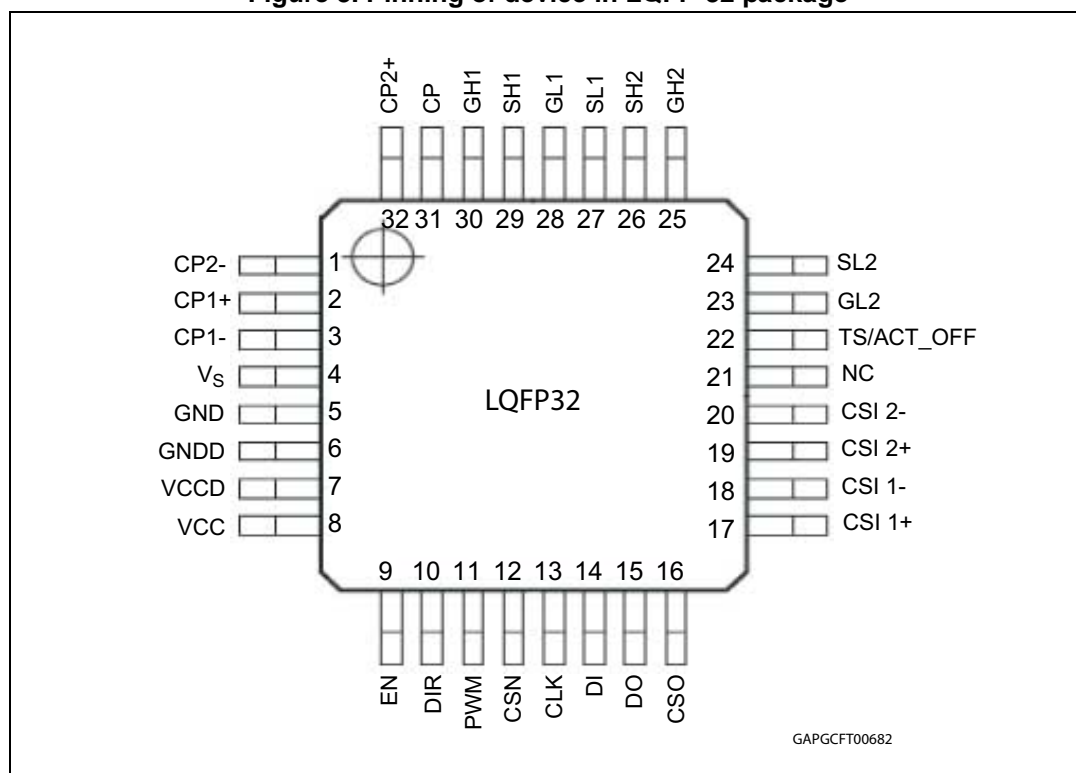
Table 3. Pin definitions and functions

Pin	Symbol	Function
1	CP2-	Charge pump pin for capacitor 2, negative side.
2	CP1+	Charge pump pin for capacitor 1, positive side.
3	CP1-	Charge pump pin for capacitor 1, negative side.
4	$V_S$	Power supply voltage (external reverse protection required). For EMI reason a ceramic capacitor as close as possible to GND is recommended.
5	GND	Ground. Reference potential, connected to slug.
6	GNDD	Digital ground. Reference potential.
7	$V_{CCD}$	Logic voltage supply 3.3 V/5 V: for this input a ceramic capacitor as close as possible to GND is recommended.
8	$V_{CC}$	Analog voltage supply 3.3 V/5 V: for this input a ceramic capacitor as close as possible to GND is recommended.
9	EN	Enable input. The enable input has a pull-down resistor.

Table 3. Pin definitions and functions (continued)

Pin	Symbol	Function
10	DIR	Direction select input for H-bridge control. This input has a pull-down current.
11	PWM	PWM input for H-bridge control. This input has a pull-down current.
12	CSN	Chip select not input: this input is low active and requires CMOS logic levels. The serial data transfer between L99H01 and microcontroller is enabled by pulling the input CSN to low-level. This input has a pull-up current.
13	CLK	Serial clock input: this input controls the internal shift register of the SPI and requires CMOS logic levels. This input has a pull-down current.
14	DI	Serial data in: the input requires CMOS logic levels and receives serial data from the microcontroller. The data is an 8-bit control word and the most significant bit (MSB, bit 7) is transferred first. This input has a pull-down current.
15	DO	Serial data out: the diagnosis data is available via the SPI and this tristate-output. The output remains in tristate, if the chip is not selected by the input CSN (CSN = high).
16	CSO	Current sense amplifier output: $V_{CC}$ compatible.
17	CSI1+	Current sense amplifier input: positive input 1, multiplexible.
18	CSI1-	Current sense amplifier input: negative input 1, multiplexible.
19	CSI2+	Current sense amplifier input: positive input 2, multiplexible.
20	CSI2-	Current sense amplifier input: negative input 2, multiplexible.
21	NC	Not connected.
22	TS/ ACT_OFF	Thermal sensor interface or external off for all gate drivers.
23	GL2	Gate driver for PowerMOS low-side switch in halfbridge 2.
24	SL2	Source of low-side switch in halfbridge 2.
25	GH2	Gate driver for PowerMOS high-side switch in halfbridge 2.
26	SH2	Source/drain of halfbridge 2.
27	SL1	Source of low-side switch in halfbridge 1.
28	GL1	Gate driver for PowerMOS low-side switch in halfbridge 1.
29	SH1	Source/drain of halfbridge 1.
30	GH1	Gate driver for PowerMOS high-side switch in halfbridge 1.
31	CP	Charge pump output.
32	CP2+	Charge pump pin for capacitor 2, positive side.

Figure 3. Pinning of device in LQFP-32 package



## 2 Electrical specifications

### 2.1 Absolute maximum ratings

Stressing the device above the rating listed in [Table 4](#) may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

**Table 4. Absolute maximum ratings**

Item	Symbol	Parameter	Value	Unit
4.1.1	$V_S$	Power supply voltage	-0,3 to 35	V
4.1.2		Single pulse $t_{max} < 400$ ms	40	V
4.2	$V_{CC}$	Stabilished supply voltage	-0.3 to 5.5	V
4.3	DI, DO, CLK, CSN, EN, DIR, PWM	Digital input / output voltage	-0.3 to $V_{CC} + 0.3$	V
4.4	CSO, TS	Analog input / output voltage	-0.3 to $V_{CC} + 0.3$	V
4.5	CSI1+, CSI1-, CSI2+, CSI2-	HV signal pins	-4 to $V_S + 5V$	V
4.6	GL2, GH2, GL1, GH1 (Gxy)	HV signal pins	$S_{xy} - 1$ to $S_{xy} + 10$ ; $V_{CP} + 0.3$	V
4.7	SL2, SH2, SL1, SH1	HV signal pins	-6 to 40	V
4.8	CP2- CP1-	HV signal pins	-0.3 to $V_S + 0.3$	V
4.9	CP1+	HV signal pins	$V_S - 0.3$ to $V_S + 10$	V
4.10	CP2+	HV signal pins	$V_S - 0.6$ to $V_S + 10$	V
4.11	CP	Power pin	$V_S - 0.3$ to $V_S + 10$	V

### 2.2 ESD protection

**Table 5. ESD protection**

Item	Parameter	Value	Unit
5.1	All pins	$\pm 2$ <sup>(1)</sup>	kV
5.2	$V_S$ versus GND	$\pm 4$ <sup>(1)</sup>	kV

1. - HBM according to MIL 883C, Method 3015.7 or EIA/JESD22-A114-A.  
 - HBM with all unzapped pins grounded.

## 2.3 Thermal data

**Table 6. Operating junction temperature**

Item	Symbol	Parameter	Value	Unit
6.1	$T_j$	Operating junction temperature	-40 to 150	°C

**Table 7. Temperature warning and thermal shutdown**

Item	Symbol	Parameter	Min.	Typ.	Max.	Unit
7.1	$T_{jTW\ ON}$	Temperature warning threshold junction temperature	135	—	165	°C
7.2	$T_{jSD\ ON}$	Thermal shutdown threshold junction temperature	155	—	185	°C
7.3	$T_{jSD\ OFF}$	Thermal shutdown threshold junction temperature	150	—	180	°C

**Table 8. Packages thermal resistance**

Item	Symbol	Parameter	Value		Unit
			PowerSSO-36	LQFP32	
8.1	$R_{thj-amb}$	Thermal resistance junction-ambient (max.)	58 <sup>(1)</sup>	80 <sup>(1)</sup>	°C/W

1. Minimum footprint.

## 2.4 Electrical characteristics

$V_S = 6\text{ V to }28\text{ V}$ ,  $V_{CC} = 3\text{ V to }5.3\text{ V}$ ,  $T_j = -40^\circ\text{C to }150^\circ\text{C}$ , unless otherwise specified.

The voltages are referred to GND and currents are assumed positive, when the current flows into the pin.

**Table 9. Supply**

Item	Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
9.1	$V_S$	Operating supply voltage range		6		28	V
9.2	$V_{VS\_OV1}$	Overvoltage disable high threshold 1	SPI: OVT = 1	28	30.5	32	V
9.3	$V_{VS\_OV1H}$	Overvoltage threshold 1 hysteresis		0.57	0.77	1.07	V
9.4	$V_{VS\_OV2}$	Overvoltage disable high threshold 2	SPI: OVT = 0	18	20	22	V
9.5	$V_{VS\_OV2H}$	Overvoltage threshold 2 hysteresis		0.42	0.62	0.82	V

Table 9. Supply (continued)

Item	Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
9.6	$V_{VS\_UV}$	Undervoltage disable low threshold		4.7	4.9	5.1	V
9.7	$V_{VS\_UVH}$	Undervoltage threshold hysteresis		0.2	0.3	0.4	V
9.8.1	$I_S$	$V_S$ DC supply current	$V_S = 13\text{ V}$ ; $V_{CC} = 5\text{ V}$ ; Active mode; Outputs floating	4.5	5.5	6.5	mA
9.8.2			$V_S = 6\text{ V to }28\text{ V}$ ; $V_{CC} = 5.0\text{ V}$ ; Active mode; Outputs floating	2.5		18	mA
9.9	$I_{SL}$	$V_S$ quiescent supply current	$V_S = 13\text{ V}$ ; $V_{CC} = 0\text{ V}$ ; Standby mode; $T_{Test} = -40^\circ\text{C}, 25^\circ\text{C}$ ; Outputs floating			5	$\mu\text{A}$
9.10	$I_{CC}$	$V_{CC}$ DC supply current	$V_S = 13\text{ V}$ ; $V_{CC} = 5\text{ V}$ ; active mode	1.5	1.8	2.5	mA
9.11	$I_{CC}$	$V_{CC}$ quiescent supply current	$V_{CC} = 5\text{ V}$ ; standby mode	30	70	150	$\mu\text{A}$
9.12	$I_{CCd}$	$V_{CCd}$ supply current	$V_S = 13\text{ V}$ ; $V_{CC} = V_{CCd} = 5\text{ V}$ ; active mode	250	500	750	$\mu\text{A}$

Table 10. Undervoltage detection

Item	Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
10.1	$V_{POR\ OFF}$	Power-on reset threshold	$V_{CC}$ increasing	2.2	2.55	2.8	V
10.2	$V_{POR\ ON}$	Power-on reset threshold	$V_{CC}$ decreasing	2.0	2.25	2.6	V
10.3	$V_{POR\ hyst}$	Power-on reset hysteresis	$V_{POR\ OFF} - V_{POR\ ON}$	0.2	0.3	0.4	V

Table 11. Watchdog

Item	Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
11.1	$T_{WDTO}$	Watchdog time out	—	50	60	100	ms

Table 12. Inputs: CSN, CLK, PWM, DIR, EN and DI

Item	Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
12.1	$V_{in\ L}$	Low-level input voltage		$0.3 * V_{CC}$	$0.4 * V_{CC}$		V
12.2	$V_{in\ H}$	High-level input voltage			$0.6 * V_{CC}$	$0.7 * V_{CC}$	V
12.3	$V_{in\ Hyst}$	Input voltage hysteresis		$0.1 * V_{CC}$			V
12.4	$I_{CSN\ in}$	Pull-up current at input CSN	$V_{CSN} = V_{CC} - 1.5\ V$	-50	-25	-10	$\mu A$
12.5	$I_{CLK\ in}$	Pull-down current at input CLK	$V_{CLK} = 1.5\ V$	10	35	50	$\mu A$
12.6	$I_{DI\ in}$	Pull-down current at input DI	$V_{DI} = 1.5\ V$	10	35	50	$\mu A$
12.7	$I_{DIR\ in}$	Pull-down current at input DIR	$V_{DIR} = 1.5\ V$	10	35	50	$\mu A$
12.8	$I_{PWM\ in}$	Pull-down current at input PWM	$V_{PWM} = 1.5\ V$	10	35	50	$\mu A$
12.9	$R_{EN\ in}$	Pull-down resistance at input EN	$V_{EN} = V_{CC}$	100	210	480	k $\Omega$
12.10	$C_{in}^{(1)}$	Input capacitance at input CSN, CLK, DI, DIR and PWM	$0\ V < V_{CC} < 5.3\ V$		10	15	pF

1. Value of input capacity is not measured in production test. Parameter guaranteed by design.

Table 13. Charge pump output

Item	Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
13.1.1	$V_{CP}$	Charge pump output voltage	$V_S = 6\ V; I_{CP} = 15\ mA$	$V_S + 6$	$V_S + 7$	$V_S + 7.5$	V
13.1.2			$V_S = 10\ V; I_{CP} = 15\ mA$	$V_S + 11$	$V_S + 12$	$V_S + 13.5$	V
13.1.3			$V_S > 12\ V; I_{CP} = 15\ mA$	$V_S + 11$	$V_S + 12$	$V_S + 13.5$	V
13.2	$I_{CP}$	Charge pump output current	$f_{CP} = f_{SYS\_CLK} / 32;$ $V_S = 14\ V; V_{CP} = V_S + 10\ V$	26	38	48	mA
13.3	$V_{CP\_LOW}$	Charge pump low threshold voltage		$V_S + 4.5$	$V_S + 5$	$V_S + 5.5$	V
13.4.1	$f_{SYS\_CLK}$	Clock frequency (internal oscillator)	$V_{CC} = 5\ V$	3	4	4.5	MHz
13.4.2			$V_{CC} = 3\ V$	2.4	3.3	3.5	MHz
13.5	$T_{CP}$	Charge pump low filter time			64		$\mu s$

Table 14. Gate drivers for external PowerMOS

Item	Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
Drivers for external high-side PowerMOS							
14.1	$I_{GHx(on)}$	Turn on current (SOURCE stage)	$T_j = 25^\circ\text{C}$ <sup>(1)</sup>	0.3	0.5 <sup>(2)</sup>	0.8	A
14.2.1	$R_{GHx}$	On-resistance of SINK stage	$V_{SHx} = 0\text{ V}; I_{GHx} = 50\text{ mA}; T_j = 25^\circ\text{C}$	3	4	5	W
14.2.2			$V_{SHx} = 0\text{ V}; I_{GHx} = 50\text{ mA}; T_j = 125^\circ\text{C}$	4.5	5.3	7	W
14.3	$V_{GHxH}$	Gate on voltage	Outputs floating	$V_{SHx} + 8\text{ V}$	$V_{SHx} + 10\text{ V}$	$V_{SHx} + 12\text{ V}$	V
14.4	$R_{GSHx}$	Passive Gate clamp resistance		11	13	15	k $\Omega$
Drivers for external low-side PowerMOS							
14.5	$I_{GLx(on)}$	Turn on current (SOURCE stage)	$T_j = 25^\circ\text{C}$ <sup>(1)</sup>	0.3	0.5 <sup>(2)</sup>	0.8	A
14.6.1	$R_{GLx}$	On-resistance of SINK stage	$V_{SLx} = 0\text{ V}; I_{GHx} = 50\text{ mA}; T_j = 25^\circ\text{C}$	3	4	5	W
14.6.2			$V_{SLx} = 0\text{ V}; I_{GHx} = 50\text{ mA}; T_j = 125^\circ\text{C}$	4.5	5.3	7	W
14.7	$V_{GLxH}$	Gate on voltage		$V_{SLx} + 8\text{ V}$	$V_{SLx} + 10\text{ V}$	$V_{SLx} + 12\text{ V}$	V
14.8	$R_{GSLx}$	Passive gate clamp resistance		11	13	15	k $\Omega$
Timing of the drivers							
14.9	$t_{GHxHL}$	Propagation delay time high to low	$V_{VS} = 13.5\text{ V}; V_{SHx} = 0; R_G = 30\text{ }\Omega; C_G = 4.7\text{ nF}$	0.8	1.4	1.9	$\mu\text{s}$
14.10	$t_{GLxHL}$	Propagation delay time low to high	$V_{VS} = 13.5\text{ V}; V_{SLx} = 0; R_G = 30\text{ }\Omega; C_G = 4.7\text{ nF}$	0.6	1.2	1.8	$\mu\text{s}$
14.11	$t_{GHxr2}$	Rise time	$V_{VS} = 13.5\text{ V}; V_{SHx} = 0; R_G = 0\text{ }\Omega; C_G = 4.7\text{ nF}$	45		170	ns
14.12	$t_{GHxf2}$	Fall time	$V_{VS} = 13.5\text{ V}; V_{SHx} = 0; R_G = 0\text{ }\Omega; C_G = 4.7\text{ nF}$	60		210	ns
14.13	$t_{GLxr2}$	Rise time	$V_{VS} = 13.5\text{ V}; V_{SLx} = 0; R_G = 0\text{ }\Omega; C_G = 4.7\text{ nF}$	45		170	ns
14.14	$t_{GLxf2}$	Fall time	$V_{VS} = 13.5\text{ V}; V_{SLx} = 0; R_G = 0\text{ }\Omega; C_G = 4.7\text{ nF}$	60		210	ns

1. Indirect measurement, parameter measured dynamically using 100 nF load capacitor and evaluating the slew rate.

2. Average value.



Table 15. Cross current protection time<sup>(1)</sup>

Item	Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
15.1	$t_{CCP0}$	Cross current protection time	—	—	250 <sup>(2)</sup>	—	ns
15.2	$t_{CCP1}$	Cross current protection time	—	250	500	750	
15.3	$t_{CCP2}$	Cross current protection time	—	500	750	1000	
15.4	$t_{CCP3}$	Cross current protection time	—	700	1000	1300	
15.5	$t_{CCP4}$	Cross current protection time	—	950	1250	1570	
15.6	$t_{CCP5}$	Cross current protection time	—	1160	1500	1880	
15.7	$t_{CCP6}$	Cross current protection time	—	1360	1750	2180	
15.8	$t_{CCP7}$	Cross current protection time	—	1560	2000	2480	

1. Test conditions:  $V_{CC} = 5\text{ V}$ ,  $V_S = 13.5\text{ V}$ 

2. Not tested

Table 16. Drain source monitoring

Item	Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
16.1	$V_{SCd1}$	Drain - source threshold voltage	—	0.15	0.5	0.7	V
16.2	$V_{SCd2}$	Drain - source threshold voltage	—	0.45	1	1.25	V
16.3	$V_{SCd3}$	Drain - source threshold voltage	—	0.9	1.5	1.8	V
16.4	$V_{SCd4}$	Drain - source threshold voltage	—	1.4	2	2.35	V
16.5	$t_{SCd}$	Drain - source filtertime	—		6		$\mu\text{s}$

Table 17. Thermal sense interface ( $4.5\text{ V} < V_{CC} < 5.3\text{ V}$ )

Item	Symbol	Parameter		Min.	Typ.	Max.	Unit
17.1	$I_{TS\_bias}$	Output bias current		200	250	300	$\mu\text{A}$
17.2	$V_{th\_TS}$	TS threshold voltage	$V_{TS} < V_{CC} - 1\text{ V}$ $n = \text{number of diodes}$ $m = \text{programmed level (0 to 7)}$		$n * (0.31 + m * 0.03)$		V

Table 18. Current sense amplifier<sup>(1)</sup>

Item	Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
DC parameters							
18.1	$V_{ICM}$	Input voltage range – common mode		-4		$V_{CP} - 8\text{ V}$	V
18.2	$V_{IOFF50}$	Input offset voltage	Gain = 50	-11	-4	3	mV
18.3	$V_{IOFF20}$	Input offset voltage	Gain = 20	-23	-8	7	mV
18.4	$V_{IOFF10}$	Input offset voltage	Gain = 10	-30	-10	10	mV
18.5	$V_{IOFF-T50}/\Delta T$	Input offset voltage drift vs. temperature	Gain = 50		-10 <sup>(2)</sup>		$\mu\text{V}/^\circ\text{K}$

Table 18. Current sense amplifier<sup>(1)</sup> (continued)

Item	Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
18.6	V <sub>IOFF-T20</sub> /ΔT	Input offset voltage drift vs. temperature	Gain = 20		-18 <sup>(2)</sup>		μV/°K
18.7	V <sub>IOFF-T10</sub> /ΔT	Input offset voltage drift vs. temperature	Gain = 10		-27 <sup>(2)</sup>		μV/°K
18.8	V <sub>IOFF-O_50</sub>	Input offset voltage with offset compensation	Gain = 50	-3.5	-1	1.5	mV
18.9	V <sub>IOFF-O_20</sub>	Input offset voltage with offset compensation	Gain = 20	-6	-2	4	mV
18.10	V <sub>IOFF-O_10</sub>	Input offset voltage with offset compensation	Gain = 10	-10	-3	6	mV
18.11	P <sub>SRR_50</sub>	Power supply rejection ratio	Gain = 50	39			dB
18.12	P <sub>SRR_20</sub>	Power supply rejection ratio	Gain = 20	31			dB
18.13	P <sub>SRR_10</sub>	Power supply rejection ratio	Gain = 10	25			dB
18.14	CMRR	Input common mode rejection	T <sub>j</sub> = 25°C, DC	60			dB
18.15	Gain <sub>50</sub>	Gain		46.75	50	53.25	
18.16	Gain <sub>20</sub>	Gain		19	20	21	
18.17	Gain <sub>10</sub>	Gain		9.5	10	10.5	
18.18.1	V <sub>CSOh</sub>	High-level output voltage	I <sub>OUT</sub> = 2 mA	V <sub>CC</sub> - 250 mV			V
18.18.2			I <sub>OUT</sub> = 200 μA	V <sub>CC</sub> - 50 mV	V <sub>CC</sub> - 20 mV		V
18.19.1	V <sub>CSOl</sub>	Low-level output voltage	I <sub>OUT</sub> = -2 mA		100	250	mV
18.19.2			I <sub>OUT</sub> = -200 μA		15	50	mV
Dynamic parameters							
18.20	SRcso_10	CSO slew rate	Gain = 10; RL = 1 kΩ; CL = 22 pF		2.8	4	V/μs
18.21	SRcso_20	CSO slew rate	Gain = 20; RL = 1 kΩ; CL = 22 pF		3	4.5	V/μs
18.22	SRcso_50	CSO slew rate	Gain = 50; RL = 1 kΩ; CL = 22 pF		4.4	6	V/μs
18.23	I <sub>CSl_10</sub>	CSI input current	Gain = 10	-114	-102	-90	μA
18.24	I <sub>CSl_20</sub>	CSI input current	Gain = 20	-80	-72	-64	μA
18.25	I <sub>CSl_50</sub>	CSI input current	Gain = 50	-39	-33	-27	μA

1. Test conditions:  $V_S = 13 \text{ V}$ ,  $V_{\text{CC}} = 5 \text{ V}$ 

2. Not tested, guaranteed by design.

Figure 4. Output timing diagram (active free wheeling)

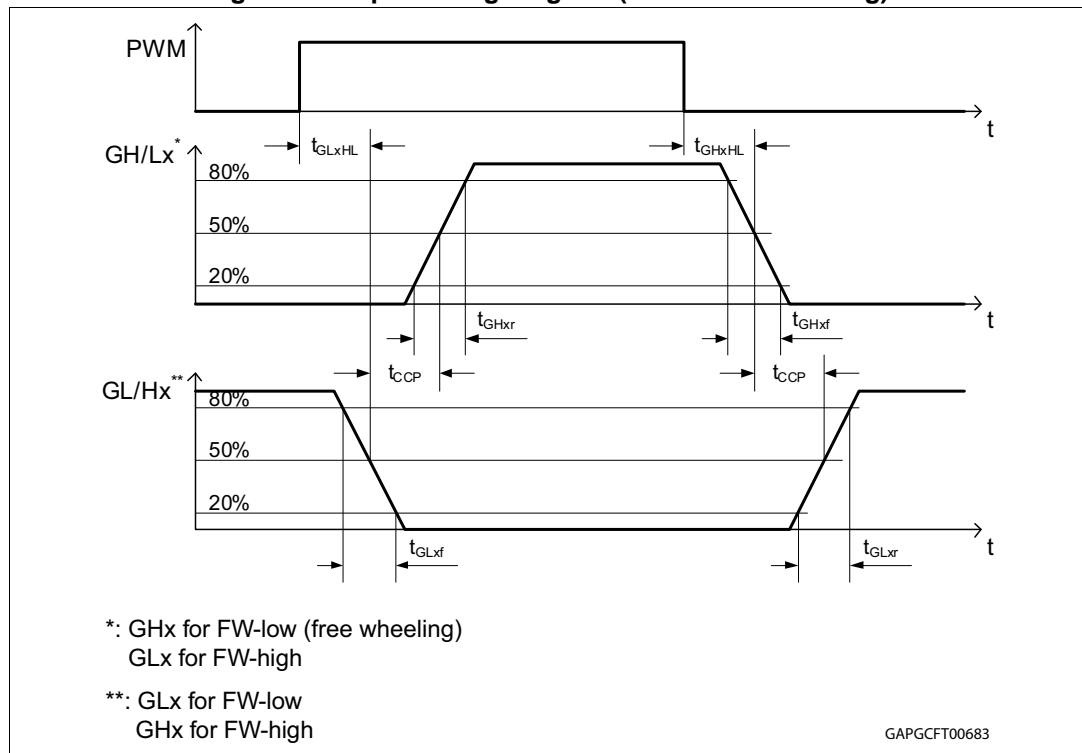
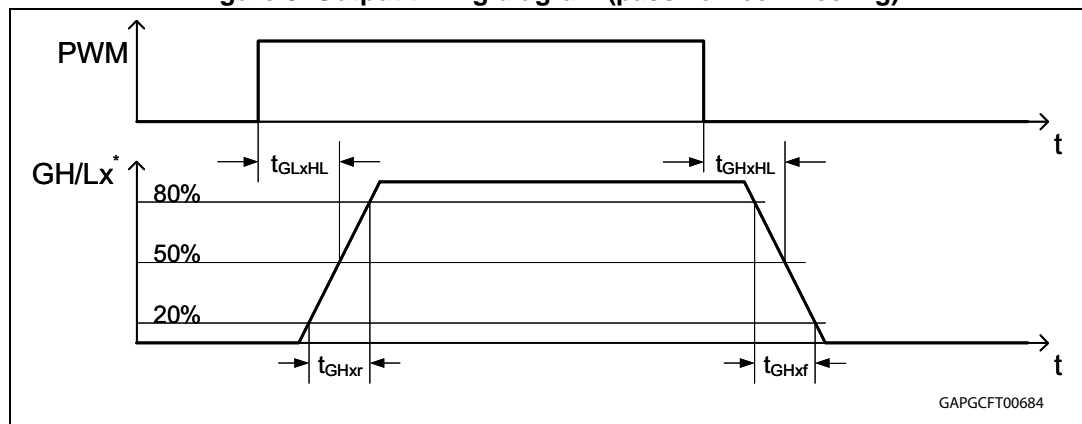


Figure 5. Output timing diagram (passive free wheeling)



## 2.5 SPI - electrical characteristics

$V_S = 6\text{ V}$  to  $28\text{ V}$ ,  $V_{CC} = 3\text{ V}$  to  $5.3\text{ V}$ ,  $T_j = -40^\circ\text{C}$  to  $150^\circ\text{C}$ , unless otherwise specified. The voltages are referred to GND and currents are assumed positive, when the current flows into the pin.

Table 19. DI timing<sup>(1)</sup>

Item	Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
19.1	$t_{CLK}$	Clock period	—	1000	—		ns
19.2	$t_{CLKH}$	Clock high time	—	400	—		ns
19.3	$t_{CLKL}$	Clock low time	—	400	—		ns
19.4	$t_{set\ CSN}$	CSN setup time, CSN low before rising edge of CLK	—	400	—		ns
19.5	$t_{set\ CLK}$	CLK setup time, CLK high before rising edge of CSN	—	400	—		ns
19.6	$t_{set\ DI}$	DI setup time	—	200	—		ns
19.7	$t_{hold\ DI}$	DI hold time	—	200	—		ns
19.8	$t_{r\ in}$	Rise time of input signal DI, CLK, CSN	—		—	100	ns
19.9	$t_{f\ in}$	Fall time of input signal DI, CLK, CSN	—		—	100	ns

1. DI timing parameters tested in production by a passed / failed test:  
 $T_j = -40^\circ\text{C}$  /  $+25^\circ\text{C}$ : SPI communication @ 2 MHz.  
 $T_j = +125^\circ\text{C}$ : SPI communication @ 1.25 MHz.

Table 20. DO

Item	Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
20.1	$V_{DOL}$	Low-level output voltage	$I_D = -4\text{ mA}$		0.2	0.4	V
20.2	$V_{DOH}$	High-level output voltage	$I_D = 4\text{ mA}$	$V_{CC} - 0.4$	$V_{CC} - 0.2$		V
20.3	$I_{DOLK}$	Tristate leakage current	$V_{CSN} = V_{CC}$ ; $0\text{ V} < V_{DO} < V_{CC}$	-10		10	$\mu\text{A}$
20.4	$C_{DO}^{(1)}$	Tristate input capacitance	$V_{CSN} = V_{CC}$ ; $0\text{ V} < V_{CC} < 5.3\text{ V}$		10	15	pF

1. Value of input capacity is not measured in production test. Parameter guaranteed by design.

Table 21. DO timing

Item	Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
21.1	$t_{r\ DO}$	DO rise time	$C_L = 100\ pF$ ; $I_{load} = -1\ mA$	—	80	140	ns
21.2	$t_{f\ DO}$	DO fall time	$C_L = 100\ pF$ ; $I_{load} = 1\ mA$	—	50	100	ns
21.3	$t_{en\ DO\ tri\ L}$	DO enable time from tristate to low-level	$C_L = 100\ pF$ ; $I_{load} = 1\ mA$ ; pull-up load to $V_{CC}$	—	100	250	ns
21.4	$t_{dis\ DO\ L\ tri}$	DO disable time from low-level to tristate	$C_L = 100\ pF$ ; $I_{load} = 4\ mA$ ; pull-up load to $V_{CC}$	—	380	450	ns
21.5	$t_{en\ DO\ tri\ H}$	DO enable time from tristate to high-level	$C_L = 100\ pF$ ; $I_{load} = -1\ mA$ ; pull-down load to GND	—	100	250	ns
21.6	$t_{dis\ DO\ H\ tri}$	DO disable time from high-level to tristate	$C_L = 100\ pF$ ; $I_{load} = -4\ mA$ ; pull-down load to GND	—	380	450	ns
21.7	$t_d\ DO$	DO delay time	$V_{DO} < 0.3\ V_{CC}$ ; $V_{DO} > 0.7\ V_{CC}$ ; $C_L = 100\ pF$	—	50	250	ns

Table 22. EN, CSN timing

Item	Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
22.1	$t_{r\ DO}$	DO rise time	$C_L = 100\ pF$ ; $I_{load} = -1\ mA$		80	140	ns
22.2	$t_{f\ DO}$	DO fall time	$C_L = 100\ pF$ ; $I_{load} = 1\ mA$		50	100	ns
22.3	$t_{CSN\_HI,min}$	CSN HI time, active mode: the min high time between two independent SPI commands.	Transfer of SPI-command to input register	2			$\mu s$

The diagram illustrates the timing relationship between several signals during a data transfer sequence:

- CSN (Chip Select Notation):** A signal that transitions from high to low to enable data output (DO) and from low to high to transfer actual data to output power switches (e.g. OUT1).
- CLK (Clock):** A periodic square wave signal used for data transfer.
- DI (Data In):** A signal that provides actual data on the rising edge of the CLK signal and new data on the falling edge. The data is shown as a sequence of bits (15 to 0) and is labeled as "actual data" and "new data".
- DO (Data Out):** A signal that provides status information on the falling edge of the CLK signal. The data is shown as a sequence of bits (15 to 0) and is labeled as "status information".
- e.g. OUT1 (Output 1):** A signal that shows old data and actual data. The transition from old data to actual data occurs when CSN transitions from low to high.

Key timing events and annotations include:

- CSN high to low: DO enabled:** Indicated by an arrow pointing to the falling edge of the CSN signal.
- DI: data will be accepted on the rising edge of CLK signal:** Indicated by an arrow pointing to the rising edge of the CLK signal.
- DO: data will change on the falling edge of CLK signal:** Indicated by an arrow pointing to the falling edge of the CLK signal.
- fault bit:** A specific bit in the DO signal, indicated by an arrow.
- CSN low to high: actual data is transferred to output power switches:** Indicated by an arrow pointing to the rising edge of the CSN signal.

The diagram is labeled with the part number **GAPGCFT00685** in the bottom right corner.

Timing diagram showing the relationship between CSN, CLK, and DI signals. The signals are shown relative to 0.2 VCC and 0.8 VCC levels.

- CSN:** Active-low signal. It transitions from 0.8 VCC to 0.2 VCC. Key timing parameters include  $t_{\text{set CSN}}$  (time from 0.8 VCC to 0.2 VCC),  $t_{\text{CLKH}}$  (high-level time), and  $t_{\text{set CLK}}$  (time from 0.2 VCC to 0.8 VCC).
- CLK:** Clock signal. It transitions between 0.2 VCC and 0.8 VCC. Key timing parameters include  $t_{\text{set DI}}$  (time from 0.2 VCC to 0.8 VCC),  $t_{\text{hold DI}}$  (time from 0.8 VCC to 0.2 VCC), and  $t_{\text{CLKL}}$  (low-level time).
- DI:** Data Input signal. It is shown as a bus signal. The signal is valid (Valid) during the time when CSN is low and CLK is high. The signal is high-impedance (represented by a zigzag line) when CSN is high or CLK is low.

Timing parameters shown:

- $t_{\text{set CSN}}$
- $t_{\text{CLKH}}$
- $t_{\text{set CLK}}$
- $t_{\text{set DI}}$
- $t_{\text{hold DI}}$
- $t_{\text{CLKL}}$

Signal levels: 0.8 VCC, 0.2 VCC.

Figure 8. SPI - DO valid data delay time and valid time

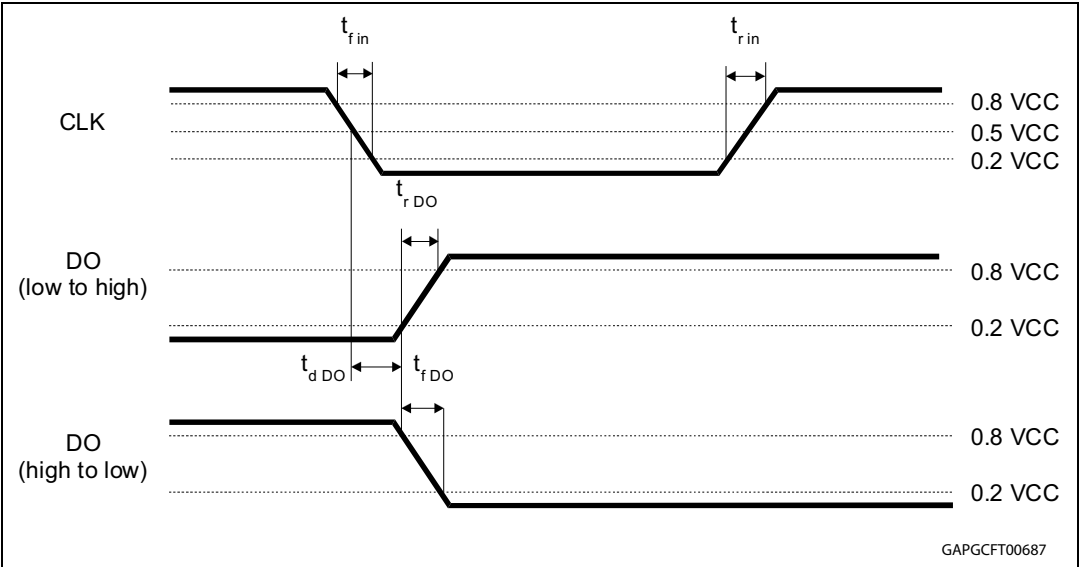


Figure 9. SPI - DO enable and disable time

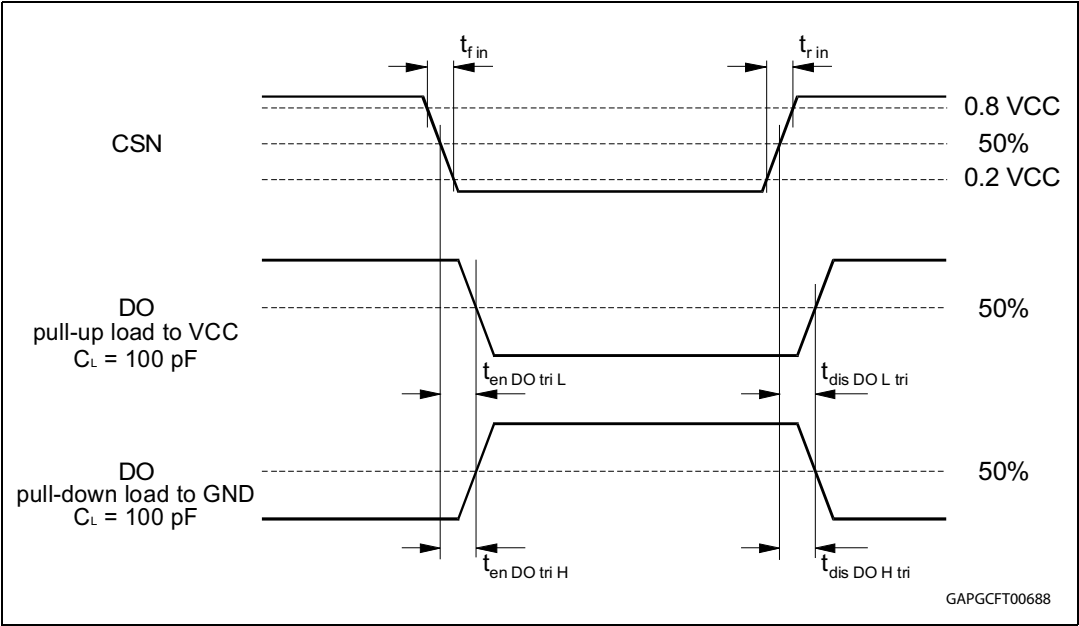
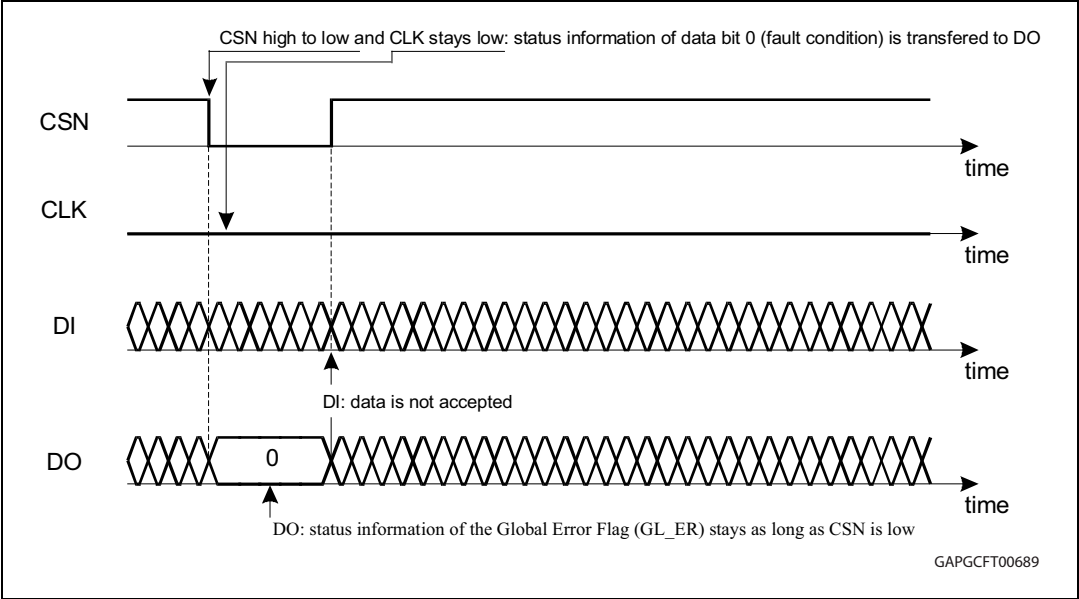


Figure 10. SPI - timing of status bit 0 (fault condition)





## 3 Device description

### 3.1 Dual power supply: $V_S$ and $V_{CC}$

The power supply voltage  $V_S$  supplies the charge-pump. An internal charge-pump is used to drive the high-side switches and the low-side switches. The logic supply voltage  $V_{CC}$  (3.3 V / 5 V) is used for the logic part and the SPI of the device. Due to the independent logic supply voltage the control and status information is not lost, even if the supply voltage  $V_S$  is switched-off. In case of power-on ( $V_{CC}$  increases from undervoltage to  $V_{POR\ OFF} = 2.5$  V, typical) the circuit is initialized by an internally generated power-on reset (POR). If the voltage  $V_{CC}$  decreases under the minimum threshold ( $V_{POR\ ON} = 2.2$  V, typical), the outputs are switched-off and the status registers are cleared.

### 3.2 Standby mode (EN)

The L99H01 is activated with enable input high signal. For enable input floating (not connected) or  $V_{EN} = 0$  V the device is in standby mode. All latched data are cleared and the inputs and outputs are switched-off. In the standby mode the current at  $V_S$  is less than 5  $\mu$ A (1  $\mu$ A) for CSN = high (DO in tristate). If  $V_{CC} > V_{POR\ OFF}$  and EN = high the device enters the active mode. In the active mode the charge-pump and the diagnostic functions are active.

### 3.3 H-bridge control (DIR, PWM, bit FW)

The DIR and PWM inputs control the drivers of the external H-bridge transistors. The motor direction can be chosen with the DIR input, the duty cycle and frequency with the PWM input. With the SPI registers FW and FW-PAS 4 different free wheeling modes (2 active and 2 passive) can be selected using the high-side transistors or the low-side transistors. Unconnected inputs are defined by internal pull-down current.

Table 23. Truth table

N°	Control pins				Control bits		Failure bits						Output pins				SPI DO	Comment
	EN	DIR	PWM	TS/ACT_OFF	FW	FW_PAS	CP_LOW	OV	UV	SC	TSD	WDTO	GH1	GL1	GH2	GL2	GL_ER	
1	0	X	X	X	X	X	X	X	X	X	X	X	RL	RL	RL	RL	T	Standby mode
2	1	X	X	X	X	X	X	X	X	X	X	X	RL	RL	RL	RL	1	Power-on reset
3	1	X	X	0	X	0	0	0	0	0	0	0	L	L	L	L	0	EXT_TS = 1 (external thermal shutdown)
4	1	X	X	0	X	0	0	0	0	0	0	0	L	L	L	L	0	EXT_TS = 0 (active Off)
5	1	X	X	1	X	X	1	0	0	0	0	0	RL	RL	RL	RL	1	Charge pump voltage too low
6	1	X	X	1	X	X	0	0	0	0	1	0	RL	RL	RL	RL	1	Internal thermal shutdown
7	1	X	X	1	X	X	0	1	0	0	0	0	L	L	L	L	1	Overvoltage
8	1	X	X	1	X	X	0	0	1	0	0	0	L	L	L	L	1	Undervoltage
9	1	X	X	1	X	X	0	0	0	1	0	0	L <sup>(1)</sup>	L <sup>(1)</sup>	L <sup>(1)</sup>	L <sup>(1)</sup>	0	Short-circuit <sup>(1)</sup>
10	1	X	X	1	X	X	0	0	0	0	0	1	L	L	L	L	1	Watchdog time out
11	1	0	1	1	X	X	0	0	0	0	0	0	L	H	H	L	0	-
12	1	X	0	1	0	0	0	0	0	0	0	0	L	H	L	H	0	Act. free wheeling mode LS
13	1	0	0	1	0	1	0	0	0	0	0	0	L	H	L	L	0	Pass. free wheeling mode LS
14	1	1	0	1	0	1	0	0	0	0	0	0	L	L	L	H	0	Pass. free wheeling mode LS
15	1	1	1	1	X	X	0	0	0	0	0	0	H	L	L	H	0	-
16	1	X	0	1	1	0	0	0	0	0	0	0	H	L	H	L	0	Act. free wheeling mode HS
17	1	0	0	1	1	1	0	0	0	0	0	0	L	L	H	L	0	Pass. free wheeling mode HS
18	1	1	0	1	1	1	0	0	0	0	0	0	H	L	L	L	0	Pass. free wheeling mode HS

1. Only the halfbridge (low-side and high-side) where one MOSFET is in short-circuit condition is switched-off. Both MOSFET'S of the other halfbridge remain active and driven by DIR and PWM.

Symbols:

- **x**: Don't care
- **1**: Logic high or active
- **0**: Logic low or not active
- **H**: Output in source condition
- **L**: Output in sink condition
- **RL**: Resistive low (see [Section 3.4](#))
- **T**: Tristate
- **FW**: Free wheeling
- **FW\_PAS**: Free wheeling passive
- **CP\_LOW**: Charge pump low
- **OV**: Overvoltage
- **UV**: Undervoltage
- **SC**: Short-circuit
- **TSD**: Thermal shutdown
- **GL\_ER**: Global error flag

### 3.4 Resistive low

The resistive output mode protects the L99H01 and the H-bridge in the standby mode and in some failure modes (internal and external thermal shutdown (TSD), charge pump low (CP\_LOW), stucked reset (STK\_RESET\_Q) and power-on reset (PORES). When a gate driver changes into the resistive output mode due to a failure a sequence is started. In this sequence the concerning driver is switched in sink condition for 32  $\mu$ s to 64  $\mu$ s to ensure a fast switch-off of the H-bridge transistor. Afterwards the driver is switched in the resistive output mode (resistive path to source).

### 3.5 Diagnostic functions

The diagnostic functions (over load, power supply over- and undervoltage, charge pump low, watchdog, temperature warning and internal/external thermal shutdown) are internally filtered and the condition has to be valid for at least 64  $\mu$ s (6  $\mu$ s for a short-circuit) before the corresponding status bit in the status registers is set. The filters are used to improve the noise immunity of the device. The internal temperature warning function is intended for information purpose and does not change the state of the output drivers. On the contrary, the over load condition switches the corresponding halfbridge in sink condition. The internal thermal shutdown condition and charge pump low disable all drivers (resistive low). The external thermal shutdown, watchdog, over- and undervoltage condition switch all driver in sink condition. The microcontroller needs to clear the status bits to reactivate the drivers.

### 3.6 Overvoltage and undervoltage detection

If the power supply voltage  $V_S$  rises above the overvoltage threshold  $V_{VS\_OVH}$  (typical 20 V / 30 V), all gate driver stages are switched in sink condition to protect the H-bridge and the load, setting the OV bit. Two values for the overvoltage threshold can be selected with the SPI. When the voltage  $V_S$  drops below the undervoltage threshold

$V_{VS\_UV}$ , all gate driver stages are switched in the sink condition to avoid driving the power devices without sufficient gate driving voltage (increased power dissipation), setting the UV bit. In both cases, overvoltage and undervoltage detection, the charge pump is disabled. If the supply voltage  $V_S$  recovers from UV/OV to normal operating voltage range and if the OV\_UV\_RD is set to 0, then the charge pump is automatically enabled. In any case, regardless of the OV\_UV\_RD bit value, the microcontroller needs to clear the status register to reactivate the gate drivers.

### 3.7 Charge pump

The charge pump uses 2 external capacitors. The output of the charge pump has a current limitation. In standby mode and after overvoltage, undervoltage or a thermal shutdown has been triggered the charge pump is disabled. If the charge pump output voltage remains too low for longer than  $T_{CP}$ , all gate drivers are switched-off (resistive output, see [Section 3.4](#)). The CP\_LOW bit has to be cleared through a software reset to reactivate the gate drivers.

### 3.8 Temperature warning and thermal shutdown

If junction temperature rises above  $T_{jTWON}$  the temperature warning flag TW is set and is detectable via the SPI. If junction temperature increases above the second threshold  $T_{jSDON}$ , the thermal shutdown bit (TSD) is set. The gate drivers and the charge pump are switched-off to protect the device. The gates of the H-bridge are discharged by the resistive low mode (see [Section 3.4](#)). In order to reactivate the output stages the junction temperature must decrease below  $T_{jSDOFF}$  and the thermal shutdown bit has to be cleared by the microcontroller.

### 3.9 Short-circuit detection / drain source monitoring

The drain - source voltage of each activated external MOSFET of the H-bridge is monitored by comparators to detect shorts to ground or battery. If the voltage drop over the external MOSFET exceeds the threshold voltage  $V_{SCd}$  for longer than the short current detection time  $t_{SCd}$  the corresponding gate driver switches the external MOSFET off and the corresponding drain source monitoring flag (DS\_MON [3:0]) is set. Until this failure flag is reset the corresponding half bridge is in sink condition. The DS\_MON bits have to be cleared through a software reset to reactivate the gate drivers. The drain source monitoring has a filter time of 6  $\mu s$ . This monitoring is only active when the corresponding gate driver is in source condition. The threshold voltage  $V_{SCd}$  can be programmed in 4 steps between 0.5 V and 2 V with the SPI.

### 3.10 Programmable cross current protection

The external Power MOSFET's transistors in H-bridge (two halfbridges) configuration are switched-on with an additional delay time  $t_{CCP}$  to prevent cross current in the halfbridge. The cross current protection time  $t_{CCP}$  can be programmed with the SPI.

### 3.11 Current sense amplifier (CSA)

The current sense amplifier (CSA) is specially designed for current shunt automotive applications. It is a bidirectional, single-supply difference amplifier for amplifying small differential voltages in a wide common mode voltage range (-4 V to ( $V_{CP} - 8$ ) V). It supports the current measurement at two shunts. The result of respective shunt can be multiplexed to the microcontroller compatible output voltage by a SPI command.

A gain of 50, 20 or 10 is SPI programmable. The inputs (CSI1+ / CSI1- and CSI2+ / CSI2-) are build as a transconductance stage. Therefore a series resistor (for filtering etc.) should not exceed 50  $\Omega$  to keep the additional gain error below 1%.

The output works at half scale:  $V_{CSO0} = (0,5 * V_{CC})$  V for  $V_{IDIFF} = 0$  V. An internal offset measurement is in normal mode available with the "OFF\_CAL" SPI-bit. If this bit is set to logic "1" the input pins are disconnected from the amplifier and a virtual zero input differential voltage is selected.

### 3.12 Thermal sensor interface / H-bridge switch-off input

The TS/ACT\_OFF pin is configurable by SPI with the EXT\_TS bit. This pin could be used as temperature sensor interface for the H-bridge or external off for all gate drivers. The output bias current ITS\_bias is on for EN = high.

#### 3.12.1 EXT\_TS-bit = low (active off)

The TS/ACT\_OFF input is used as a logic driver control input, without filter delay and without latching the information.

Pulling the TS/ACT\_OFF pin below the programmed threshold all gate drivers are switched-off and the OT\_EXT bit is set.

Increasing the voltage at TS/ACT\_OFF pin above the programmed threshold the device remains to the status set by DIR and PWM-pins and the OT\_EXT bit is reseted.

The threshold is programmable by SPI with the registers EXTTH\_5:0.

#### 3.12.2 EXT\_TS-bit = high (thermal sensor interface)

With the thermal sensor interface external diodes can be used to control the temperature of the external H-bridge. When the diode forward voltage decreases below the reference voltage for longer than the internal filter time (64  $\mu$ s) the OT\_EXT bit is set and the driver switches in resistive low (see [Section 3.4: Resistive low](#)).

In this mode the OT\_EXT-status-bit has to be cleared to reactivate the gate drivers.

The threshold is programmable by SPI with the registers EXTTH\_5:0.

### 3.13 Watchdog

The tasks of the watchdog is to monitor the microcontroller during normal operation within a nominal trigger cycle of 60 ms. The microcontroller has to restart the watchdog timer by sending the watchdog restart bit via SPI repeatedly within the watchdog time  $T_{WDTO}$ . If no correct watchdog service is sent from the microcontroller, all gate drivers switch in sink

condition and the watchdog time out bit (WDTO) is set. Once the watchdog times out, the gate drivers can only be reactivated by sending a software reset.

## 4 Functional description of the SPI

### 4.1 Signal description

#### 4.1.1 Serial clock (CLK)

This input signal provides the timing of the serial interface. Data present at serial data input (DI) is latched on the rising edge of serial clock (CLK). Data on Serial Data Out (DO) is shifted out at the falling edge of serial clock (CLK).

The serial clock CLK must be active only during a frame (CSN low phase). Any other switching of CLK close to any CSN edge could generate setup/hold violations in the SPI logic of the device.

#### 4.1.2 Serial data input (DI)

This input is used to transfer data serially into the device. Values are latched on the rising edge of serial clock (CLK).

#### 4.1.3 Serial data output (DO)

This output signal is used to transfer data serially out of the device. Data is shifted out on the falling edge of serial clock (CLK).

DO also reflects the status of the *<Global Error Flag>* (*<Global Status Byte>*[7]) while CSN is low and no clock signal is present.

#### 4.1.4 Chip select not (CSN)

When this input signal is high, the communication interface of the device is deselected and serial data output (DO) is high impedance. Driving this input low enables the communication. The communication must start and stop on a low-level of serial clock (CLK).

The SPI can be driven by a microcontroller with its SPI peripheral running in following mode: CPOL = 0 and CPHA = 0.

For timing details and figures refer to [Section 2.5](#).

### 4.2 General data description

The SPI communication is based on a SPI interface structure using CSN (chip select not), DI (serial data in), DO (serial data out/error) and CLK (serial clock) signal lines.

Each DI communication frame consists of a *<Command Byte>* which is followed by 1 *<Data Byte>*.

The data returned on DO within the same frame always starts with the *<Global Status Byte>*, which provides general status information about the device. This byte is followed by 1 *<Data Byte>* (*'In-frame-response'*).

Table 24. DI

Command byte								DI - data byte							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OC1	OC0	A5	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0

Table 25. DO

Global Status byte								DO - data byte							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
GL_ER	FE	STK_RESET_Q	TSD	TW	UV	OV	WDTO	D7	D6	D5	D4	D3	D2	D1	D0

### 4.2.1 Command byte

Each communication frame starts with a command byte. It consists of an operating code which specifies the type of operation (<Read>, <Write>, <Fault Reset>, <Read Device Information>) and a 6-bit address.

Table 26. Command byte

Command byte							
MSB				LSB			
Op code		Address					
OC1	OC0	A5	A4	A3	A2	A1	A0

Comments:

- **OCx**: Operating code
- **Ax**: Address

### 4.2.2 OpCode definition

Table 27. Operating code definition

OC1	OC0	Meaning
0	0	<Write Mode>
0	1	<Read Mode>
1	0	<Clear Status>
1	1	<Read Device Information>

The <Write Mode> and <Read Mode> operations allow access to the RAM of the device.

The <Clear Status> operation is used to read a status register and subsequently clear its content.

<Read Device Information> allows access to the ROM area which contains device related information such as <ID-Header>, <Product Code>, <Silicon Version and Category> and <SPI-frame-ID>.



More detailed descriptions of the *device information* are available in [Section 4.7](#).

## 4.3 Device memory map

### 4.3.1 Control and status (RAM) address map

Table 28. Control and status (RAM) address map

Name	Access	Address						Content							
		A5	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
Stat Reg0	Read/ Clear	0	0	0	0	0	0	DS_MON_3	DS_MON_2	DS_MON_1	DS_MON_0	0	0	OT_EXT	CP_LOW
Appl Reg1	Read/ Write	0	0	0	0	0	1	RWD	FW_PAS	OFF_CAL	CLK_SPCTR	OVT	OV_UV_R D	DIAG_1	DIAG_0
Appl Reg2	Read/ Write	0	0	0	0	1	0	RWD	COPT_2	COPT_1	COPT_0	FW	MCSA	GCSA_1	GCSA_0
Appl Reg3	Read/ Write	0	0	0	0	1	1	RWD	EXT_TS	EXTTH_5	EXTTH_4	EXTTH_3	EXTTH_2	EXTTH_1	EXTTH_0

### 4.3.2 Device (ROM) address map (access with OC0 and OC1 set to '1')

Table 29. Device (ROM) address map (access with OC0 and OC1 set to '1')

Name	Access	Address						Content							
		A5	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
ID-Header	Read device	0	0	0	0	0	0	FAM_1	FAM_0	NR_PI_5	NR_PI_4	NR_PI_3	NR_PI_2	NR_PI_1	NR_PI_0
Product Code 1	Read device	0	0	0	0	0	1	PR_ID_7	PR_ID_6	PR_ID_5	PR_ID_4	PR_ID_3	PR_ID_2	PR_ID_1	PR_ID_0
Product Code 2	Read device	0	0	0	0	1	0	PR_ID_15	PR_ID_14	PR_ID_13	PR_ID_12	PR_ID_11	PR_ID_10	PR_ID_9	PR_ID_8
SPI-Frame-ID	Read device	0	0	0	0	1	1	BR	AR5	AR4	AR3	32 bits	24 bits	16 bits	8 bits
Reserved	Read device	1	1	1	1	1	1	Reserved, accessing this address is recognized as a failure, the device enters a fail-safe state (see <a href="#">Table 30: STK_RESET_Q</a> ).							

## 4.4 Global status byte

This byte is shifted out first at DO at every SPI access.

The GL\_ER bit is present at DO with the falling edge of CSN.

This byte could be reseted with the command <clear status>.

**Table 30. STK\_RESET\_Q**

Bit	15	14	13	12	11	10	9	8
Name	GL_ER	FE	STK_RESET_Q	TSD	TW	UV	OV	WDTO
<default>	0	0	1	0	0	0	0	0

Comments:

- **GL\_ER**: Global error flag. This signal is a logical OR among all the errors of all the channels of the device.
- **FE**: Frame error. If the number of clock pulses within the previous frame is not 16 the frame is ignored and this bit is set.
- **STK\_RESET\_Q**: If a stuck at '1' on SPI\_DI during any SPI frame occurs, or if a power-on reset occurs. STK\_RESET\_Q is reset ('1') with any SPI command. When STK\_RESET\_Q is active ('0'), the gate drivers are switched-off (see [Section 3.4: Resistive low](#)). After a startup of the circuit the STK\_RESET\_Q is active because of the POR pulse and the gate drivers are switched-off. The Gate drivers can only be activated after the STK\_RESET\_Q has been reset with a SPI command.
- **TSD**: Thermal shutdown due to an internal sensor. All the gate drivers and the charge pump must be switched-off (see [Section 3.4: Resistive low](#)). The gate drivers can only be activated after the TSD has been reset with a SPI command.
- **TW**: Thermal warning
- **UV**: Logical OR among the filtered undervoltage signals.
- **OV**: Logical OR among the filtered overvoltage signals.
- **WDTO**: Watchdog time out.

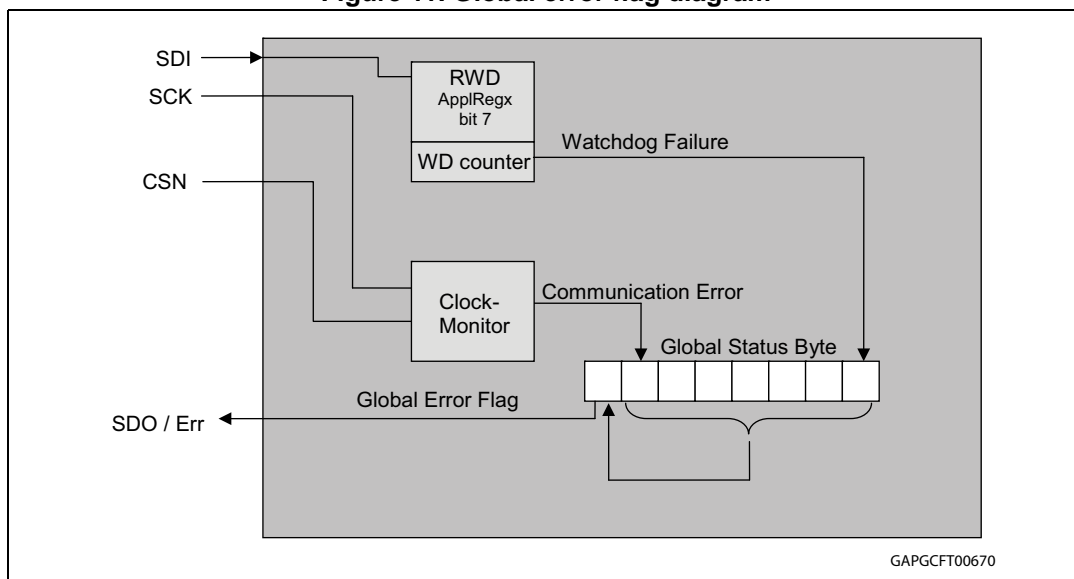
Failures of <Global Status Register>[8:14] are always linked to the <Global Error Flag>.

The <Global Error Flag> is generated by an OR combination of all failure events of the device (<Global Status Register>[8:14]).

The flag is reflected via the DO pin while CSN is held low and no clock signal is available. The flag remains as long as CSN is low. This operation does not cause the <communication error> bit in the <Global Status Byte> to be set.

#### 4.4.1 SPI clock monitor and watchdog

Figure 11. Global error flag diagram



1. Writing a "1" to RWD - bit in ApplRegx restarts the internal watchdog counter.

The clock monitor counts the number of clock pulses during a communication frame (while CSN is low). If the number of SCK pulses does not correspond with the frame width indicated in the <SPI-frame-ID> (ROM address 03hex) the frame is ignored and the bit <frame error> in the <Global Status Byte> is set.

**Note:** Due to this safety functionality, daisy chaining the SPI is not possible. Instead, a parallel operation of the SPI bus by controlling the CSN signal of the connected ICs is recommended.

## 4.5 Detailed byte description of status register (StatReg0)

The read operation starts always with the command byte followed by 1 data byte. The content of the send data byte has to be '0'. The content of the addressed register is shifted out at DO within the same frame ('in-frame response').

The device uses 1 status register to monitor the state of the device. [Table 31](#) shows the address and the content of the register.

**Table 31. Address 0<00(hex)>:StatReg 0 - read only<sup>(1)</sup>**

Bit	7	6	5	4	3	2	1	0
Name	DS_MON_3	DS_MON_2	DS_MON_1	DS_MON_0	X	X	OT_EXT	CP_LOW
<default>	0	0	0	0	0	0	0	0

1. The errors of the status register are not linked to the <Global Error Flag>.

Comments:

- **DS\_MON[3:0]:** If max drain source voltage exceeds the defined thresholds, the DS\_MON are set and the corresponding drivers go to sink mode. The DS\_MON bits have to be cleared through a software reset to reactivate the drivers.

**Table 32. DS\_MON - drivers relations**

Register	Deactivated driver
DS_MON_3	High-side 2
DS_MON_2	High-side 1
DS_MON_1	Low-side 2
DS_MON_0	Low-side 1

- **OT\_EXT:** Depending on EXT\_TS bit following two meanings exist:
  - EXT\_TS = low (active off):  
TS/ACT\_OFF pin is used as input to switch the H-bridge in tristate and back. Details are described in [Section 3.12.1](#).
  - EXT\_TS = high (thermal sensor interface):  
TS/ACT\_OFF pin is used as thermal sensor interface for external temperature diodes. Details are described in [Section 3.12.2](#).
- **CP\_LOW:** If a charge pump output voltage low occurs, all gate drivers must be switched-off (resistive low). The CP\_LOW bit has to be cleared through a software reset to reactivate the gate driver.

## 4.6 Detailed byte description of application registers (ApplRegX)

The write/read operation starts always with a command byte followed by 1 data byte.

### 4.6.1 Description of the data byte

The device uses 3 application registers to configure the device. Note that the last row shows the logic levels during a reset phase.

**Table 33. Address 1 <01(hex)>:ApplReg1-read/write**

Bit	7	6	5	4	3	2	1	0
Name	RWD	FW_PAS	OFF_CAL	CLK_SPCTR	OVT	OV_UV_RD	DIAG1	DIAG0
<default>	0	0	0	0	0	0	0	0

Comments:

- **RWD**: Restarts the watchdog counter
- **FW\_PAS**: Enables passive free wheeling according to [Table 23](#)
- **OFF\_CAL**: Offset calibration mode for CSA
- **OVT**: Overvoltage threshold
- **CLK\_SPCTR**: Switch the clock to the charge pump
  - **0**: 125 KHz (50% duty cycle)
  - **1**: pulses train (max = 8  $\mu$ s, min = 2  $\mu$ s) to optimize power spectrum

**Table 34. Overvoltage threshold of the Vs monitoring**

OVT	Threshold
0	20 V
1	29 V

- **OV\_UV\_RD**: Over/undervoltage recovery disabled.
  - **0**: If  $V_S$  recovers from OV/UV condition to normal operating voltage range, the charge pump is automatically enabled;
  - **1**: If  $V_S$  recovers from OV/UV condition to normal operating voltage range, the charge pump remains disabled;

In both cases the microcontroller has to clear the status register to enable the gate drivers

- **DIAG[1:0]**: Drain source monitoring threshold voltage

**Table 35. DIAG monitoring of source voltages**

DIAG[1]	DIAG[0]	Monitoring threshold voltage
0	0	$V_{SCD1} = 0.5 \text{ V}$
0	1	$V_{SCD2} = 1 \text{ V}$
1	0	$V_{SCD3} = 1.5 \text{ V}$
1	1	$V_{SCD4} = 2 \text{ V}$

**Table 36. Address 2 <02(hex)>: ApplReg2 – read/write**

Bit	7	6	5	4	3	2	1	0
Name	RWD	COPT_2	COPT_1	COPT_0	FW	MCSA	GCSA_1	GCSA_0
<default>	0	0	0	0	0	0	0	0

Comments:

- **RWD**: Restarts the watchdog counter
- **COPT[2:0]**: Filter time to protect the two external halfbridges against cross current.

**Table 37. Cross current protection time ( $t_{CCP}$ )**

COPT_2	COPT_1	COPT_0	Protection time
0	0	0	250 ns
0	0	1	500 ns
0	1	0	750 ns
0	1	1	1000 ns
1	0	0	1250 ns
1	0	1	1500 ns
1	1	0	1750 ns
1	1	1	2000 ns

- **FW**: Selects high-side or low-side free wheeling
- **MCSA**: Multiplexer for current sense amplifier.

**Table 38. Multiplexer for current sense amplifier**

MCSA	Selected amplifier
0	CSA2 (CSI2+ / CSI2-)
1	CSA1 (CSI1+ / CSI1-)

- **GCSA[1:0]**: Gain of the current sense amplifier.

**Table 39. Gain of current sense amplifier**

GCSA_1	GCSA_0	Gain
0	0	10
0	1	20
1	0	50
1	1	Not applicable

Table 40. Address 3 &lt;03(hex)&gt; : ApplReg3 – read/write

Bit	7	6	5	4	3	2	1	0
Name	RWD	EXT_TS	EXTTH_5	EXTTH_4	EXTTH_3	EXTTH_2	EXTTH_1	EXTTH_0
<default>	0	0	0	0	0	0	0	0

Comments:

- **RWD**: Restarts the watchdog counter
- **EXT\_TS**: The bit select the mode of the input pin TS/ACT\_OFF:
  - EXT\_TS = low (active off):  
TS/ACT\_OFF pin is used as input to switch the H-bridge in tristate and back.  
Details are described in [Section 3.12.1](#).
  - EXT\_TS = high (thermal sensor interface):  
TS/ACT\_OFF pin is used as thermal sensor interface for external temperature diodes. Details are described in [Section 3.12.2](#).
- **EXTTH[5:0]**: Determines the threshold of the external thermal shutdown/warning

Table 41. External threshold voltage, factor n

EXTTH_5	EXTTH_4	EXTTH_3	n
0	0	0	7
0	0	1	6
0	1	0	5
0	1	1	4
1	0	0	3
1	0	1	2
1	1	0	1
1	1	1	0

Table 42. External threshold voltage, factor m

EXTTH_2	EXTTH_1	EXTTH_0	m
0	0	0	7
0	0	1	6
0	1	0	5
0	1	1	4
1	0	0	3
1	0	1	2
1	1	0	1
1	1	1	0



**Equation 1**

$$V_{th} = n * (0.31 + m * 0.03) V$$

The purpose of factor n is to determine the number of external temperature sense diodes (in series). With factor m the level of the threshold voltage can be fine tuned.

## 4.7 Read device information (ROM)

The device information is stored at the ROM addresses defined below and is read using the respective operating code.

**Table 43. Read device information (ROM)**

Op code		Address	Device information
OC1	OC0	Ax	
1	1	00H	<ID-Header>
1	1	01H	<Product Code 1>
1	1	02H	<Product Code 2>
1	1	03H	<SPI-frame-ID>
1	1	3FH	Reserved, accessing this address is recognized as a failure, the device enters a fail-safe state (see <a href="#">Table 30: STK_RESET_Q</a> ).

The <ID-Header> indicates the product family and specifies how many bytes of device information are available.

**Table 44. Address 0 <00(hex)> : ID-header - read only<sup>(1)</sup>**

Bit	7	6	5	4	3	2	1	0
Name	FAM_1	FAM_0	NR_PI_5	NR_PI_4	NR_PI_3	NR_PI_2	NR_PI_1	NR_PI_0
<default>	0	1	0	0	0	0	1	0

1. Addressable only through a read device information command.

- **FAM[1:0]**: Family identifier, FAM[1:0] = [0:1] stands for ASSPs.
- **NR\_PI[5:0]**: Number of product information bytes.

The <Product Code 1 and 2> represents a unique identifier of the device and version.

**Table 45. Address 1 <01(hex)>: product ID (LSB) - read only<sup>(1)</sup>**

Bit	7	6	5	4	3	2	1	0
Name	PR_ID_7	PR_ID_6	PR_ID_5	PR_ID_4	PR_ID_3	PR_ID_2	PR_ID_1	PR_ID_0
<default>	0	0	0	0	0	0	0	1

1. Addressable only through a read device information command.

**Table 46. Address 2 <02(hex)>: product ID (MSB) - read only<sup>(1)</sup>**

Bit	7	6	5	4	3	2	1	0
Name	PR_ID_15	PR_ID_14	PR_ID_13	PR_ID_12	PR_ID_11	PR_ID_10	PR_ID_9	PR_ID_8
<default>	0	0	1	0	1	X	X	X

1. Addressable only through a read device Information command.

The <SPI-frame-ID> (ROM address 03H) provides information about the register width (1, 2, 3 bytes) and the availability of 'burst mode read' option.

**Table 47. Address 3 <03(hex)>: SPI frame ID - read only<sup>(1)</sup>**

Bit	7	6	5	4	3	2	1	0
Name	BR	AR5	AR4	AR3	32 bits	24 bits	16 bits	8 bits
<default>	0	0	0	0	0	0	1	0

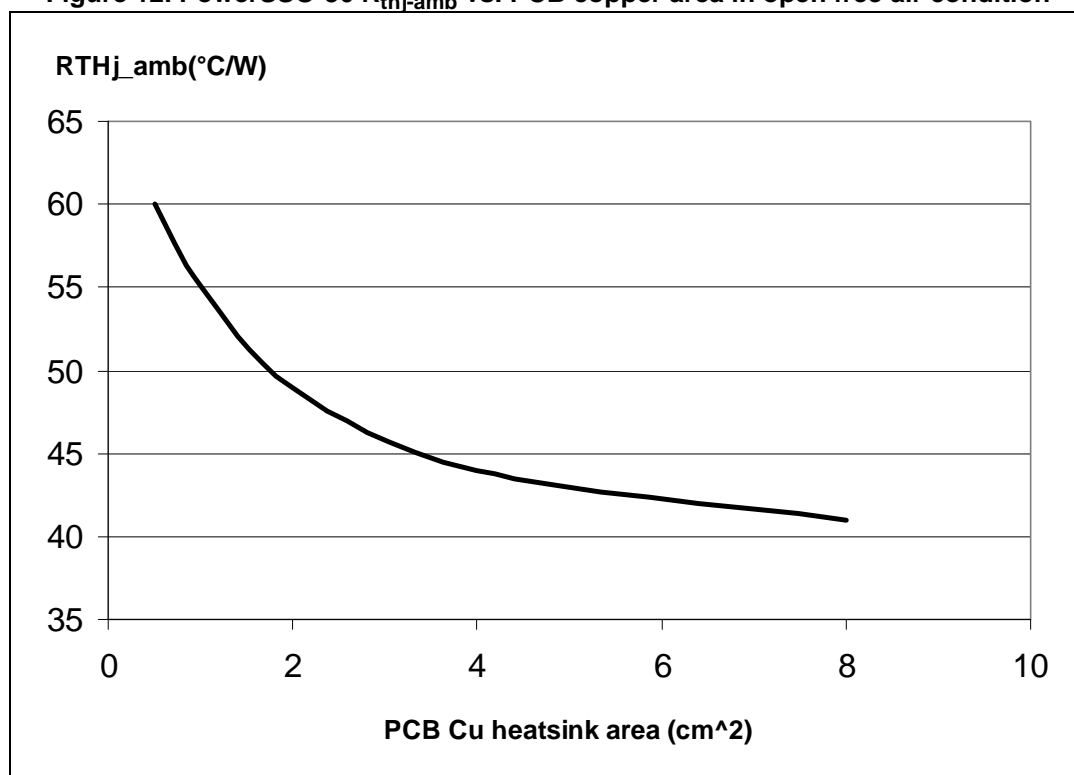
1. Addressable only through a Read Device Information command.

Comments:

- **BR:** Burst mode read. Not supported
- **AR5:** Address width reduction. Not supported
- **AR4:** Address width reduction. Not supported
- **AR3:** Address width reduction. Not supported
- **32 bits:** 32 bits frame width. Not supported
- **24 bits:** 24 bits frame width. Not supported
- **16 bits:** 16 bits frame width, 8 bits command and 8 bits data
- **8 bits:** 8 bits frame width. Not supported

## 5 Packages thermal data

Figure 12. PowerSSO-36  $R_{thj-amb}$  vs. PCB copper area in open free air condition



1. Layout condition of  $R_{th}$  and  $Z_{th}$  measurements (PCB: double layer, thermal vias, FR4 area = 129 mm x 60 mm, PCB thickness = 1,6 mm, Cu thickness = 70  $\mu m$  (front and back side), Copper areas: from minimum pad layout to 8  $cm^2$ ).

## 6 Package and packing information

### 6.1 ECOPACK®

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK® is an ST trademark.

6.2 PowerSSO-36 package information

Figure 13. PowerSSO-36 package dimensions

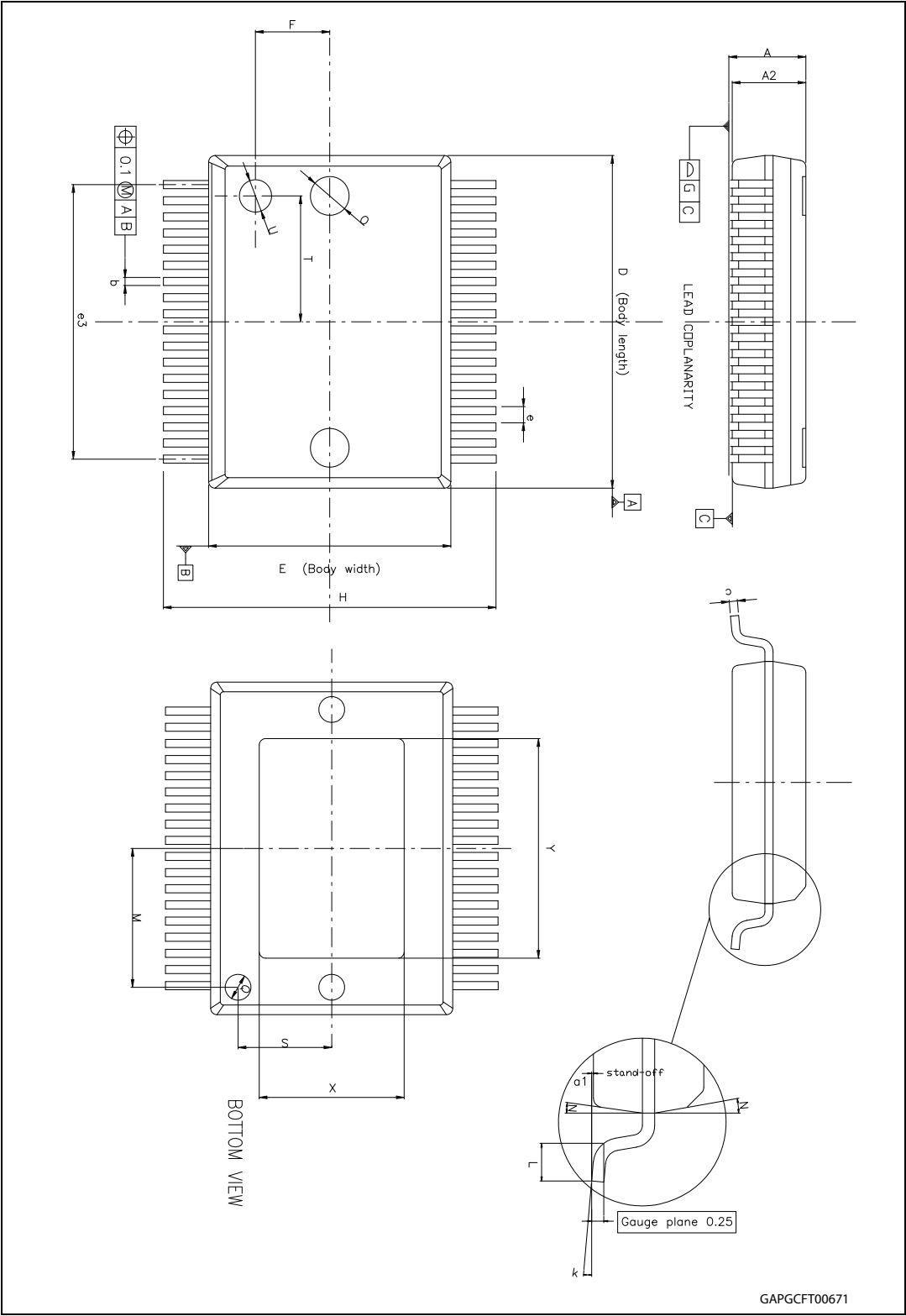


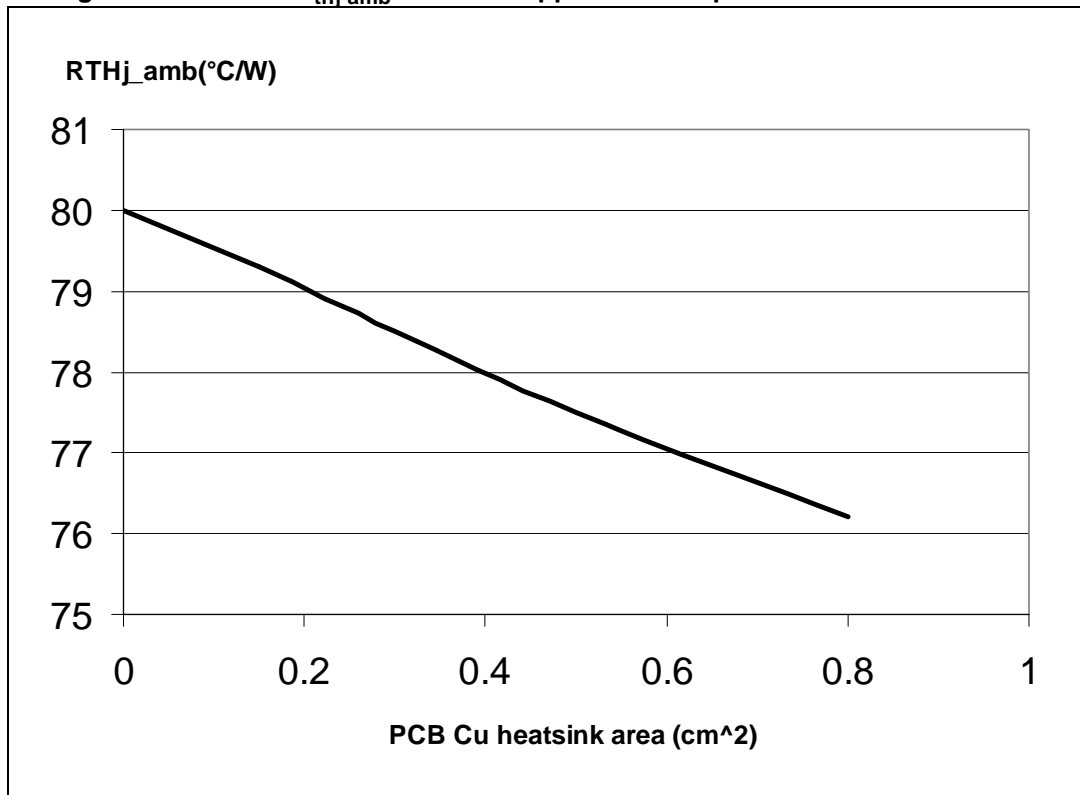
Table 48. PowerSSO-36 mechanical data

Symbol	Millimeters		
	Min.	Typ.	Max.
A	2.15	-	2.45
A2	2.15	-	2.35
a1	0	-	0.1
b	0.18	-	0.36
c	0.23	-	0.32
D <sup>(1)</sup>	10.10	-	10.50
E <sup>(1)</sup>	7.4	-	7.6
e	-	0.5	-
e3	-	8.5	-
F	-	2.3	-
G	-	-	0.1
H	10.1	-	10.5
h	-	-	0.4
k	0°	-	8°
L	0.55	-	0.85
M	-	4.3	-
N	-	-	10°
O	-	1.2	-
Q	-	0.8	-
S	-	2.9	-
T	-	3.65	-
U	-	1	-
X	4.1	-	4.7
Y	6.5	-	7.1

1. "D" and "E" do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15 mm per side (0.006").

### 6.3 Packages thermal data

Figure 14. LQFP32  $R_{thj-amb}$  vs. PCB copper area in open box free air condition



1. Layout condition of  $R_{th}$  and  $Z_{th}$  measurements (PCB: double layer, thermal vias, FR4 area = 78 mm x 86 mm, PCB thickness = 1.6 mm, Cu thickness = 70  $\mu m$  (front and back side), copper areas: from minimum pad layout to 8  $cm^2$ ).

## 6.4 LQFP32 package information

Figure 15. LQFP32 package dimensions

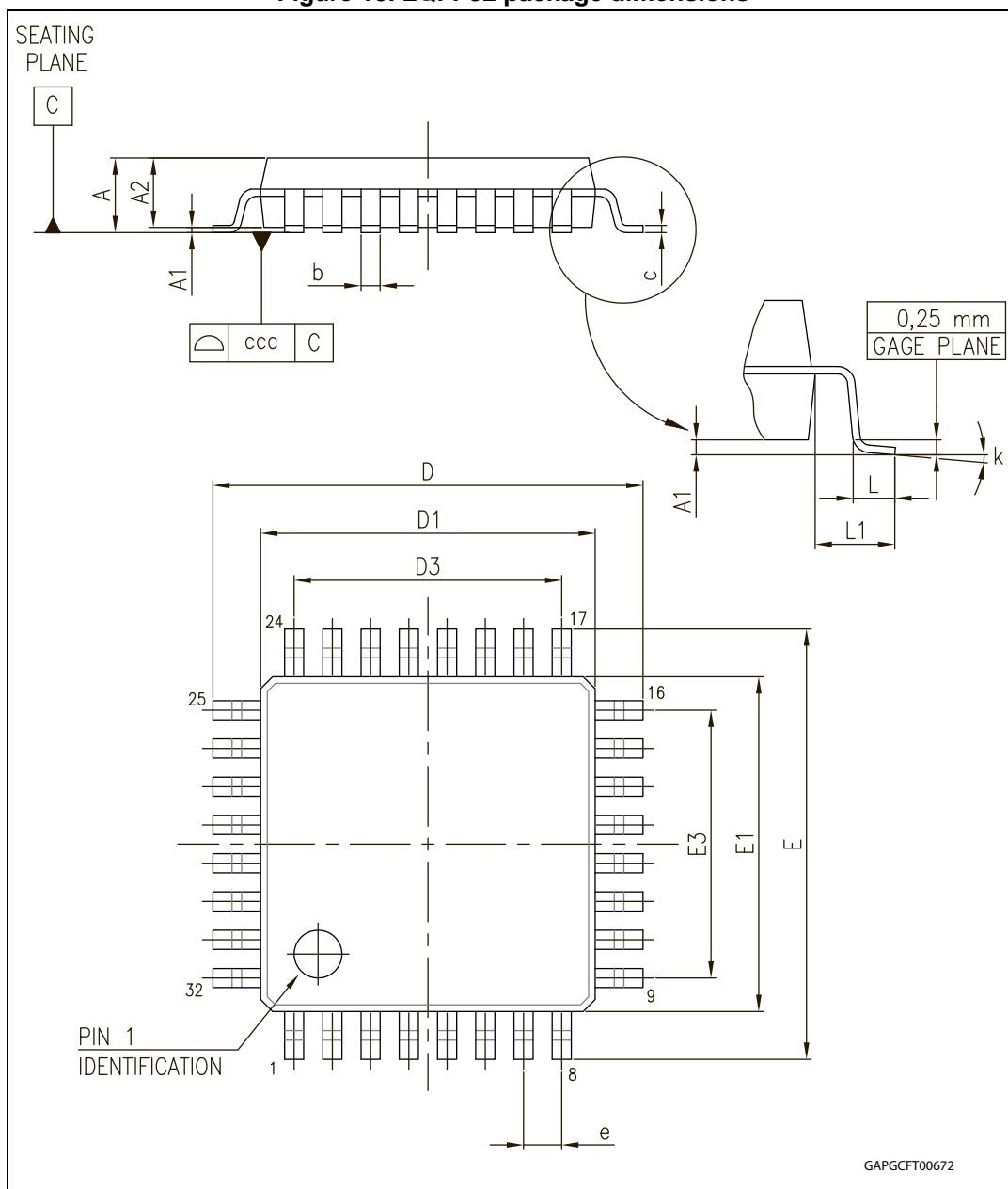




Table 49. LQFP32 mechanical data

Dim.	Millimeter		
	Min.	Typ.	Max.
A			1.60
A1	0.05		0.15
A2 <sup>(1)</sup>	1.35	1.40	1.45
b	0.30	0.37	0.45
c	0.09		0.20
D	8.80	9.00	9.20
D1	6.80	7.00	7.20
D3		5.60	
E	8.80	9.00	9.20
E1	6.80	7.00	7.20
E3		5.60	
e		0.80	
L	0.45	0.60	0.75
L1		1.00	
K	0°	3.5°	7°
ccc			0.10

1. LQFP stands for low profile quad flat package.  
Low profile: Body thickness (A2 = 1.40 mm)

## 6.5 PowerSSO-36 packing information

Figure 16. PowerSSO-36 tube shipment (no suffix)

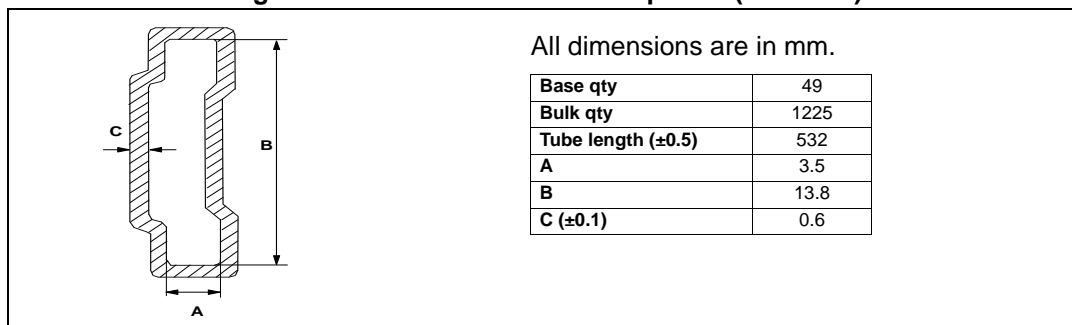
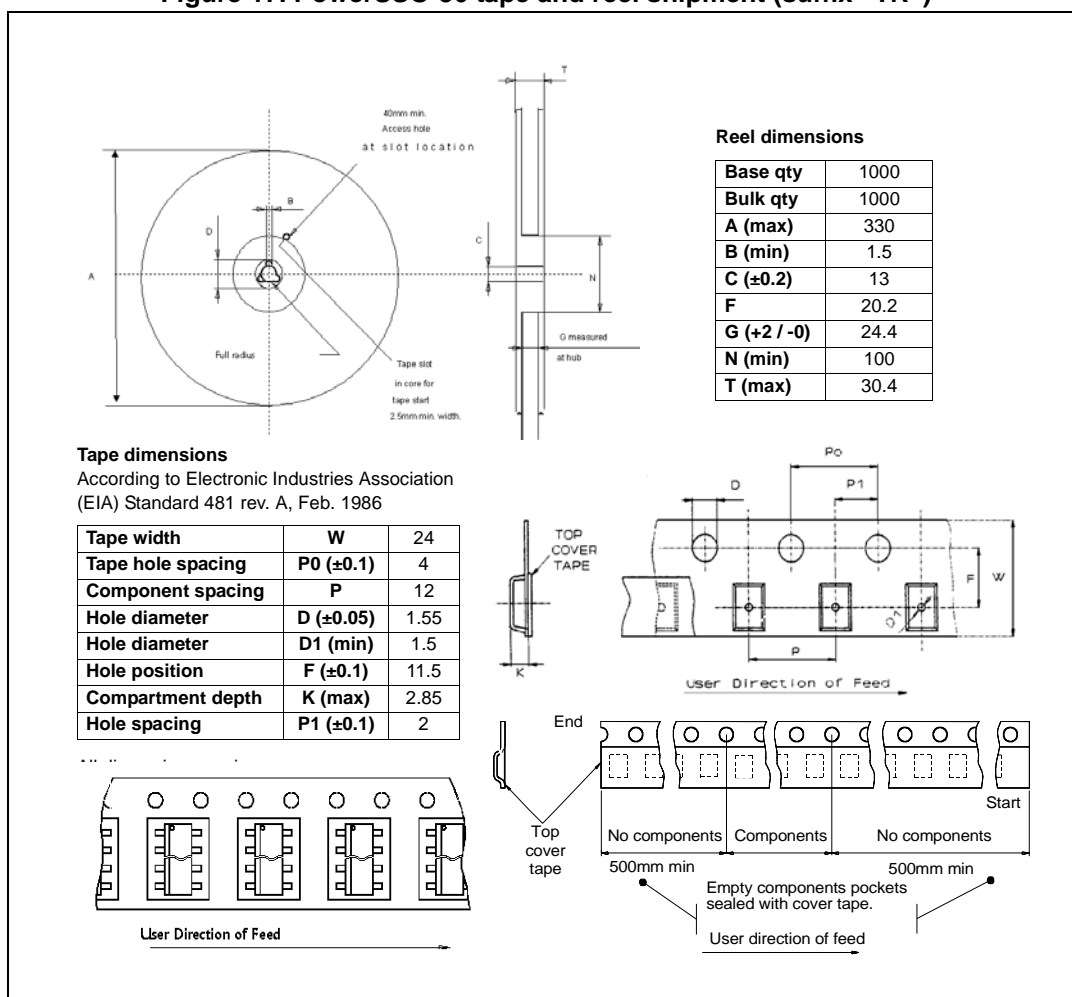
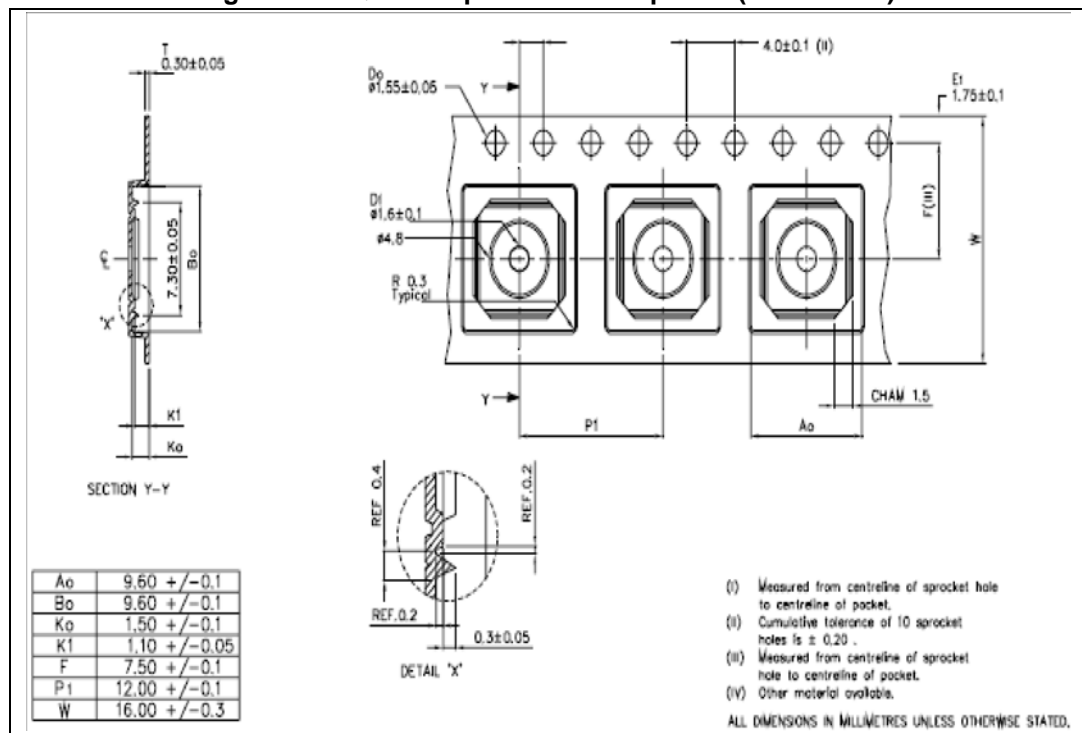


Figure 17. PowerSSO-36 tape and reel shipment (suffix "TR")

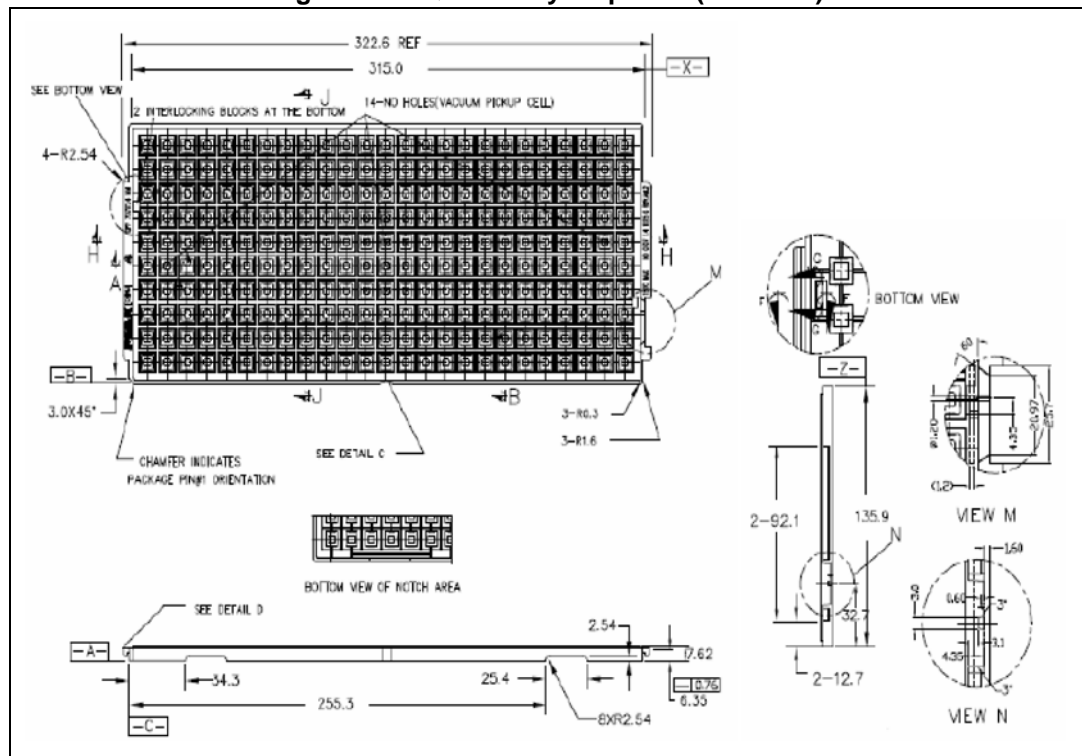


## 6.6 LQFP32 packing information

**Figure 18. LQFP32 tape and reel shipment (suffix “TR”)**



**Figure 19. LQFP32 tray shipment (no suffix)**



## 7 Revision history

Table 50. Document revision history

Date	Revision	Changes
17-Apr-2009	1	Initial release.
19-Aug-2009	2	<p>Updated corporate template from V3 to V3.1</p> <p>Updated <a href="#">Figure 4</a>.</p> <p>Removed items 17.16, 17.18 and 17.20 of the <a href="#">Table 18: Current sense amplifier</a>.</p> <p>Added <a href="#">Table 15: Cross current protection time</a></p> <p><a href="#">Table 18: Current sense amplifier</a>.</p> <ul style="list-style-type: none"> <li>– <math>V_{\text{IOFF}50}</math>, <math>V_{\text{IOFF}20}</math>, <math>V_{\text{IOFF}10}</math>: added min/typ/max value, deleted "<math>T_j = 25\text{ }^{\circ}\text{C}</math>" for test condition</li> <li>– <math>V_{\text{IOFF-T}50}/\Delta T</math>: changed symbol (it was <math>V_{\text{IOFF-T}50}</math>), updated whole row.</li> <li>– <math>V_{\text{IOFF-T}20}/\Delta T</math>: changed symbol (it was <math>V_{\text{IOFF-T}20}</math>), updated whole row.</li> <li>– <math>V_{\text{IOFF-T}10}/\Delta T</math>: changed symbol (it was <math>V_{\text{IOFF-T}10}</math>), updated whole row.</li> <li>– <math>V_{\text{IOFF-}50}</math>, <math>V_{\text{IOFF-}20}</math>, <math>V_{\text{IOFF-}10}</math>: added min/typ/max value</li> <li>– Gain<sub>50</sub>, Gain<sub>20</sub>, Gain<sub>10</sub>: added min/typ/max value</li> <li>– Setting time: deleted row</li> </ul> <p>Added <a href="#">Figure 5: Output timing diagram (passive free wheeling)</a></p> <p>Updated <a href="#">Table 23: Truth table</a>.</p> <p>Updated <a href="#">Section 3.9</a>, <a href="#">Section 3.11</a>, <a href="#">Section 3.12.1</a> and <a href="#">Section 3.12.2</a>.</p> <p><a href="#">Table 30: STK_RESET_Q</a>: changed title (it was "Global status byte")</p> <p>Updated <a href="#">Section 4.4.1</a> and <a href="#">Section 4.6.1</a>.</p> <p>Updated <a href="#">Table 43</a>.</p>
20-Apr-2010	3	Updated the CP value in <a href="#">Table 4: Absolute maximum ratings</a>
30-Apr-2012	4	<p><a href="#">Table 9: Supply</a>:</p> <ul style="list-style-type: none"> <li>– <math>V_{\text{VS\_OV}1}</math>: : changed symbol (it was <math>V_{\text{VS\_OVH}1}</math>)</li> <li>– <math>V_{\text{VS\_OV}1\text{H}}</math>: : changed symbol (it was <math>V_{\text{VS\_OVH}1}</math>)</li> <li>– <math>V_{\text{VS\_OV}2}</math>: : changed symbol (it was <math>V_{\text{VS\_OVH}2}</math>)</li> <li>– <math>V_{\text{VS\_OV}2\text{H}}</math>: : changed symbol (it was <math>V_{\text{VS\_OVH}2}</math>)</li> <li>– <math>V_{\text{VS\_UV}}</math>: : changed symbol (it was <math>V_{\text{VS\_UVH}}</math>)</li> </ul> <p>Updated <a href="#">Section 3.6: Overvoltage and undervoltage detection</a> and <a href="#">Section 3.7: Charge pump</a></p> <p><a href="#">Section 4.6.1: Description of the data byte</a>:</p> <ul style="list-style-type: none"> <li>– updated OV_UV_RD bit description</li> </ul> <p><a href="#">Table 48: PowerSSO-36 mechanical data</a>:</p> <ul style="list-style-type: none"> <li>– L: updated values</li> </ul>
21-Jun-2013	5	Updated <a href="#">Table 17: Thermal sense interface (4.5 V &lt; <math>V_{\text{CC}}</math> &lt; 5.3 V)</a>
19-Sep-2013	6	Updated disclaimer.

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