March 1998

FAIRCHILD SEMICONDUCTOR™

DM74LS395
4-Bit Shift Register with 3-STATE Outputs

General Description

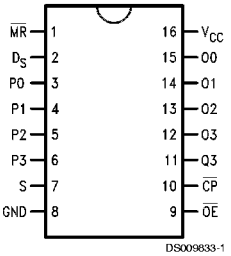
The LS395 is a 4-bit shift register with 3-STATE outputs and can operate in either a synchronous parallel load or a serial shift-right mode, as determined by the Select input. An asynchronous active LOW Master Reset ($\overline{MR}$) input overrides the synchronous operations and clears the register. An active LOW Output Enable ($\overline{OE}$) input controls the 3-STATE output buffers, but does not interfere with the other operations. The fourth stage also has a conventional output for linking purposes in multi-stage serial operations.

Features

- Shift right or parallel 4-bit register
- 3-STATE outputs
- Input clamp diodes limit high speed termination effects
- Fully CMOS and TTL compatible

Connection Diagram

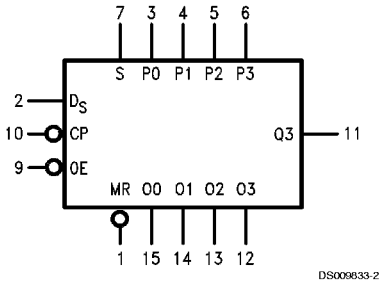
Dual-In-Line Package



DS009833-1

Order Number DM74LS395WM or DM74LS395N
See Package Number M16B or N16E

Logic Symbol



DS009833-2

V_{CC} = Pin 16
GND = Pin 8

Mode Select Table

Operating Mode	Inputs @ t_n					Outputs @ t_{n+1}			
	$\overline{MR}$	$\overline{CP}$	S	D_S	P_n	O0	O1	O2	O3
Asynchronous Reset	L	X	X	X	X	L	L	L	L
Shift, SET First Stage	H	⌐	L	H	X	H	$O0_n$	$O1_n$	02_n
Shift, RESET First Stage	H	⌐	L	L	X	L	$O0_n$	$O1_n$	02_n
Parallel Load	H	⌐	H	X	Pn	P0	P1	P2	P3

t_n, t_{n+1} = Time before and after CP HIGH-to-LOW transition
H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Recommended Operating Conditions

Symbol	Parameter	Min	Nom	Max	Units
V_{CC}	Supply Voltage	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			V
V_{IL}	Low Level Input Voltage			0.8	V
I_{OH}	High Level Output Current			−0.4	mA
I_{OL}	Low Level Output Current			8	mA
T_A	Free Air Operating Temperature	0		70	°C
t_s (H)	Setup Time HIGH or LOW	20			ns
t_s (L)	S, D_S or P_n to CP	20			
t_h (H)	Hold Time HIGH or LOW	5			ns
t_h (L)	S, D_S or P_n to $\overline{CP}$	5			
t_w (L)	$\overline{CP}$ Pulse Width LOW	18			ns
t_w (L)	$\overline{MR}$ Pulse Width LOW	20			ns

Note 1: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Electrical Characteristics

Over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ (Note 2)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA			−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max	2.7			V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IH} = Min		0.35	0.5	V
		I_{OL} = 4 mA, V_{CC} = Min		0.25	0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 7V			0.1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V			20	µA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V			−0.4	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 3)	−20		−100	mA
I_{CC}	Supply Current with Outputs OFF	V_{CC} = Max, $\overline{OE}$, D_S, S = 4.5V $\overline{CP}$ = ⌒, P_n = GND			29	mA
	Supply Current with Outputs ON	V_{CC} = Max, D_S, S = 4.5V $\overline{OE}$, $\overline{CP}$, P_n = GND			25	mA
I_{OZH}	3-STATE Output Off Current HIGH	V_{CC} = V_{CCH} V_{OZH} = 2.7V			20	µA
I_{OZL}	3-STATE Output Off Current LOW	V_{CC} = V_{CCH} V_{OZL} = 0.4V			−20	µA

Note 2: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 3: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Switching Characteristics

V_{CC} = +5.0V, T_A = +25°C

Symbol	Parameter	R_L =2 kΩ, C_L = 15 pF		Units
		Min	Max	
f_{max}	Maximum Shift Frequency	30		MHz
t_{PLH}	Propagation Delay		35	ns
t_{PHL}	$\overline{CP}$ to O_n		25	
t_{PHL}	Propagation Delay		35	ns
	$\overline{MR}$ to O_n			
t_{PZH}	Output Enable Time		20	ns
t_{PZL}			20	
t_{PHZ}	Output Disable Time		17	ns
t_{PLZ}			23	

Functional Description

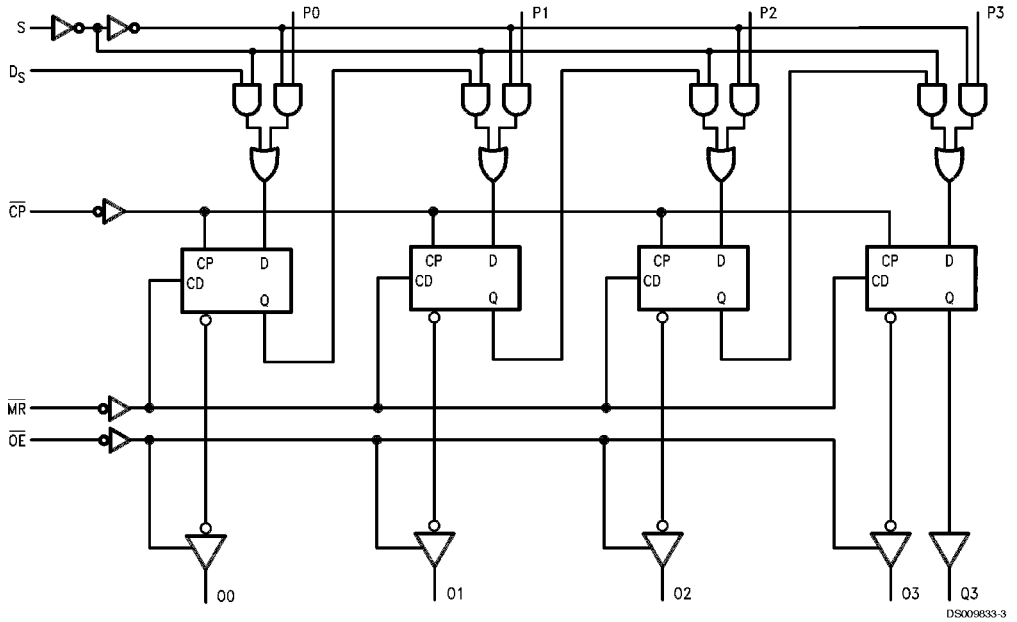
The 'LS395 contains four D-type edge-triggered flip-flops and auxiliary gating to select a D input either from a Parallel (P_n) input or from the preceding stage. When the Select input is HIGH, the P_n inputs are enabled. A LOW signal in the S input enables the serial inputs for shift-right operations, as indicated in the Truth Table.

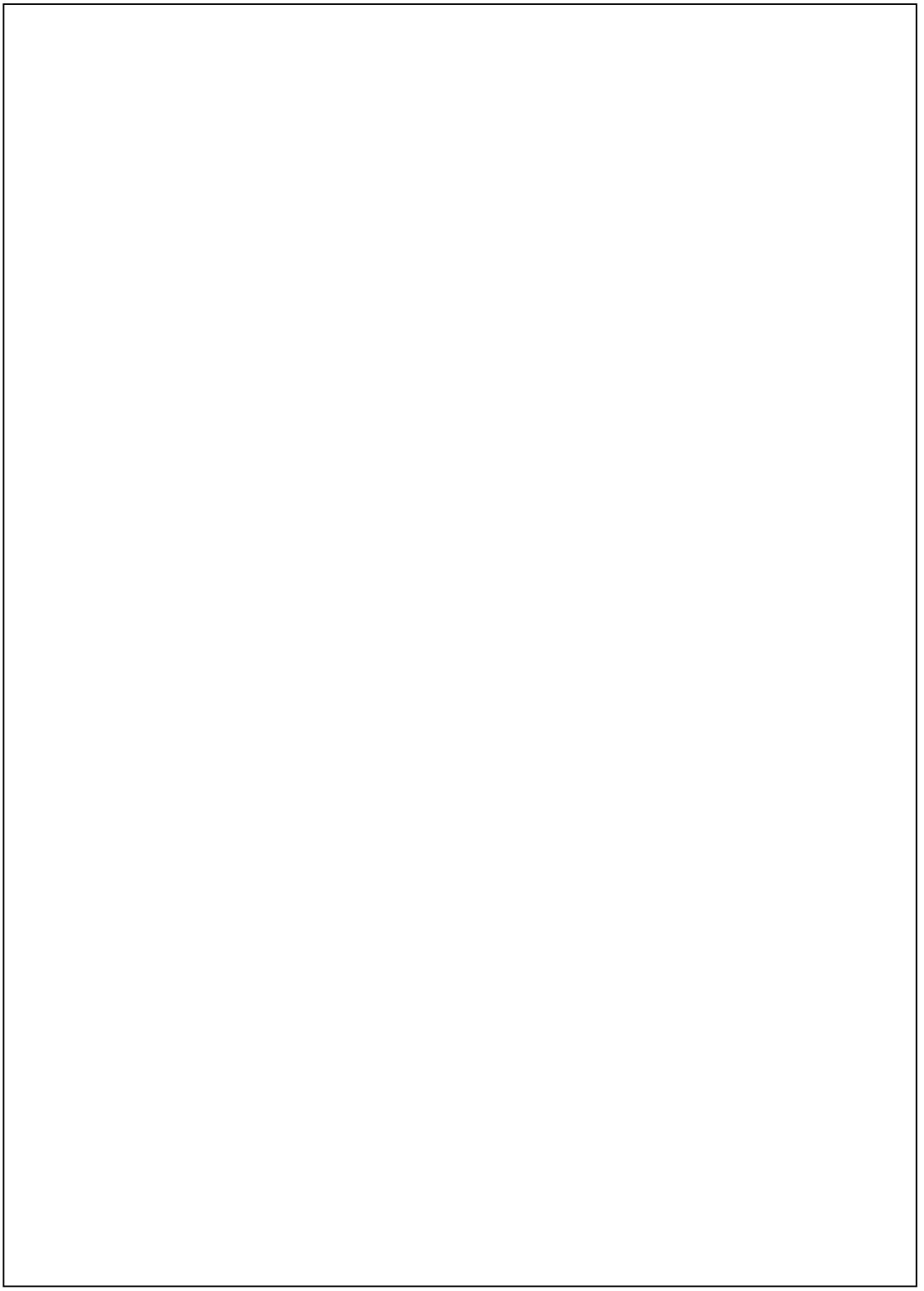
State changes are initiated by HIGH-to-LOW transitions on the Clock Pulse ($\overline{CP}$) input. Signals on the P_n, D_S and S inputs can change when the Clock is in either state, provided that the recommended setup and hold times are observed.

When the S input is LOW, a $\overline{CP}$ HIGH-LOW transition transfers data in O0 to O1, O1 to O2, and O2 to O3. A left-shift is accomplished by connecting the outputs back to the P_n inputs, but offset one place to the left, i.e., O3 to P2, O2 to P1, and O1 to P0, with P3 acting as the linking input from another package.

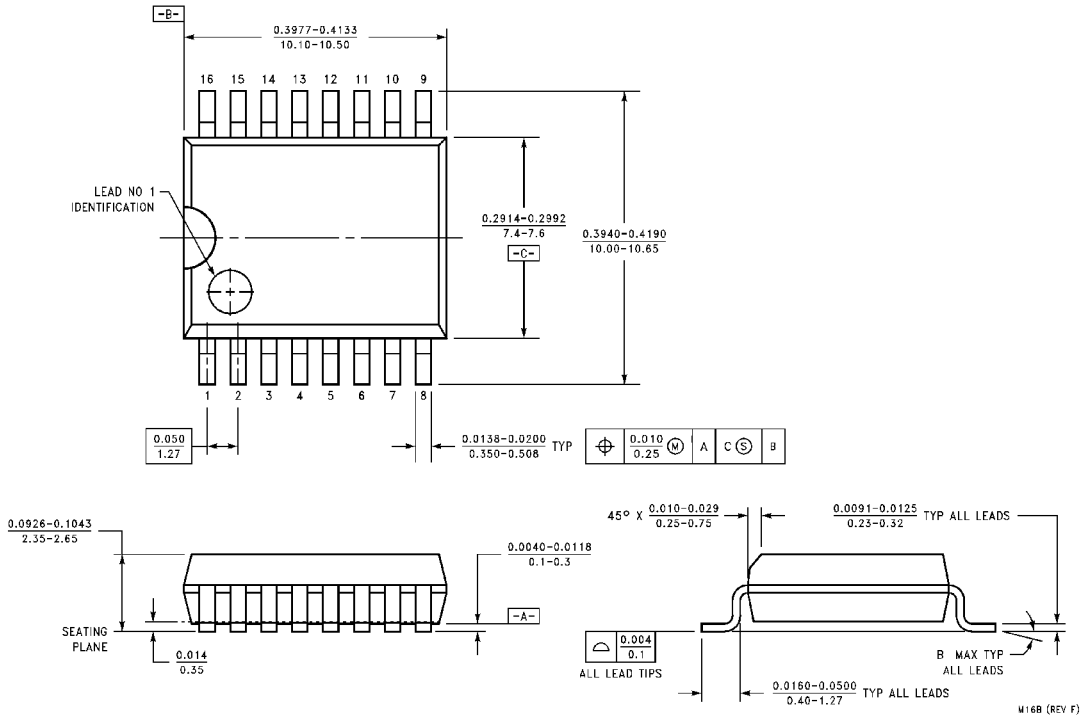
When the $\overline{OE}$ input is HIGH, the output buffers are disabled and the O0–O3 outputs are in a high impedance condition. The shifting, parallel loading or resetting operations can still be accomplished, however.

Logic Diagram

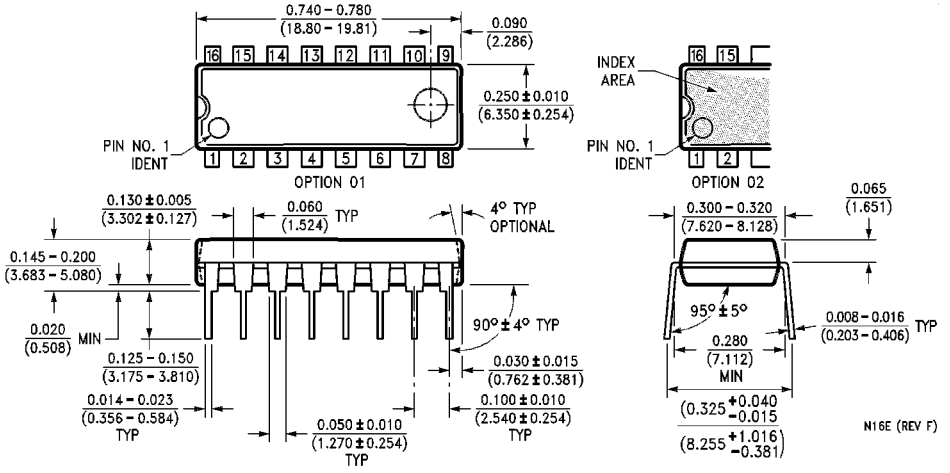




Physical Dimensions inches (millimeters) unless otherwise noted



16-Lead Wide Small Outline Molded Package (M)
Order Number DM74LS395WM
Package Number M16B



16-Lead Molded Dual-In-Line Package (N)
Order Number DM74LS395N
Package Number N16E