

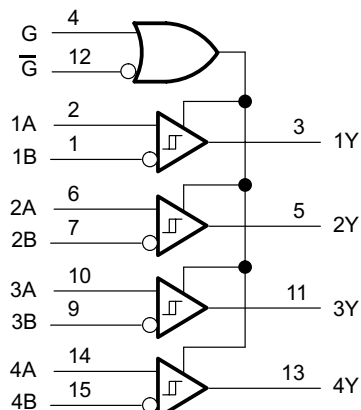
# AM26LS32Ax, AM26LS33Ax Quadruple Differential Line Receivers

## 1 Features

- AM26LS32A Devices meet or exceed the requirements of ANSI TIA/EIA-422-B, TIA/EIA-423-B, and ITU recommendations V.10 and V.11
- AM26LS32A Devices have  $\pm 7$ -V Common-mode range with  $\pm 200$ -mV sensitivity
- AM26LS33A Devices have  $\pm 15$ -V common-mode range with  $\pm 500$ -mV sensitivity
- Input hysteresis 50 mV typical
- Operate from a single 5-V supply
- Low-power Schottky circuitry
- 3-State outputs
- Complementary output-enable inputs
- Input impedance 12 k $\Omega$  minimum
- Open input fail-safe

## 2 Applications

- High-reliability automotive applications
- [Factory automation](#)
- [ATM](#) and cash counters
- Smart grids
- AC and [servo motor](#) drives



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Pin numbers are for D, N, NS, or PW packages only.

### Logic Diagram (Positive Logic)

## 3 Description

The AM26LS32Ax and AM26LS33Ax devices are quadruple differential line receivers for balanced and unbalanced digital data transmission. The enable function is common to all four receivers and offers a choice of active-high or active-low input. The 3-state outputs permit connection directly to a bus-organized system. When the inputs are open, the fail-safe design makes sure the outputs always are high.

Compared to the AM26LS32 and the AM26LS33, the AM26LS32A and AM26LS33A incorporate an additional stage of amplification to improve sensitivity. The input impedance has been increased, resulting in less loading of the bus line. The additional stage has increased propagation delay; however, this does not affect interchangeability in most applications.

The AM26LS32AC and AM26LS33AC are characterized for operation from 0°C to 70°C. The AM26LS32AI is characterized for operation from –40°C to 85°C. The AM26LS32AM and AM26LS33AM are characterized for operation over the full military temperature range of –55°C to 125°C.

### Package Information

PART NUMBER	PACKAGE <sup>(1)</sup>	PACKAGE SIZE <sup>(2)</sup>
AM26LS3xAC	PDIP (16)	19.3 mm × 9.4 mm
AM26LS32AI	SOIC (16)	9.9 mm × 6 mm
AM26LS32AC	SO (16)	10.2 mm × 7.8 mm
	TSSOP (16)	5. mm × 6.4 mm
AM26LS3xAM	CDIP (16)	19.56 mm × 6.92 mm
	LCCC (20)	8.9 mm × 8.9 mm

- (1) For all available packages, see the orderable addendum at the end of the data sheet.
- (2) The package size (length × width) is a nominal value and includes pins, where applicable.



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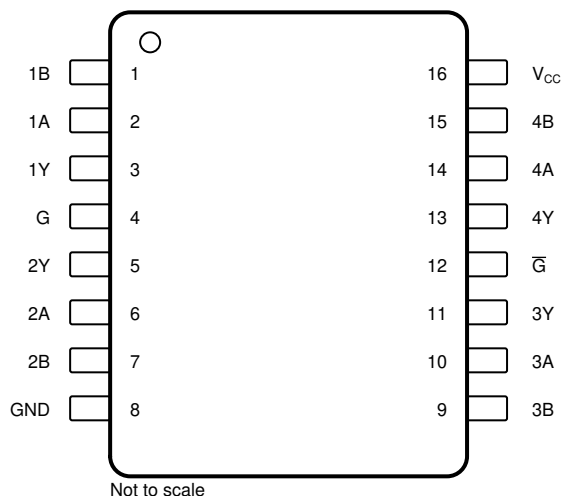
## 4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

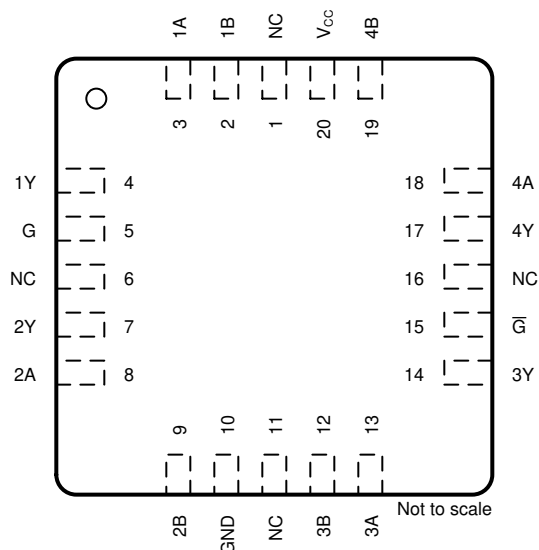
<b>Changes from Revision F (August 2016) to Revision G (August 2023)</b>	<b>Page</b>
• Changed the Device Information table to the <i>Package Information</i> table.....	<b>1</b>
• Changed the <i>Thermal Information</i> table.....	<b>5</b>
• Changed the <i>Typical Characteristics</i> .....	<b>8</b>

<b>Changes from Revision E (October 2007) to Revision F (August 2016)</b>	<b>Page</b>
• Added <i>Applications</i> section, <i>ESD Ratings</i> table, <i>Feature Description</i> section, <i>Device Functional Modes</i> , <i>Application and Implementation</i> section, <i>Power Supply Recommendations</i> section, <i>Layout</i> section, <i>Device and Documentation Support</i> section, and <i>Mechanical, Packaging, and Orderable Information</i> section.....	<b>1</b>
• Changed R <sub>θJA</sub> values in the <i>Thermal Information</i> table: 73 to 75.7 for (D), 67 to 45.3 (N), 64 to 75.8 (NS), and 108 to 102.7 (PW).....	<b>5</b>

## 5 Pin Configuration and Functions



**Figure 5-1. D, J, N, NS, and PW Package 16-Pin  
SOIC, CDIP, PDIP, SO, and TSSOP  
(Top View)**



NC - No internal connection

**Figure 5-2. FK Package, 20-Pin LCCC  
(Top View)**

NAME	PIN		TYPE	DESCRIPTION
	SOIC, CDIP, PDIP, SO, TSSOP	LCCC		
1A	2	3	I	RS422/RS485 differential input (noninverting)
1B	1	2	I	RS422/RS485 differential input (inverting)
1Y	3	4	O	Logic level output
2A	6	8	I	RS422/RS485 differential input (noninverting)
2B	7	9	I	RS422/RS485 differential input (inverting)
2Y	5	7	O	Logic level output
3A	10	13	I	RS422/RS485 differential input (noninverting)
3B	9	12	I	RS422/RS485 differential input (inverting)
3Y	11	14	O	Logic level output
4A	14	18	I	RS422/RS485 differential input (noninverting)
4B	15	19	I	RS422/RS485 differential input (inverting)
4Y	13	17	O	Logic level output
$\bar{G}$	12	15	I	Active-Low select
G	4	5	I	Active-High select
GND	8	10	—	Ground
NC	—	1, 6, 11, 16	—	No internal connection
V <sub>CC</sub>	16	20	—	Power supply

## 6 Specifications

### 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

		MIN	MAX	UNIT
Supply voltage, $V_{CC}$ <sup>(2)</sup>			7	V
Input voltage, $V_I$	Any differential input		±25	V
	Other inputs		7	
Differential input voltage, $V_{ID}$ <sup>(3)</sup>			±25	V
Continuous total power dissipation		See <a href="#">Section 6.7</a>		
Case temperature, $T_C$ , FK package (60 s)			260	°C
Lead temperature <sup>(4)</sup>	D or N package (10 s)		260	°C
	J package (60 s)		300	
Storage temperature, $T_{stg}$		–65	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltage values, except differential voltages, are with respect to the network ground terminal.
- (3) Differential voltage values are at the noninverting (A) input terminals with respect to the inverting (B) input terminals.
- (4) 1.6 mm (1/16 inch) from case

### 6.2 ESD Ratings

		VALUE	UNIT
$V_{(ESD)}$ Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>	±500	V
	Charged-device model (CDM), per JEDEC specification JESD22-C101 <sup>(2)</sup>	±2000	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

### 6.3 Recommended Operating Conditions

		MIN	NOM	MAX	UNIT
$V_{CC}$ Supply voltage	AM26LS32AC, AM26LS32AI, AM26LS33AC	4.75	5	5.25	V
	AM26LS32AM, AM26LS33AM	4.5	5	5.5	
$V_{IH}$ High-level input voltage		2			V
$V_{IL}$ Low-level input voltage				0.8	V
$V_{IC}$ Common-mode input voltage	AM26LS32A			±7	V
	AM26LS33A			±15	
$I_{OH}$ High-level output current				–440	μA
$I_{OL}$ Low-level output current				8	mA
$T_A$ Operating free-air temperature	AM26LS32AC, AM26LS33AC	0		70	°C
	AM26LS32AI	–40		85	
	AM26LS32AM, AM26LS33AM	–55		125	

## 6.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>	AM26LS3xAC, AM26LS32AI				AM26LS32AC				UNIT
	D (SOIC)	DR (SOIC-Reel)	N (PDIP)	NR (PDIP-Reel)	NS (SO)	NSR (SO-Reel)	PW (TSSOP)	PWR (TSSOP-Reel)	
	16 PINS	16 PINS	16 PINS	16 PINS	16 PINS	16 PINS	16 PINS	16 PINS	
$R_{\theta JA}$ Junction-to-ambient thermal resistance	75.7	84.6	45.3	60.6	75.8	88.5	102.7	107.5	°C/W
$R_{\theta JC(top)}$ Junction-to-case (top) thermal resistance	35	43.5	32.7	48.1	32.9	46.2	37.8	38.4	°C/W
$R_{\theta JB}$ Junction-to-board thermal resistance	33.3	43.2	25.3	40.6	36.6	50.7	47.7	53.7	°C/W
$\Psi_{JT}$ Junction-to-top characterization parameter	6.6	10.4	17.8	27.5	6	13.5	3	3.2	°C/W
$\Psi_{JB}$ Junction-to-board characterization parameter	33	42.8	25.1	40.3	36.3	50.3	47.1	53.1	°C/W

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

## 6.5 Electrical Characteristics

over recommended ranges of  $V_{CC}$ ,  $V_{IC}$ , and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP <sup>(1)</sup>	MAX	UNIT
$V_{IT+}$	Positive-going input threshold voltage	$V_O = V_{OHmin}$ , $I_{OH} = -440 \mu A$	AM26LS32A			0.2	V
			AM26LS33A			0.5	
$V_{IT-}$	Negative-going input threshold voltage	$V_O = 0.45 V$ , $I_{OL} = 8 mA$	AM26LS32A	-0.2 <sup>(2)</sup>			V
			AM26LS33A	-0.5 <sup>(2)</sup>			
$V_{hys}$	Hysteresis voltage ( $V_{IT+} - V_{IT-}$ )				50		mV
$V_{IK}$	Enable-input clamp voltage	$V_{CC} = MIN$ , $I_I = -18 mA$				-1.5	V
$V_{OH}$	High-level output voltage	$V_{CC} = MIN$ , $V_{ID} = 1 V$ , $V_{I(G)} = 0.8 V$ , $I_{OH} = -440 \mu A$	AM26LS32AC, AM26LS33AC		2.7		V
			AM26LS32AM, AM26LS32AI, AM26LS33AM		2.5		
$V_{OL}$	Low-level output voltage	$V_{CC} = MIN$ , $V_{ID} = -1 V$ , $V_{I(G)} = 0.8 V$	$I_{OL} = 4 mA$			0.4	V
			$I_{OL} = 8 mA$			0.45	
$I_{OZ}$	Off-state (high-impedance state) output current	$V_{CC} = MAX$	$V_O = 2.4 V$			20	$\mu A$
			$V_O = 0.4 V$			-20	
$I_I$	Line input current	$V_I = 15 V$ , other input at $-10 V$ to $15 V$				1.2	mA
		$V_I = -15 V$ , other input at $-15 V$ to $10 V$				-1.7	
$I_{I(EN)}$	Enable input current	$V_I = 5.5 V$				100	$\mu A$
$I_H$	High-level enable current	$V_I = 2.7 V$				20	$\mu A$
$I_L$	Low-level enable current	$V_I = 0.4 V$				-0.36	mA
$r_i$	Input resistance	$V_{IC} = -15 V$ to $15 V$ , one input to ac ground		12	15		k $\Omega$
$I_{OS}$	Short-circuit output current <sup>(3)</sup>	$V_{CC} = MAX$		-15		-85	mA
$I_{CC}$	Supply current	$V_{CC} = MAX$ , all outputs disabled			52	70	mA

(1) All typical values are at  $V_{CC} = 5 V$ ,  $T_A = 25^\circ C$ , and  $V_{IC} = 0$ .

(2) The algebraic convention, in which the less positive (more negative) limit is designated as minimum, is used in this data sheet for threshold levels only.

(3) Not more than one output must be shorted to ground at a time, and duration of the short circuit must not exceed one second.

## 6.6 Switching Characteristics

$C_L = 15 \text{ pF}$ ,  $V_{CC} = 5 \text{ V}$ , and  $T_A = 25^\circ\text{C}$  (see [Section 7](#); unless otherwise noted)

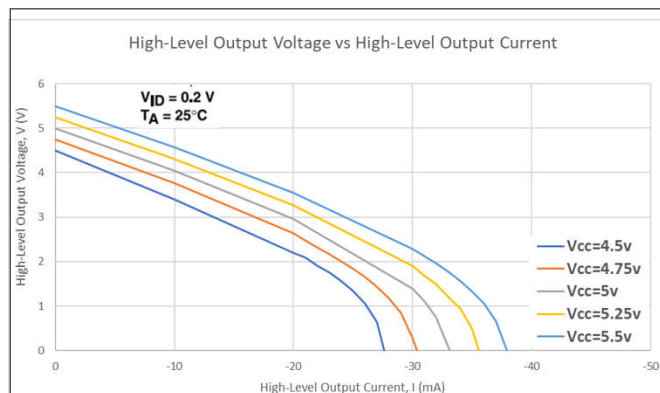
PARAMETER		MIN	TYP <sup>(1)</sup>	MAX	UNIT
$t_{PLH}$	Propagation delay time, low-to-high-level output		20	35	ns
$t_{PHL}$	Propagation delay time, high-to-low-level output		22	35	ns
$t_{PZH}$	Output enable time to high level		17	22	ns
$t_{PZL}$	Output enable time to low level		20	25	ns
$t_{PHZ}$	Output disable time from high level		21	30	ns
$t_{PLZ}$	Output disable time from low level		30	40	ns

(1) All typical values are at  $V_{CC} = 5 \text{ V}$ ,  $T_A = 25^\circ\text{C}$ , and  $V_{IC} = 0$ .

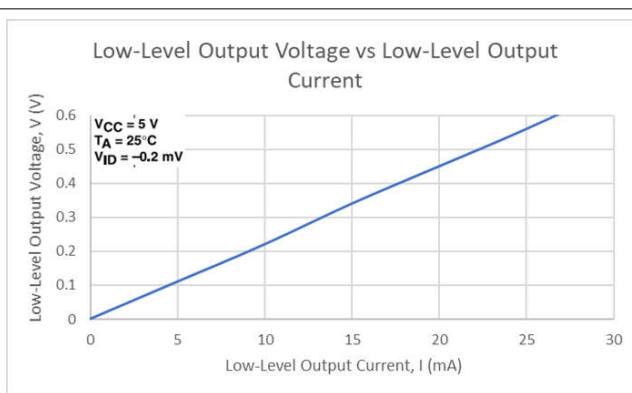
## 6.7 Dissipation Ratings

PACKAGE	$T_A \leq 25^\circ\text{C}$ POWER RATING	DERATION FACTOR ABOVE $T_A = 25^\circ\text{C}$	$T_A = 70^\circ\text{C}$ POWER RATING	$T_A = 125^\circ\text{C}$ POWER RATING
FK	1375 mW	11 mW/ $^\circ\text{C}$	880 mW	275 mW
J	1375 mW	11 mW/ $^\circ\text{C}$	880 mW	275 mW

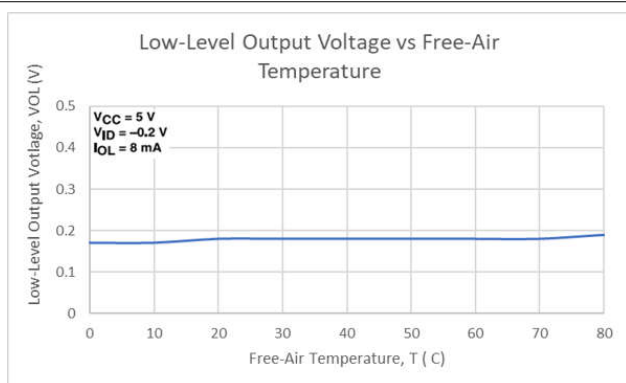
## 6.8 Typical Characteristics



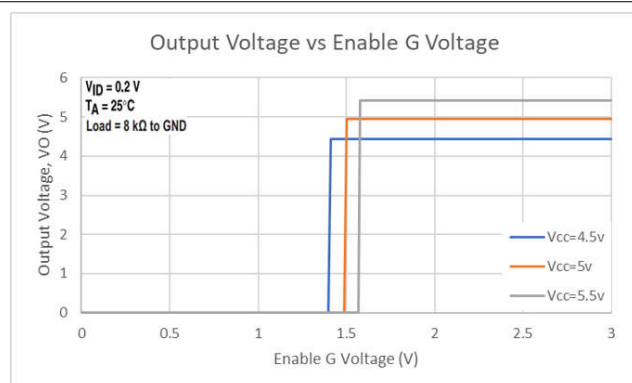
**Figure 6-1. High-Level Output Voltage vs High-Level Output Current**



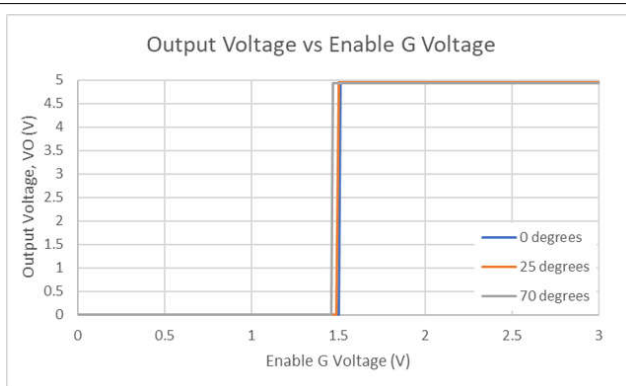
**Figure 6-2. Low-Level Output Voltage vs Low-Level Output Current**



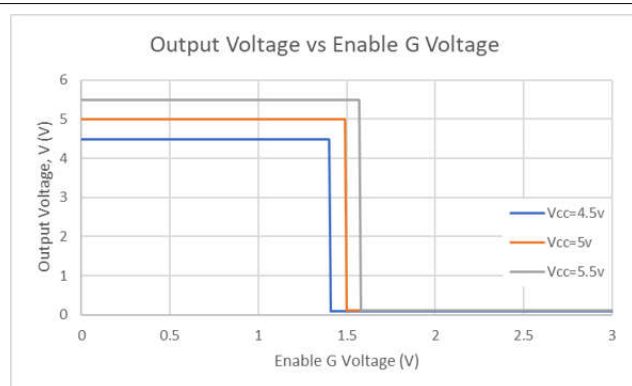
**Figure 6-3. Low-Level Output Voltage vs Free-Air Temperature**



**Figure 6-4. Output Voltage vs Enable G Voltage**

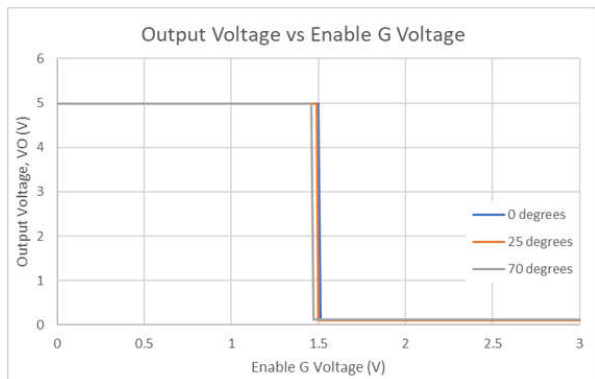


**Figure 6-5. Output Voltage vs Enable G Voltage**

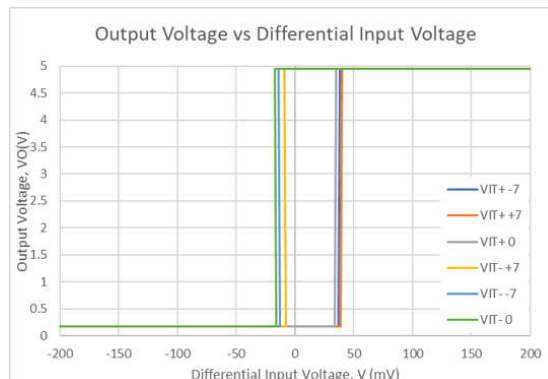


**Figure 6-6. Output Voltage vs Enable G Voltage**

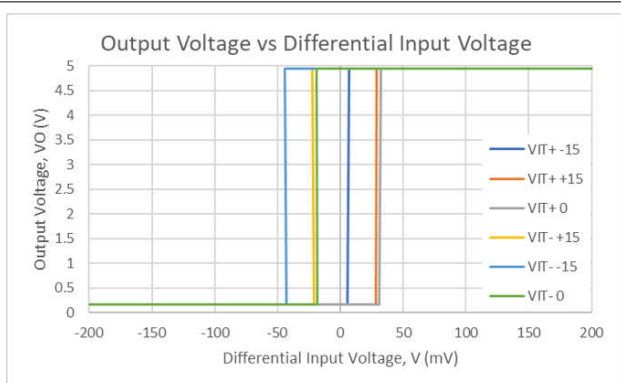




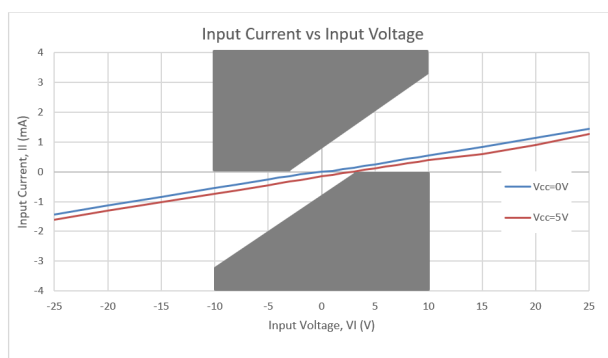
**Figure 6-7. Output Voltage vs Enable G Voltage**



**Figure 6-8. AM26LS32A Output Voltage vs Differential Input Voltage**



**Figure 6-9. AM26LS33A Output Voltage vs Differential Input Voltage**



The unshaded area shows requirements of paragraph 4.2.1 of ANSI Standards EIA/TIA-422-B and EIA/TIA-423-B.

**Figure 6-10. Input Current vs Input Voltage**

## 7 Parameter Measurement Information

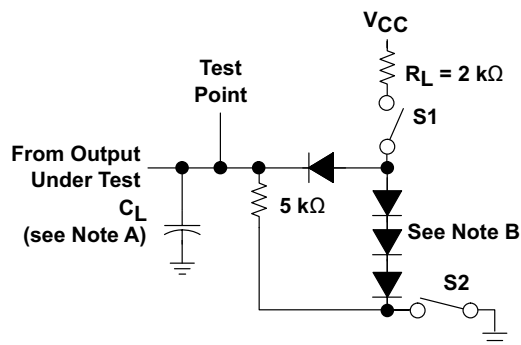


Figure 7-1. Test Circuit

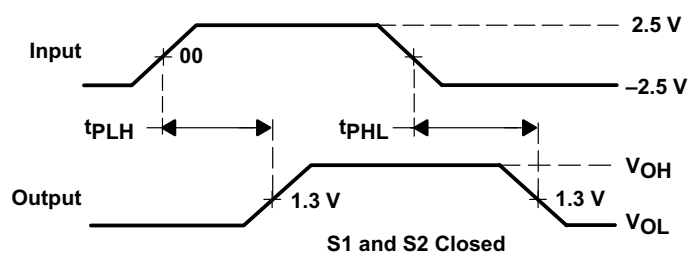


Figure 7-2. Voltage Waveforms For  $t_{PLH}$ ,  $t_{PHL}$

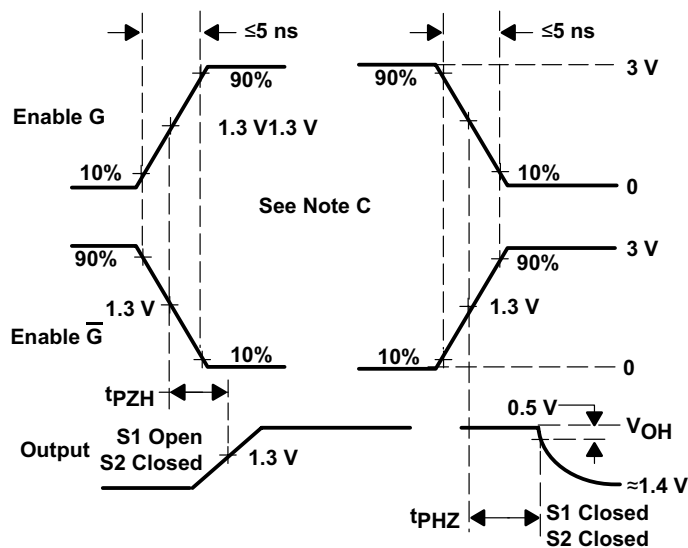
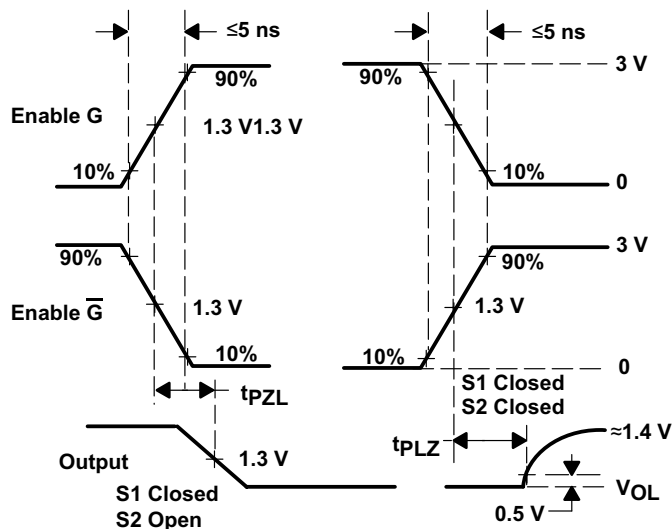
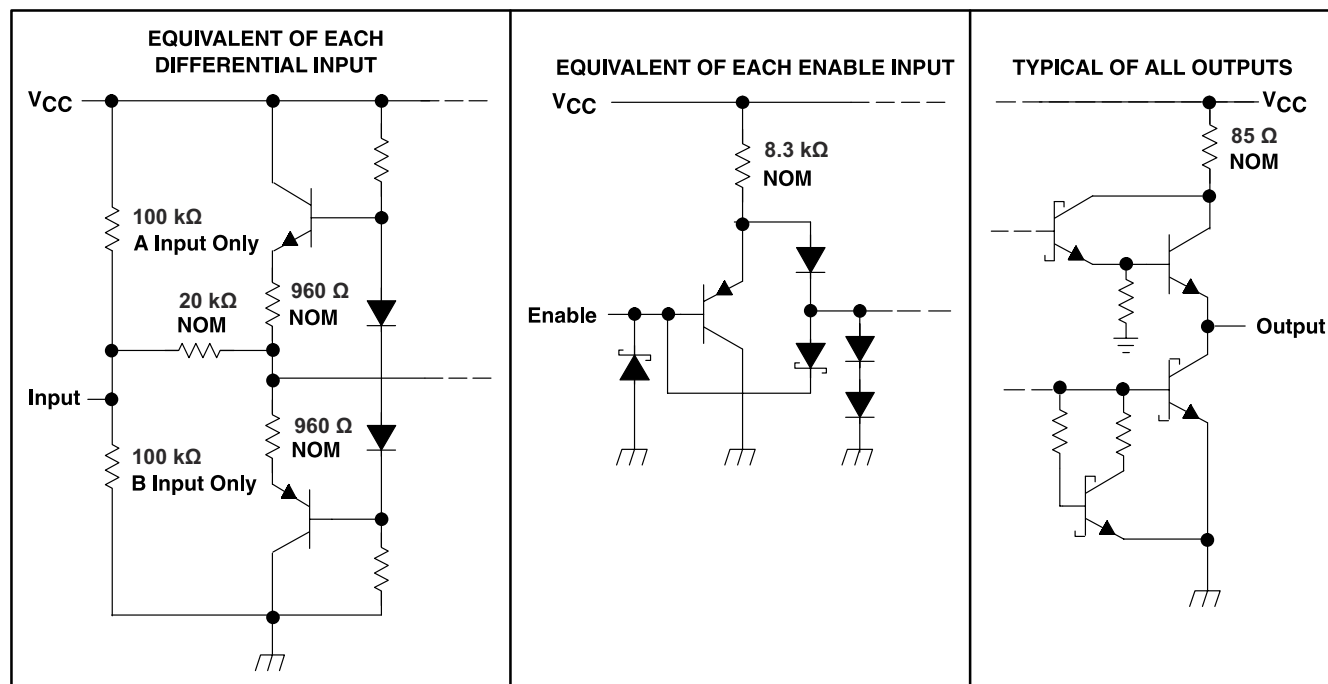


Figure 7-3. Voltage Waveforms For  $t_{PHZ}$ ,  $t_{PZH}$



- A. CL includes probe and jig capacitance.
- B. All diodes are 1N3064 or equivalent.
- C. Enable G is tested with  $\bar{G}$  high,  $\bar{G}$  is tested with G low.

Figure 7-4. Voltage Waveforms For  $t_{PLZ}$ ,  $t_{PZL}$



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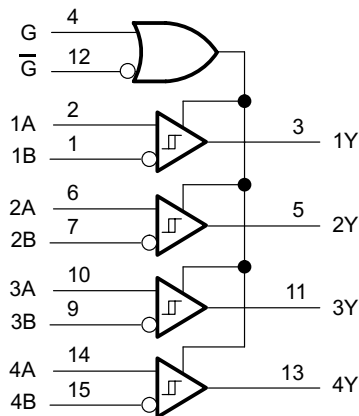
Figure 7-5. Schematics of Inputs and Outputs

## 8 Detailed Description

### 8.1 Overview

The AM26LS32 is a quadruple-differential line receiver that meets the necessary requirements for NSI TIA/EIA-422-B, TIA/EIA-423-B, and ITU Recommendation V.10 and V.11. This device allows a low-power or low-voltage MCU to interface with heavy machinery, subsystems, and other devices through long wires of up to 1000 m, giving any design a reliable and easy-to-use connection. As any RS422 interface, the AM26LS32 works in a differential voltage range, which enables very good signal integrity.

### 8.2 Functional Block Diagram



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**Figure 8-1. Logic Diagram (Positive Logic)**

### 8.3 Feature Description

The device can be configured using the G and  $\bar{G}$  logic inputs to select receiver output. The high voltage or logic 1 on the G pin allows the device to operate on an active-high, and having a low voltage or logic 0 on the G enables active low operation. These are simple ways to configure the logic to match that of the receiving or transmitting controller or microprocessor.

### 8.4 Device Functional Modes

The receivers implemented in these RS422 devices can be configured using the G and  $\bar{G}$  logic pins to be enabled or disabled. This allows users to ignore or filter out transmissions as desired.

**Table 8-1. Function Table, Each Receiver**

DIFFERENTIAL A–B	ENABLES <sup>(1)</sup>		OUTPUT <sup>(1)</sup> Y
	G	$\bar{G}$	
$V_{ID} \geq V_{IT+}$	H	X	H
	X	L	H
$V_{IT-} \leq V_{ID} \leq V_{IT+}$	H	X	?
	X	L	?
$V_{ID} \leq V_{IT-}$	H	X	L
	X	L	L
X	L	H	Z
Open	H	X	H
	X	L	H

(1) H = High level, L = Low level, X = Irrelevant, Z = High impedance (off), ? = Indeterminate

## 9 Application and Implementation

### Note

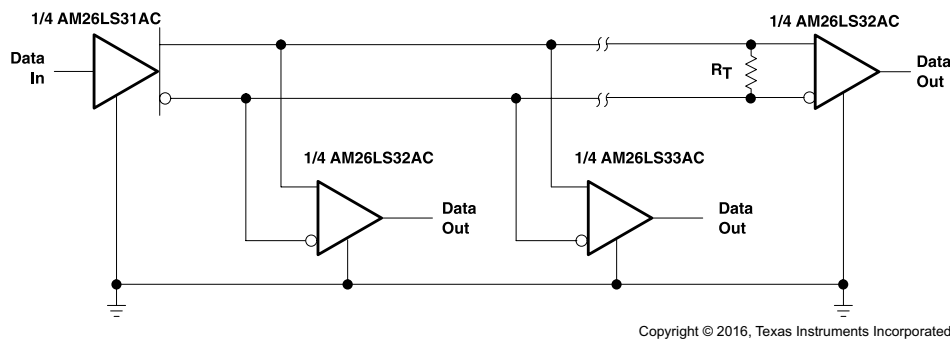
Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

### 9.1 Application Information

When using AM26LS32A as a receiver, the AM26LS31AC can allow multiple AM26LS32As to be used causing an increase in the amount of outputs.

### 9.2 Typical Application

Figure 9-1 shows a configuration with no termination. Although reflections are present at the receiver inputs at a data signaling rate of 200 kbps with no termination, the RS-422-compliant receiver reads only the input differential voltage and produces a clean signal at the output.



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<sup>†</sup>R<sub>T</sub> equals the characteristic impedance of the line.

**Figure 9-1. Application Diagram**

#### 9.2.1 Design Requirements

Resistor and capacitor (if used) termination values are shown for each laboratory experiment, but vary from system to system. For example, the termination resistor, R<sub>T</sub>, must be within 20% of the characteristic impedance, Z<sub>O</sub>, of the cable and can vary from about 80 Ω to 120 Ω.

#### 9.2.2 Detailed Design Procedure

Add a V<sub>CC</sub> bypass capacitor (0.1 μF or more). Either enable (G pin) input can turn on the receivers, so connect the desired enable to a compatible logic line output. The other enable input must be tied to the inactive state supply rail. If the receivers must always be active, then connect both enables to the supply rail such that at least one is set to an active-state rail. V<sub>CC</sub> must be 5 V within 10% and logic inputs must provide TTL-compatible voltage levels. A & B Inputs can lead to an external connector or can be left unconnected. The last receiver on a cable requires termination, either on-board or use as an external resistor. Unused Y outputs can be left unconnected.

### 9.2.3 Application Curve

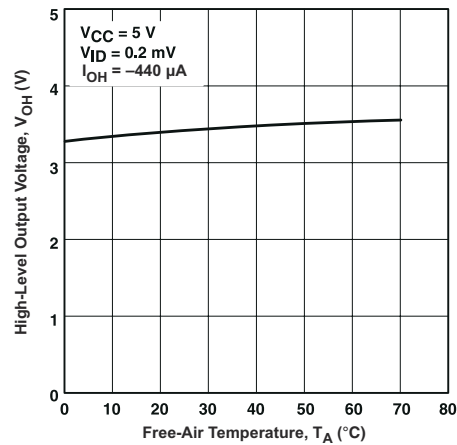


Figure 9-2. High-Level Output Voltage vs Free-Air Temperature

## 9.3 Power Supply Recommendations

Place 0.1- $\mu$ F bypass capacitors close to the power-supply pins to reduce errors coupling in from noisy or high-impedance power supplies.

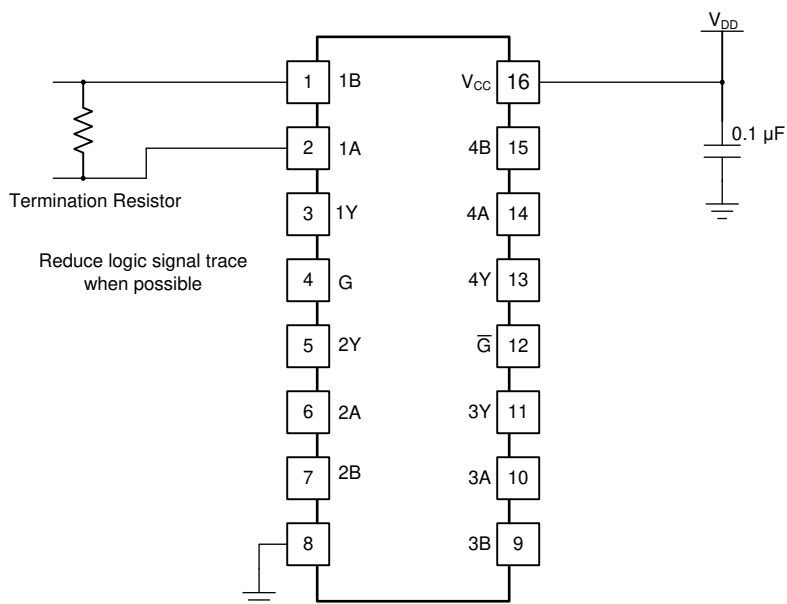
## 9.4 Layout

### 9.4.1 Layout Guidelines

For best operational performance of the device, use good PCB layout practices including:

- Noise can propagate into analog circuitry through the power pins of the circuit as a whole, as well as the operational amplifier. Bypass capacitors are used to reduce the coupled noise by providing low impedance power sources local to the analog circuitry.
- Connect low-ESR, 0.1- $\mu$ F ceramic bypass capacitors between each supply pin and ground, placed as close to the device as possible. A single bypass capacitor from  $V+$  to ground is applicable for single supply applications.
- Separate grounding for analog and digital portions of circuitry is one of the simplest and most-effective methods of noise suppression. One or more layers on multilayer PCBs are usually devoted to ground planes. A ground plane helps distribute heat and reduces EMI noise pickup. Make sure to physically separate digital and analog grounds, paying attention to the flow of the ground current.
- To reduce parasitic coupling, run the input traces as far away from the supply or output traces as possible. If it is not possible to keep them separate, it is much better to cross the sensitive trace perpendicular as opposed to in parallel with the noisy trace.
- Place the external components as close to the device as possible. Keeping RF and RG close to the inverting input minimizes parasitic capacitance.
- Keep the length of input traces as short as possible. Always remember that the input traces are the most sensitive part of the circuit.
- Consider a driven, low-impedance guard ring around the critical traces. A guard ring can significantly reduce leakage currents from nearby traces that are at different potentials.

## 9.4.2 Layout Example



**Figure 9-3. Layout with PCB Recommendations**

## 10 Device and Documentation Support

### 10.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on [ti.com](https://www.ti.com). Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

### 10.2 Support Resources

TI E2E™ [support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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### 10.3 Trademarks

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### 10.4 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

### 10.5 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

## 11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.



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