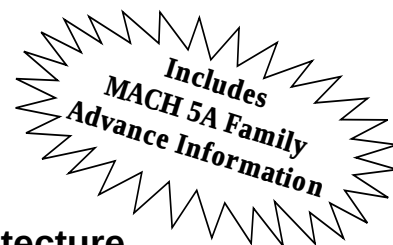




MACH 5 CPLD Family

Fifth Generation MACH Architecture



FEATURES

- ◆ **High logic densities and I/Os for increased logic integration**
 - 128 to 512 macrocell densities
 - 68 to 256 I/Os
- ◆ **Wide selection of density and I/O combinations to support most application needs**
 - 6 macrocell density options
 - 8 I/O options
 - Up to 5 I/O options per macrocell density
 - Up to 6 density & I/O options for each package
- ◆ **Performance features to fit system needs**
 - 5.5 ns t_{PD} Commercial, 7.5 ns t_{PD} Industrial
 - 182 MHz f_{CNT}
 - Four programmable power/speed settings per block
- ◆ **Flexible architecture facilitates logic design**
 - Multiple levels of switch matrices allow for performance-based routing
 - 100% routability and pin-out retention
 - Synchronous and asynchronous clocking, including dual-edge clocking
 - Asynchronous product- or sum-term set or reset
 - 16 to 64 output enables
 - Functions of up to 32 product terms
- ◆ **Advanced capabilities for easy system integration**
 - 3.3-V & 5-V JEDEC-compliant operations
 - JTAG (IEEE 1149.1) compliant for boundary scan testing
 - 3.3-V & 5-V JTAG in-system programming
 - PCI compliant (-5/-6/-7/-10/-12 speed grades)
 - Safe for mixed supply voltage system design
 - Programmable pull-up or Bus-Friendly™ Inputs & I/Os
 - Individual output slew rate control
 - Hot socketing
 - Programmable security bit
- ◆ **Advanced EE CMOS process provides high performance, cost effective solutions**
- ◆ **Supported by Vantis DesignDirect™ software for rapid logic development**
 - Supports HDL design methodologies with results optimized for Vantis
 - Flexibility to adapt to user requirements
 - Software partnerships that ensure customer success
- ◆ **Vantis and Third-party hardware programming support**
 - Lattice/VantisPRO™ (formerly known as MACHPRO®) software for in-system programmability support on PCs and Automated Test Equipment
 - Programming support on all major programmers including Data I/O, BP Microsystems, Advin, and System General

Table 1. MACH 5 Device Features ¹

Feature	M5-128 M5LV-128		M5-192	M5-256 M5LV-256		M5-320 M5LV-320		M5-384 M5LV-384		M5-512 M5LV-512	
Supply Voltage (V)	5	3.3	5	5	3.3	5	3.3	5	3.3	5	3.3
Macrocells	128	128	192	256	256	320	320	384	384	512	512
Maximum User I/O Pins	120	120	160	160	160	192	192	192	192	256	256
t _{PD} (ns)	7.5	5.5	7.5	7.5	5.5	7.5	7.5	7.5	7.5	7.5	7.5
t _{SS} (ns)	4.0	3.0	4.0	4.0	3.0	4.0	4.0	4.0	4.0	4.0	4.0
t _{COS} (ns)	6.0	4.5	6.0	6.0	4.5	6.0	6.0	6.0	6.0	6.0	6.0
f _{CNT} (MHz)	125	182	125	125	182	125	125	125	125	125	125
Static Power (mA)	35	35	45	55	55	70	70	75	75	100	100
JTAG-Compliant	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
PCI-Compliant	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes

Note:

1. “M5-xxx” is for 5-V devices. “M5LV-xxx” is for 3.3-V devices.

Table 2. MACH 5A Device Features ^{1,2}

Feature	M5A3-128 M5A5-128		M5A3-192 M5A5-192		M5A3-256 M5A5-256		M5A3-320	M5A3-384	M5A3-512
Supply Voltage (V)	3.3	5	3.3	5	3.3	5	3.3	3.3	3.3
Macrocells	128	128	192	192	256	256	320	384	512
Maximum User I/O Pins	120	120	120	120	160	160	192	192	256
t _{PD} (ns)	5.5	5.5	5.5	5.5	5.5	5.5	5.5	5.5	5.5
t _{SS} (ns)	3.0	3.0	3.0	3.0	3.0	3.0	3.0	3.0	3.0
t _{COS} (ns)	4.5	4.5	4.5	4.5	4.5	4.5	4.5	4.5	4.5
f _{CNT} (MHz)	182	182	182	182	182	182	182	182	182
Static Power (mA)	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD
JTAG-Compliant	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
PCI-Compliant	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes

Notes:

1. All information on MACH 5A devices is Advance Information. Please contact a Vantis sales representative for details on availability.

2. “M5A5-xxx” is for 5-V devices “M5A3-xxx” is for 3.3-V devices.

GENERAL DESCRIPTION

The MACH[®] 5 family consists of a broad range of high-density and high-I/O Complex Programmable Logic Devices (CPLDs). The fifth-generation MACH architecture yields fast speeds at high CPLD densities, low power, and supports additional features such as in-system programmability, JTAG testability, and advanced clocking options (Tables 1 and 2). Both the MACH 5 and the MACH 5A families offer 5-V (M5-xxx and M5A5-xxx) and 3.3-V (M5LV-xxx and M5A3-xxx) operation.

Manufactured in state-of-the-art ISO 9000 qualified fabrication facilities on EECMOS process technologies, MACH 5 devices are available with pin-to-pin delays as fast as 5.5 ns (Tables 3 and 4). The 5.5, 6.5, 7.5, 10, and 12-ns devices are compliant with the *PCI Local Bus Specification*.

Table 3. MACH 5 Speed Grades

Device	Speed Grade ¹					
	-5	-7	-10	-12	-15	-20
M5-128		C	C, I	C, I	C, I	I
M5LV-128	C	C, I	C, I	C, I	I	
M5-192		C	C, I	C, I	C, I	I
M5-256		C	C, I	C, I	C, I	I
M5LV-256	C	C, I	C, I	C, I	I	
M5-320		C	C, I	C, I	C, I	I
M5LV-320		C	C, I	C, I	C, I	I
M5-384		C	C, I	C, I	C, I	I
M5LV-384		C	C, I	C, I	C, I	I
M5-512		C	C, I	C, I	C, I	I
M5LV-512		C	C, I	C, I	C, I	I

Note:

1. C = Commercial grade, I = Industrial grade

Table 4. MACH 5A Speed Grades

Device	Speed Grade ¹					
	-5	-6	-7	-10	-12	-15
M5A3-128	C		C, I	C, I	C, I	I
M5A5-128	C		C, I	C, I	C, I	I
M5A3-192	C		C, I	C, I	C, I	I
M5A5-192	C		C, I	C, I	C, I	I
M5A3-256	C		C, I	C, I	C, I	I
M5A5-256	C		C, I	C, I	C, I	I
M5A3-320	C (Note 2)	C (Note 2)	C, I (Note 2)	C, I	C, I	I
M5A3-384	C (Note 2)	C (Note 2)	C, I (Note 2)	C, I	C, I	I
M5A3-512		C (Note 2)	C, I (Note 2)	C, I	C, I	I

Notes:

1. C = Commercial grade, I = Industrial grade. All information on MACH 5A devices is Advance Information. Please contact a Vantis sales representative for details on availability.
2. The -5 and -6 commercial and -7 industrial speed grades are under development for M5A3-320, M5A3-384, and M5A3-512. Please contact a Vantis sales representative for details on availability.

With Vantis' unique hierarchical architecture, the MACH 5 family provides densities up to 512 macrocells to support full system logic integration. Extensive routing resources ensure pinout retention as well as high utilization. It is ideal for PAL[®] block device integration and a wide range of other applications including high-speed computing, low-power applications, communications, and embedded control. At each macrocell density point, Vantis offers several I/O and package options to meet a wide range of design needs (Tables 5 and 6).

Table 5. MACH 5 Package and I/O Options ¹

Package	M5-128 M5LV-128	M5-192	M5-256 M5LV-256	M5-320 M5LV-320	M5-384 M5LV-384	M5-512 M5LV-512
100-pin TQFP	68, 74*	68	68, 74*			
100-pin PQFP	68	68	68			
144-pin TQFP	104*		104*			
144-pin PQFP	104	104	104			
160-pin PQFP	120	120	120	120	120	120
208-pin PQFP		160	160	160	160	160
240-pin PQFP				184	184	184
256-ball BGA				192	192	192
352-ball BGA						256

Note:

1. The I/O options indicated with a "*" are only available for the "LV" devices.

Table 6. MACH 5A Package and I/O Options¹

Package	M5A3-128 M5A5-128	M5A3-192 M5A5-192	M5A3-256 M5A5-256	M5A3-320	M5A3-384	M5A3-512
100-pin PQFP	68	68	68			
100-pin TQFP	74	74	74			
144-pin TQFP	104	104	104			
160-pin PQFP	120	120	120	120	120	120
208-pin PQFP			160	160	160	160
256-ball BGA				192	192	192
352-ball BGA						256

Note:

1. All information on MACH 5A devices is Advance Information. Please contact a Vantis sales representative for details on availability.

Advanced power management options allow designers to incrementally reduce power while maintaining the level of performance needed for today's complex designs. I/O safety features allow for mixed-voltage design, and both the 3.3-V and the 5-V device versions are in-system programmable through a JTAG-compliant interface.

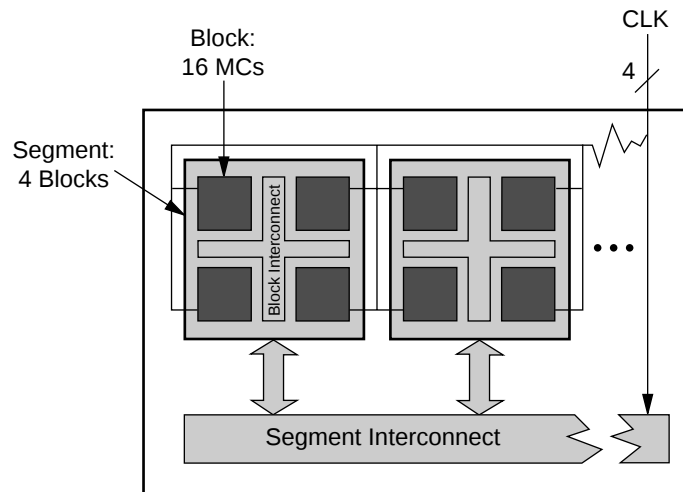
Vantis offers software design support for MACH devices in both the MACHXL[®] and DesignDirect development systems. The DesignDirect development system is the Vantis implementation software that includes support for all Vantis CPLD, FPGA and SPLD devices. This system is supported under Windows '95, '98 and NT as well as Sun Solaris and HP/UX.

DesignDirect software is designed for use with design entry, simulation and verification software from leading-edge tool vendors such as Cadence, Exemplar Logic, Mentor Graphics, Model Technology, Synopsys, Synplicity, Viewlogic and others. It accepts EDIF 2.0.0 input netlists, generates JEDEC files for Vantis PLDs and creates industry standard EDIF, Verilog, VITAL compliant VHDL and SDF simulation netlists for design verification.

DesignDirect software is also available in product configurations that include VHDL and Verilog synthesis from Exemplar Logic and VHDL, Verilog RTL and gate level timing simulation from Model Technology. Schematic capture and ABEL entry, as well as functional simulation, are also provided.

FUNCTIONAL DESCRIPTION

The MACH 5 architecture consists of PAL blocks connected by two levels of interconnect. The **block interconnect** provides routing among 4 PAL blocks. This grouping of PAL blocks joined by the block interconnect is called a **segment**. The second level of interconnect, the **segment interconnect**, ties all of the segments together. The only logic difference between any two MACH 5 devices is the number of segments. Therefore, once a designer is familiar with one device, consistent performance can be expected across the entire family. All devices have four clock pins available which can also be used as logic inputs.



20446G-001

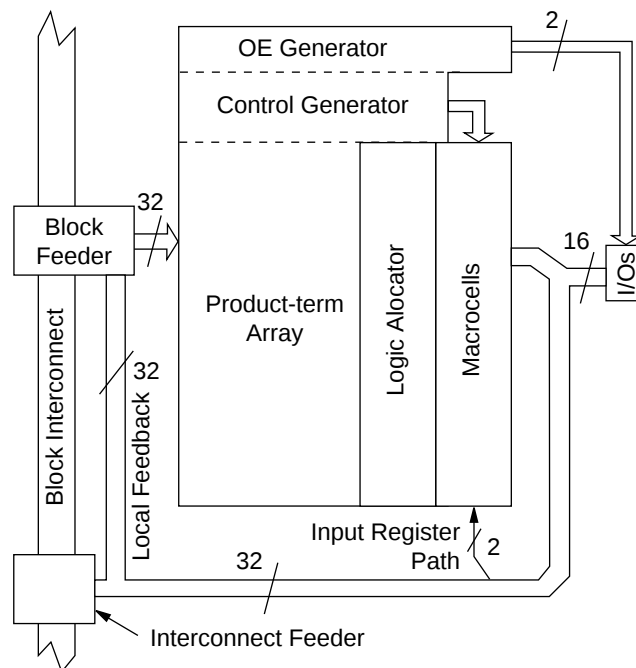
Figure 1. MACH 5 Block Diagram

The MACH 5 PAL blocks consist of the elements listed below (Figure 2). While each PAL block resembles an independent PAL device, it has superior control and logic generation capabilities.

- ◆ I/O cells
- ◆ Product-term array and Logic Allocator
- ◆ Macrocells
- ◆ Register control generator
- ◆ Output enable generator

I/O Cells

The I/Os associated with each PAL block have a path directly back to that PAL block called **local feedback**. If the I/O is used in another PAL block, the **interconnect feeder** assigns a **block interconnect** line to that signal. The interconnect feeder acts as an input switch matrix. The block and segment interconnects provide connections between any two signals in a device. The **block feeder** assigns block interconnect lines and local feedback lines to the PAL block inputs.



20446G-002

Figure 2. PAL Block Structure

PRODUCT-TERM ARRAY AND LOGIC ALLOCATOR

The product-term array uses the same sum-of-products architecture as Vantis' PAL devices and consists of 32 inputs (plus their complements) and 64 product terms arranged in 16 **clusters**. A cluster is a sum-of-products function with either 3 or 4 product terms.

Logic allocators assign the clusters to macrocells. Each macrocell can accept up to eight clusters of three or four product terms, but a given cluster can only be steered to one macrocell (Table 7). If only three product terms in a cluster are steered, the fourth can be used as an input to an XOR gate for separate logic generation and/or polarity control.

The **wide logic allocator** is comprised of all 16 of the individual logic allocators and acts as an output switch matrix by reassigning logic to macrocells to retain pinout as designs change. The logic allocation scheme in the MACH 5 device allows for the implementation of large equations (up to 32 product terms) with only one pass through the logic array.

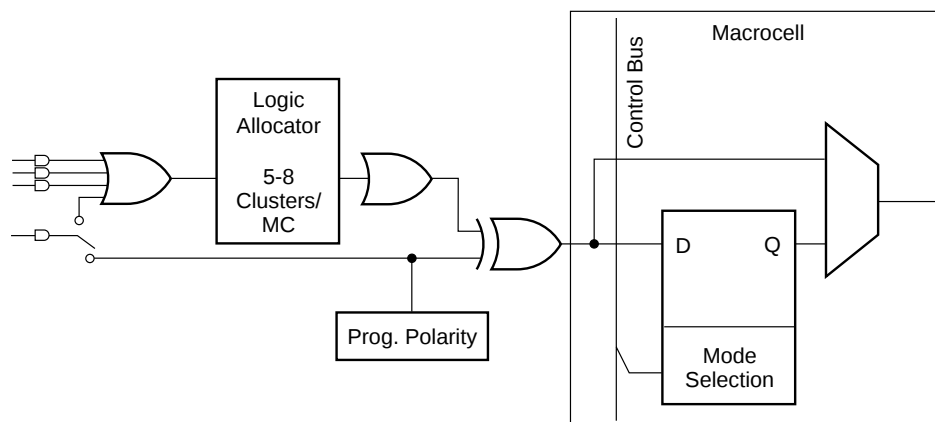
Table 7. Product Term Steering Options for PT Clusters and Macrocells

Macrocell	Available Clusters	Macrocell	Available Clusters
M ₀	C ₀ , C ₁ , C ₂ , C ₃ , C ₄	M ₈	C ₅ , C ₆ , C ₇ , C ₈ , C ₉ , C ₁₀ , C ₁₁ , C ₁₂
M ₁	C ₀ , C ₁ , C ₂ , C ₃ , C ₄ , C ₅	M ₉	C ₆ , C ₇ , C ₈ , C ₉ , C ₁₀ , C ₁₁ , C ₁₂ , C ₁₃
M ₂	C ₀ , C ₁ , C ₂ , C ₃ , C ₄ , C ₅ , C ₆	M ₁₀	C ₇ , C ₈ , C ₉ , C ₁₀ , C ₁₁ , C ₁₂ , C ₁₃ , C ₁₄
M ₃	C ₀ , C ₁ , C ₂ , C ₃ , C ₄ , C ₅ , C ₆ , C ₇	M ₁₁	C ₈ , C ₉ , C ₁₀ , C ₁₁ , C ₁₂ , C ₁₃ , C ₁₄ , C ₁₅
M ₄	C ₀ , C ₁ , C ₂ , C ₃ , C ₄ , C ₅ , C ₆ , C ₇	M ₁₂	C ₈ , C ₉ , C ₁₀ , C ₁₁ , C ₁₂ , C ₁₃ , C ₁₄ , C ₁₅
M ₅	C ₁ , C ₂ , C ₃ , C ₄ , C ₅ , C ₆ , C ₇ , C ₈	M ₁₃	C ₉ , C ₁₀ , C ₁₁ , C ₁₂ , C ₁₃ , C ₁₄ , C ₁₅
M ₆	C ₂ , C ₃ , C ₄ , C ₅ , C ₆ , C ₇ , C ₈ , C ₉	M ₁₄	C ₁₀ , C ₁₁ , C ₁₂ , C ₁₃ , C ₁₄ , C ₁₅
M ₇	C ₃ , C ₄ , C ₅ , C ₆ , C ₇ , C ₈ , C ₉ , C ₁₀	M ₁₅	C ₁₁ , C ₁₂ , C ₁₃ , C ₁₄ , C ₁₅

Macrocells

The macrocells for MACH 5 devices consist of a storage element which can be configured for combinatorial, registered or latched operation (Figure 3). The D-type flip-flops can be configured as T-type, J-K, or S-R operation through the use of the XOR gate associated with each macrocell.

Each PAL block has the capability to provide two input registers by using macrocells 0 and 15. In order to use this option, these macrocells must be accessed via the I/O pins associated with macrocells 3 and 12, respectively. Once the macrocell is used as an input register, it cannot be used for logic, so its clusters can be re-directed through the logic allocator to another macrocell. The I/O pins associated with macrocells 0 and 15 can still be used as input pins. Although the I/O pins for macrocells 3 and 12 are used to connect to the input registers, these macrocells can still be used as “buried” macrocells to drive device logic via the matrix.



20446G-003

Figure 3. Macrocell Diagram

Control Generator

The control generator provides four configurable clock lines and three configurable set/reset lines to each macrocell in a PAL block. Any of the four clock lines and any of the three set/reset lines can be independently selected by any flip-flop within a block. The clock lines can be configured to provide synchronous global (pin) clocks and asynchronous product term clocks, sum term clocks, and latch enables (Figure 4). Three of the four global clocks, as well as two product-term clocks and one sum-term clock, are available per PAL block. Positive or negative edge clocking is available as well as advanced clocking features such as **complementary** and **biphase** clocking. Complementary clocking provides two clock lines exactly 180 degrees out of phase, and is useful in applications such as fast data paths. A biphase clock line clocks flip-flops on both the positive and negative edges of the clock. The configuration options for the four clock lines per PAL block are as follows:

Clock Line 0 Options

- ◆ Global clock (0, 1, 2, or 3) with positive or negative edge clock enable
- ◆ Product-term clock ($A*B*C$)
- ◆ Sum-term clock ($A+B+C$)

Clock Line 1 Options

- ◆ Global clock (0, 1, 2, or 3) with positive edge clock enable

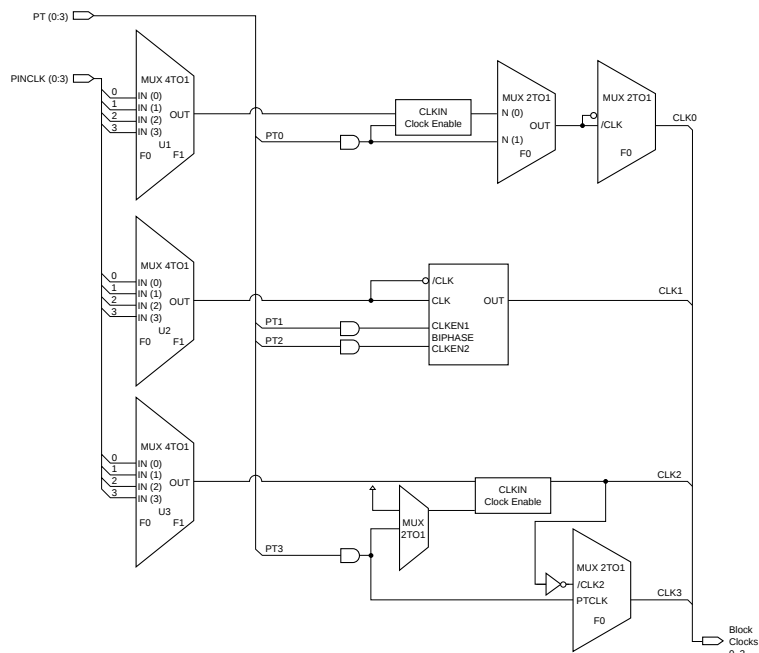
- ◆ Global clock (0, 1, 2, or 3) with negative edge clock enable
- ◆ Global clock (0, 1, 2, or 3) with positive and negative edge clock enable (biphase)

Clock Line 2 Options

- ◆ Global clock (0, 1, 2, or 3) with clock enable

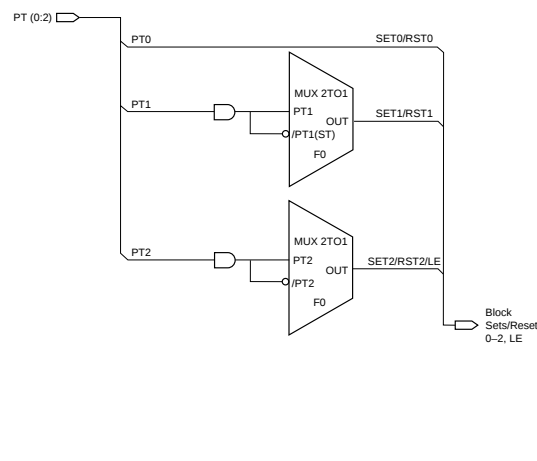
Clock Line 3 Options

- ◆ Complement of clock line 2 (same clock enable)
- ◆ Product-term clock (if clock line 2 does not use clock enable)



20446G-004

Figure 4. Clock Generator



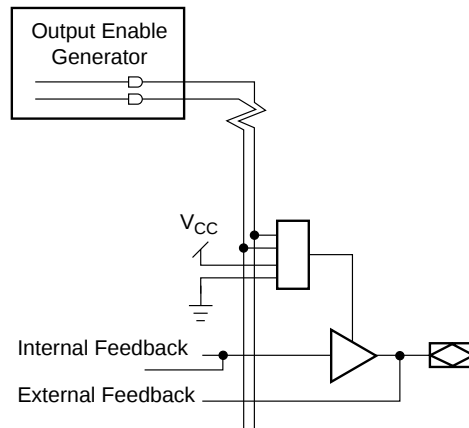
20446G-005

Figure 5. Set/Reset Generator

The set/reset generation portion of the control generator (Figure 5) creates three set/reset lines for the PAL block. Each macrocell can choose one of these three lines or choose no set/reset at all. All three lines can be configured for product term set/reset and two of the three lines can be configured as sum term set/reset and one of the lines can be configured as product-term or sum-term latch enable. While the set/reset signals are generated in the control generator, whether that signal sets or resets a flip-flop is determined within the individual macrocell. The same signal can set one flip-flop and reset another. PT2 or /PT2 can also be used as a latch enable for macrocells configured as latches.

OE Generator

There is one output enable (OE) generator per PAL block that generates two product-term driven output enables. Each I/O cell is simply an output buffer. Each I/O cell within the PAL block can choose to be permanently enabled, permanently disabled, or choose one of the two product term output enables per PAL block (Figure 6).



20446G-006

Figure 6. Output Enable Generator and I/O Cell

MACH 5 TIMING MODEL

The primary focus of the MACH 5 timing model is to accurately represent the timing in a MACH 5 device, and at the same time, be easy to understand. This model accurately describes all combinatorial and registered paths through the device, making a distinction between **internal feedback** and **external feedback**. A signal uses internal feedback when it is fed back into the switch matrix or block without having to go through the output buffer. The input register specifications are also reported as internal feedback. When a signal is fed back into the switch matrix after having gone through the output buffer, it is using external feedback.

The parameter, t_{BUF} , is defined as the time it takes to go through the output buffer to the I/O pad. If a signal goes to the internal feedback rather than to the I/O pad, the parameter designator is followed by an “i”. By adding t_{BUF} to this internal parameter, the external parameter is derived. For example, $t_{PD} = t_{PDi} + t_{BUF}$. A diagram representing the modularized MACH 5 timing model is shown in Figure 7. Refer to the Technical Note entitled *MACH 5 Timing and High Speed Design* for a more detailed discussion about the timing parameters.

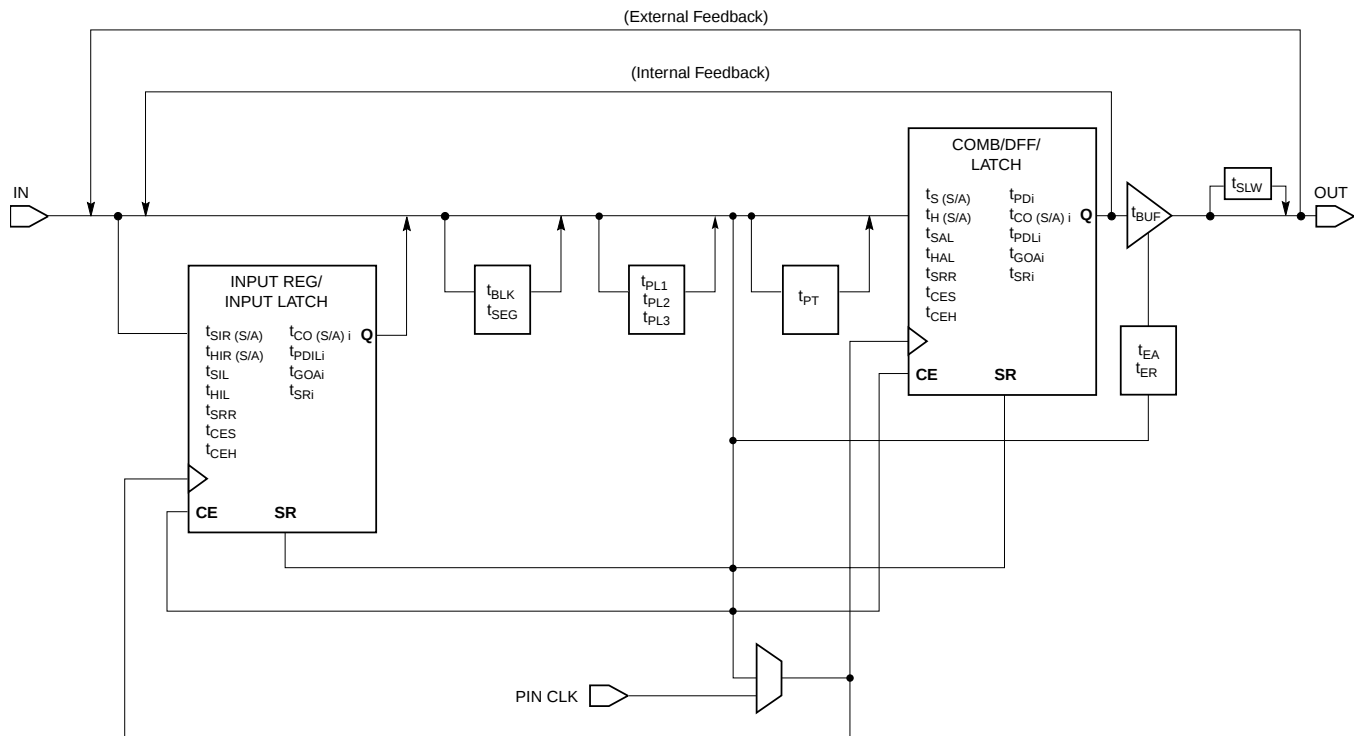


Figure 7. MACH 5 Timing Model

20446G-014

MULTIPLE I/O AND DENSITY OPTIONS

The MACH 5 family offers six macrocell densities in a number of I/O options. This allows designers to choose a device close to their logic density and I/O requirements, thus minimizing costs. For the same package type, every density has the same pin-out. With proper design considerations, a design can be moved to a higher or lower density part as required.

JTAG BOUNDARY SCAN TESTABILITY

All MACH 5 devices have JTAG boundary scan cells and are compliant to the JTAG standard, IEEE 1149.1. This allows functional testing of the circuit board on which the device is mounted through a serial scan path that can access all critical logic nodes. Internal registers are linked internally, allowing test data to be shifted in and loaded directly onto test nodes, or test node data to be captured and shifted out for verification. In addition, these devices can be linked into a board-level serial scan path for more complete board-level testing.

JTAG IN-SYSTEM PROGRAMMING

Programming devices in-system provides a number of significant benefits including: rapid prototyping, lower inventory levels, higher quality, and the ability to make in-field modifications. All MACH 5 devices provide in-system programming (ISP) capability through their JTAG ports. This capability has been implemented in a manner that insures that the JTAG port remains compliant to the IEEE 1149.1 standard. By using JTAG as the communication interface through which ISP is achieved, customers get the benefit of a standard, well-defined interface.

MACH 5 devices can be programmed across the commercial temperature and voltage range. Vantis provides its free PC-based Lattice/VantisPRO software to facilitate in-system programming. Lattice/VantisPRO software takes the JEDEC file output produced by Vantis' design implementation software, along with information about the JTAG chain, and creates a set of vectors that are used to drive the JTAG chain. Lattice/VantisPRO software can use these vectors to drive a JTAG chain via the parallel port of a PC. Alternatively, Lattice/VantisPRO software can output files in formats understood by common automated test equipment. This equipment can then be used to program MACH 5 devices during the testing of a circuit board. For more information about in-system programming, refer to the separate document entitled *MACH ISP Manual*.

PCI COMPLIANT

MACH 5(A) devices in the -5/-6/-7/-10/-12 speed grades are compliant with the *PCI Local Bus Specification* version 2.1, published by the PCI Special Interest Group (SIG). The 5-V devices are fully PCI-compliant. The 3.3-V devices are mostly compliant but do not meet the PCI condition to clamp the inputs as they rise above V_{CC} because of their 5-V input tolerant feature. MACH 5 devices provide the speed, drive, density, output enables and I/Os for the most complex PCI designs.

SAFE FOR MIXED SUPPLY VOLTAGE SYSTEM DESIGNS ¹

Both the 3.3-V and 5-V V_{CC} MACH 5 devices are safe for mixed supply voltage system designs. The 5-V devices will not overdrive 3.3-V devices above the output voltage of 3.3 V, while they accept inputs from other 3.3-V devices. The 3.3-V devices will accept inputs up to 5.5 V. Both the 3.3-V and 5-V versions have the same high-speed performance and provide easy-to-use mixed-voltage design capability.

Note:

1. Except for M5-128, M5-192, and M5-256. Please refer to Application Note titled "Hot Socketing and Mixed Supply Design with MACH 4 and MACH 5 Devices".

PULL-UP OR BUS-FRIENDLY INPUTS AND I/OS

All MACH 5 devices have inputs and I/Os which feature the Bus-Friendly circuitry incorporating two inverters in series which loop back to the input. This double inversion weakly holds the input at its last driven logic state. While it is a good design practice to tie unused pins to a known state, the Bus-Friendly input structure pulls pins away from the input threshold voltage where noise can cause high-frequency switching. At power-up, the Bus-Friendly latches are reset to a logic level "1." For the circuit diagram, please refer to the *Input/Output Equivalent Schematics (page 393)* in the General Information Section of the Vantis 1999 Data Book. All MACH 5A devices have a programmable bit that configures all input and I/Os with either pull-up or Bus-Friendly characteristics. If the device is configured in pull-up mode, all inputs and I/Os are weakly pulled up. For the circuit diagram, please refer to the *Input/Output Equivalent Schematics (page 393)* in the General Information Section of the Vantis 1999 Data Book.

POWER MANAGEMENT

There are 4 power/speed options in each MACH 5 PAL block (Table 8). The speed and power tradeoff can be tailored for each design. The signal speed paths in the lower-power PAL blocks will be slower than those in the higher-power PAL blocks. This feature allows speed critical paths to run at maximum frequency while the rest of the signal paths operate in a lower-power mode. In large designs, there may be several different speed requirements for different portions of the design.

Table 8. Power Levels

High Speed/High Power	100% Power
Medium High Speed/Medium High Power	67% Power
Medium Low Speed/Medium Low Power	40% Power
Low Speed/Low Power	20% Power

PROGRAMMABLE SLEW RATE

Each MACH 5 device I/O has an individually programmable output slew rate control bit. Each output can be individually configured for the higher speed transition (3 V/ns) or for the lower noise transition (1 V/ns). For high-speed designs with long, unterminated traces, the slow-slew rate will introduce fewer reflections, less noise, and keep ground bounce to a minimum. For designs with short traces or well terminated lines, the fast slew rate can be used to achieve the highest speed. The slew rate is adjusted independent of power.

POWER-UP RESET/SET

All flip-flops power up to a known state for predictable system initialization. If a macrocell is configured to SET on a signal from the control generator, then that macrocell will be SET during device power-up. If a macrocell is configured to RESET on a signal from the control generator or is not configured for set/reset, then that macrocell will RESET on power-up. To guarantee initialization values, the V_{CC} rise must be monotonic and the clock must be inactive until the reset delay time has elapsed.

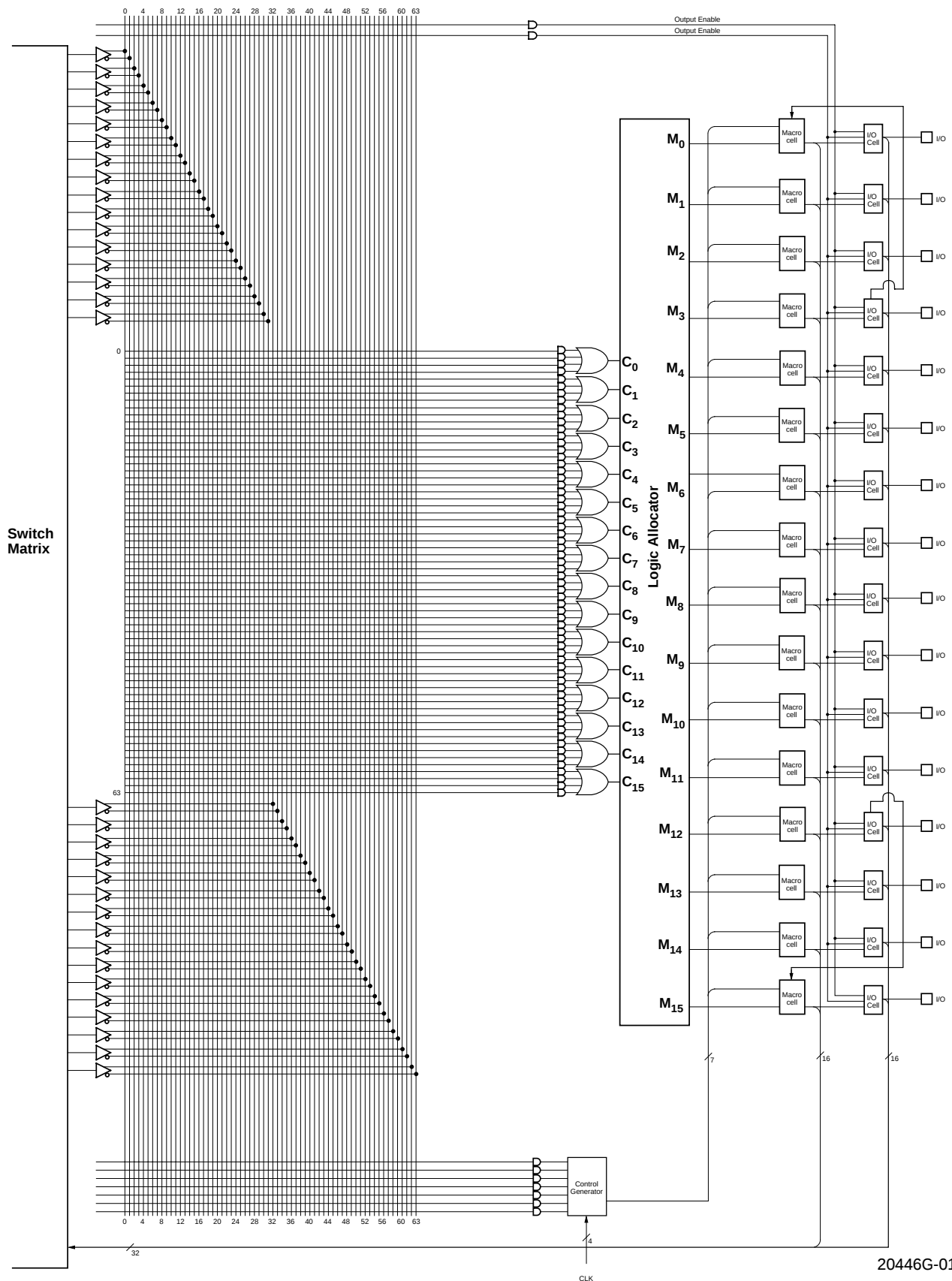
SECURITY BIT

A programmable security bit is provided on the MACH 5 devices as a deterrent to unauthorized copying of the array configuration patterns. Once programmed, this bit defeats readback of the programmed pattern by a device programmer, securing proprietary designs from competitors. Programming and verification are also defeated by the security bit. The bit can only be reset by erasing the entire device.

HOT SOCKETING

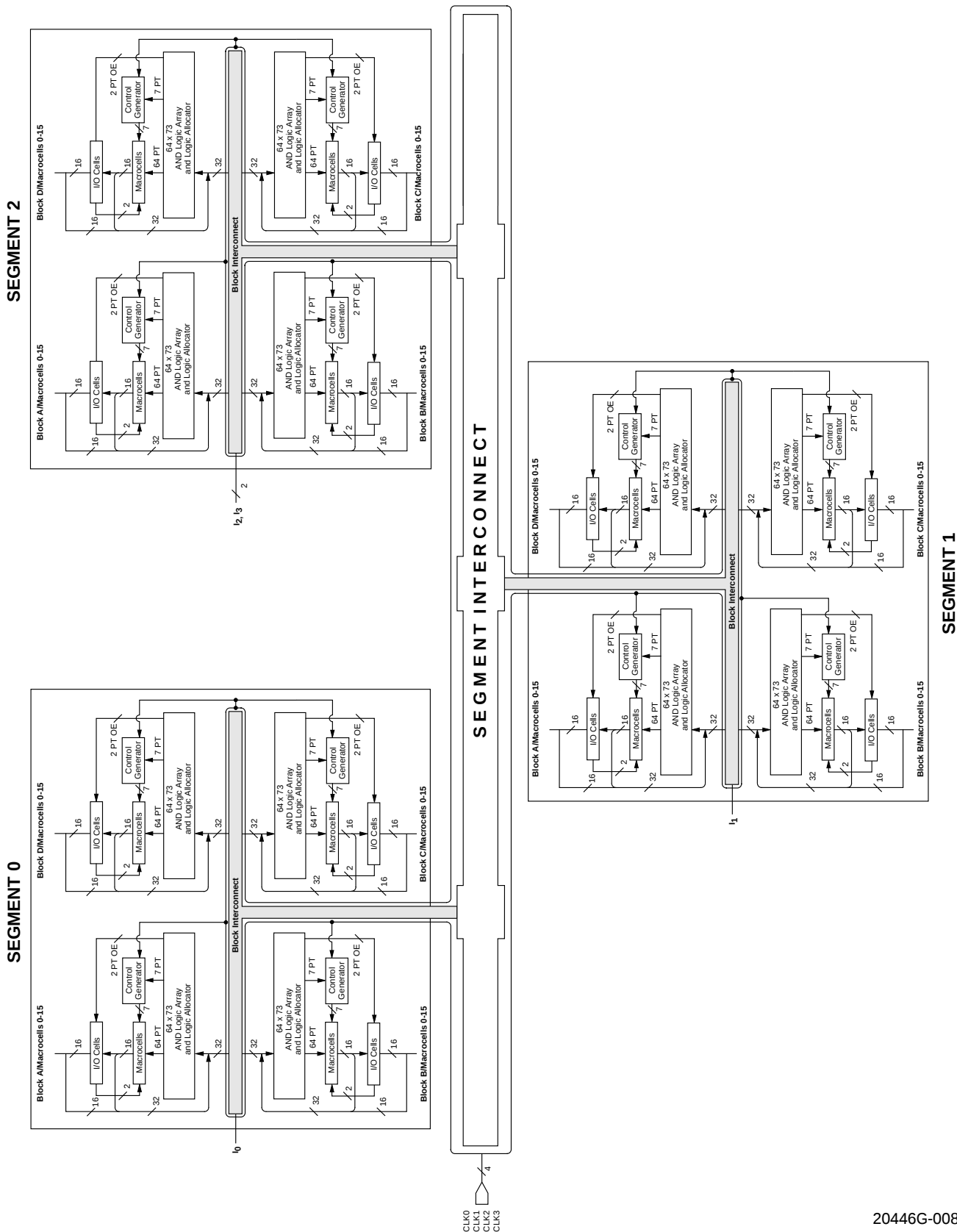
MACH 5A devices are well-suited for those applications that require hot socket capability. Hot socketing a device requires that the device, when powered-down, can tolerate active signals on the I/Os and inputs without being damaged. Additionally, it requires that the effects of the powered-down MACH device be minimal on active signals.

MACH 5 PAL BLOCK



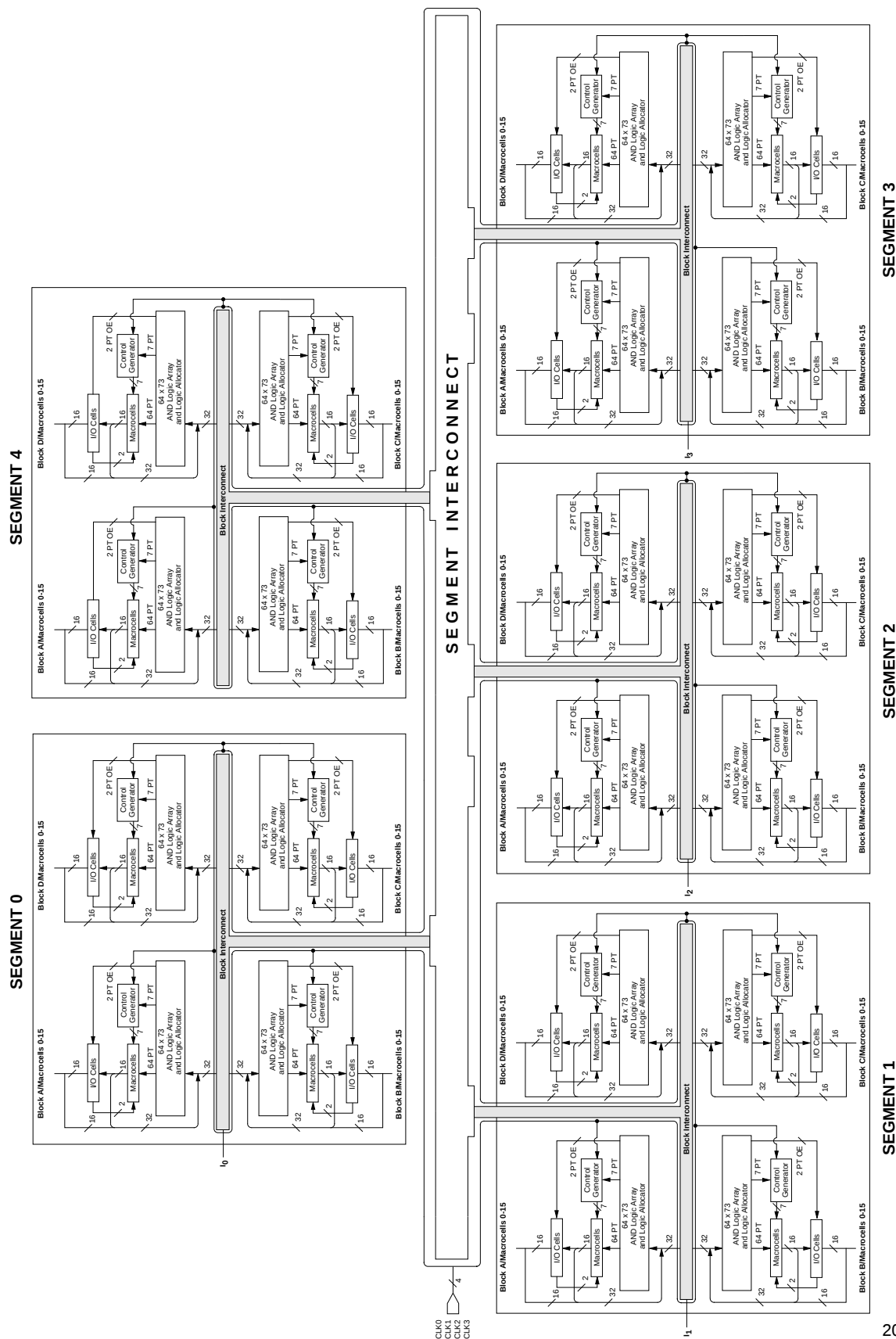
20446G-015

BLOCK DIAGRAM — M5-192/XXX, M5A(3,5)-192/XXX



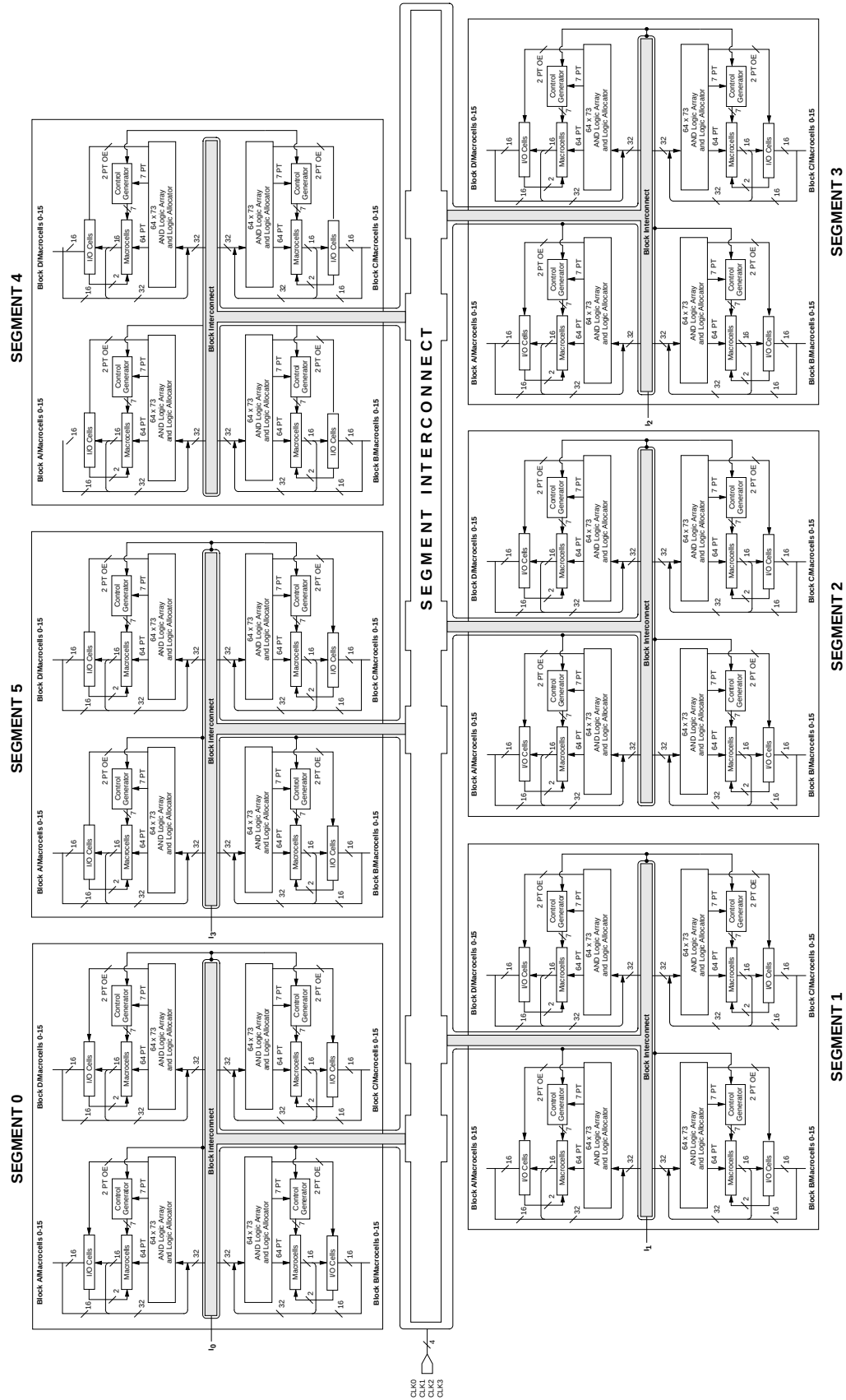
20446G-008

BLOCK DIAGRAM — M5(LV)-320/XXX, M5A3-320/XXX

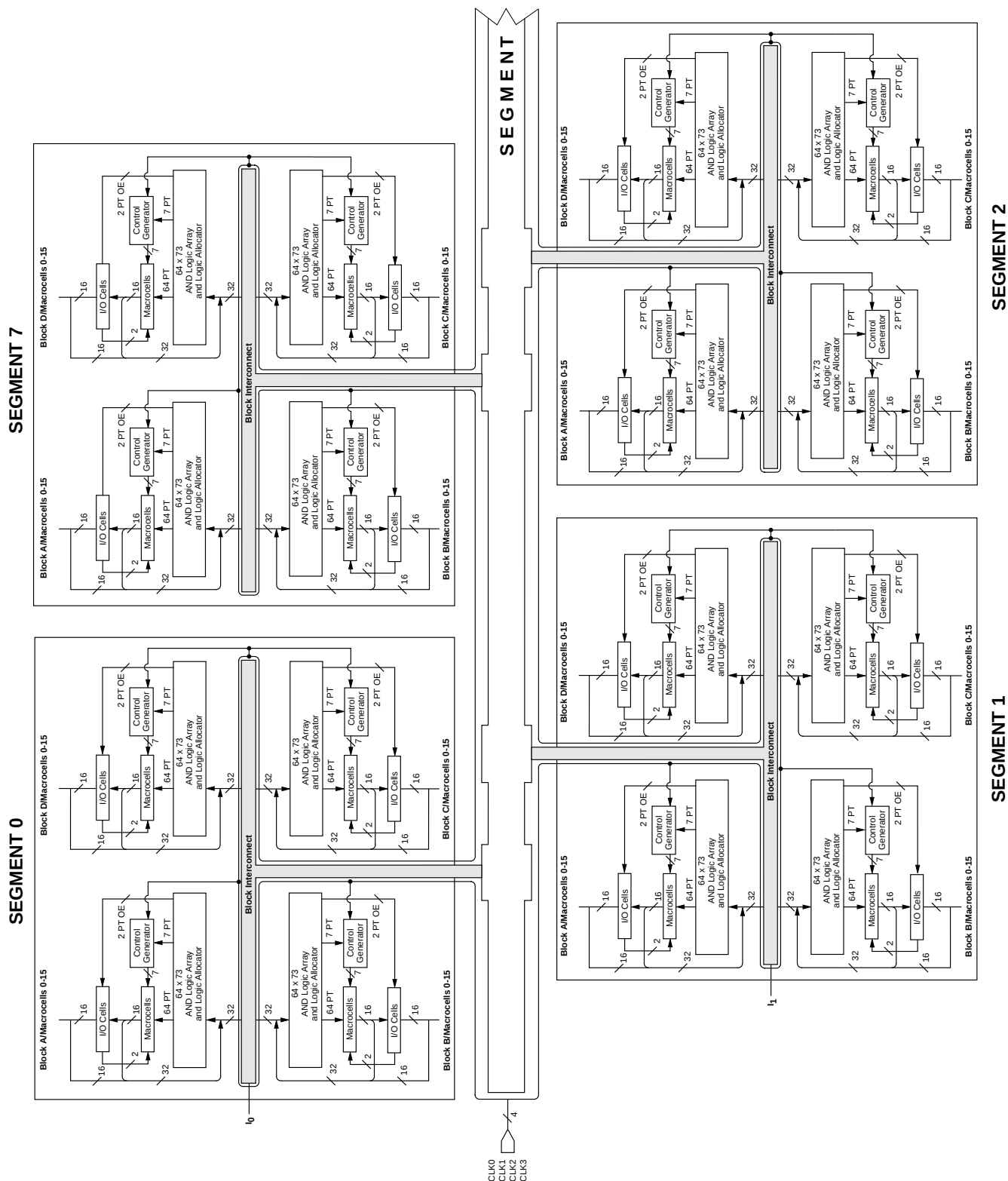


20446G-010

BLOCK DIAGRAM — M5(LV)-384/XXX, M5A3-384/XXX

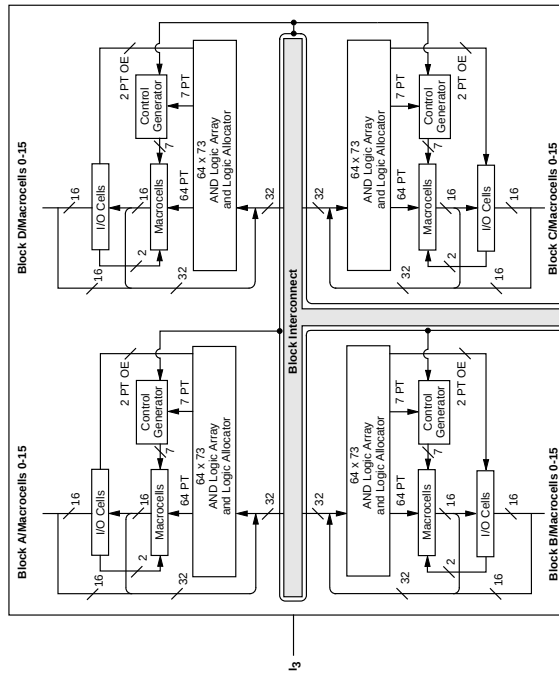


20446G-011

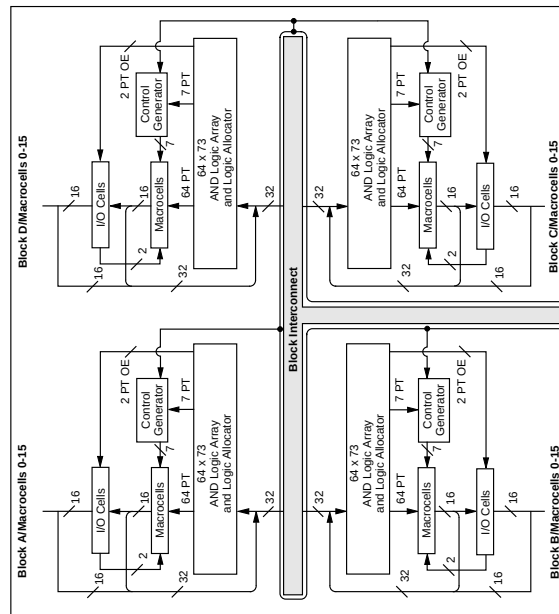


BLOCK DIAGRAM — M5(LV)-512/XXX, M5A3-512/XXX

SEGMENT 5

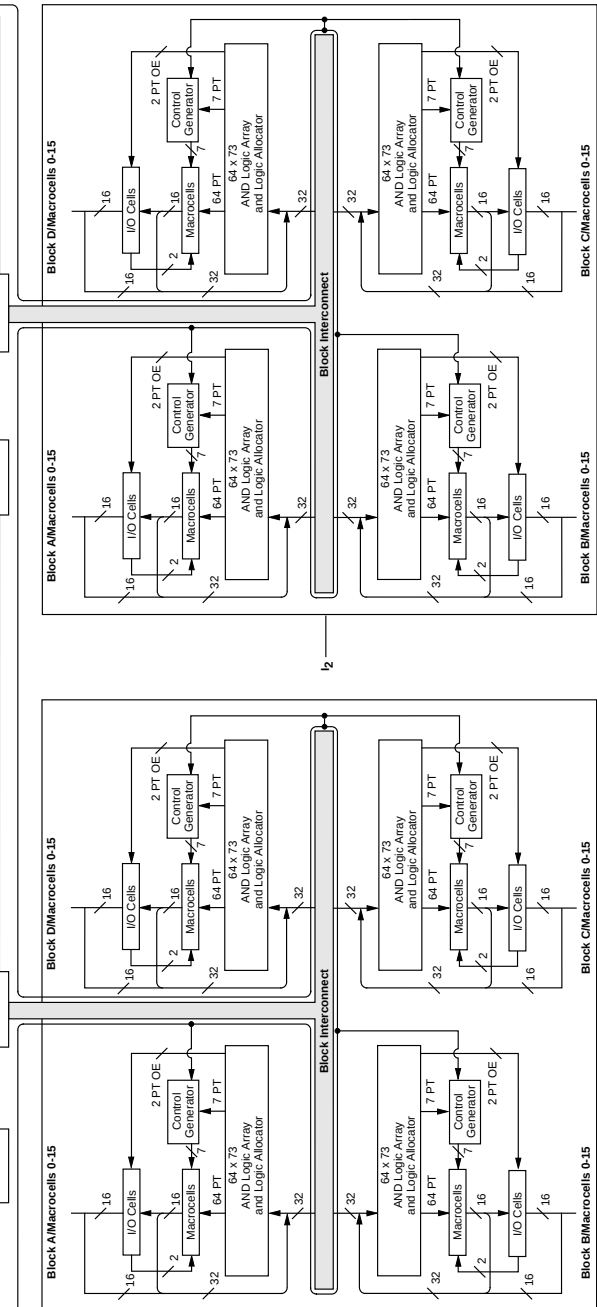


SEGMENT 6



Continued

INTERCONNECT



SEGMENT 4

SEGMENT 3

20446G-013

ABSOLUTE MAXIMUM RATINGS

M5 and M5A5

Storage Temperature -65°C to +150°C
 Device Junction
 Temperature (Note 1) +130°C or +150°C
 Supply Voltage
 with Respect to Ground -0.5 V to +7.0 V
 DC Input Voltage -0.5 V to 5.5 V
 Static Discharge Voltage 2000 V
 Latchup Current (-40°C to +85°C) 200 mA

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices

Ambient Temperature (T_A)
 Operating in Free Air 0°C to +70°C
 Supply Voltage (V_{CC})
 with Respect to Ground +4.75 V to +5.25 V

Industrial (I) Devices

Ambient Temperature (T_A)
 Operating in Free Air -40°C to +85°C
 Supply Voltage (V_{CC})
 with Respect to Ground +4.5 V to +5.5 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

5-V DC CHARACTERISTICS OVER OPERATING RANGES

Parameter Symbol	Parameter Description	Test Description	Min	Typ	Max	Unit
V_{OH}	Output HIGH Voltage (For M5-320, M5-384, M5-512, M5A5-128, M5A5-192, M5A5-256 Devices)	$I_{OH} = -3.2 \text{ mA}$, $V_{CC} = \text{Min}$, $V_{IN} = V_{IH} \text{ or } V_{IL}$	2.4			V
		$I_{OH} = 0 \text{ mA}$, $V_{CC} = \text{Max}$, $V_{IN} = V_{IH} \text{ or } V_{IL}$			3.3	V
	Output HIGH Voltage (For M5-128, M5-192, M5-256 Devices)	$I_{OH} = -3.2 \text{ mA}$, $V_{CC} = \text{Min}$, $V_{IN} = V_{IH} \text{ or } V_{IL}$	2.4			V
		$I_{OH} = -2.5 \text{ mA}$, $V_{CC} = 5.25 \text{ V}$, $V_{IN} = V_{IH} \text{ or } V_{IL}$			3.6	V
V_{OL}	Output LOW Voltage (Note 2)	$I_{OL} = +16 \text{ mA}$, $V_{CC} = \text{Min}$, $V_{IN} = V_{IH} \text{ or } V_{IL}$			0.5	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 3)	2.0			V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 3)			0.8	V
I_{IH}	Input HIGH Leakage Current	$V_{IN} = 5.25$, $V_{CC} = \text{Max}$ (Note 4)			10	μA
I_{IL}	Input LOW Leakage Current	$V_{IN} = 0$, $V_{CC} = \text{Max}$ (Note 4)			-10	μA
I_{OZH}	Off-State Output Leakage Current HIGH	$V_{OUT} = 5.25$, $V_{CC} = \text{Max}$, $V_{IN} = V_{IH} \text{ or } V_{IL}$ (Note 4)			10	μA
I_{OZL}	Off-State Output Leakage Current LOW	$V_{OUT} = 0$, $V_{CC} = \text{Max}$, $V_{IN} = V_{IH} \text{ or } V_{IL}$ (Note 4)			-10	μA
I_{SC}	Output Short-Circuit Current	$V_{OUT} = 0.5 V_{CC} = \text{Max}$, $V_{IN} = V_{IH} \text{ or } V_{IL}$ (Note 5)	-30		-180	mA

Note:

- 150° for M5-128, M5-192 and M5-256 devices. 130° for M5-320, M5-384, M5-512 and all M5A5-xxx devices.
- Total I_{OL} between ground pins should not exceed 64 mA.
- These are absolute values with respect to device ground, and all overshoots due to system and/or tester noise are included.
- I/O pin leakage is the worst case of I_{IL} and I_{OZL} or I_{IH} and I_{OZH} .
- Not more than one output should be shorted at a time. Duration of the short-circuit should not exceed one second.

ABSOLUTE MAXIMUM RATINGS

M5LV and M5A3

Storage Temperature -65°C to +150°C
 Device Junction Temperature +130°C
 Supply Voltage
 with Respect to Ground -0.5 V to +4.5 V
 DC Input Voltage -0.5 V to 5.5 V
 Static Discharge Voltage 2000 V
 Latchup Current (-40°C to +85°C) 200 mA

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices

Ambient Temperature (T_A)
 Operating in Free Air 0°C to +70°C
 Supply Voltage (V_{CC})
 with Respect to Ground +3.0 V to +3.6 V

Industrial (I) Devices

Ambient Temperature (T_A)
 Operating in Free Air -40°C to +85°C
 Supply Voltage (V_{CC})
 with Respect to Ground +3.0 V to +3.6 V
Operating ranges define those limits between which the functionality of the device is guaranteed.

3.3-V DC CHARACTERISTICS OVER OPERATING RANGES

Parameter Symbol	Parameter Description	Test Description		Min	Max	Unit
V_{OH}	Output HIGH Voltage	$V_{CC} = \text{Min}$	$I_{OH} = -100 \mu A$	$V_{CC} - 0.2$		V
		$V_{IN} = V_{IH} \text{ or } V_{IL}$	$I_{OH} = 3.2 \text{ mA}$	2.4		V
V_{OL}	Output LOW Voltage	$V_{CC} = \text{Min}$	$I_{OL} = 100 \mu A$		0.2	V
		$V_{IN} = V_{IH} \text{ or } V_{IL}$	$I_{OH} = 16 \text{ mA (Note 1)}$		0.5	V
V_{IH}	Input HIGH Voltage	$V_{OUT} \geq V_{OH} \text{ Min or } V_{OUT} \leq V_{OL} \text{ Max (Note 2)}$		2.0	5.5	V
V_{IL}	Input LOW Voltage	$V_{OUT} \geq V_{OH} \text{ Min or } V_{OUT} \leq V_{OL} \text{ Max (Note 2)}$		-0.3	0.8	V
I_{IH}	Input HIGH Leakage Current	$V_{IN} = 3.6, V_{CC} = \text{Max (Note 3)}$			10	μA
I_{IL}	Input LOW Leakage Current	$V_{IN} = 0, V_{CC} = \text{Max (Note 3)}$			-10	μA
I_{OZH}	Off-State Output Leakage Current HIGH	$V_{OUT} = 3.6, V_{CC} = \text{Max}, V_{IN} = V_{IH} \text{ or } V_{IL} \text{ (Note 3)}$			10	μA
I_{OZL}	Off-State Output Leakage Current LOW	$V_{OUT} = 0, V_{CC} = \text{Max}, V_{IN} = V_{IH} \text{ or } V_{IL} \text{ (Note 3)}$			-10	μA
I_{SC}	Output Short-Circuit Current	$V_{OUT} = 0.5 V_{CC} = \text{Max}, V_{IN} = V_{IH} \text{ or } V_{IL} \text{ (Note 4)}$		-15	-160	mA

Notes:

1. Total I_{OL} between ground pins should not exceed 64 mA.
2. These are absolute values with respect to device ground, and all overshoots due to system and/or tester noise are included.
3. I/O pin leakage is the worst case of I_{IL} and I_{OZL} or I_{IH} and I_{OZH} .
4. Not more than one output should be shorted at one time. Duration of the short-circuit should not exceed one second.

M5(LV) TIMING PARAMETERS OVER OPERATING RANGES¹

		-5		-7		-10		-12		-15		-20		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Combinatorial Delay:														
t _{PDi}	Internal combinatorial propagation delay		3.5		5.5		8.0		10.0		13.0		18.0	ns
t _{PD}	Combinatorial propagation delay		5.5		7.5		10.0		12.0		15.0		20.0	ns
Registered Delays:														
t _{SS}	Synchronous clock setup time	3.0		4.0		5.0		6.0		8.0		10.0		ns
t _{SA}	Asynchronous clock setup time	3.0		4.0		5.0		6.0		7.0		8.0		ns
t _{HS}	Synchronous clock hold time	0.0		0.0		0.0		0.0		0.0		0.0		ns
t _{HA}	Asynchronous clock hold time	3.0		4.0		5.0		6.0		7.0		8.0		ns
t _{COSi}	Synchronous clock to internal output		2.5		4.0		5.0		6.0		8.0		10.0	ns
t _{COS}	Synchronous clock to output		4.5		6.0		7.0		8.0		10.0		12.0	ns
t _{COAi}	Asynchronous clock to internal output		6.0		8.0		10.0		13.0		15.0		18.0	ns
t _{COA}	Asynchronous clock to output		8.0		10.0		12.0		15.0		17.0		20.0	ns
Latched Delays:														
t _{SAL}	Latch setup time	3.0		4.0		5.0		6.0		7.0		8.0		ns
t _{HAL}	Latch hold time	3.0		4.0		5.0		6.0		7.0		8.0		ns
t _{PDLi}	Transparent latch internal		6.0		7.0		8.0		9.0		10.0		10.0	ns
t _{PDL}	Propagation delay through transparent latch		8.0		9.0		10.0		11.0		12.0		12.0	ns
t _{GOAi}	Gate to internal output		7.0		8.0		9.0		10.0		11.0		12.0	ns
t _{GOA}	Gate to output		9.0		10.0		11.0		12.0		13.0		14.0	ns
Input Register Delays:														
t _{SIRS}	Input register setup time using a synchronous clock	2.0		2.0		3.0		3.0		3.0		3.0		ns
t _{SIRA}	Input register setup time using an asynchronous clock	0.0		0.0		0.0		0.0		0.0		0.0		ns
t _{HIRS}	Input register hold time using a synchronous clock	3.0		3.0		4.0		4.0		4.0		4.0		ns
t _{HIRA}	Input register hold time using an asynchronous clock	6.0		6.0		7.0		7.0		7.0		7.0		ns
Input Latch Delays:														
t _{SIL}	Input latch setup time	2.0		2.0		3.0		3.0		3.0		3.0		ns
t _{HIL}	Input latch hold time	6.0		6.0		7.0		7.0		7.0		7.0		ns
t _{PDILi}	Transparent input latch		5.0		5.0		6.0		6.0		6.0		6.0	ns
Output Delays:														
t _{BUF}	Output buffer delay		2.0		2.0		2.0		2.0		2.0		2.0	ns
t _{SLW}	Slow slew rate delay		2.5		2.5		2.5		2.5		2.5		2.5	ns
t _{EA}	Output enable time		7.5		9.5		10.0		12.0		15.0		20.0	ns
t _{ER}	Output disable time		7.5		9.5		10.0		12.0		15.0		20.0	ns

M5(LV) TIMING PARAMETERS OVER OPERATING RANGES¹ (CONTINUED)

		-5		-7		-10		-12		-15		-20		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Power Delays:														
t _{PL1}	Power level 1 delay (Note 2)		4.0 (5.0)		4.0 (5.0)		4.0 (5.0)		4.0 (5.0)		4.0 (5.0)		4.0 (5.0)	ns
t _{PL2}	Power level 2 delay (Note 2)		6.0 (9.0)		6.0 (9.0)		6.0 (9.0)		6.0 (9.0)		6.0 (9.0)		6.0 (9.0)	ns
t _{PL3}	Power level 3 delay (Note 2)		9.0 (17.5)		9.0 (17.5)		9.0 (17.5)		9.0 (17.5)		9.0 (17.5)		9.0 (17.5)	ns
Additional Cluster Delay:														
t _{PT}	Product term cluster delay		0.3		0.3		0.3		0.3		0.3		0.3	ns
Interconnect Delays:														
t _{BLK}	Block interconnect delay		1.5		1.5		2.0		2.0		2.0		2.0	ns
t _{SEG}	Segment interconnect delay		4.5		5.0		6.0		6.0		6.0		6.0	ns
Reset and Preset Delays:														
t _{SRi}	Asynchronous reset or preset to internal register output		6.0		8.0		10.0		12.0		14.0		16.0	ns
t _{SR}	Asynchronous reset or preset to register output		8.0		10.0		12.0		14.0		16.0		18.0	ns
t _{SRR}	Reset and set register recovery time	5.5		7.5		8.0		9.0		10.0		11.0		ns
t _{SRW}	Asynchronous reset or preset width	3.0		4.0		5.0		6.0		7.0		8.0		ns
Clock Enable Delays:														
t _{CES}	Clock enable setup time	4.0		5.0		6.0		7.0		7.0		8.0		ns
t _{CEH}	Clock enable hold time	3.0		4.0		5.0		6.0		6.0		7.0		ns
Width:														
t _{WLS}	Global clock width low (Note 3)	2.5		3.0		4.0		5.0		6.0		6.0		ns
t _{WHS}	Global clock width high (Note 3)	2.5		3.0		4.0		5.0		6.0		6.0		ns
t _{WLA}	Product term clock width low	3.0		4.0		5.0		6.0		7.0		8.0		ns
t _{WHA}	Product term clock width high	3.0		4.0		5.0		6.0		7.0		8.0		ns
t _{GWA}	Gate width low (for low transparent) or high (for high transparent)	3.0		4.0		5.0		6.0		7.0		8.0		ns
t _{WIR}	Input register clock width low or high	3.0		4.0		5.0		6.0		7.0		8.0		ns

M5(LV) TIMING PARAMETERS OVER OPERATING RANGES¹ (CONTINUED)

		-5		-7		-10		-12		-15		-20		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Frequency:														
f _{MAX}	External feedback, PAL block level. Min of 1/(t _{WLS} + t _{WHS}) or 1/(t _{SS} + t _{COS})	133		100		83.3		71.4		55.6		45.5		MHz
	Internal feedback, PAL block level. Min of 1/(t _{WLS} + t _{WHS}) or 1/(t _{SS} +t _{COSi})	182		125		100		83.3		62.5		50.0		MHz
	No feedback PAL block level. Min of 1/(t _{WLS} + t _{WHS}) or 1/(t _{SS} + t _{HS})	200		167		125		100		83.3		83.3		MHz
f _{MAXA}	External feedback, PAL block level. Min of 1/(t _{WLA} + t _{WHA}) or 1/(t _{SA} + t _{COA})	91		71.4		58.8		47.6		41.7		35.7		MHz
	Internal feedback, PAL block level. Min of 1/(t _{WLA} + t _{WHA}) or 1/(t _{SA} +t _{COAi})	111		83.3		66.7		52.6		45.5		38.5		MHz
	No feedback, PAL block level. Min of 1/(t _{WLA} + t _{WHA}) or 1/(t _{SA} + t _{HA})	167		125		100		83.3		71.4		62.5		MHz
f _{MAXI}	Maximum input register frequency 1/(t _{SIRS} +t _{HIRS}) or 1/(2 x t _{WICW})	167		125		100		83.3		71.4		62.5		MHz

Notes:

1. See "Switching Test Circuits" in the General Information Section of the Vantis 1999 Data Book.
2. Numbers in parentheses are for M5-128, M5-192, and M5-256.
3. If a signal is used as both a clock and a logic array input, then the maximum input frequency applies ($f_{MAX}/2$).

M5A(3,5) TIMING PARAMETERS OVER OPERATING RANGES ¹

		-5		-6		-7		-10		-12		-15		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Combinatorial Delay:														
t _{PDi}	Internal combinatorial propagation delay		3.5		4.5		5.5		8.0		10.0		13.0	ns
t _{PD}	Combinatorial propagation delay		5.5		6.5		7.5		10.0		12.0		15.0	ns
Registered Delays:														
t _{SS}	Synchronous clock setup time	3.0		3.0		4.0		5.0		6.0		8.0		ns
t _{SA}	Asynchronous clock setup time	2.0		2.0		4.0		5.0		6.0		7.0		ns
t _{HS}	Synchronous clock hold time	0.0		0.0		0.0		0.0		0.0		0.0		ns
t _{HA}	Asynchronous clock hold time	2.0		2.0		4.0		5.0		6.0		7.0		ns
t _{COSi}	Synchronous clock to internal output		2.5		3.0		4.0		5.0		6.0		8.0	ns
t _{COS}	Synchronous clock to output		4.5		5.0		6.0		7.0		8.0		10.0	ns
t _{COAi}	Asynchronous clock to internal output		5.0		5.0		8.0		10.0		13.0		15.0	ns
t _{COA}	Asynchronous clock to output		7.0		7.0		10.0		12.0		15.0		17.0	ns
Latched Delays:														
t _{SAL}	Latch setup time	3.0		4.0		4.0		5.0		6.0		7.0		ns
t _{HAL}	Latch hold time	3.0		3.0		4.0		5.0		6.0		7.0		ns
t _{PDLi}	Transparent latch internal		6.0		7.0		7.0		8.0		9.0		10.0	ns
t _{PDL}	Propagation delay through transparent latch		8.0		9.0		9.0		10.0		11.0		12.0	ns
t _{GOAi}	Gate to internal output		7.0		8.0		8.0		9.0		10.0		11.0	ns
t _{GOA}	Gate to output		9.0		10.0		10.0		11.0		12.0		13.0	ns
Input Register Delays:														
t _{SIRS}	Input register setup time using a synchronous clock	2.0		2.0		2.0		3.0		3.0		3.0		ns
t _{SIRA}	Input register setup time using an asynchronous clock	0.0		0.0		0.0		0.0		0.0		0.0		ns
t _{HIRS}	Input register hold time using a synchronous clock	3.0		3.0		3.0		4.0		4.0		4.0		ns
t _{HIRA}	Input register hold time using an asynchronous clock	6.0		6.0		6.0		7.0		7.0		7.0		ns
Input Latch Delays:														
t _{SIL}	Input latch setup time	2.0		2.0		2.0		3.0		3.0		3.0		ns
t _{HIL}	Input latch hold time	6.0		6.0		6.0		7.0		7.0		7.0		ns
t _{PDILi}	Transparent input latch		5.0		5.0		5.0		6.0		6.0		6.0	ns
Output Delays:														
t _{BUF}	Output buffer delay		2.0		2.0		2.0		2.0		2.0		2.0	ns
t _{SLW}	Slow slew rate delay		2.5		2.5		2.5		2.5		2.5		2.5	ns
t _{EA}	Output enable time		7.5		9.5		9.5		10.0		12.0		15.0	ns
t _{ER}	Output disable time		7.5		9.5		9.5		10.0		12.0		15.0	ns
Power Delays:														
t _{PL1}	Power level 1 delay		4.0		4.0		4.0		4.0		4.0		4.0	ns
t _{PL2}	Power level 2 delay		6.0		6.0		6.0		6.0		6.0		6.0	ns
t _{PL3}	Power level 3 delay		9.0		9.0		9.0		9.0		9.0		9.0	ns
Additional Cluster Delay:														
t _{PT}	Product term cluster delay		0.3		0.3		0.3		0.3		0.3		0.3	ns

M5A(3,5) TIMING PARAMETERS OVER OPERATING RANGES ¹ (CONTINUED)

		-5		-6		-7		-10		-12		-15		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Interconnect Delays:														
t _{BLK}	Block interconnect delay 320, 384 and 512 Macrocells		1.0		1.0		1.5		1.5		1.5		1.5	ns
t _{SEG}	Segment interconnect delay 320, 384, and 512 Macrocells		2.0		2.0		2.5		4.0		4.0		4.0	ns
t _{BLK}	Block interconnect delay 128, 192 and 256 Macrocells		1.5		1.5		1.5		1.5		1.5		1.5	ns
t _{SEG}	Segment interconnect delay 128, 192 and 256 Macrocells		2.5		2.5		2.5		4.0		4.0		4.0	ns
Reset and Preset Delays:														
t _{SRI}	Asynchronous reset or preset to internal register output		6.0		8.0		8.0		10.0		12.0		14.0	ns
t _{SR}	Asynchronous reset or preset to register output		8.0		10.0		10.0		12.0		14.0		16.0	ns
t _{SRR}	Reset and set register recovery time	5.5		7.5		7.5		8.0		9.0		10.0		ns
t _{SRW}	Asynchronous reset or preset width	3.0		4.0		4.0		5.0		6.0		7.0		ns
Clock Enable Delays:														
t _{CES}	Clock enable setup time	4.0		5.0		5.0		6.0		7.0		7.0		ns
t _{CEH}	Clock enable hold time	3.0		4.0		4.0		5.0		6.0		6.0		ns
Width:														
t _{WLS}	Global clock width low (Note 2)	2.5		3.0		3.0		4.0		5.0		6.0		ns
t _{WHS}	Global clock width high (Note 2)	2.5		3.0		3.0		4.0		5.0		6.0		ns
t _{WLA}	Product term clock width low	3.0		4.0		4.0		5.0		6.0		7.0		ns
t _{WHA}	Product term clock width high	3.0		4.0		4.0		5.0		6.0		7.0		ns
t _{GWA}	Gate width low (for low transparent) or high (for high transparent)	3.0		4.0		4.0		5.0		6.0		7.0		ns
t _{WIR}	Input register clock width low or high	3.0		4.0		4.0		5.0		6.0		7.0		ns
Frequency:														
f _{MAX}	External feedback, PAL block level Min of 1/(t _{WLS} + t _{WHS}) or 1/(t _{SS} + t _{COs})	133		125		100		83.3		71.4		55.6		MHz
	Internal feedback, PAL block level Min of 1/(t _{WLS} + t _{WHS}) or 1/(t _{SS} +t _{COs} i)	182		167		125		100		83.3		62.5		MHz
	No feedback, PAL block level Min of 1/(t _{WLS} + t _{WHS}) or 1/(t _{SS} + t _{HS})	200		167		167		125		100		83.3		MHz
f _{MAXA}	External feedback, PAL block level Min of 1/(t _{WLA} + t _{WHA}) or 1/(t _{SA} + t _{COA})	111		111		71.4		58.8		47.6		41.7		MHz
	Internal feedback, PAL block level Min of 1/(t _{WLA} + t _{WHA}) or 1/(t _{SA} +t _{COA} i)	143		125		83.3		66.6		52.6		45.5		MHz
	No feedback, PAL block level Min of 1/(t _{WLA} + t _{WHA}) or 1/(t _{SA} + t _{HA})	167		125		125		100		83.3		71.4		MHz
f _{MAXI}	Maximum input register frequency 1/(t _{SIRS} +t _{HIRS}) or 1/(2 x t _{WICW})	167		125		125		100		83.3		71.4		MHz

Notes:

- See "Switching Test Circuit" in the General Information Section of the Vantis 1999 Data Book.
- If a signal is used as both a clock and a logic array input, then the maximum input frequency applies (f_{MAX}/2)

CAPACITANCE¹

Parameter Symbol	Parameter Description	Test conditions		Typ	Unit
C_{IN}	I/CLK pin	$V_{IN} = 2.0 \text{ V}$	3.3 V or 5 V, 25 °C, 1 MHz	12	pF
$C_{I/O}$	I/O pin	$V_{OUT} = 2.0 \text{ V}$	3.3 V or 5 V, 25 °C, 1 MHz	10	pF

Note:

1. These parameters are not 100% tested, but are calculated at initial characterization and at any time the design is modified where these parameters may be affected.

I_{CC} vs. FREQUENCY

These curves represent the typical power consumption for a particular device at system frequency. The selected “typical” pattern is a 16-bit up-down counter. This pattern fills the device and exercises every macrocell. Maximum frequency shown uses internal feedback and a D-type register. Power/Speed are optimized to obtain the highest counter frequency and the lowest power. The highest frequency (LSBs) is placed in common PAL blocks, which are set to high power. The lowest frequency signals (MSBs) are placed in a common PAL block and set to lowest power. For a more detailed discussion about MACH 5 power consumption, refer to the application note entitled *MACH 5 Power* in the Application Notes section of the Vantis 1999 Data Book.

I_{CC} CURVES AT HIGH /LOW POWER MODES

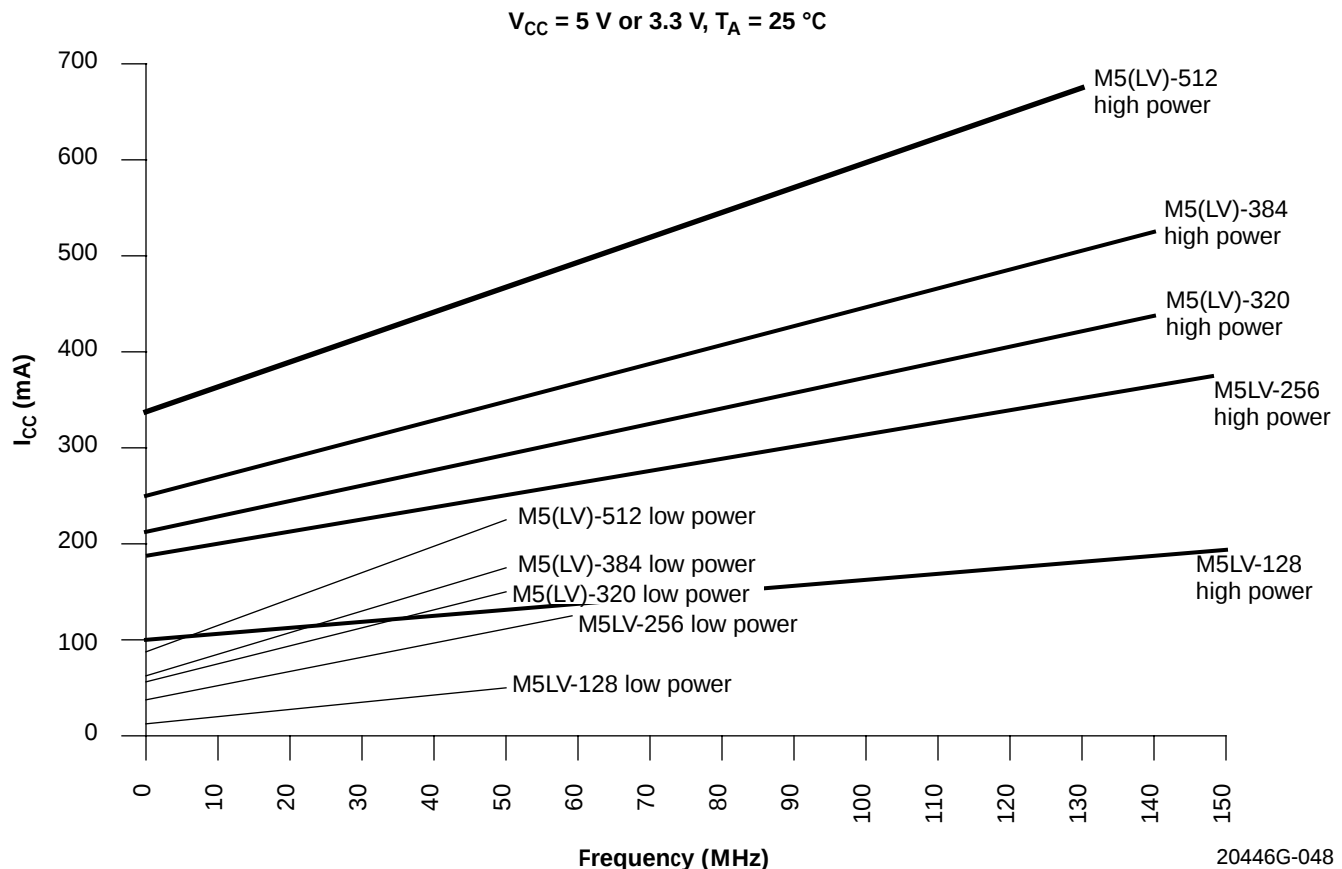


Figure 8. I_{CC} Curves at High/Low Power Modes

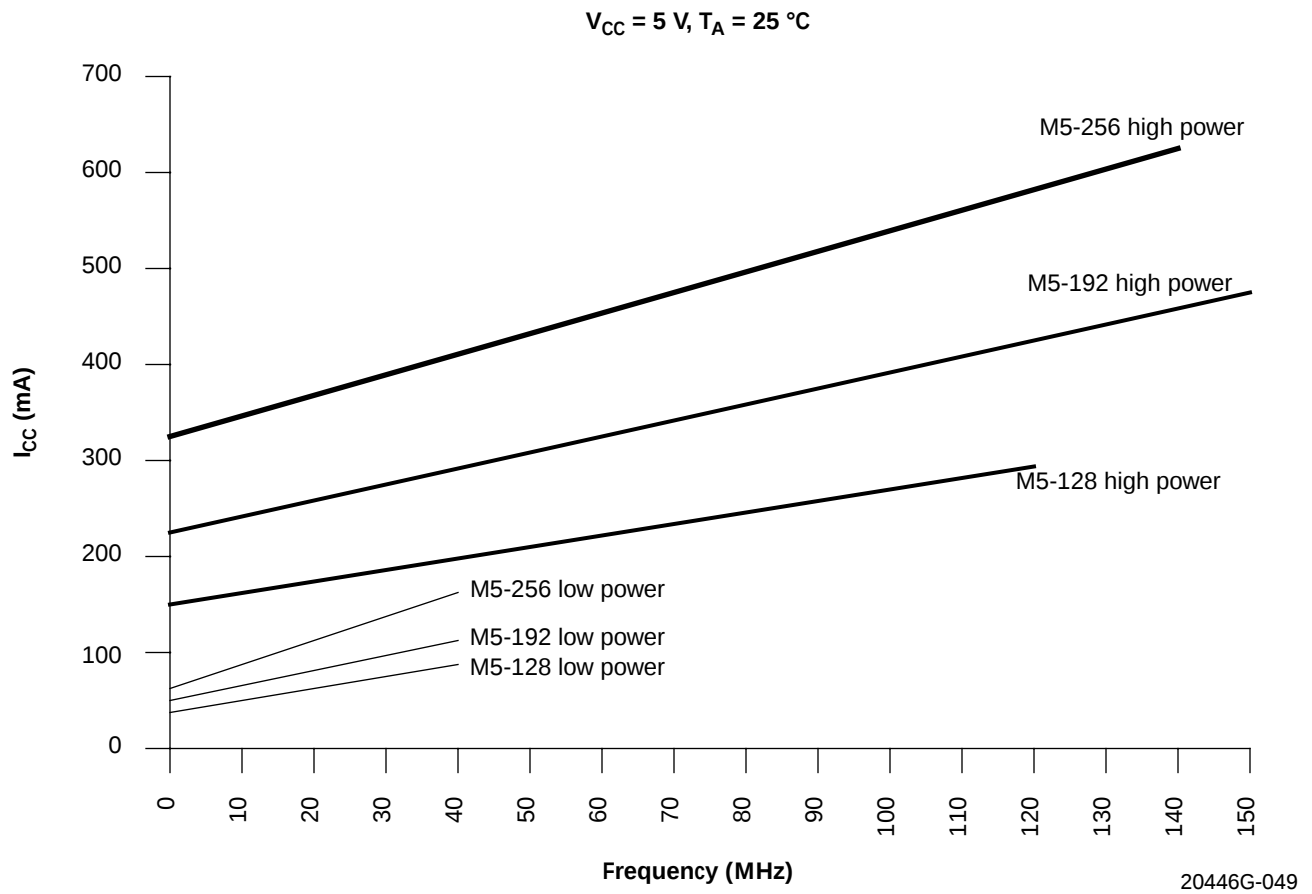
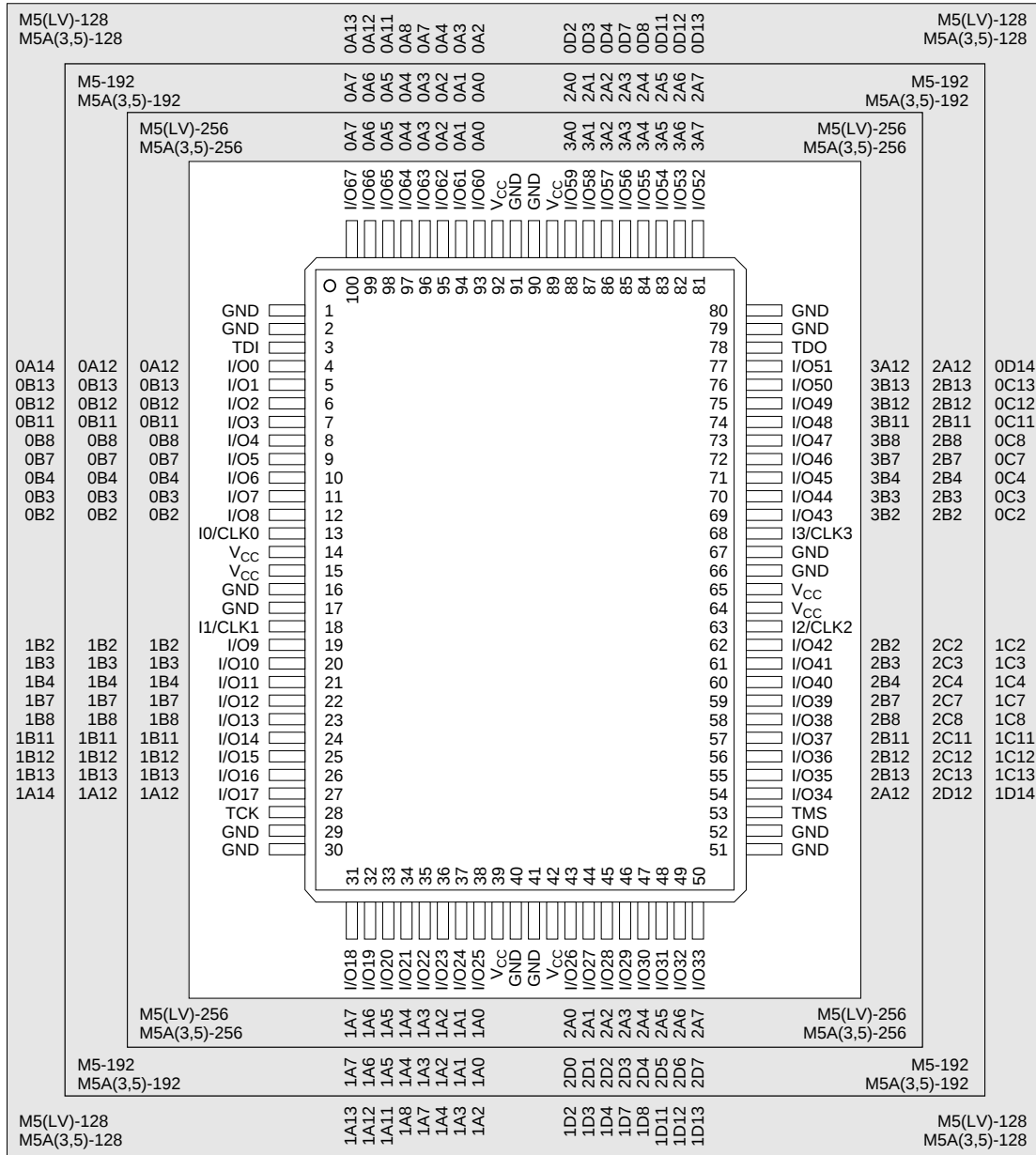


Figure 9. I_{CC} Curves at High/Low Power Modes

100-PIN PQFP CONNECTION DIAGRAM

Top View

100-Pin PQFP (68 I/O)

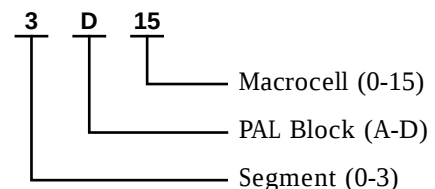


20446G-016

Pin Designations

CLK = Clock
GND = Ground
I = Input
I/O = Input/Output
NC = No Connect

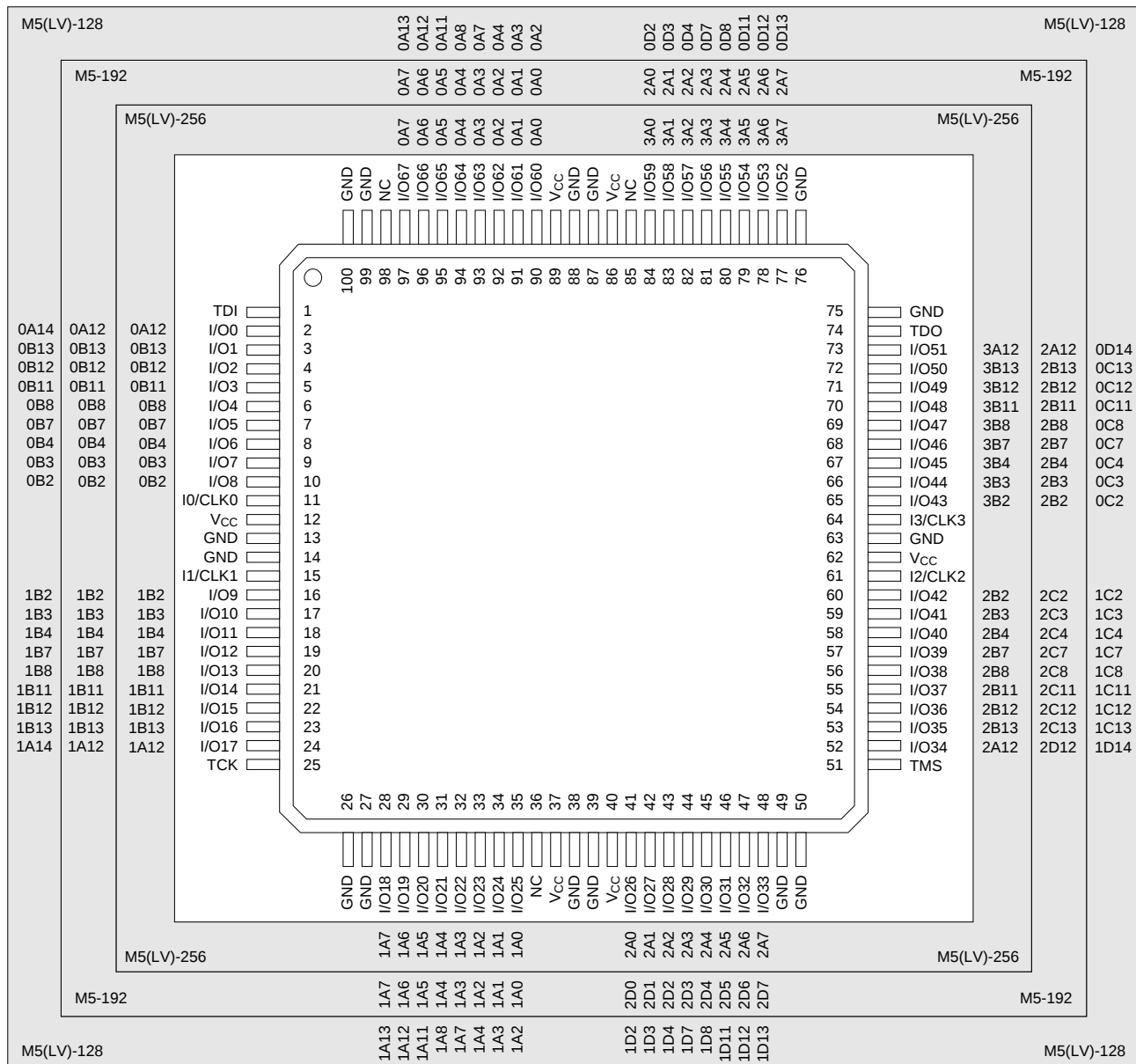
V_{CC} = Supply Voltage
TDI = Test Data In
TCK = Test Clock
TMS = Test Mode Select
TDO = Test Data Out



100-PIN TQFP CONNECTION DIAGRAM

Top View

100-Pin TQFP (68 I/O)

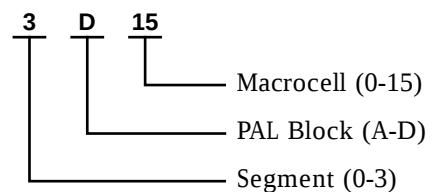


20446G-017

Pin Designations

CLK = Clock
 GND = Ground
 I = Input
 I/O = Input/Output
 NC = No Connect

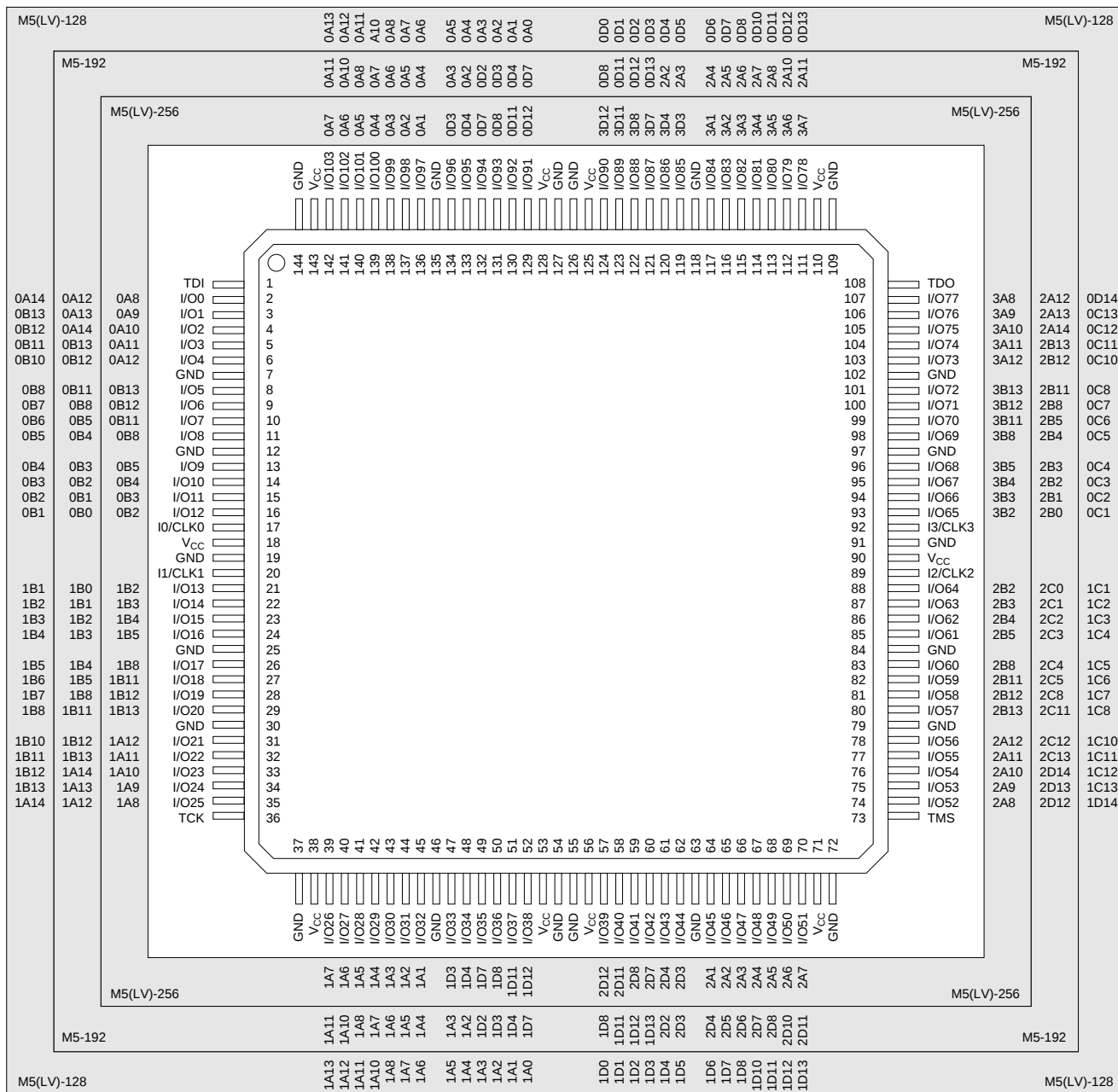
V_{CC} = Supply Voltage
 TDI = Test Data In
 TCK = Test Clock
 TMS = Test Mode Select
 TDO = Test Data Out



144-PIN PQFP CONNECTION DIAGRAM

Top View

144-Pin PQFP

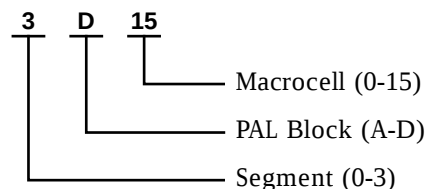


20446G-019

Pin Designations

CLK = Clock
 GND = Ground
 I = Input
 I/O = Input/Output
 NC = No Connect

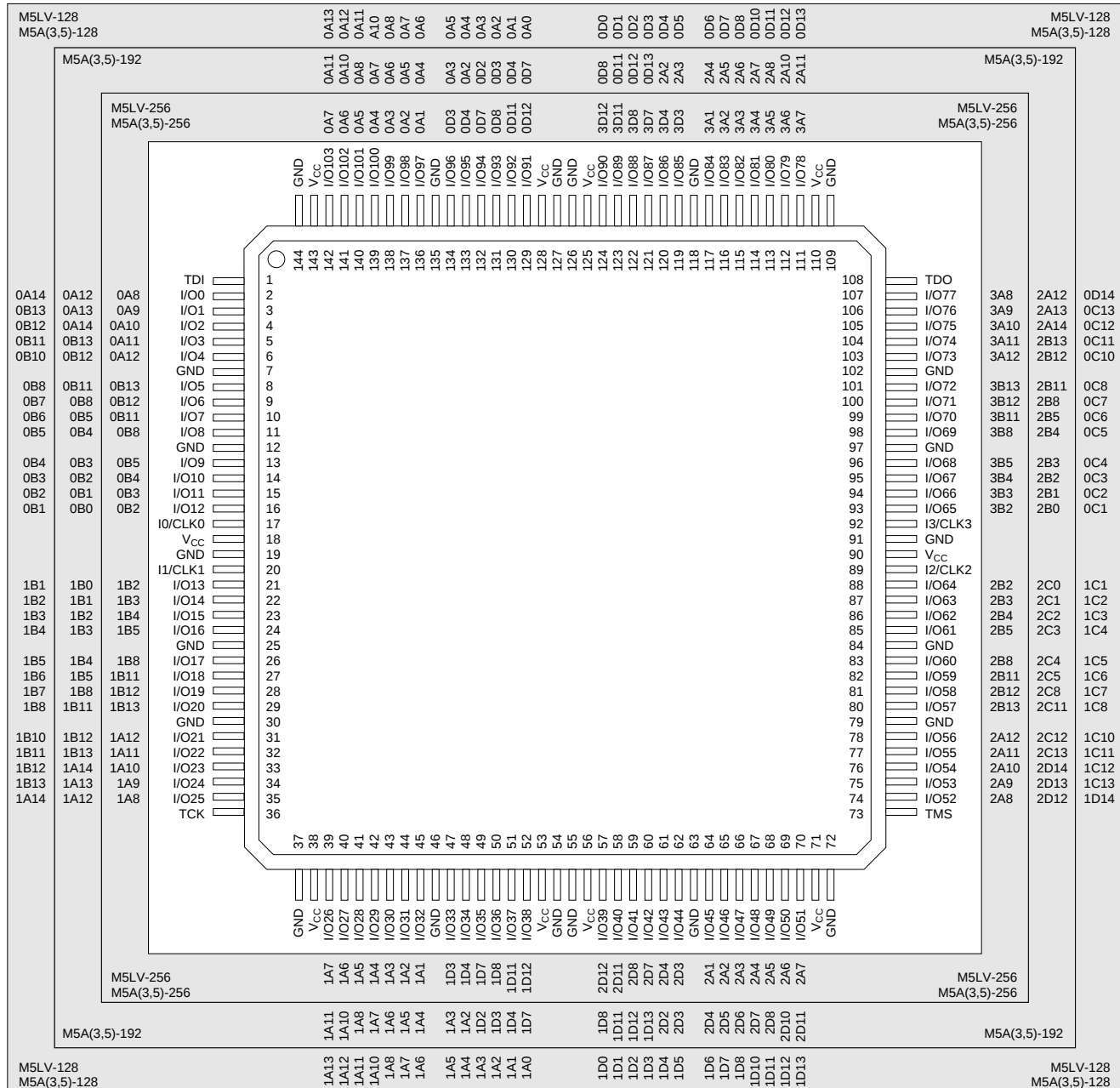
V_{CC} = Supply Voltage
 TDI = Test Data In
 TCK = Test Clock
 TMS = Test Mode Select
 TDO = Test Data Out



144-PIN TQFP CONNECTION DIAGRAM

Top View

144-Pin TQFP

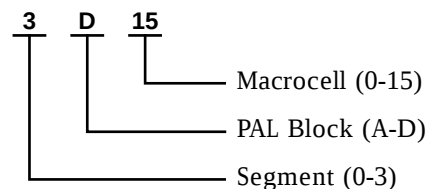


20446G-020

Pin Designations

CLK = Clock
GND = Ground
I = Input
I/O = Input/Output
NC = No Connect

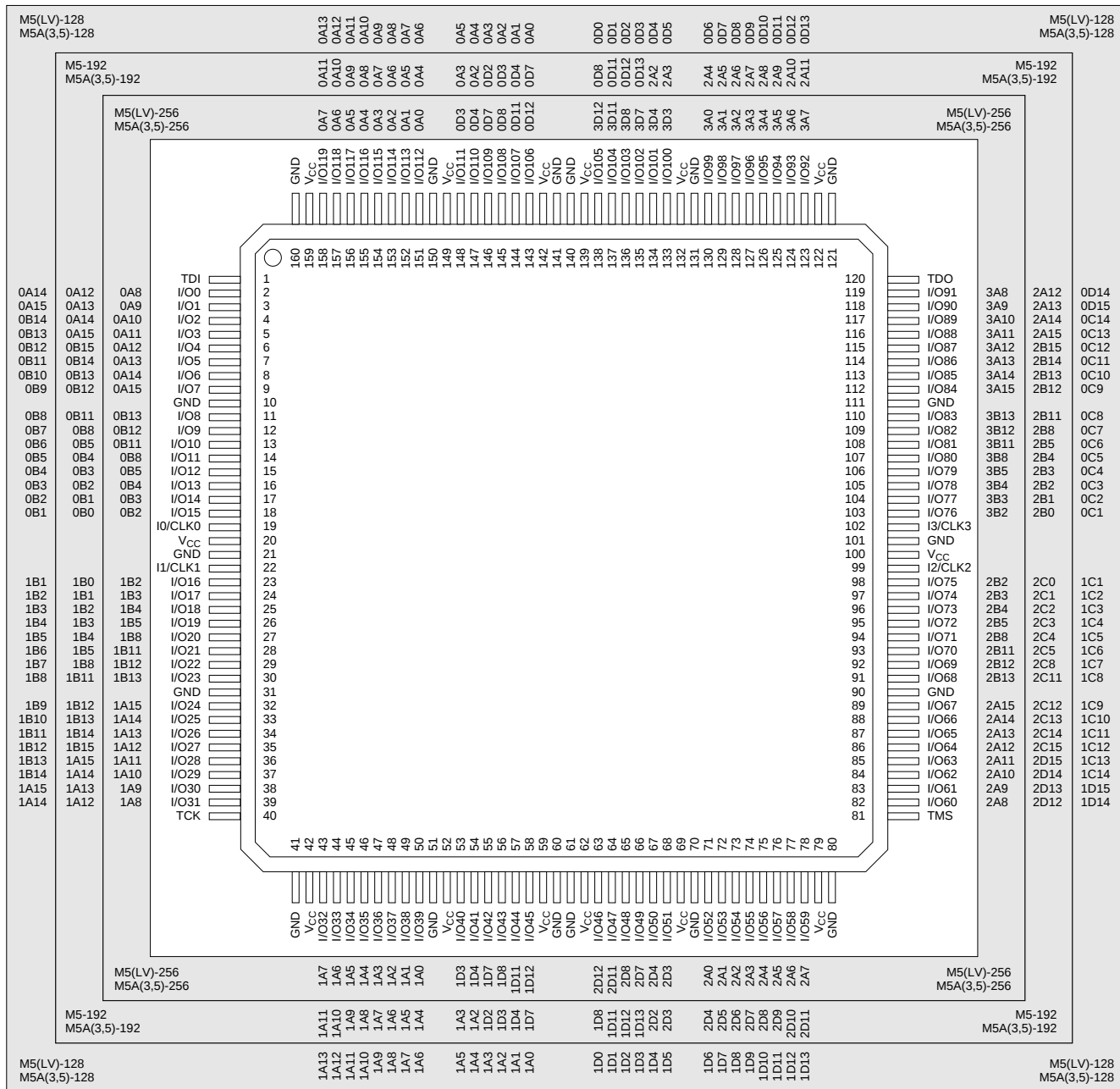
V_{CC} = Supply Voltage
TDI = Test Data In
TCK = Test Clock
TMS = Test Mode Select
TDO = Test Data Out



160-PIN PQFP CONNECTION DIAGRAM

Top View

160-Pin PQFP (128, 192, 256 Macrocells)

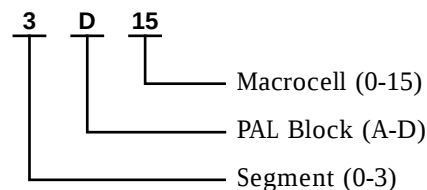


20446G-021

Pin Designations

CLK = Clock
 GND = Ground
 I = Input
 I/O = Input/Output
 NC = No Connect

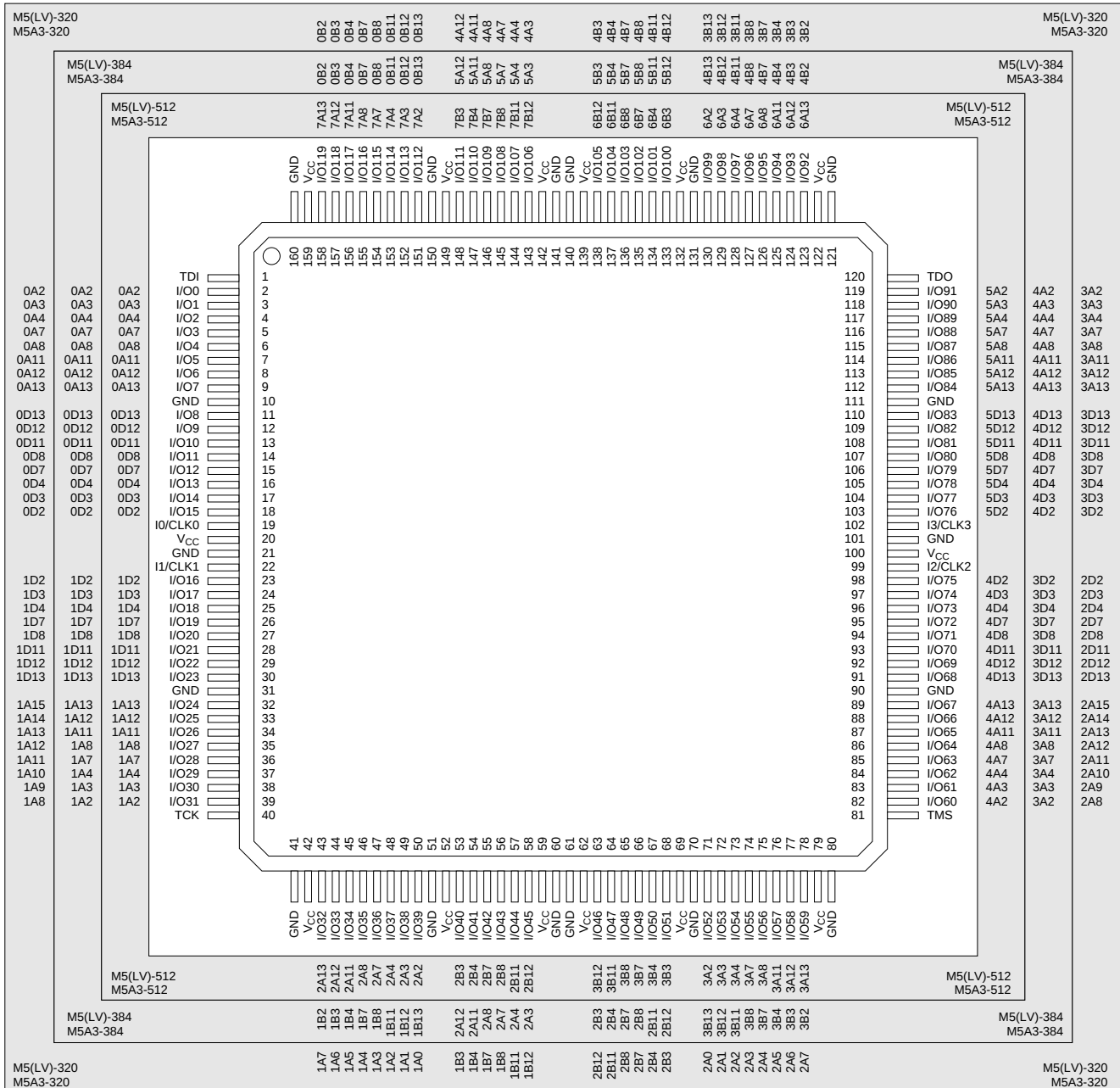
V_{CC} = Supply Voltage
 TDI = Test Data In
 TCK = Test Clock
 TMS = Test Mode Select
 TDO = Test Data Out



160-PIN PQFP CONNECTION DIAGRAM

Top View

160-Pin PQFP (320, 384, 512 Macrocells)

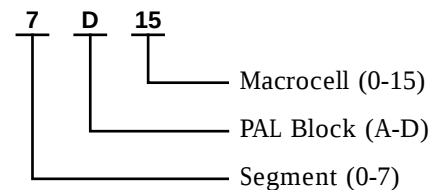


20446G-022

Pin Designations

CLK = Clock
GND = Ground
I = Input
I/O = Input/Output
NC = No Connect

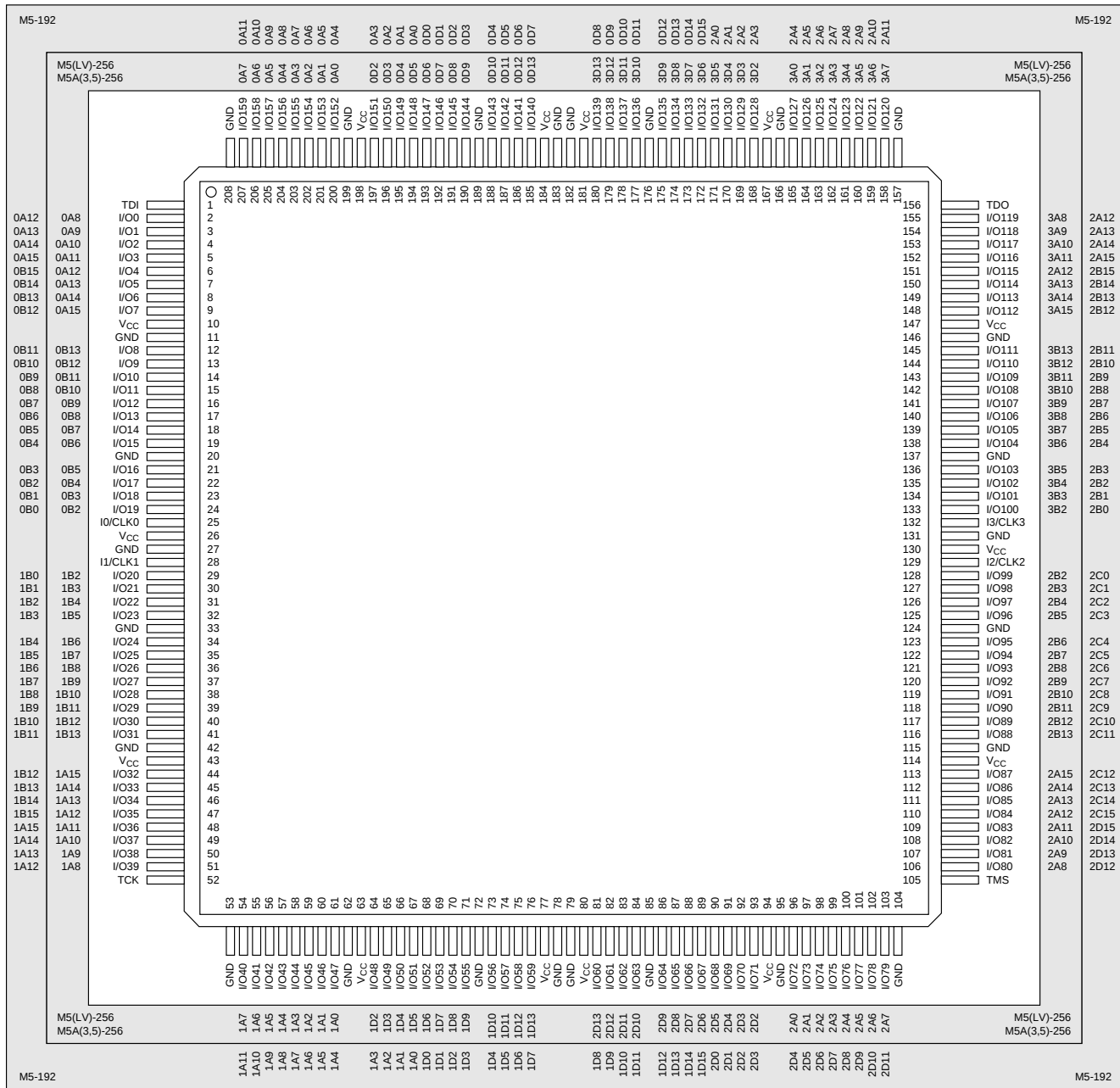
V_{CC} = Supply Voltage
TDI = Test Data In
TCK = Test Clock
TMS = Test Mode Select
TDO = Test Data Out



208-PIN PQFP CONNECTION DIAGRAM

Top View

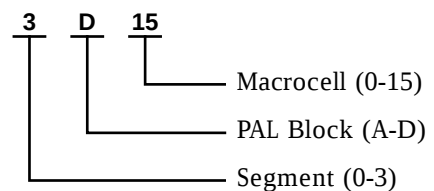
208-Pin PQFP (192, 256 Macrocells)



20446G-023

Pin Designations

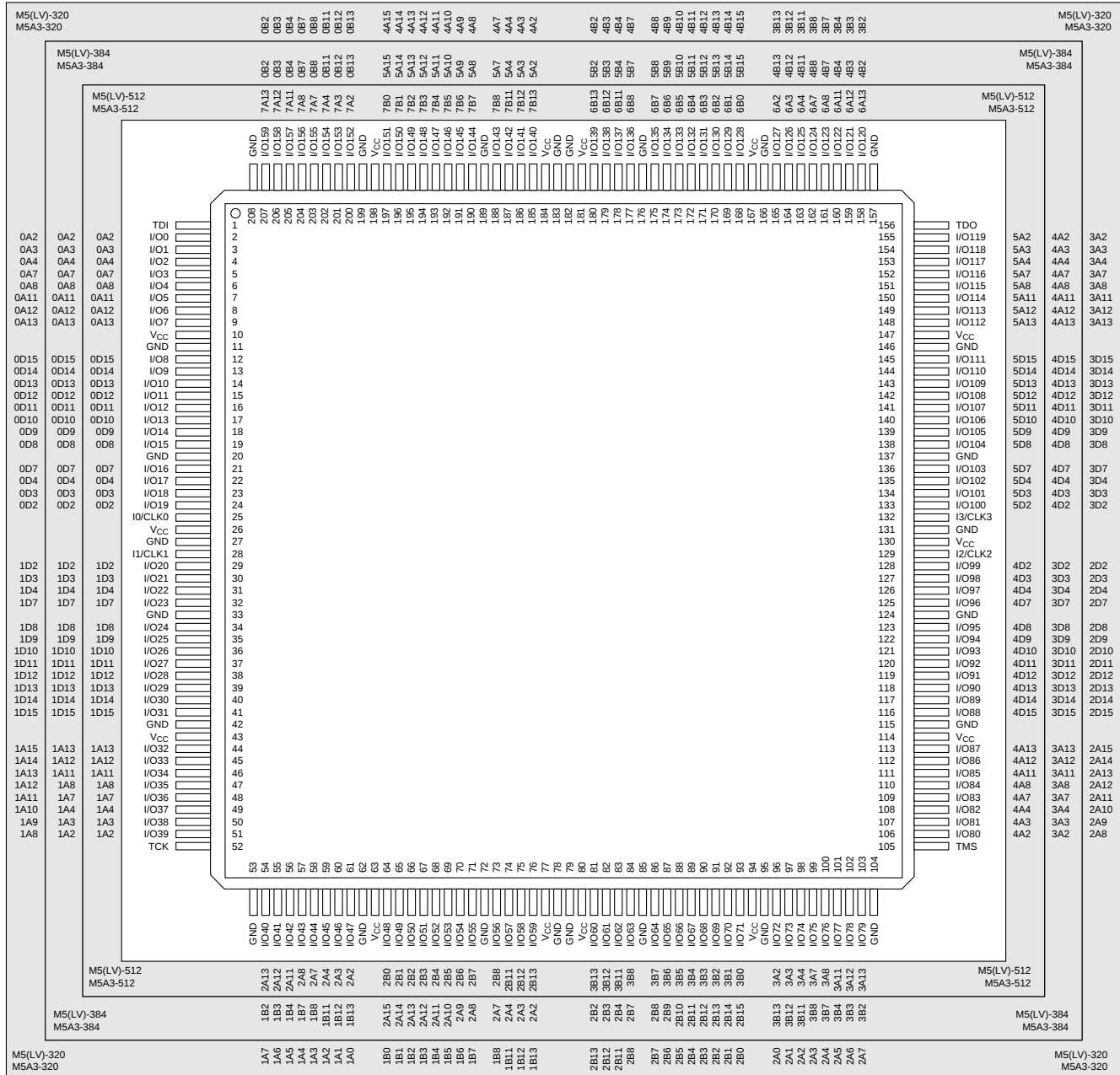
CLK	=	Clock	V _{CC}	=	Supply Voltage
GND	=	Ground	TDI	=	Test Data In
I	=	Input	TCK	=	Test Clock
I/O	=	Input/Output	TMS	=	Test Mode Select
NC	=	No Connect	TDO	=	Test Data Out



208-PIN PQFP CONNECTION DIAGRAM

Top View

208-Pin PQFP (320, 384, 512 Macrocells)

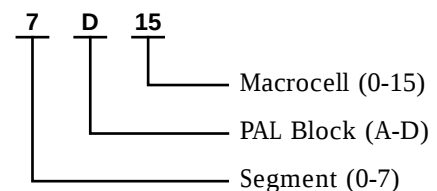


20446G-024

Pin Designations

CLK = Clock
GND = Ground
I = Input
I/O = Input/Output
NC = No Connect

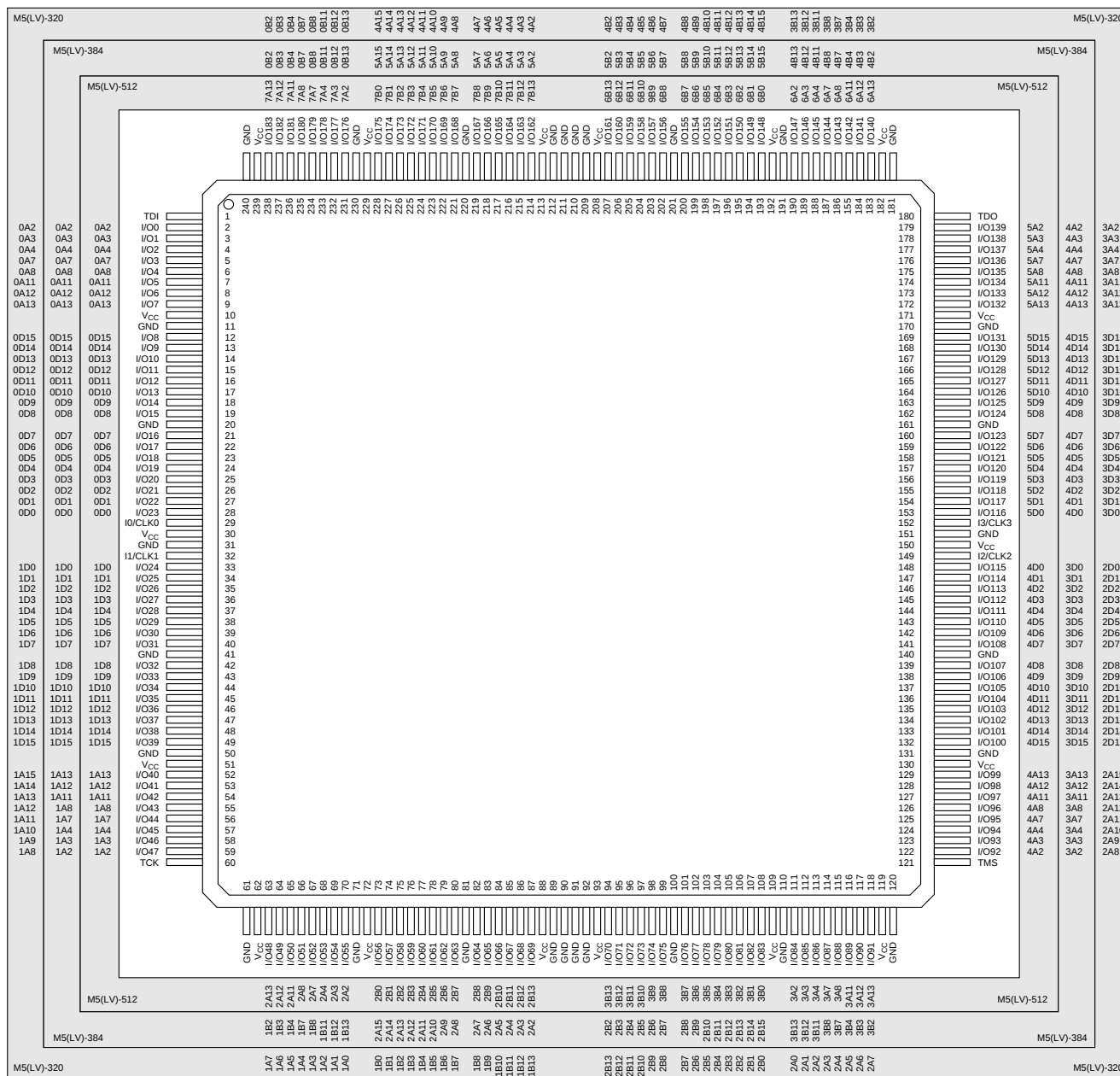
VCC = Supply Voltage
TDI = Test Data In
TCK = Test Clock
TMS = Test Mode Select
TDO = Test Data Out



204-PIN PQFP CONNECTION DIAGRAM

Top View

240-Pin PQFP

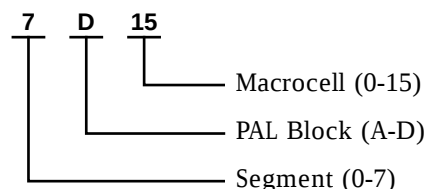


20446G-025

Pin Designations

CLK = Clock
 GND = Ground
 I = Input
 I/O = Input/Output
 NC = No Connect

V_{CC} = Supply Voltage
 TDI = Test Data In
 TCK = Test Clock
 TMS = Test Mode Select
 TDO = Test Data Out



256-BALL BGA CONNECTION DIAGRAM — M5(LV)-320, M5(LV)-384, M5(LV)-512, M5A3-320, M5A3-384, M5A3-512 Bottom View (I/O Pin-outs)

256-Ball BGA

	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	A
A	GND	I/O11	GND	I/O44	I/O58	GND	I/O70	I/O76	GND	GND	GND	GND	I/O108	I/O116	GND	I/O128	I/O134	GND	GND	GND	GND
B	GND	I/O12	I/O28	I/O45	I/O59	I/O64	I/O71	I/O77	I/O84	I/O90	I/O96	I/O102	I/O109	I/O117	I/O122	I/O129	I/O135	I/O148	I/O164	GND	GND
C	I/O0	I/O13	V _{CC}	I/O46	I/O60	I/O65	I/O72	I/O78	I/O85	I/O91	I/O97	I/O103	I/O110	I/O118	I/O123	I/O130	I/O136	V _{CC}	I/O165	I/O181	I/O181
D	I/O1	I/O14	I/O29	V _{CC}	V _{CC}	I/O66	V _{CC}	I/O79	I/O86	I/O92	I/O98	I/O104	I/O111	V _{CC}	I/O124	V _{CC}	V _{CC}	I/O149	I/O166	I/O182	I/O182
E	I/O2	I/O15	I/O30	TDI	I/O58	GND	I/O70	I/O76	GND	GND	GND	GND	I/O108	I/O116	GND	I/O128	I/O134	GND	GND	GND	GND
F	GND	I/O16	I/O31	I/O47	I/O59	I/O64	I/O71	I/O77	I/O84	I/O90	I/O96	I/O102	I/O109	I/O117	I/O122	I/O129	I/O135	I/O148	I/O164	GND	GND
G	I/O3	I/O17	I/O32	V _{CC}	I/O60	I/O65	I/O72	I/O78	I/O85	I/O91	I/O97	I/O103	I/O110	I/O118	I/O123	I/O130	I/O136	V _{CC}	I/O165	I/O181	I/O181
H	GND	I/O18	I/O33	I/O48	I/O58	GND	I/O70	I/O76	GND	GND	GND	GND	I/O108	I/O116	GND	I/O128	I/O134	GND	GND	GND	GND
J	I/O4	I/O19	I/O34	I/O49	I/O59	I/O64	I/O71	I/O77	I/O84	I/O90	I/O96	I/O102	I/O109	I/O117	I/O122	I/O129	I/O135	I/O148	I/O164	GND	GND
K	GND	I/O20	I/O35	I/O50	I/O58	GND	I/O70	I/O76	GND	GND	GND	GND	I/O108	I/O116	GND	I/O128	I/O134	GND	GND	GND	GND
L	I/O5	I/O21	I/O36	I/O51	I/O59	I/O64	I/O71	I/O77	I/O84	I/O90	I/O96	I/O102	I/O109	I/O117	I/O122	I/O129	I/O135	I/O148	I/O164	GND	GND
M	I/O6	I/O22	I/O37	I/O52	I/O58	GND	I/O70	I/O76	GND	GND	GND	GND	I/O108	I/O116	GND	I/O128	I/O134	GND	GND	GND	GND
N	GND	I/O23	I/O38	I/O53	I/O59	I/O64	I/O71	I/O77	I/O84	I/O90	I/O96	I/O102	I/O109	I/O117	I/O122	I/O129	I/O135	I/O148	I/O164	GND	GND
P	I/O7	I/O24	I/O39	V _{CC}	I/O58	GND	I/O70	I/O76	GND	GND	GND	GND	I/O108	I/O116	GND	I/O128	I/O134	GND	GND	GND	GND
R	GND	I/O25	I/O40	I/O54	I/O59	I/O64	I/O71	I/O77	I/O84	I/O90	I/O96	I/O102	I/O109	I/O117	I/O122	I/O129	I/O135	I/O148	I/O164	GND	GND
T	I/O8	I/O26	I/O41	TCK	I/O58	GND	I/O70	I/O76	GND	GND	GND	GND	I/O108	I/O116	GND	I/O128	I/O134	GND	GND	GND	GND
U	I/O9	I/O27	I/O42	V _{CC}	I/O58	GND	I/O70	I/O76	GND	GND	GND	GND	I/O108	I/O116	GND	I/O128	I/O134	GND	GND	GND	GND
V	I/O10	I/O28	V _{CC}	I/O55	I/O61	I/O68	I/O73	I/O79	I/O86	I/O92	I/O98	I/O104	I/O111	V _{CC}	I/O124	V _{CC}	V _{CC}	I/O149	I/O166	I/O182	I/O182
W	GND	I/O29	I/O43	I/O56	I/O62	I/O69	I/O74	I/O80	I/O87	I/O93	I/O99	I/O105	I/O112	V _{CC}	I/O125	V _{CC}	V _{CC}	I/O145	I/O163	I/O179	I/O180
Y	GND	GND	GND	I/O57	I/O63	GND	I/O75	I/O81	I/O88	I/O94	I/O100	I/O106	I/O113	I/O119	I/O126	I/O131	I/O146	I/O163	I/O179	I/O180	I/O180
	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	

Pin Designations

CLK	=	Clock
GND	=	Ground
I	=	Input
I/O	=	Input/Output
NC	=	No Connect
V _{CC}	=	Supply Voltage
TDI	=	Test Data In
TCK	=	Test Clock
TMS	=	Test Mode Select
TDO	=	Test Data Out

20446G-026

256-BALL BGA CONNECTION DIAGRAM — M5(LV)-320, M5A3-320

Bottom View (Macrocell Association)

256-Ball BGA

	A	B	C	D	E	F	G	H	J	K	L	M	N	P	R	T	U	V	W	Y													
1	GND	GND	3A11	3D15	3D12	GND	3D7	GND	3D3	3D2	GND	2D2	GND	2D7	GND	2D10	2D13	2D15	GND	GND	1												
2	GND	3B2	3A3	3A8	3A13	3D13	3D9	3D8	3D4	13/CLK3	12/CLK2	2D3	2D4	2D8	2D12	2A15	2A13	2A12	2A9	2A7	2												
3	GND	3B8	V _{CC}	3A2	3A4	3A12	3D14	3D10	3D5	3D0	2D0	2D5	2D9	2D14	2A14	2A10	2A8	V _{CC}	2A3	GND	3												
4	3B13	3B11	3B3	V _{CC}	TDO	3A7	V _{CC}	3D11	3D6	3D1	2D1	2D6	2D11	V _{CC}	2A11	TMS	V _{CC}	2A6	2A2	2A0	4												
5	4B14	4B15	3B4	V _{CC}	Pin Designations CLK = Clock GND = Ground I = Input I/O = Input/Output NC = No Connect V_{CC} = Supply Voltage TDI = Test Data In TCK = Test Clock TMS = Test Mode Select TDO = Test Data Out 4 D 15 Macrocell (0-15) PAL Block (A-D) Segment (0-4) <td>V_{CC}</td> <td>2A4</td> <td>2A1</td> <td>2B0</td> <td>2B1</td> <td>5</td>												V _{CC}	2A4	2A1	2B0	2B1	5											
6	GND	4B11	3B12	3B7													V _{CC}	2B3	2B8	2B13	1B13	1B8	1B3	V _{CC}	1A4	V _{CC}	1A5	1A8	V _{CC}	1A6	1A3	GND	6
7	4B8	4B10	4B13	V _{CC}													2B6	2B9	2B10	2B14	1B14	1B10	1B6	1B2	1A1	1B5	1B0	1A9	1A7	1A4	GND	7	
8	4B4	4B6	4B9	4B12													2B7	2B11	2B12	2B15	1B15	1B12	1B9	1B7	GND	1A2	1A0	1A14	1A12	1A13	1A15	1A11	8
9	GND	4B3	4B5	4B7													GND	2B4	2B5	2B11	2B12	2B13	2B14	2B15	GND	1A3	1A0	1A14	1A12	1A13	1A15	1A11	9
10	GND	4B0	4B1	4B2													2B7	2B11	2B12	2B13	2B14	2B15	GND	1A3	1A0	1A14	1A12	1A13	1A15	1A11	1A11	1A11	10
11	GND	4A0	4A1	4A2													2B7	2B11	2B12	2B13	2B14	2B15	GND	1A3	1A0	1A14	1A12	1A13	1A15	1A11	1A11	1A11	11
12	GND	4A3	4A5	4A7													2B7	2B11	2B12	2B13	2B14	2B15	GND	1A3	1A0	1A14	1A12	1A13	1A15	1A11	1A11	1A11	12
13	4A4	4A6	4A9	4A12													2B7	2B11	2B12	2B13	2B14	2B15	GND	1A3	1A0	1A14	1A12	1A13	1A15	1A11	1A11	1A11	13
14	4A8	4A10	4A13	V _{CC}													2B7	2B11	2B12	2B13	2B14	2B15	GND	1A3	1A0	1A14	1A12	1A13	1A15	1A11	1A11	1A11	14
15	GND	4A11	OB12	OB7	2B7	2B11	2B12	2B13	2B14	2B15	GND	1A3	1A0	1A14	1A12	1A13	1A15	1A11	1A11	1A11	15												
16	4A14	4A15	OB4	V _{CC}	2B7	2B11	2B12	2B13	2B14	2B15	GND	1A3	1A0	1A14	1A12	1A13	1A15	1A11	1A11	1A11	16												
17	OB13	OB11	OB3	V _{CC}	2B7	2B11	2B12	2B13	2B14	2B15	GND	1A3	1A0	1A14	1A12	1A13	1A15	1A11	1A11	1A11	17												
18	GND	OB8	V _{CC}	OA2	2B7	2B11	2B12	2B13	2B14	2B15	GND	1A3	1A0	1A14	1A12	1A13	1A15	1A11	1A11	1A11	18												
19	OB2	OA3	OA8	OA11	2B7	2B11	2B12	2B13	2B14	2B15	GND	1A3	1A0	1A14	1A12	1A13	1A15	1A11	1A11	1A11	19												
20	GND	GND	OD15	OD13	2B7	2B11	2B12	2B13	2B14	2B15	GND	1A3	1A0	1A14	1A12	1A13	1A15	1A11	1A11	1A11	20												
A	OD10	OD12	OD7	OD14	2B7	2B11	2B12	2B13	2B14	2B15	GND	1A3	1A0	1A14	1A12	1A13	1A15	1A11	1A11	1A11													
B	OD11	OD9	OD6	OD11	2B7	2B11	2B12	2B13	2B14	2B15	GND	1A3	1A0	1A14	1A12	1A13	1A15	1A11	1A11	1A11													
C	OD12	OD8	OD5	OD6	2B7	2B11	2B12	2B13	2B14	2B15	GND	1A3	1A0	1A14	1A12	1A13	1A15	1A11	1A11	1A11													
D	OD13	OD4	OD3	OD0	2B7	2B11	2B12	2B13	2B14	2B15	GND	1A3	1A0	1A14	1A12	1A13	1A15	1A11	1A11	1A11													
E	OD14	OD0	OD1	OD1	2B7	2B11	2B12	2B13	2B14	2B15	GND	1A3	1A0	1A14	1A12	1A13	1A15	1A11	1A11	1A11													
F	GND	OD12	OD8	OD14	2B7	2B11	2B12	2B13	2B14	2B15	GND	1A3	1A0	1A14	1A12	1A13	1A15	1A11	1A11	1A11													
G	OD7	OD8	OD5	OD6	2B7	2B11	2B12	2B13	2B14	2B15	GND	1A3	1A0	1A14	1A12	1A13	1A15	1A11	1A11	1A11													
H	GND	OD4	OD3	OD0	2B7	2B11	2B12	2B13	2B14	2B15	GND	1A3	1A0	1A14	1A12	1A13	1A15	1A11	1A11	1A11													
J	OD2	OD3	OD0	OD1	2B7	2B11	2B12	2B13	2B14	2B15	GND	1A3	1A0	1A14	1A12	1A13	1A15	1A11	1A11	1A11													
K	GND	10/CLK0	1D0	1D1	2B7	2B11	2B12	2B13	2B14	2B15	GND	1A3	1A0	1A14	1A12	1A13	1A15	1A11	1A11	1A11													
L	1D2	11/CLK1	1D0	1D1	2B7	2B11	2B12	2B13	2B14	2B15	GND	1A3	1A0	1A14	1A12	1A13	1A15	1A11	1A11	1A11													
M	1D3	1D4	1D5	1D6	2B7	2B11	2B12	2B13	2B14	2B15	GND	1A3	1A0	1A14	1A12	1A13	1A15	1A11	1A11	1A11													
N	GND	1D8	1D10	1D11	2B7	2B11	2B12	2B13	2B14	2B15	GND	1A3	1A0	1A14	1A12	1A13	1A15	1A11	1A11	1A11													
P	1D7	1D9	1D14	V _{CC}	2B7	2B11	2B12	2B13	2B14	2B15	GND	1A3	1A0	1A14	1A12	1A13	1A15	1A11	1A11	1A11													
R	GND	1D13	1A14	1A11	2B7	2B11	2B12	2B13	2B14	2B15	GND	1A3	1A0	1A14	1A12	1A13	1A15	1A11	1A11	1A11													
T	1D12	1A15	1A10	TCK	2B7	2B11	2B12	2B13	2B14	2B15	GND	1A3	1A0	1A14	1A12	1A13	1A15	1A11	1A11	1A11													
U	1D15	1A12	1A8	V _{CC}	2B7	2B11	2B12	2B13	2B14	2B15	GND	1A3	1A0	1A14	1A12	1A13	1A15	1A11	1A11	1A11													
V	1A13	1A9	V _{CC}	1A6	2B7	2B11	2B12	2B13	2B14	2B15	GND	1A3	1A0	1A14	1A12	1A13	1A15	1A11	1A11	1A11													
W	GND	1A7	1A3	1A2	2B7	2B11	2B12	2B13	2B14	2B15	GND	1A3	1A0	1A14	1A12	1A13	1A15	1A11	1A11	1A11													
Y	GND	GND	GND	1A0	2B7	2B11	2B12	2B13	2B14	2B15	GND	1A3	1A0	1A14	1A12	1A13	1A15	1A11	1A11	1A11													

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256-BALL BGA CONNECTION DIAGRAM — M5(LV)-384, M5A3-384

Bottom View (Macrocell Association)

256-Ball BGA

	A	B	C	D	E	F	G	H	J	K	L	M	N	P	R	T	U	V	W	Y		
1	GND	GND	4A11	4D15	4D12	GND	4D7	GND	4D3	4D2	GND	3D2	GND	3D7	GND	3D10	3D13	3D15	GND	GND	1	
2	GND	4B2	4A3	4A8	4A13	4D13	4D9	4D8	4D4	I3/CLK3	I2/CLK2	3D3	3D4	3D8	3D12	3A13	3A11	3A8	3A3	3B2	2	
3	GND	4B8	V _{CC}	4A2	4A4	4A12	4D14	4D10	4D5	4D0	3D0	3D5	3D9	3D14	3A12	3A4	3A2	V _{CC}	3B8	GND	3	
4	4B13	4B11	4B3	V _{CC}	TDO	4A7	V _{CC}	4D11	4D6	4D1	3D1	3D6	3D11	V _{CC}	3A7	TMS	V _{CC}	3B3	3B11	3B13	4	
5	5B14	5B15	4B4	V _{CC}	Pin Designations CLK = Clock GND = Ground I = Input I/O = Input/Output NC = No Connect V_{CC} = Supply Voltage TDI = Test Data In TCK = Test Clock TMS = Test Mode Select TDO = Test Data Out 5 D 15 Macrocell (0-15) PAL Block (A-D) Segment (0-5) <td>V_{CC}</td> <td>3B7</td> <td>3B4</td> <td>2B15</td> <td>2B14</td> <td>5</td>												V _{CC}	3B7	3B4	2B15	2B14	5
6	GND	5B11	4B12	4B7													V _{CC}	2B12	2B11	GND	6	
7	5B8	5B10	5B13	V _{CC}													2B7	2B9	2B10	2B8	7	
8	5B4	5B6	5B9	5B12													2B12	2B6	2B4		8	
9	GND	5B3	5B5	5B7													2B7	2B5	GND		9	
10	GND	5B0	5B1	5B2													2B2	2B1	2B0	GND	10	
11	GND	5A0	5A1	5A2													2A2	2A1	2A0	GND	11	
12	GND	5A3	5A5	5A7													2A7	2A5	2A3	GND	12	
13	5A4	5A6	5A9	5A12													2A12	2A9	2A6	2A4	13	
14	5A8	5A10	5A13	V _{CC}													V _{CC}	2A13	2A10	2A8	14	
15	GND	5A11	0B12	0B7													1B7	1B12	2A11	GND	15	
16	5A14	5A15	0B4	V _{CC}													V _{CC}	1B4	2A15	2A14	16	
17	0B13	0B11	0B3	V _{CC}	TDI	0A7	V _{CC}	0D11	0D6	0D1	1D1	1D6	1D11	V _{CC}	1A7	TCK	V _{CC}	1B3	1B11	1B13	17	
18	GND	0B8	V _{CC}	0A2	0A4	0A12	0D14	0D9	0D5	0D0	1D0	1D5	1D10	1D14	1A12	1A4	1A2	V _{CC}	1B8	GND	18	
19	0B2	0A3	0A8	0A11	0A13	0D12	0D8	0D4	0D3	I0/CLK0	I1/CLK1	1D4	1D8	1D9	1D13	1A13	1A8	1A3	1B2	GND	19	
20	GND	GND	0D15	0D13	0D10	GND	0D7	GND	0D2	GND	1D2	1D3	GND	1D7	GND	1D12	1D15	1A11	GND	GND	20	

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256-BALL BGA CONNECTION DIAGRAM — M5(LV)-512, M5A3-512

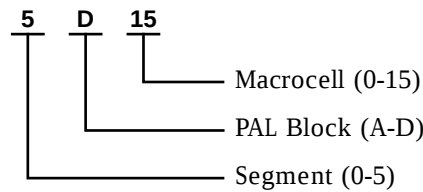
Bottom View (Macrocell Association)

256-Ball BGA

	A	B	C	D	E	F	G	H	J	K	L	M	N	P	R	T	U	V	W	Y	
1	GND	GND	5A11	5D15	5D12	GND	5D7	GND	5D3	5D2	GND	4D2	GND	4D7	GND	4D10	4D13	4D15	GND	GND	1
2	GND	6A13	5A3	5A8	5A13	5D13	5D9	5D8	5D4	13/CLK3	12/CLK2	4D3	4D4	4D8	4D12	4A13	4A11	4A8	4A3	3A13	2
3	GND	6A7	V _{CC}	5A2	5A4	5A12	5D14	5D10	5D5	5D0	4D0	4D5	4D9	4D14	4A12	4A4	4A2	V _{CC}	3A7	GND	3
4	6A2	6A4	6A12	V _{CC}	TDO	5A7	V _{CC}	5D11	5D6	5D1	4D1	4D6	4D11	V _{CC}	4A7	TMS	V _{CC}	3A12	3A4	3A2	4
5	6B1	6B0	6A11	V _{CC}													V _{CC}	3A11	3B0	3B1	5
6	GND	6B4	6A3	6A8													3A8	3A3	3B4	GND	6
7	6B7	6B5	6B2	V _{CC}													V _{CC}	3B2	3B5	3B7	7
8	6B11	6B9	6B6	6B3													3B3	3B6	3B9	3B11	8
9	GND	6B12	6B10	6B8													3B8	3B10	3B12	GND	9
10	GND	6B15	6B14	6B13													3B13	3B14	3B15	GND	10
11	GND	7B15	7B14	7B13													2B13	2B14	2B15	GND	11
12	GND	7B12	7B10	7B8													2B8	2B10	2B12	GND	12
13	7B11	7B9	7B6	7B3													2B3	2B6	2B9	2B11	13
14	7B7	7B5	7B2	V _{CC}													V _{CC}	2B2	2B5	2B7	14
15	GND	7B4	7A3	7A8													2A8	2A3	2B4	GND	15
16	7B1	7B0	7A11	V _{CC}													V _{CC}	2A11	2B0	2B1	16
17	7A2	7A4	7A12	V _{CC}													V _{CC}	2A12	2A4	2A2	17
18	GND	7A7	V _{CC}	0A2													1A2	V _{CC}	2A7	GND	18
19	7A13	0A3	0A8	0A11													1A8	1A3	2A13	GND	19
20	GND	0D15	0D13	0D10													1D15	1A11	GND	GND	20
A					0D10	0A13	0A4	TDI									V _{CC}	2A12	2A4	2A2	
B					GND	0D12	0A12	0A7									1D1	2A12	2A4	2A2	
C					0D7	0D8	0D14	V _{CC}									1D2	2A12	2A4	2A2	
D					GND	0D4	0D9	0D11									1D3	2A12	2A4	2A2	
E					0D2	0D3	0D5	0D6									1D4	2A12	2A4	2A2	
F					GND	10/CLK0	0D0	0D1									1D5	2A12	2A4	2A2	
G					1D2	11/CLK1	1D0	1D1									1D6	2A12	2A4	2A2	
H					GND	1D8	1D10	1D11									1D7	2A12	2A4	2A2	
J					1D7	1D9	1D14	V _{CC}									1D12	2A12	2A4	2A2	
K					GND	1D13	1A12	1A7									1D15	2A12	2A4	2A2	
L					1D12	1A13	1A4	TCK									1A11	2A12	2A4	2A2	
M					1D15	1A8	1A2	V _{CC}									1A13	2A12	2A4	2A2	
N					1A11	1A3	V _{CC}	2A12									1A15	2A12	2A4	2A2	
P					GND	2A13	2A7	2A4									1A11	2A12	2A4	2A2	
R					GND	2A13	2A7	2A4									1A11	2A12	2A4	2A2	
T					GND	2A13	2A7	2A4									1A11	2A12	2A4	2A2	
U					GND	2A13	2A7	2A4									1A11	2A12	2A4	2A2	
V					GND	2A13	2A7	2A4									1A11	2A12	2A4	2A2	
W					GND	2A13	2A7	2A4									1A11	2A12	2A4	2A2	
Y					GND	2A13	2A7	2A4									1A11	2A12	2A4	2A2	

Pin Designations

CLK = Clock
 GND = Ground
 I = Input
 I/O = Input/Output
 NC = No Connect
 V_{CC} = Supply Voltage
 TDI = Test Data In
 TCK = Test Clock
 TMS = Test Mode Select
 TDO = Test Data Out



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352-BALL BGA CONNECTION DIAGRAM — M5(LV)-512, M5A3-512

Bottom View (I/O Pin-outs)

352-Ball BGA

	A	B	C	D	E	F	G	H	J	K	L	M	N	P	R	T	U	V	W	Y	AA	AB	AC	AD	AE	AF	
1	NC	NC	NC	GND	NC	I/O189	I/O190	I/O191	V _{CC}	I/O192	V _{CC}	I/O193	I/O194	I/O195	V _{CC}	I/O196	I/O197	I/O198	V _{CC}	I/O199	V _{CC}	I/O200	I/O201	V _{CC}	I/O202	I/O203	I/O204
2	NC	NC	NC	GND	NC	I/O188	I/O187	I/O177	I/O178	I/O165	I/O166	I/O167	I/O168	I/O169	I/O170	I/O171	I/O172	I/O173	I/O174	I/O175	I/O176	I/O177	I/O178	I/O179	I/O180	I/O181	I/O182
3	GND	GND	NC	NC	I/O205	I/O206	I/O207	I/O208	I/O209	I/O210	I/O211	I/O212	I/O213	I/O214	I/O215	I/O216	I/O217	I/O218	I/O219	I/O220	I/O221	I/O222	I/O223	I/O224	TMS	NC	NC
4	NC	I/O188	NC	TDO	V _{CC}	I/O189	I/O190	I/O191	I/O192	I/O193	I/O194	I/O195	I/O196	I/O197	I/O198	I/O199	I/O200	I/O201	I/O202	I/O203	I/O204	I/O205	I/O206	I/O207	I/O208	I/O209	I/O210
5	GND	I/O183	I/O184	V _{CC}	I/O185	I/O186	I/O187	I/O188	I/O189	I/O190	I/O191	I/O192	I/O193	I/O194	I/O195	I/O196	I/O197	I/O198	I/O199	I/O200	I/O201	I/O202	I/O203	I/O204	I/O205	I/O206	I/O207
6	NC	I/O176	I/O177	I/O178	I/O179	I/O180	I/O181	I/O182	I/O183	I/O184	I/O185	I/O186	I/O187	I/O188	I/O189	I/O190	I/O191	I/O192	I/O193	I/O194	I/O195	I/O196	I/O197	I/O198	I/O199	I/O200	I/O201
7	GND	I/O169	I/O170	I/O171	I/O172	I/O173	I/O174	I/O175	I/O176	I/O177	I/O178	I/O179	I/O180	I/O181	I/O182	I/O183	I/O184	I/O185	I/O186	I/O187	I/O188	I/O189	I/O190	I/O191	I/O192	I/O193	I/O194
8	I/O162	I/O163	I/O164	I/O165	I/O166	I/O167	I/O168	NC	I/O169	I/O170	I/O171	I/O172	I/O173	I/O174	I/O175	I/O176	I/O177	I/O178	I/O179	I/O180	I/O181	I/O182	I/O183	I/O184	I/O185	I/O186	I/O187
9	I/O156	I/O157	I/O158	I/O159	V _{CC}	I/O160	I/O161	GND	I/O162	I/O163	I/O164	I/O165	I/O166	I/O167	I/O168	I/O169	I/O170	I/O171	I/O172	I/O173	I/O174	I/O175	I/O176	I/O177	I/O178	I/O179	I/O180
10	GND	I/O150	I/O151	V _{CC}	I/O152	I/O153	I/O154	I/O155	I/O156	I/O157	I/O158	I/O159	I/O160	I/O161	I/O162	I/O163	I/O164	I/O165	I/O166	I/O167	I/O168	I/O169	I/O170	I/O171	I/O172	I/O173	I/O174
11	I/O142	I/O143	I/O144	I/O145	I/O146	I/O147	I/O148	I/O149	I/O150	I/O151	I/O152	I/O153	I/O154	I/O155	I/O156	I/O157	I/O158	I/O159	I/O160	I/O161	I/O162	I/O163	I/O164	I/O165	I/O166	I/O167	I/O168
12	I/O134	I/O135	I/O136	I/O137	I/O138	I/O139	I/O140	I/O141	I/O142	I/O143	I/O144	I/O145	I/O146	I/O147	I/O148	I/O149	I/O150	I/O151	I/O152	I/O153	I/O154	I/O155	I/O156	I/O157	I/O158	I/O159	I/O160
13	I/O128	I/O129	I/O130	I/O131	I/O132	I/O133	I/O134	I/O135	I/O136	I/O137	I/O138	I/O139	I/O140	I/O141	I/O142	I/O143	I/O144	I/O145	I/O146	I/O147	I/O148	I/O149	I/O150	I/O151	I/O152	I/O153	I/O154
14	GND	I/O122	I/O123	V _{CC}	I/O124	I/O125	I/O126	I/O127	I/O128	I/O129	I/O130	I/O131	I/O132	I/O133	I/O134	I/O135	I/O136	I/O137	I/O138	I/O139	I/O140	I/O141	I/O142	I/O143	I/O144	I/O145	I/O146
15	I/O114	I/O115	I/O116	I/O117	I/O118	I/O119	I/O120	I/O121	I/O122	I/O123	I/O124	I/O125	I/O126	I/O127	I/O128	I/O129	I/O130	I/O131	I/O132	I/O133	I/O134	I/O135	I/O136	I/O137	I/O138	I/O139	I/O140
16	NC	I/O107	I/O108	I/O109	I/O110	I/O111	I/O112	I/O113	I/O114	I/O115	I/O116	I/O117	I/O118	I/O119	I/O120	I/O121	I/O122	I/O123	I/O124	I/O125	I/O126	I/O127	I/O128	I/O129	I/O130	I/O131	I/O132
17	I/O101	I/O102	I/O103	I/O104	V _{CC}	I/O105	I/O106	GND	I/O107	I/O108	I/O109	I/O110	I/O111	I/O112	I/O113	I/O114	I/O115	I/O116	I/O117	I/O118	I/O119	I/O120	I/O121	I/O122	I/O123	I/O124	I/O125
18	GND	I/O95	I/O96	V _{CC}	I/O97	I/O98	I/O99	I/O100	I/O101	I/O102	I/O103	I/O104	I/O105	I/O106	I/O107	I/O108	I/O109	I/O110	I/O111	I/O112	I/O113	I/O114	I/O115	I/O116	I/O117	I/O118	I/O119
19	I/O87	I/O88	I/O89	I/O90	I/O91	I/O92	I/O93	I/O94	I/O95	I/O96	I/O97	I/O98	I/O99	I/O100	I/O101	I/O102	I/O103	I/O104	I/O105	I/O106	I/O107	I/O108	I/O109	I/O110	I/O111	I/O112	I/O113
20	I/O80	I/O81	I/O82	I/O83	I/O84	I/O85	I/O86	GND	I/O87	I/O88	I/O89	I/O90	I/O91	I/O92	I/O93	I/O94	I/O95	I/O96	I/O97	I/O98	I/O99	I/O100	I/O101	I/O102	I/O103	I/O104	I/O105
21	I/O73	I/O74	I/O75	I/O76	I/O77	I/O78	I/O79	NC	I/O80	I/O81	I/O82	I/O83	I/O84	I/O85	I/O86	I/O87	I/O88	I/O89	I/O90	I/O91	I/O92	I/O93	I/O94	I/O95	I/O96	I/O97	I/O98
22	GND	I/O68	I/O69	I/O70	V _{CC}	I/O71	I/O72	GND	I/O73	I/O74	I/O75	I/O76	I/O77	I/O78	I/O79	I/O80	I/O81	I/O82	I/O83	I/O84	I/O85	I/O86	I/O87	I/O88	I/O89	I/O90	I/O91
23	I/O51	I/O52	I/O53	V _{CC}	I/O54	I/O55	I/O56	I/O57	I/O58	I/O59	I/O60	I/O61	I/O62	I/O63	I/O64	I/O65	I/O66	I/O67	I/O68	I/O69	I/O70	I/O71	I/O72	I/O73	I/O74	I/O75	I/O76
24	NC	NC	TDI	I/O32	I/O33	I/O34	I/O35	I/O36	I/O37	I/O38	I/O39	I/O40	I/O41	I/O42	I/O43	I/O44	I/O45	I/O46	I/O47	I/O48	I/O49	I/O50	I/O51	I/O52	I/O53	I/O54	I/O55
25	GND	GND	I/O11	I/O12	I/O13	I/O14	I/O15	I/O16	I/O17	I/O18	I/O19	I/O20	I/O21	I/O22	I/O23	I/O24	I/O25	I/O26	I/O27	I/O28	I/O29	I/O30	I/O31	I/O32	I/O33	I/O34	I/O35
26	NC	NC	GND	I/O0	NC	GND	I/O1	I/O2	GND	I/O3	I/O4	I/O5	GND	I/O6	I/O7	GND	I/O8	I/O9	GND	I/O10	NC	GND	I/O11	I/O12	I/O13	I/O14	I/O15

Pin Designations

CLK = Clock

GND = Ground

I = Input

I/O = Input/Output

NC = No Connect

V_{CC} = Supply Voltage

TDI = Test Data In

TCK = Test Clock

TMS = Test Mode Select

TDO = Test Data Out

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Pin Designations

- CLK = Clock
- GND = Ground
- I = Input
- I/O = Input/Output
- NC = No Connect
- V_{CC} = Supply Voltage
- TDI = Test Data In
- TCK = Test Clock
- TMS = Test Mode Select
- TDO = Test Data Out

20446G-030

352-BALL BGA CONNECTION DIAGRAM — M5(LV)-512, M5A3-512

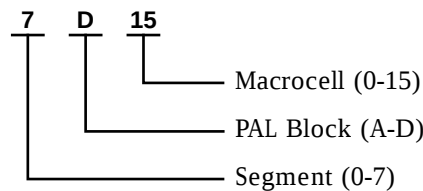
Bottom View (I/O Pin-outs)

352-Ball BGA

	A	B	C	D	E	F	G	H	J	K	L	M	N	P	R	T	U	V	W	Y	AA	AB	AC	AD	AE	AF	
1	NC	NC	NC	GND	NC	5A12	GND	5D15	5D11	GND	5D6	5D3	13/CLK3	GND	4D1	4D5	4D9	GND	4D15	4A13	GND	NC	4A6	GND	NC	NC	1
2	NC	NC	NC	5A2	5A5	5A9	5A14	5A15	5D13	5D10	5D8	5D4	5D0	4D0	4D2	4D6	4D10	4D13	4A15	4A12	4A9	4A8	4A3	4A1	GND	GND	2
3	GND	GND	NC	5A1	5A4	5A7	5A8	5A10	5A13	5D14	5D9	5D5	5D1	12/CLK2	4D4	4D7	4D11	4D14	4A14	4A10	4A7	4A5	4A2	TMS	NC	NC	3
4	NC	6A14	NC	TDO	5A0	5A3	5A6	V _{CC}	5A11	V _{CC}	5D12	5D7	5D2	V _{CC}	4D3	4D8	4D12	V _{CC}	4A11	V _{CC}	4A4	4A0	V _{CC}	3A15	3A13	3A12	4
5	GND	6A12	6A13	V _{CC}																			3A14	3A11	3A9	GND	5
6	NC	6A9	6A10	6A15																			3A10	3A8	3A7	3A5	6
7	GND	6A6	6A8	6A11																			3A6	3A4	3A3	3A0	7
8	6A1	6A4	6A5	6A7																			3A2	3A1	3B0	NC	8
9	6B1	6A0	6A2	6A3																			V _{CC}	3B1	3B2	GND	9
10	GND	6B2	6B0	V _{CC}																			3B3	3B4	3B5	3B6	10
11	6B6	6B5	6B4	6B3																			3B7	3B8	3B9	3B10	11
12	6B10	6B9	6B8	6B7																			3B11	3B12	3B13	3B14	12
13	6B14	6B13	6B12	6B11																			V _{CC}	2B15	3B15	GND	13
14	GND	7B15	6B15	V _{CC}																			2B11	2B12	2B13	2B14	14
15	7B14	7B13	7B12	7B11																			2B7	2B8	2B9	2B10	15
16	NC	7B10	7B9	7B8																			2B3	2B4	2B5	2B6	16
17	7B7	7B6	7B5	7B4																			V _{CC}	2B0	2B2	GND	17
18	GND	7B3	7B2	V _{CC}																			2A3	2A2	2A0	2B1	18
19	7B1	7B0	7A1	7A4																			2A7	2A5	2A4	2A1	19
20	7A0	7A2	7A3	7A8																			2A11	2A8	2A6	GND	20
21	7A5	7A6	7A7	7A12																			2A15	2A10	2A9	NC	21
22	GND	7A9	7A11	7A15																			V _{CC}	2A13	2A12	GND	22
23	7A10	7A13	7A14	V _{CC}																			TCK	NC	2A14	NC	23
24	NC	NC	TDI	0A2	0A0	0A4	V _{CC}	0A11	V _{CC}	0D12	0D8	0D3	10/CLK0	1D2	1D1	1D5	1D12	V _{CC}	1A11	1A6	1A3	1A4	1A1	NC	GND	GND	24
25	GND	GND	0A1	0A3	0A8	0A7	0A10	0A15	0D13	0D10	0D6	0D2	0D0	1D0	1D4	1D8	1D10	1D13	1A15	1A14	1A9	1A5	1A2	NC	NC	NC	25
26	NC	NC	GND	0A6	NC	GND	0A13	0D15	GND	0D9	0D5	0D1	GND	11/CLK1	1D3	1D6	GND	1D11	1D15	GND	1A12	NC	GND	NC	NC	NC	26

Pin Designations

CLK = Clock
 GND = Ground
 I = Input
 I/O = Input/Output
 NC = No Connect
 V_{CC} = Supply Voltage
 TDI = Test Data In
 TCK = Test Clock
 TMS = Test Mode Select
 TDO = Test Data Out



20446G-031

5V M5 AND M5A5 ORDERING INFORMATION

Vantis standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of the elements below.

	M5-	512	/256	-7	A	C	
FAMILY TYPE							OPERATING CONDITIONS
M5- = MACH 5 (5-V V_{CC})							C = Commercial (0°C to +70°C)
M5A5- = MACH 5A(5-V V_{CC})							I = Industrial (-40°C to +85°C)
MACROCELL DENSITY							PACKAGE TYPE
128 = 128 Macrocells							Y = Plastic Quad Flat Pack (PQFP)
192 = 192 Macrocells							V = Thin Quad Flat Pack (TQFP)
256 = 256 Macrocells							A = Ball Grid Array (BGA)
320 = 320 Macrocells							H = Plastic Quad Flat Pack (PQFP)
384 = 384 Macrocells							with exposed heat sink
512 = 512 Macrocells							
I/Os							SPEED
/68 = 68 I/Os in 100-pin PQFP or TQFP							-5 = 5.5 ns t_{PD}
/74 = 74 I/Os in 100-pin TQFP							-7 = 7.5 ns t_{PD}
/104 = 104 I/Os in 144-pin PQFP or TQFP							-10 = 10 ns t_{PD}
/120 = 120 I/Os in 160-pin PQFP							-12 = 12 ns t_{PD}
/160 = 160 I/Os in 208-pin PQFP							-15 = 15 ns t_{PD}
/184 = 184 I/Os in 240-pin PQFP							-20 = 20 ns t_{PD}
/192 = 192 I/Os in 256-ball BGA							
/256 = 256 I/Os in 352-ball BGA							

Valid Combinations		
M5-128/68	Commercial: M5: -7, -10, -12, -15 M5A5: -5, -7, -10, -12 Industrial: M5: -10, -12, -15, -20 M5A5: -7, -10, -12, -15	YC, VC, YI, VI
M5A5-128/68		YC, YI
M5A5-128/74		VC, VI
M5-128/104		YC, YI
M5A5-128/104		VC, VI
M5-128/120		YC, YI
M5A5-128/120		YC, YI
M5-192/68		YC, VC, YI, VI
M5A5-192/68		YC, YI
M5A5-192/74		VC, VI
M5-192/104		YC, YI
M5A5-192/104		VC, VI
M5-192/120		YC, YI
M5A5-192/120		YC, YI
M5-192/160		YC, YI
M5-256/68		YC, VC, YI, VI
M5A5-256/68		YC, YI
M5A5-256/74		VC, VI
M5-256/104		YC, YI
M5A5-256/104		VC, VI
M5-256/120		YC, YI
M5A5-256/120		YC, YI
M5-256/160		YC, YI
M5A5-256/160		YC, YI

Device Marking

Actual device marking differs from the ordering part number (OPN). “MACH 5” is marked on a device wherever “M5-” is used in the OPN. All MACH devices are dual-marked with both Commercial and Industrial grades. The Industrial grade is slower, i.e., MACH5-512/256-7AC-10AI.

Valid Combinations		
M5-320/120	Commercial: -7, -10, -12, -15 Industrial: -10, -12, -15, -20	HC, HI
M5-320/160		HC, HI
M5-320/184		HC, HI
M5-320/192		AC, AI
M5-384/120		HC, HI
M5-384/160		HC, HI
M5-384/184		HC, HI
M5-384/192		AC, AI
M5-512/120		HC, HI
M5-512/160		HC, HI
M5-512/184		HC, HI
M5-512/192		AC, AI
M5-512/256		AC, AI

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local Vantis sales office to confirm availability of specific valid combinations and to check on newly released combinations.

3.3V M5LV AND M5A3 ORDERING INFORMATION

Vantis standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of the elements below.

	M5LV-	512	/256	-7	A	C	
FAMILY TYPE							OPERATING CONDITIONS
M5LV- = MACH 5 Low Voltage (3.3-V V_{CC})							C = Commercial (0°C to +70°C)
M5A3- = MACH 5A Low Voltage (3.3-V V_{CC})							I = Industrial (-40°C to +85°C)
MACROCELL DENSITY							PACKAGE TYPE
128 = 128 Macrocells							Y = Plastic Quad Flat Pack (PQFP)
192 = 192 Macrocells							V = Thin Quad Flat Pack (TQFP)
256 = 256 Macrocells							A = Ball Grid Array (BGA)
320 = 320 Macrocells							H = Plastic Quad Flat Pack (PQFP)
384 = 384 Macrocells							with exposed heat sink
512 = 512 Macrocells							
I/Os							SPEED
/68 = 68 I/Os in 100-pin PQFP or TQFP							-5 = 5.5 ns t_{PD}
/74 = 74 I/Os in 100-pin TQFP							-6 = 6.5 ns t_{PD}
/104 = 104 I/Os in 144-pin PQFP or TQFP							-7 = 7.5 ns t_{PD}
/120 = 120 I/Os in 160-pin PQFP							-10 = 10 ns t_{PD}
/160 = 160 I/Os in 208-pin PQFP							-12 = 12 ns t_{PD}
/184 = 184 I/Os in 240-pin PQFP							-15 = 15 ns t_{PD}
/192 = 192 I/Os in 256-ball BGA							-20 = 20 ns t_{PD}
/256 = 256 I/Os in 352-ball BGA							

Valid Combinations		
M5LV-128/68	Commercial: M5LV: -5, -7, -10, -12 M5A3: -5, -7, -10, -12 Industrial: M5LV: -7, -10, -12, -15 M5A3: -7, -10, -12, -15	YC, VC, YI, VI
M5A3-128/68		YC, YI
M5LV-128/74		VC, VI
M5A3-128/74		VC, VI
M5LV-128/104		YC, VC, YI, VI
M5A3-128/104		VC, VI
M5LV-128/120		YC, YI
M5A3-128/120		YC, YI
M5A3-192/68		YC, YI
M5A3-192/74		VC, VI
M5A3-192/104		VC, VI
M5A3-192/120		YC, YI
M5LV-256/68		YC, VC, YI, VI
M5A3-256/68		YC, YI
M5LV-256/74		VC, VI
M5A3-256/74		VC, VI
M5LV-256/104		YC, VC, YI, VI
M5A3-256/104		VC, VI
M5LV-256/120		YC, YI
M5A3-256/120		YC, YI
M5LV-256/160		YC, YI
M5A3-256/160		YC, YI

Device Marking

Actual device marking differs from the ordering part number (OPN). “MACH 5” is marked on a device wherever “M5-” is used in the OPN. All MACH devices are dual-marked with both Commercial and Industrial grades. The Industrial grade is slower, i.e., MACH5 LV-512/256-7AC-10AI.

Valid Combinations		
M5LV-320/120	Commercial: M5LV: -7, -10, -12, -15 M5A3: -5, -6, -7, -10, -12 Industrial: M5LV: -10, -12, -15, -20 M5A3: -7, -10, -12, -15	HC, HI
M5A3-320/120		HC, HI
M5LV-320/160		HC, HI
M5A3-320/160		HC, HI
M5LV-320/184		HC, HI
M5LV-320/192		AC, AI
M5A3-320/192		AC, AI
M5LV-384/120		HC, HI
M5A3-384/120		HC, HI
M5LV-384/160		HC, HI
M5A3-384/160		HC, HI
M5LV-384/184		HC, HI
M5LV-384/192		AC, AI
M5A3-384/192		AC, AI
M5LV-512/120		HC, HI
M5A3-512/120		HC, HI
M5LV-512/160		HC, HI
M5A3-512/160		HC, HI
M5LV-512/184		HC, HI
M5LV-512/192		AC, AI
M5A3-512/192		AC, AI
M5LV-512/256		AC, AI
M5A3-512/256		AC, AI

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local Vantis sales office to confirm availability of specific valid combinations and to check on newly released combinations.