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Team Nexperia

74ALVT16821

20-bit bus interface D-type flip-flop; positive-edge trigger;
3-state

Rev. 03 — 13 June 2005

Product data sheet

1. General description

The 74ALVT16821 high-performance Bipolar Complementary Metal Oxide Semiconductor (BiCMOS) device combines low static and dynamic power dissipation with high speed and high output drive. It is designed for V_{CC} operation at 2.5 V or 3.3 V with I/O compatibility to 5 V.

The 74ALVT16821 has two 10-bit, edge triggered registers, with each register coupled to a 3-state output buffer. The two sections of each register are controlled independently by the clock (nCP) and output enable ($n\overline{OE}$) control gates.

Each register is fully edge triggered. The state of each D input, one set-up time before the LOW-to-HIGH clock transition, is transferred to the corresponding flip-flops Q output.

The 3-state output buffers are designed to drive heavily loaded 3-state buses, MOS memories, or MOS microprocessors.

The active low output enable ($n\overline{OE}$) controls all ten 3-state buffers independent of the register operation. When $n\overline{OE}$ is LOW, the data in the register appears at the outputs. When $n\overline{OE}$ is HIGH, the outputs are in high-impedance OFF-state, which means they will neither drive nor load the bus.

2. Features

- 20-bit positive-edge triggered register
- 5 V I/O compatible
- Multiple V_{CC} and GND pins minimize switching noise
- Bus hold data inputs eliminate the need for external pull-up resistors to hold unused inputs
- Live insertion and extraction permitted
- Power-up reset
- Power-up 3-state
- Output capability: +64 mA and -32 mA
- Latch-up protection:
 - ◆ JESD78: exceeds 500 mA
- ESD protection:
 - ◆ MIL STD 883, method 3015: exceeds 2000 V
 - ◆ Machine model: exceeds 200 V

PHILIPS

3. Quick reference data

Table 1: Quick reference data

$GND = 0\text{ V}$; $T_{amb} = 25\text{ }^{\circ}\text{C}$.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{CC} = 2.5\text{ V}$						
t_{PLH}	propagation delay nCP to nQx	$C_L = 50\text{ pF}$	-	2.6	-	ns
t_{PHL}	propagation delay nCP to nQx	$C_L = 50\text{ pF}$	-	2.7	-	ns
C_i	input capacitance	$V_I = 0\text{ V}$ or V_{CC}		3	-	pF
C_o	output capacitance	$V_O = 0\text{ V}$ or V_{CC}		9	-	pF
I_{CC}	supply current	outputs disabled	-	40	-	μA
$V_{CC} = 3.3\text{ V}$						
t_{PLH}	propagation delay nCP to nQx	$C_L = 50\text{ pF}$	-	1.7	-	ns
t_{PHL}	propagation delay nCP to nQx	$C_L = 50\text{ pF}$	-	1.8	-	ns
C_i	input capacitance	$V_I = 0\text{ V}$ or V_{CC}		3	-	pF
C_o	output capacitance	$V_O = 0\text{ V}$ or V_{CC}		9	-	pF
I_{CC}	supply current	outputs disabled	-	70	-	μA

4. Ordering information

Table 2: Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74ALVT16821DL	$-40\text{ }^{\circ}\text{C}$ to $+85\text{ }^{\circ}\text{C}$	SSOP56	plastic shrink small outline package; 56 leads; body width 7.5 mm	SOT371-1
74ALVT16821DGG	$-40\text{ }^{\circ}\text{C}$ to $+85\text{ }^{\circ}\text{C}$	TSSOP56	plastic thin shrink small outline package; 56 leads; body width 6.1 mm	SOT364-1



5. Functional diagram

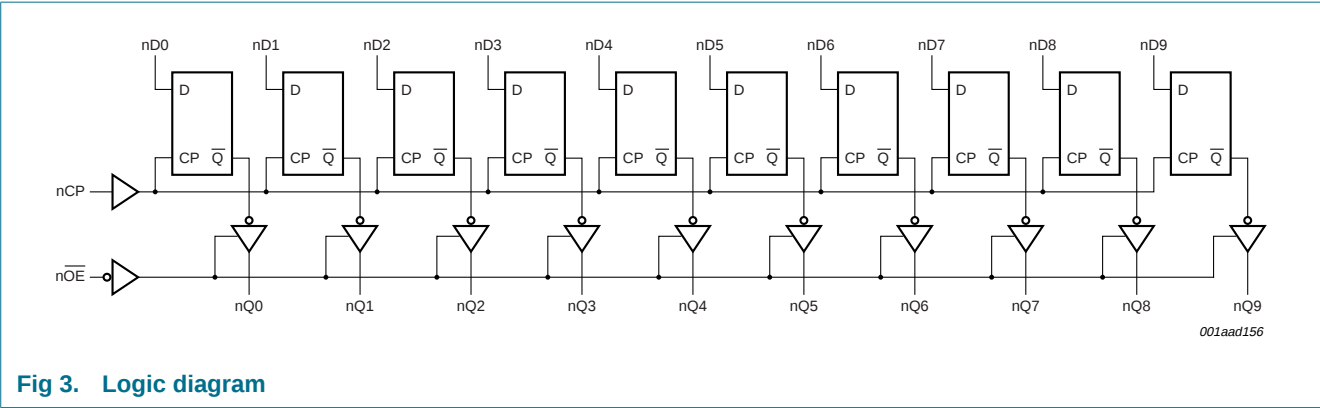
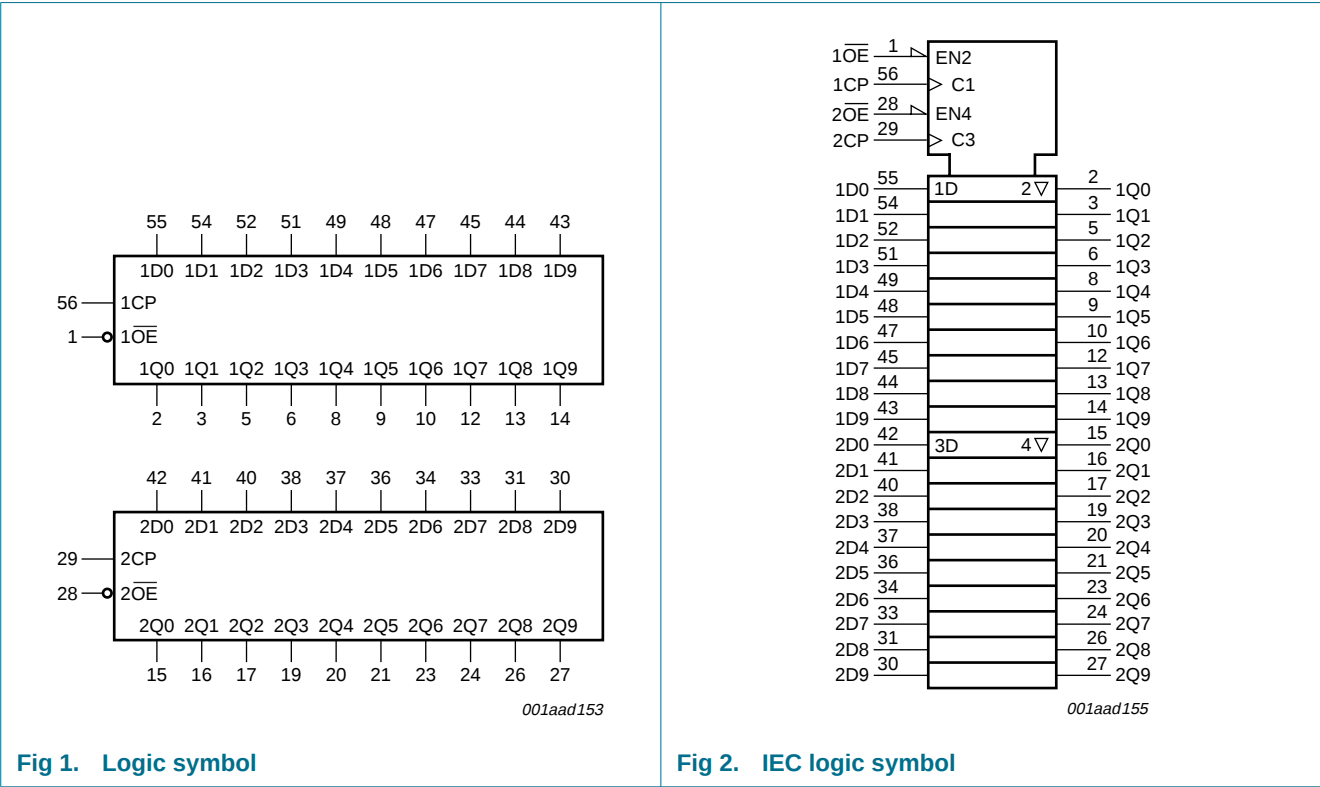
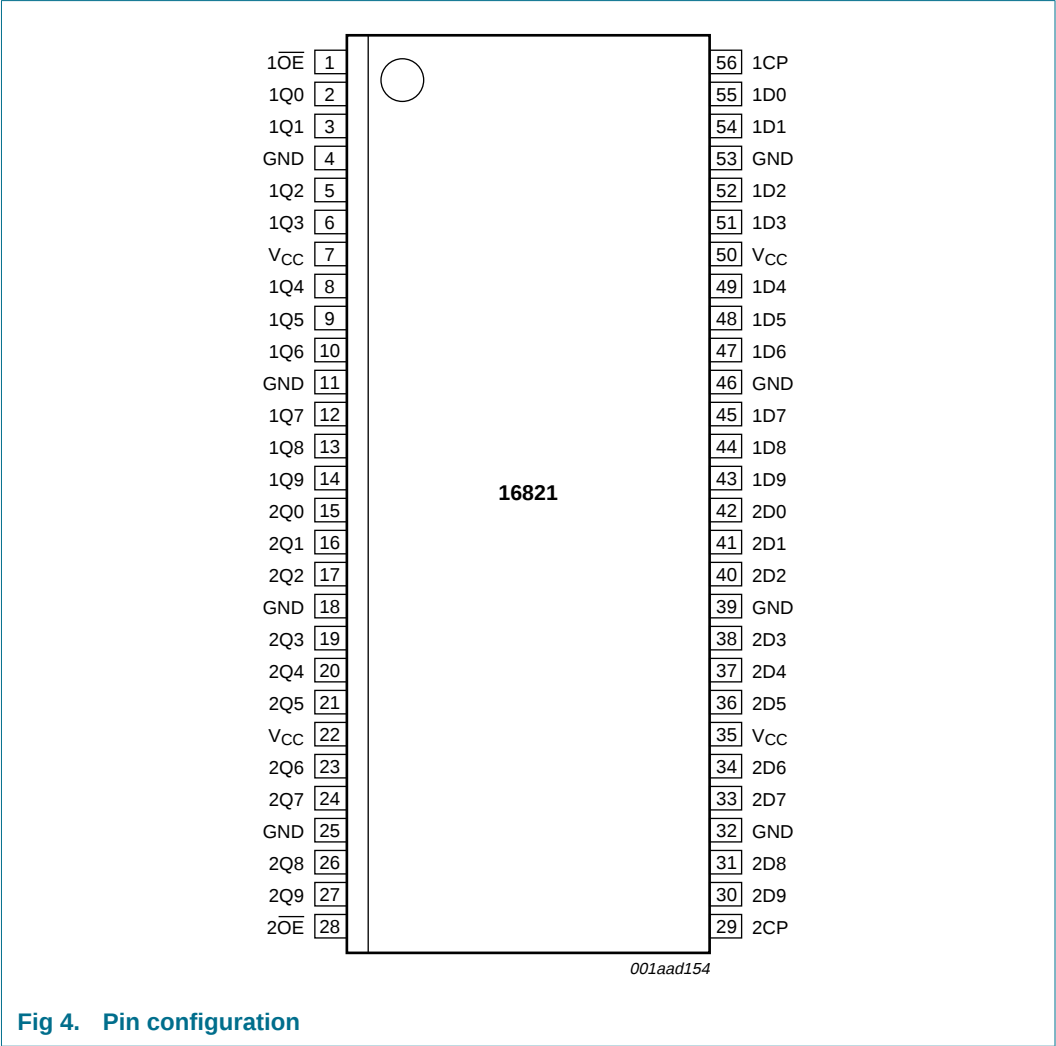


Fig 3. Logic diagram



6. Pinning information

6.1 Pinning



6.2 Pin description

Table 3: Pin description

Symbol	Pin	Description
1OE	1	1 output enable input (active LOW)
1Q0	2	1 data output 0
1Q1	3	1 data output 1
GND	4	ground (0 V)
1Q2	5	1 data output 2
1Q3	6	1 data output 3
VCC	7	supply voltage
1Q4	8	1 data output 4

Table 3: Pin description ...continued

Symbol	Pin	Description
1Q5	9	1 data output 5
1Q6	10	1 data output 6
GND	11	ground (0 V)
1Q7	12	1 data output 7
1Q8	13	1 data output 8
1Q9	14	1 data output 9
2Q0	15	2 data output 0
2Q1	16	2 data output 1
2Q2	17	2 data output 2
GND	18	ground (0 V)
2Q3	19	2 data output 3
2Q4	20	2 data output 4
2Q5	21	2 data output 5
V _{CC}	22	supply voltage
2Q6	23	2 data output 6
2Q7	24	2 data output 7
GND	25	ground (0 V)
2Q8	26	2 data output 8
2Q9	27	2 data output 9
2 $\overline{OE}$	28	2 output enable input (active LOW)
2CP	29	2 clock pulse input (active rising edge)
2D9	30	2 data input 9
2D8	31	2 data input 8
GND	32	ground (0 V)
2D7	33	2 data input 7
2D6	34	2 data input 6
V _{CC}	35	supply voltage
2D5	36	2 data input 5
2D4	37	2 data input 4
2D3	38	2 data input 3
GND	39	ground (0 V)
2D2	40	2 data input 2
2D1	41	2 data input 1
2D0	42	2 data input 0
1D9	43	1 data input 9
1D8	44	1 data input 8
1D7	45	1 data input 7
GND	46	ground (0 V)
1D6	47	1 data input 6
1D5	48	1 data input 5
1D4	49	1 data input 4

Table 3: Pin description ...continued

Symbol	Pin	Description
V _{CC}	50	supply voltage
1D3	51	1 data input 3
1D2	52	1 data input 2
GND	53	ground (0 V)
1D1	54	1 data input 1
1D0	55	1 data input 0
1CP	56	1 clock pulse input (active rising edge)

7. Functional description

7.1 Function table

Table 4: Function table [1]

Operating mode	Input			Internal register	Output nQx
	nOE	nCP	nDx		
Load and read register	L	↑	l	L	L
	L	↑	h	H	H
Hold	L	NC	X	NC	NC
Disable outputs	H	NC	X	NC	Z
	H	↑	Dx	Dx	Z

- [1] H = HIGH voltage level;
 h = HIGH voltage level one set-up time prior to the LOW-to-HIGH clock transition;
 L = LOW voltage level;
 l = LOW voltage level one set-up time prior to the LOW-to-HIGH clock transition;
 NC = no change;
 X = don't care;
 Z = high-impedance OFF-state;
 ↑ = LOW-to-HIGH clock transition.

8. Limiting values

Table 5: Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V _{CC}	supply voltage		−0.5	+4.6	V
V _I	input voltage		[1] −1.2	+7.0	V
V _O	output voltage	output in OFF-state or HIGH-state	[1] −0.5	+7.0	V
I _{IK}	input diode current	V _I < 0 V	-	−50	mA
I _{OK}	output diode current	V _O < 0 V	-	−50	mA

Table 5: Limiting values ...continued

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
I_O	output current	output in LOW-state	-	128	mA
		output in HIGH-state	-	-64	mA
T_{stg}	storage temperature		-65	+150	°C
T_j	junction temperature		[2] -	150	°C

[1] The input and output negative voltage ratings may be exceeded if the input and output clamp current ratings are observed.

[2] The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability.

9. Recommended operating conditions

Table 6: Recommended operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{CC} = 2.5\text{ V}$						
V_{CC}	supply voltage		2.3	-	2.7	V
V_I	input voltage		0	-	5.5	V
V_{IH}	HIGH-level input voltage		1.7	-	-	V
V_{IL}	LOW-level input voltage		-	-	0.7	V
I_{OH}	HIGH-level output current		-	-	-8	mA
I_{OL}	LOW-level output current	none	-	-	8	mA
		current duty cycle $\leq 50\%$; $f \geq 1\text{ kHz}$	-	-	24	mA
$\Delta t/\Delta V$	input transition rise or fall rate	outputs enabled	-	-	10	ns/V
T_{amb}	ambient temperature	free-air	-40	-	+85	°C
$V_{CC} = 3.3\text{ V}$						
V_{CC}	supply voltage		3.0	-	3.6	V
V_I	input voltage		0	-	5.5	V
V_{IH}	HIGH-level input voltage		2.0	-	-	V
V_{IL}	LOW-level input voltage		-	-	0.8	V
I_{OH}	HIGH-level output current		-	-	-32	mA
I_{OL}	LOW-level output current	none	-	-	32	mA
		current duty cycle $\leq 50\%$; $f \geq 1\text{ kHz}$	-	-	64	mA
$\Delta t/\Delta V$	input transition rise or fall rate	outputs enabled	-	-	10	ns/V
T_{amb}	ambient temperature	free-air	-40	-	+85	°C

10. Static characteristics

Table 7: Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

$T_{amb} = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$ [1]						
V_{IK}	input diode voltage	$V_{CC} = 2.3\text{ V}$; $I_{IK} = -18\text{ mA}$	-	-0.85	-1.2	V
V_{OH}	HIGH-level output voltage	$V_{CC} = 2.3\text{ V}$ to 3.6 V ; $I_O = -100\text{ }\mu\text{A}$	$V_{CC} - 0.2$	V_{CC}	-	V
		$V_{CC} = 2.3\text{ V}$; $I_O = -8\text{ mA}$	1.8	2.1	-	V
V_{OL}	LOW-level output voltage	$V_{CC} = 2.3\text{ V}$; $I_O = 100\text{ }\mu\text{A}$	-	0.07	0.2	V
		$V_{CC} = 2.3\text{ V}$; $I_O = 24\text{ mA}$	-	0.3	0.5	V
		$V_{CC} = 2.3\text{ V}$; $I_O = 8\text{ mA}$	-	-	0.4	V
V_{RST}	power-up LOW-state output voltage	$V_{CC} = 2.7\text{ V}$; $I_O = 1\text{ mA}$; $V_I = V_{CC}$ or GND	[2] -	-	0.55	V
I_{LI}	input leakage current					
		control pins	$V_{CC} = 2.7\text{ V}$; $V_I = V_{CC}$ or GND	-	0.1	$\pm 1\text{ }\mu\text{A}$
		I/O data pins	$V_{CC} = 0\text{ V}$ or 2.7 V ; $V_I = 5.5\text{ V}$	[3]	0.1	10 μA
			$V_{CC} = 2.7\text{ V}$; $V_I = V_{CC}$	[3] -	0.1	1 μA
I_{OFF}	power-down leakage current	$V_{CC} = 2.7\text{ V}$; $V_I = 0\text{ V}$	[3] -	+0.1	-5	μA
		$V_{CC} = 0\text{ V}$; V_I or $V_O = 0\text{ V}$ to 4.5 V	-	0.1	± 100	μA
I_{HOLD}	data input bus hold current	$V_{CC} = 2.3\text{ V}$; $V_I = 0.7\text{ V}$	[4] -	90	-	μA
		$V_{CC} = 2.3\text{ V}$; $V_I = 1.7\text{ V}$	[4] -	-10	-	μA
I_{EX}	external current into output	output HIGH-state; $V_O = 5.5\text{ V}$; $V_{CC} = 2.3\text{ V}$	-	10	125	μA
I_{PU}	power-up 3-state output current	$V_{CC} \leq 1.2\text{ V}$; $V_O = 0.5\text{ V}$ to V_{CC} ; $V_I = \text{GND}$ or V_{CC} ; $V_{OE} = \text{don't care}$	[5] -	1	± 100	μA
I_{PD}	power-down 3-state output current	$V_{CC} \leq 1.2\text{ V}$; $V_O = 0.5\text{ V}$ to V_{CC} ; $V_I = \text{GND}$ or V_{CC} ; $V_{OE} = \text{don't care}$	[5] -	1	± 100	μA
I_{OZ}	3-state OFF-state output current	$V_{CC} = 3.6\text{ V}$; $V_I = V_{IL}$ or V_{IH}				
		output HIGH-state; $V_O = 3.0\text{ V}$	-	0.5	5	μA
		output LOW-state; $V_O = 0.5\text{ V}$	-	+0.5	-5	μA
I_{CC}	supply current	$V_{CC} = 3.6\text{ V}$; $V_I = \text{GND}$ or V_{CC} ; $I_O = 0\text{ A}$				
		outputs HIGH-state	-	0.04	0.1	mA
		outputs LOW-state	-	2.3	4.5	mA
		outputs disabled	[6]	0.04	0.1	mA
ΔI_{CC}	additional supply current per input pin	$V_{CC} = 2.3\text{ V}$ to 2.7 V ; one input at $V_{CC} - 0.6\text{ V}$, other inputs at V_{CC} or GND	[7] -	0.04	0.4	mA
C_i	input capacitance	$V_I = 0\text{ V}$ or V_{CC}	-	3	-	pF
C_o	output capacitance	$V_O = 0\text{ V}$ or V_{CC}	-	9	-	pF

Table 7: Static characteristics ...continued

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

 $T_{amb} = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$ [8]						
V_{IK}	input diode voltage	$V_{CC} = 3.0\text{ V}$; $I_{IK} = -18\text{ mA}$	-	-0.85	-1.2	V
V_{OH}	HIGH-level output voltage	$V_{CC} = 3.0\text{ V}$ to 3.6 V ; $I_O = -100\text{ }\mu\text{A}$	$V_{CC} - 0.2$	V_{CC}	-	V
		$V_{CC} = 3.0\text{ V}$; $I_O = -32\text{ mA}$	2.0	2.3	-	V
V_{OL}	LOW-level output voltage	$V_{CC} = 3.0\text{ V}$				
		$I_O = 100\text{ }\mu\text{A}$	-	0.07	0.2	V
		$I_O = 16\text{ mA}$	-	0.25	0.4	V
		$I_O = 32\text{ mA}$	-	0.3	0.5	V
V_{OL}	LOW-level output voltage	$I_O = 64\text{ mA}$	-	0.4	0.55	V
V_{RST}	power-up LOW-state output voltage	$V_{CC} = 3.6\text{ V}$; $I_O = 1\text{ mA}$; $V_I = V_{CC}$ or GND	[2] -	-	0.55	V
I_{LI}	input leakage current					
		control pins	$V_{CC} = 3.6\text{ V}$; $V_I = V_{CC}$ or GND	-	0.1	± 1 μA
		I/O data pins	$V_{CC} = 0\text{ V}$ or 3.6 V ; $V_I = 5.5\text{ V}$	[3] -	0.1	10 μA
			$V_{CC} = 3.6\text{ V}$; $V_I = V_{CC}$	[3] -	0.5	1 μA
I_{LI}	input leakage current		$V_{CC} = 3.6\text{ V}$; $V_I = 0\text{ V}$	[3] -	+0.1	-5 μA
I_{OFF}	power-down leakage current	$V_{CC} = 0\text{ V}$; V_I or $V_O = 0\text{ V}$ to 4.5 V	-	0.1	± 100	μA
I_{HOLD}	data input bus hold current	$V_{CC} = 3\text{ V}$; $V_I = 0.8\text{ V}$	[4] 75	130	-	μA
		$V_{CC} = 3\text{ V}$; $V_I = 2.0\text{ V}$	[4] -75	-140	-	μA
		$V_{CC} = 0\text{ V}$ to 3.6 V ; $V_{CC} = 3.6\text{ V}$	[4] ± 500	-	-	μA
I_{EX}	external current into output	output HIGH-state; $V_O = 5.5\text{ V}$; $V_{CC} = 2.3\text{ V}$	-	10	125	μA
I_{PU}	power-up 3-state output current	$V_{CC} \leq 1.2\text{ V}$; $V_O = 0.5\text{ V}$ to V_{CC} ; $V_I = \text{GND}$ or V_{CC} ; $V_{OE} = \text{don't care}$	[9] -	1	± 100	μA
I_{PD}	power-down 3-state output current	$V_{CC} \leq 1.2\text{ V}$; $V_O = 0.5\text{ V}$ to V_{CC} ; $V_I = \text{GND}$ or V_{CC} ; $V_{OE} = \text{don't care}$	[9] -	1	± 100	μA
I_{OZ}	3-state OFF-state output current	$V_{CC} = 3.6\text{ V}$; $V_I = V_{IL}$ or V_{IH}				
		output HIGH-state; $V_O = 3.0\text{ V}$	-	0.5	5	μA
		output LOW-state; $V_O = 0.5\text{ V}$	-	+0.5	-5	μA
I_{CC}	supply current	$V_{CC} = 3.6\text{ V}$; $V_I = \text{GND}$ or V_{CC} ; $I_O = 0\text{ A}$				
		outputs HIGH-state	-	0.07	0.1	mA
		outputs LOW-state	-	5.1	7	mA
		outputs disabled	[6] -	0.07	0.1	mA
ΔI_{CC}	additional supply current per input pin	$V_{CC} = 3\text{ V}$ to 3.6 V ; one input at $V_{CC} - 0.6\text{ V}$, other inputs at V_{CC} or GND	[7] -	0.04	0.4	mA
C_i	input capacitance	$V_I = 0\text{ V}$ or V_{CC}	-	3	-	pF
C_o	output capacitance	$V_O = 0\text{ V}$ or V_{CC}	-	9	-	pF

[1] All typical values are measured at $V_{CC} = 2.5\text{ V}$ and $T_{amb} = 25^{\circ}\text{C}$.

[2] For valid test results, data must not be loaded into the flip-flops (or latches) after applying power.

[3] Unused pins at V_{CC} or GND.

[4] This is the bus hold overdrive current required to force the input to the opposite logic state.

- [5] This parameter is valid for any V_{CC} between 0 V and 1.2 V with a transition time of up to 10 ms. From $V_{CC} = 1.2$ V to (2.5 ± 0.2) V a transition time of 100 μ s is permitted. This parameter is valid for $T_{amb} = 25$ °C only.
- [6] I_{CC} is measured with outputs pulled up to V_{CC} or pulled down to ground.
- [7] This is the increase in supply current for each input at the specified voltage level other than V_{CC} or GND.
- [8] All typical values are measured at $V_{CC} = 3.3$ V and $T_{amb} = 25$ °C.
- [9] This parameter is valid for any V_{CC} between 0 V and 1.2 V with a transition time of up to 10 ms. From $V_{CC} = 1.2$ V to (3.3 ± 0.3) V a transition time of 100 μ s is permitted. This parameter is valid for $T_{amb} = 25$ °C only.

11. Dynamic characteristics

Table 8: Dynamic characteristics

Voltages are referenced to GND (ground = 0 V); for test circuit see [Figure 9](#).

$T_{amb} = -40$ °C to $+85$ °C.

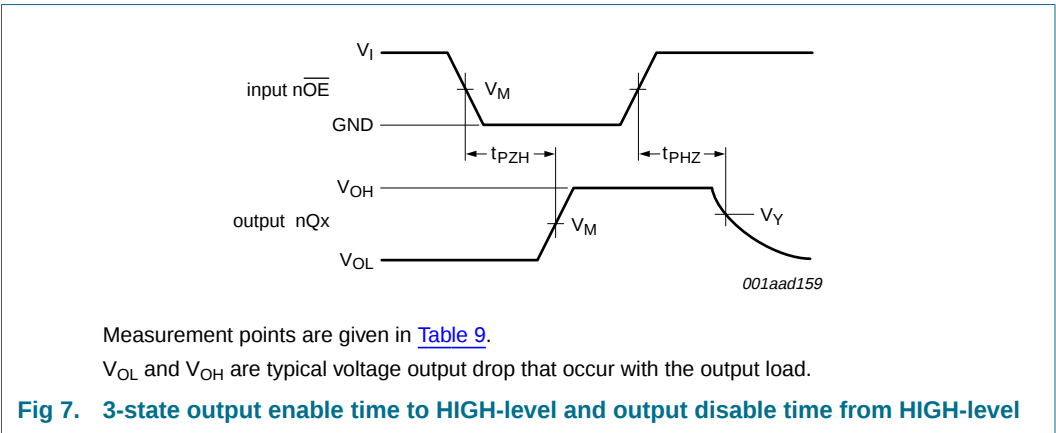
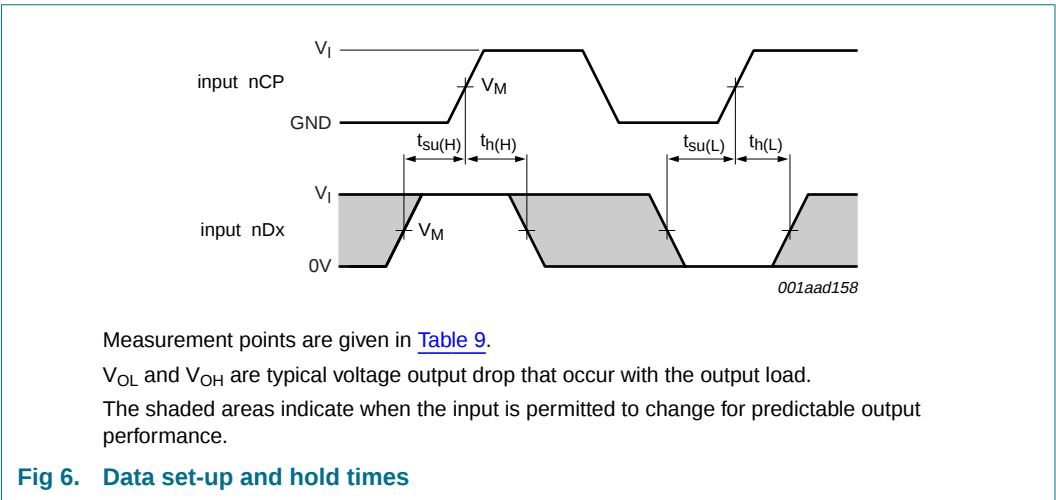
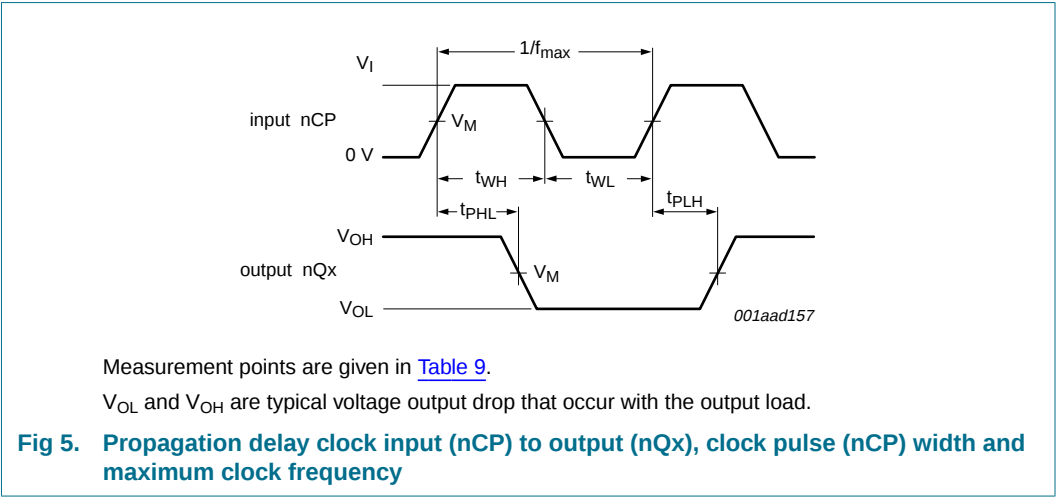
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{CC} = 2.5$ V $\pm$ 0.2 V [1]						
t_{PLH}	propagation delay nCP to nQx	see Figure 5	1.0	2.6	4.0	ns
t_{PHL}	propagation delay nCP to nQx	see Figure 5	1.0	2.7	4.4	ns
t_{PZH}	output enable time $\overline{nOE}$ to nQx	see Figure 7	1.5	2.8	4.6	ns
t_{PZL}	output enable time $\overline{nOE}$ to nQx	see Figure 8	1.0	1.8	4.1	ns
t_{PHZ}	output disable time $\overline{nOE}$ to nQx	see Figure 7	1.5	2.7	4.4	ns
t_{PLZ}	output disable time $\overline{nOE}$ to nQx	see Figure 8	1.0	2.1	3.3	ns
$t_{su(H)}$	set-up time HIGH nDx to nCP	see Figure 6	1.5	0.1	-	ns
$t_{su(L)}$	set-up time LOW nDx to nCP	see Figure 6	2.0	0.5	-	ns
$t_{h(H)}$	hold time HIGH nDx to nCP	see Figure 6	0.3	-0.5	-	ns
$t_{h(L)}$	hold time LOW nDx to nCP	see Figure 6	0.5	-0.1	-	ns
t_{WH}	nCP pulse width HIGH	see Figure 5	1.5	-	-	ns
t_{WL}	nCP pulse width LOW	see Figure 5	1.5	-	-	ns
f_{max}	maximum clock frequency	see Figure 5	150	-	-	MHz
$V_{CC} = 3.3$ V $\pm$ 0.3 V [2]						
t_{PLH}	propagation delay nCP to nQx	see Figure 5	0.5	1.7	3.0	ns
t_{PHL}	propagation delay nCP to nQx	see Figure 5	0.5	1.8	3.2	ns
t_{PZH}	output enable time $\overline{nOE}$ to nQx	see Figure 7	1.0	2.1	3.5	ns
t_{PZL}	output enable time $\overline{nOE}$ to nQx	see Figure 8	0.5	1.4	3.0	ns
t_{PHZ}	output disable time $\overline{nOE}$ to nQx	see Figure 7	1.5	2.9	4.2	ns
t_{PLZ}	output disable time $\overline{nOE}$ to nQx	see Figure 8	1.5	2.4	3.4	ns
$t_{su(H)}$	set-up time HIGH nDx to nCP	see Figure 6	1.5	0.1	-	ns
$t_{su(L)}$	set-up time LOW nDx to nCP	see Figure 6	1.5	0.1	-	ns
$t_{h(H)}$	hold time, HIGH nDx to nCP	see Figure 6	0.5	0.1	-	ns
$t_{h(L)}$	hold time, LOW nDx to nCP	see Figure 6	0.5	0.1	-	ns
t_{WH}	nCP pulse width HIGH	see Figure 5	1.5	-	-	ns
t_{WL}	nCP pulse width LOW	see Figure 5	1.5	-	-	ns
f_{max}	maximum clock frequency	see Figure 5	150	-	-	MHz

[1] All typical values are measured at $V_{CC} = 2.5$ V and $T_{amb} = 25$ °C.

[2] All typical values are measured at $V_{CC} = 3.3$ V and $T_{amb} = 25$ °C.



12. Waveforms



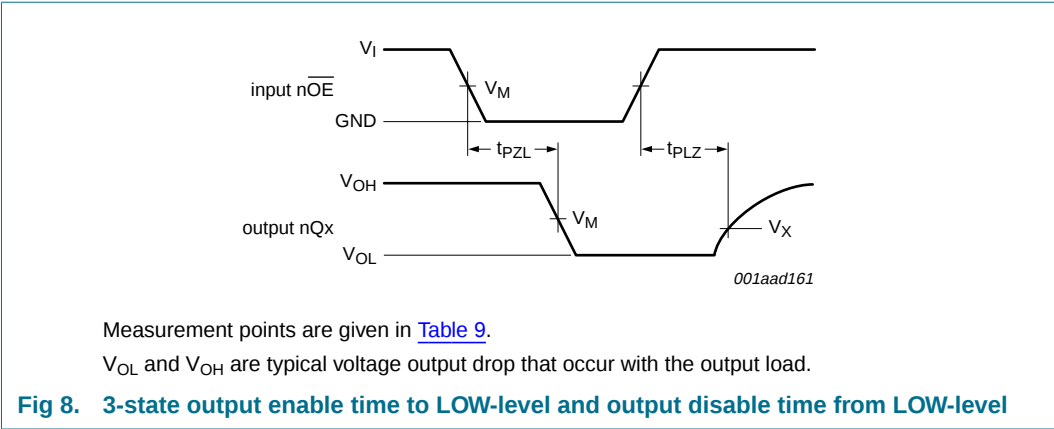
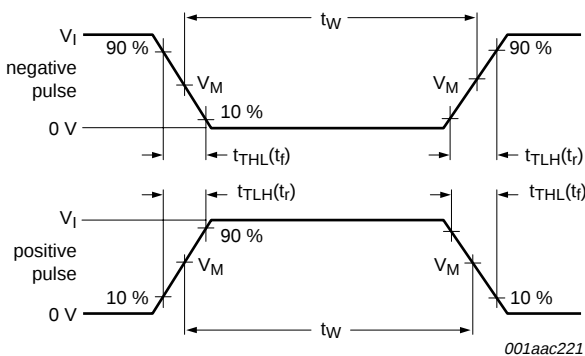


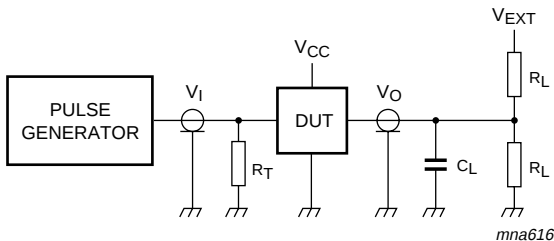
Table 9: Measurement points

Supply voltage	Input	Output		
	V_M	V_M	V_X	V_Y
$\geq 3\text{ V}$	1.5 V	1.5 V	$V_{OL} + 0.3\text{ V}$	$V_{OH} - 0.3\text{ V}$
$\leq 2.7\text{ V}$	$0.5 \times V_{CC}$	$0.5 \times V_{CC}$	$V_{OL} + 0.15\text{ V}$	$V_{OH} - 0.15\text{ V}$



Measurement points are given in [Table 9](#).

a. Input pulse definition



Test data is given in [Table 10](#).

Definitions test circuit:

R_L = Load resistor.

C_L = Load capacitance including jig and probe capacitance.

R_T = Termination resistance should be equal to output impedance Z_o of the pulse generator.

V_{EXT} = Test voltage for switching times.

b. Test circuit

Fig 9. Load circuitry for switching times

Table 10: Test data

Input				Load		V_{EXT}			
V_I	f_i	t_W	t_r, t_f	C_L	R_L	t_{PLZ}, t_{PZL}	t_{PLH}, t_{PHL}	t_{PHZ}, t_{PZH}	
3.0 V or V_{CC} whichever is less	≤ 10 MHz	500 ns	≤ 2.5 ns	50 pF	500 Ω	6 V or $2 \times V_{CC}$	open	GND	

13. Package outline

SSOP56: plastic shrink small outline package; 56 leads; body width 7.5 mm

SOT371-1

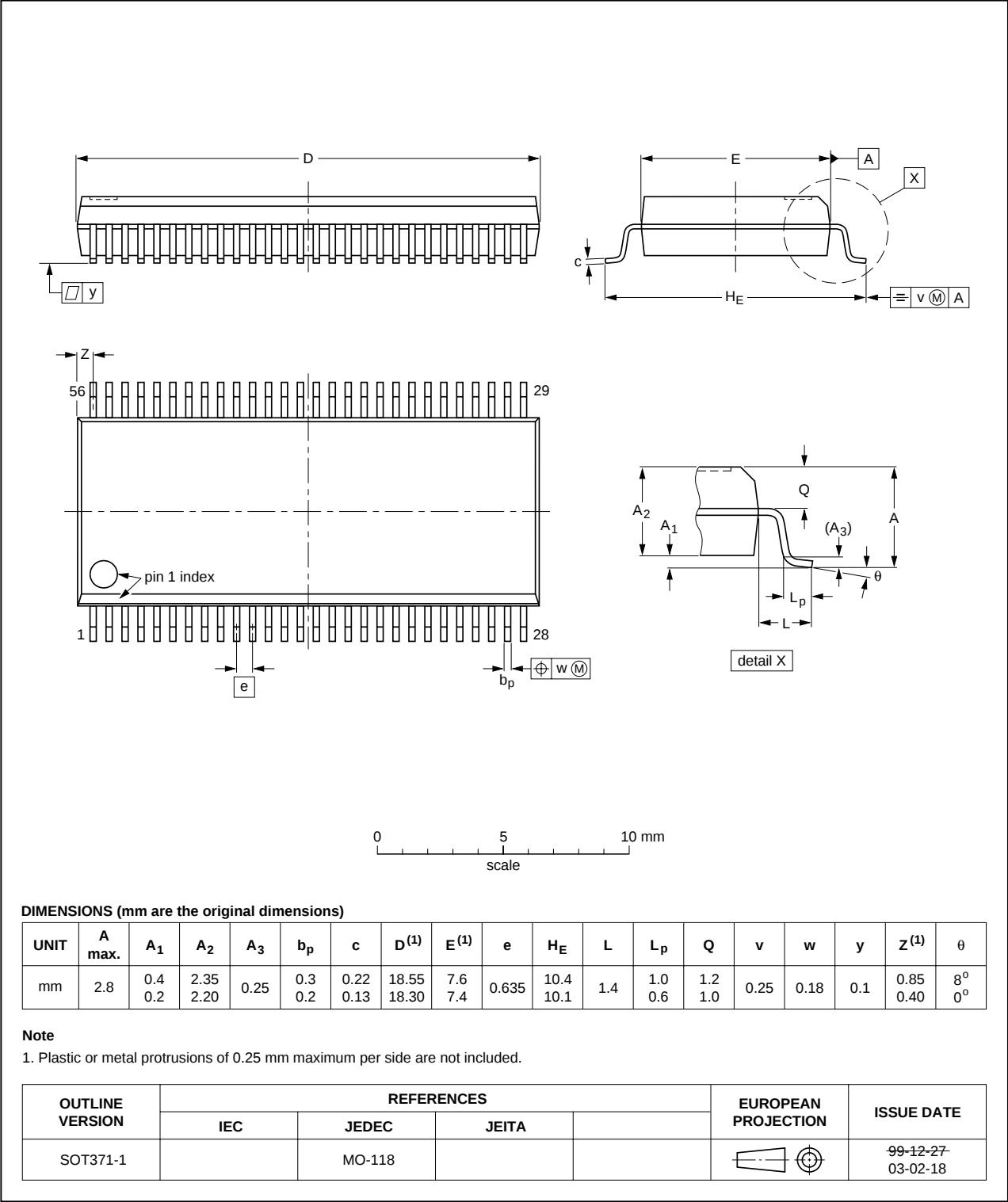


Fig 10. Package outline SOT371-1 (SSOP56)

TSSOP56: plastic thin shrink small outline package; 56 leads; body width 6.1 mm

SOT364-1

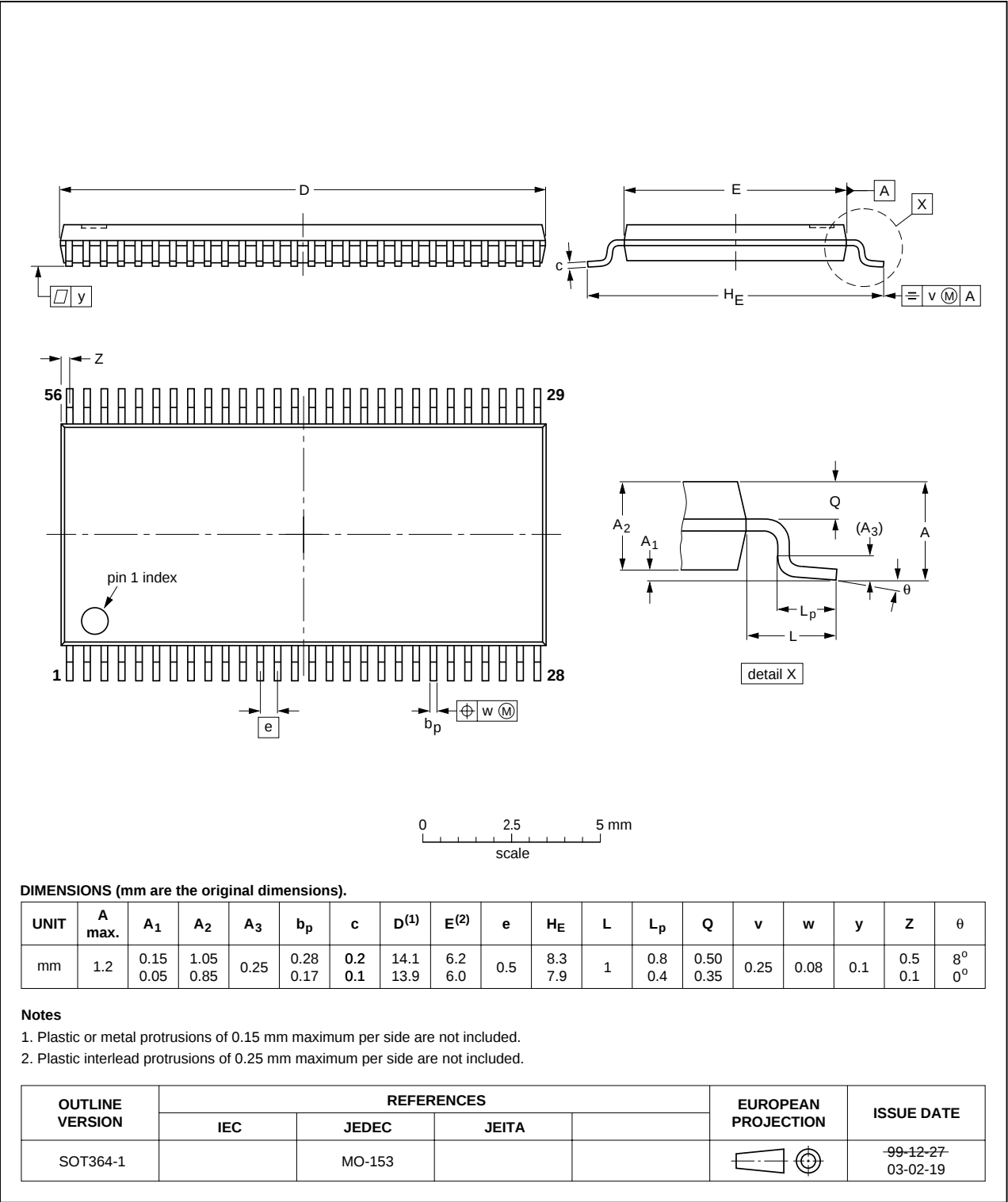


Fig 11. Package outline SOT364-1 (TSSOP56)

14. Revision history

Table 11: Revision history

Document ID	Release date	Data sheet status	Change notice	Doc. number	Supersedes
74ALVT16821_3	20050613	Product data sheet	-	9397 750 15123	74ALVT16821_2
Modifications:					
- The format of this data sheet has been redesigned to comply with the new presentation and information standard of Philips Semiconductors. Section 2: modified 'JEDEC Std 17' into 'JESD78'. Table 8: changed maximum values of propagation delay, output enable time and output disable time.					
74ALVT16821_2	19980213	Product specification		9397 750 03574	74ALVT16821_1
74ALVT16821_1	19970501	Product specification		-	-

15. Data sheet status

Level	Data sheet status ^[1]	Product status ^{[2] [3]}	Definition
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
II	Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
III	Product data	Production	This data sheet contains data from the product specification. Philips Semiconductors reserves the right to make changes at any time in order to improve the design, manufacturing and supply. Relevant changes will be communicated via a Customer Product/Process Change Notification (CPCN).

[1] Please consult the most recently issued data sheet before initiating or completing a design.

[2] The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL <http://www.semiconductors.philips.com>.

[3] For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

16. Definitions

Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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