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Kind regards,

Team Nexperia

74AHC1G79; 74AHCT1G79

Single D-type flip-flop; positive-edge trigger

Rev. 6 — 23 September 2014

Product data sheet

1. General description

74AHC1G79 and 74AHCT1G79 are high-speed Si-gate CMOS devices. They provide a single positive-edge triggered D-type flip-flop.

Information on the data input is transferred to the Q output on the LOW-to-HIGH transition of the clock pulse. The D input must be stable one set-up time prior to the LOW-to-HIGH clock transition for predictable operation.

The AHC device has CMOS input switching levels and supply voltage range 2 V to 5.5 V.

The AHCT device has TTL input switching levels and supply voltage range 4.5 V to 5.5 V.

2. Features and benefits

- Symmetrical output impedance
- High noise immunity
- Low power dissipation
- Balanced propagation delays
- SOT353-1 and SOT753 package options
- ESD protection:
 - ◆ HBM JESD22-A114F: exceeds 2000 V
 - ◆ MM JESD22-A115-A: exceeds 200 V
 - ◆ CDM JESD22-C101C: exceeds 1000 V
- Specified from -40 °C to +125 °C

3. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74AHC1G79GW	-40 °C to +125 °C	TSSOP5	plastic thin shrink small outline package; 5 leads; body width 1.25 mm	SOT353-1
74AHCT1G79GW				
74AHC1G79GV	-40 °C to +125 °C	SC-74A	plastic surface-mounted package; 5 leads	SOT753
74AHCT1G79GV				



4. Marking

Table 2. Marking codes

Type number	Marking ^[1]
74AHC1G79GW	AP
74AHC1G79GV	A79
74AHCT1G79GW	CP
74AHCT1G79GV	C79

[1] The pin 1 indicator is located on the lower left corner of the device, below the marking code.

5. Functional diagram

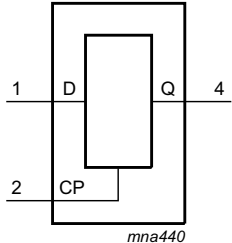


Fig 1. Logic symbol

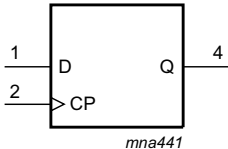


Fig 2. IEC logic symbol

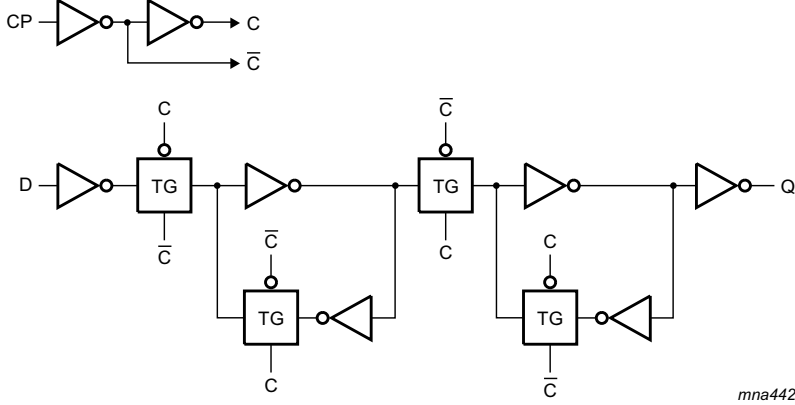
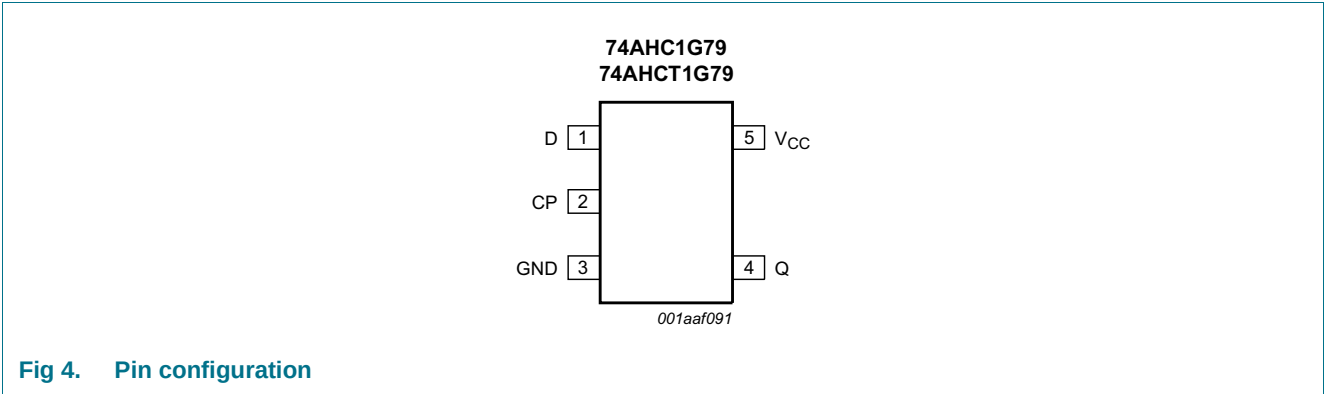


Fig 3. Logic diagram

6. Pinning information

6.1 Pinning



6.2 Pin description

Table 3. Pin description

Symbol	Pin	Description
D	1	data input
CP	2	clock pulse input
GND	3	ground (0 V)
Q	4	data output
V _{CC}	5	supply voltage

7. Functional description

Table 4. Function table^[1]

Inputs		Output
CP	D	Q + 1
↑	L	L
↑	H	H
L	X	Q

[1] H = HIGH voltage level;
L = LOW voltage level;
↑ = LOW-to-HIGH CP transition;
X = don't care;
Q + 1 = state after the next LOW-to-HIGH CP transition.

8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		-0.5	+7.0	V
V_I	input voltage		-0.5	+7.0	V
I_{IK}	input clamping current	$V_I < -0.5$ V	-20	-	mA
I_{OK}	output clamping current	$V_O < -0.5$ V or $V_O > V_{CC} + 0.5$ V [1]	-	±20	mA
I_O	output current	-0.5 V < V_O < $V_{CC} + 0.5$ V	-	±25	mA
I_{CC}	supply current		-	75	mA
I_{GND}	ground current		-75	-	mA
T_{stg}	storage temperature		-65	+150	°C
P_{tot}	total power dissipation	$T_{amb} = -40$ °C to +125 °C [2]	-	250	mW

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] For both TSSOP5 and SC-74A packages: above 87.5 °C the value of P_{tot} derates linearly with 4.0 mW/K.

9. Recommended operating conditions

Table 6. Recommended operating conditions

Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	74AHC1G79			74AHCT1G79			Unit
			Min	Typ	Max	Min	Typ	Max	
V_{CC}	supply voltage		2.0	5.0	5.5	4.5	5.0	5.5	V
V_I	input voltage		0	-	5.5	0	-	5.5	V
V_O	output voltage		0	-	V_{CC}	0	-	V_{CC}	V
T_{amb}	ambient temperature		-40	+25	+125	-40	+25	+125	°C
$\Delta t/\Delta V$	input transition rise and fall rate	$V_{CC} = 3.3$ V ± 0.3 V	-	-	100	-	-	-	ns/V
		$V_{CC} = 5.0$ V ± 0.5 V	-	-	20	-	-	20	ns/V

10. Static characteristics

Table 7. Static characteristics

Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	25 °C			−40 °C to +85 °C		−40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
For type 74AHC1G79										
V _{IH}	HIGH-level input voltage	V _{CC} = 2.0 V	1.5	-	-	1.5	-	1.5	-	V
		V _{CC} = 3.0 V	2.1	-	-	2.1	-	2.1	-	V
		V _{CC} = 5.5 V	3.85	-	-	3.85	-	3.85	-	V
V _{IL}	LOW-level input voltage	V _{CC} = 2.0 V	-	-	0.5	-	0.5	-	0.5	V
		V _{CC} = 3.0 V	-	-	0.9	-	0.9	-	0.9	V
		V _{CC} = 5.5 V	-	-	1.65	-	1.65	-	1.65	V

Table 7. Static characteristics ...continued
 Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	25 °C			–40 °C to +85 °C		–40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
V _{OH}	HIGH-level output voltage	V _I = V _{IH} or V _{IL}								
		I _O = –50 µA; V _{CC} = 2.0 V	1.9	2.0	-	1.9	-	1.9	-	V
		I _O = –50 µA; V _{CC} = 3.0 V	2.9	3.0	-	2.9	-	2.9	-	V
		I _O = –50 µA; V _{CC} = 4.5 V	4.4	4.5	-	4.4	-	4.4	-	V
		I _O = –4.0 mA; V _{CC} = 3.0 V	2.58	-	-	2.48	-	2.40	-	V
		I _O = –8.0 mA; V _{CC} = 4.5 V	3.94	-	-	3.8	-	3.70	-	V
V _{OL}	LOW-level output voltage	V _I = V _{IH} or V _{IL}								
		I _O = 50 µA; V _{CC} = 2.0 V	-	0	0.1	-	0.1	-	0.1	V
		I _O = 50 µA; V _{CC} = 3.0 V	-	0	0.1	-	0.1	-	0.1	V
		I _O = 50 µA; V _{CC} = 4.5 V	-	0	0.1	-	0.1	-	0.1	V
		I _O = 4.0 mA; V _{CC} = 3.0 V	-	-	0.36	-	0.44	-	0.55	V
		I _O = 8.0 mA; V _{CC} = 4.5 V	-	-	0.36	-	0.44	-	0.55	V
I _I	input leakage current	V _I = 5.5 V or GND; V _{CC} = 0 V to 5.5 V	-	-	0.1	-	1.0	-	2.0	µA
I _{CC}	supply current	V _I = V _{CC} or GND; I _O = 0 A; V _{CC} = 5.5 V	-	-	1.0	-	10	-	40	µA
C _I	input capacitance		-	1.5	10	-	10	-	10	pF
For type 74AHCT1G79										
V _{IH}	HIGH-level input voltage	V _{CC} = 4.5 V to 5.5 V	2.0	-	-	2.0	-	2.0	-	V
V _{IL}	LOW-level input voltage	V _{CC} = 4.5 V to 5.5 V	-	-	0.8	-	0.8	-	0.8	V
V _{OH}	HIGH-level output voltage	V _I = V _{IH} or V _{IL} ; V _{CC} = 4.5 V								
		I _O = –50 µA	4.4	4.5	-	4.4	-	4.4	-	V
		I _O = –8.0 mA	3.94	-	-	3.8	-	3.70	-	V
V _{OL}	LOW-level output voltage	V _I = V _{IH} or V _{IL} ; V _{CC} = 4.5 V								
		I _O = 50 µA	-	0	0.1	-	0.1	-	0.1	V
		I _O = 8.0 mA	-	-	0.36	-	0.44	-	0.55	V
I _I	input leakage current	V _I = 5.5 V or GND; V _{CC} = 0 V to 5.5 V	-	-	0.1	-	1.0	-	2.0	µA
I _{CC}	supply current	V _I = V _{CC} or GND; I _O = 0 A; V _{CC} = 5.5 V	-	-	1.0	-	10	-	40	µA
ΔI _{CC}	additional supply current	per input pin; V _I = 3.4 V; other inputs at V _{CC} or GND; I _O = 0 A; V _{CC} = 5.5 V	-	-	1.35	-	1.5	-	1.5	mA
C _I	input capacitance		-	1.5	10	-	10	-	10	pF

11. Dynamic characteristics

Table 8. Dynamic characteristics

$GND = 0\text{ V}$; $t_r = t_f = \leq 3.0\text{ ns}$. For test circuit see [Figure 6](#). For waveforms see [Figure 5](#).

Symbol	Parameter	Conditions	25 °C			−40 °C to +85 °C		−40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
For type 74AHC1G79										
t _{pd}	propagation delay	CP to Q [1]								
		V _{CC} = 3.0 V to 3.6 V [2]								
		C _L = 15 pF	-	4.9	8.4	1.0	9.8	1.0	11.5	ns
		C _L = 50 pF	-	6.9	12.0	1.0	14.0	1.0	15.5	ns
		V _{CC} = 4.5 V to 5.5 V [3]								
		C _L = 15 pF	-	3.5	5.6	1.0	7.0	1.0	8.0	ns
		C _L = 50 pF	-	5.1	8.0	1.0	10.0	1.0	11.0	ns
t _{su}	set-up time	D to CP	3.0	1.0	-	3.0	-	4.0	-	ns
t _h	hold time	D to CP	+2.0	−1.0	-	2.0	-	3.0	-	ns
t _W	pulse width	clock HIGH or LOW	3.0	-	-	3.0	-	4.0	-	ns
f _{max}	maximum frequency		90	-	-	90	-	70	-	MHz
C _{PD}	power dissipation capacitance	per buffer; C _L = 50 pF; f = 1 MHz; V _I = GND to V _{CC} [4]	-	15	-	-	-	-	-	pF
For type 74AHCT1G79										
t _{pd}	propagation delay	CP to Q [1]								
		V _{CC} = 4.5 V to 5.5 V [3]								
		C _L = 15 pF	-	3.5	5.0	1.0	6.0	1.0	8.0	ns
		C _L = 50 pF	-	5.0	8.0	1.0	10.0	1.0	11.0	ns
t _{su}	set-up time	D to CP	3.0	1.0	-	3.0	-	4.0	-	ns
t _h	hold time	D to CP	+2.0	−1.0	-	2.0	-	3.0	-	ns
t _W	pulse width	clock HIGH or LOW	3.0	-	-	3.0	-	4.0	-	ns
f _{max}	maximum frequency		90	-	-	90	-	70	-	MHz
C _{PD}	power dissipation capacitance	per buffer; C _L = 50 pF; f = 1 MHz; V _I = GND to V _{CC} [4]	-	16	-	-	-	-	-	pF

[1] t_{pd} is the same as t_{PLH} and t_{PHL} .

[2] Typical values are measured at $V_{CC} = 3.3\text{ V}$.

[3] Typical values are measured at $V_{CC} = 5.0\text{ V}$.

[4] C_{PD} is used to determine the dynamic power dissipation P_D (μW).

$P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o)$ where:

f_i = input frequency in MHz;

f_o = output frequency in MHz;

C_L = output load capacitance in pF;

V_{CC} = supply voltage in Volts.

12. Waveforms

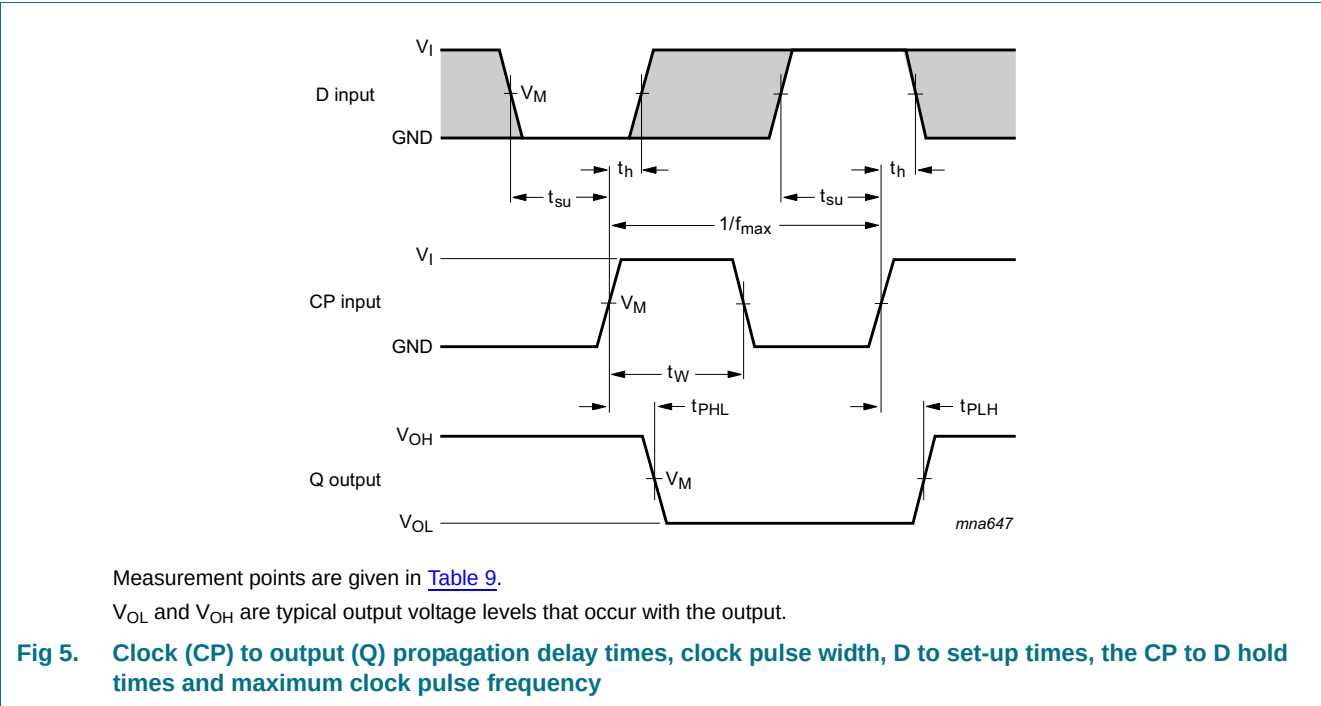
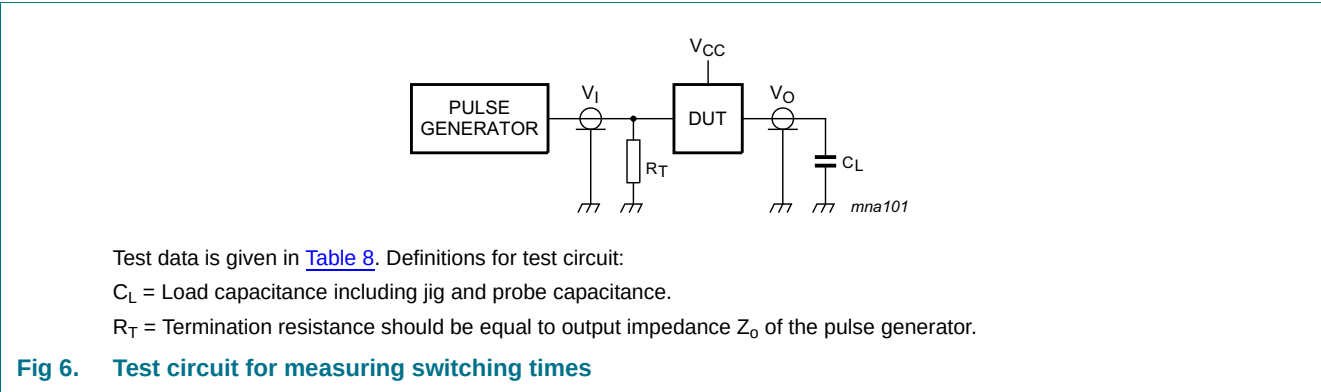


Table 9. Measurement points

Type	Inputs		Output
	V_I	V_M	V_M
74AHC1G79	GND to V_{CC}	$0.5 \times V_{CC}$	$0.5 \times V_{CC}$
74AHCT1G79	GND to 3.0 V	1.5 V	$0.5 \times V_{CC}$



13. Package outline

TSSOP5: plastic thin shrink small outline package; 5 leads; body width 1.25 mm

SOT353-1

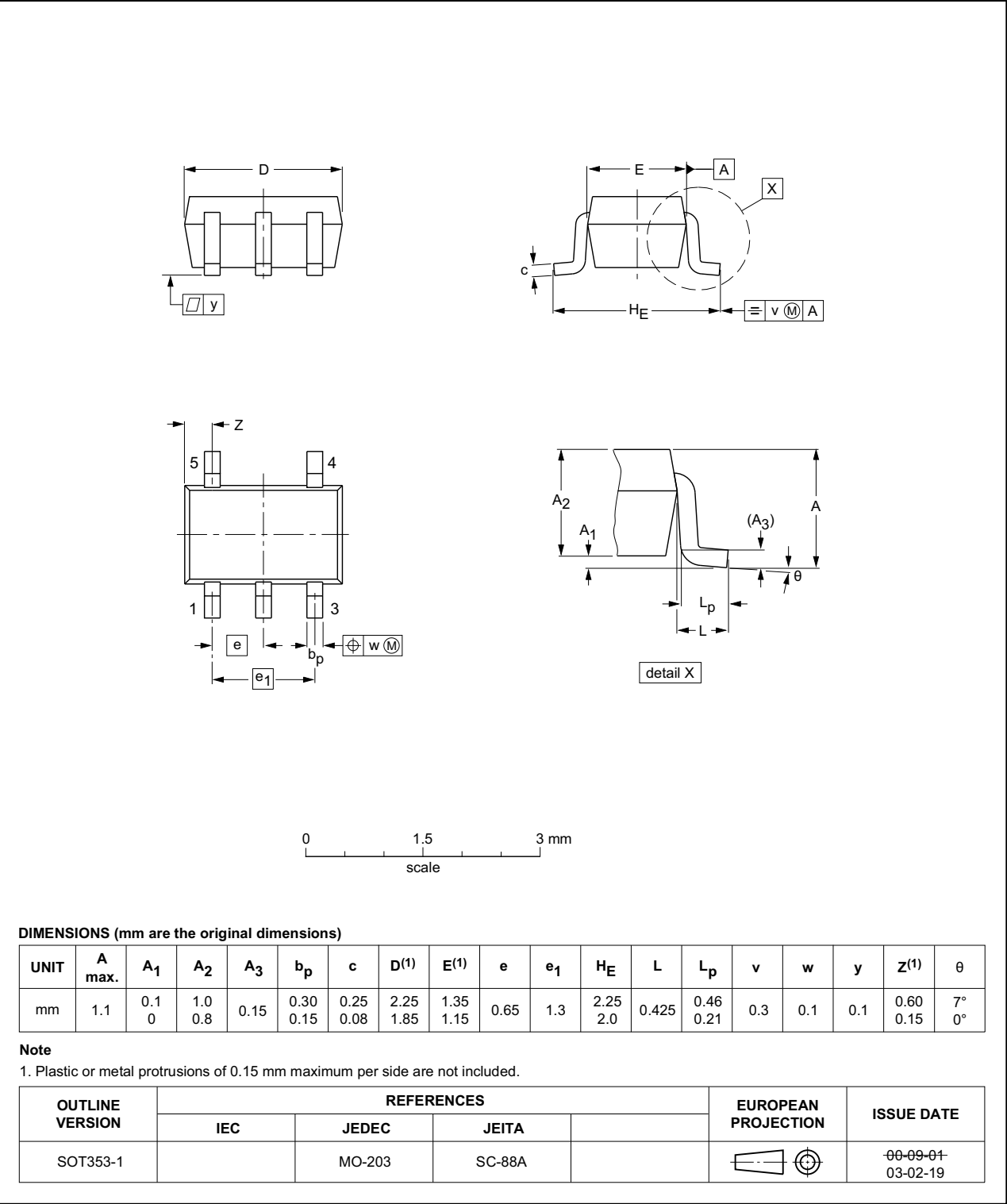


Fig 7. Package outline SOT353-1 (TSSOP5)

Plastic surface-mounted package; 5 leads

SOT753

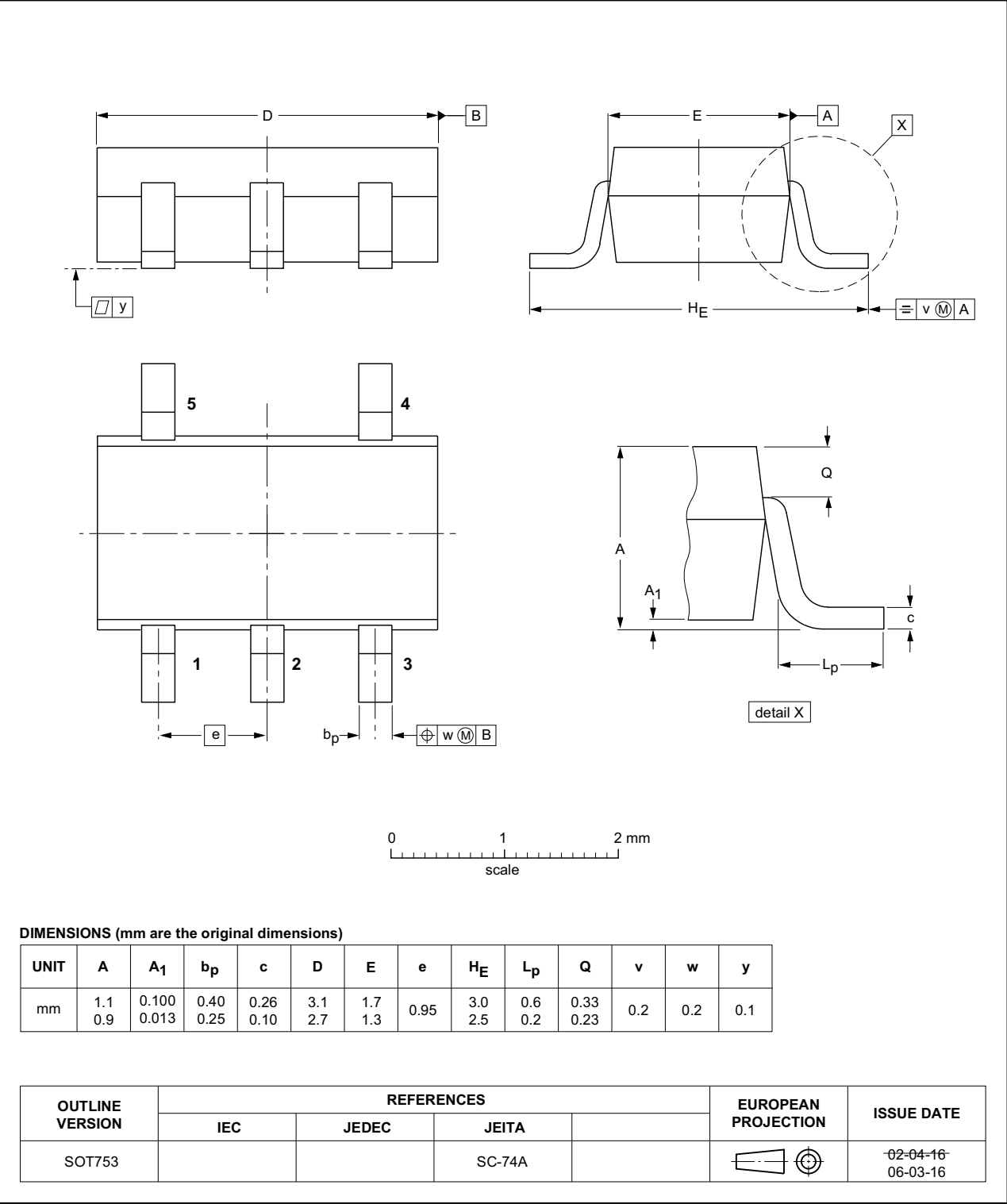


Fig 8. Package outline SOT753 (SC-74A)

14. Abbreviations

Table 10. Abbreviations

Acronym	Description
CDM	Charged Device Model
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model
TTL	Transistor-Transistor Logic

15. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74AHC_AHCT1G79 v.6	20140923	Product data sheet	-	74AHC_AHCT1G79 v.5
Modifications:	• Section 4 : table note added.			
74AHC_AHCT1G79 v.5	20070702	Product data sheet	-	74AHC_AHCT1G79 v.4
74AHC_AHCT1G79 v.4	20020606	Product specification	-	74AHC_AHCT1G79 v.3
74AHC_AHCT1G79 v.3	20020218	Product specification	-	74AHC_AHCT1G79 v.2
74AHC_AHCT1G79 v.2	20010222	Product specification	-	74AHC_AHCT1G79 v.1
74AHC_AHCT1G79 v.1	19990518	Product specification	-	-

16. Legal information

16.1 Data sheet status

Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
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[2] The term 'short data sheet' is explained in section "Definitions".

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