QUALITY SEMICONDUCTOR, INC.

High-Speed CMOS Bus Interface 8-Bit Latches

QS54/74FCT573T
QS54/74FCT2573T

FEATURES/BENEFITS

- Pin and function compatible to the 74F573 74FCT573 and 74FCT573T
- Industrial temperature –40°C to 85°C
- CMOS power levels: <7.5mW static
- Available in DIP, SOIC, QSOP, ZIP, HQSOP
- Undershoot clamp diodes on all inputs
- TTL-compatible input and output levels
- Ground bounce controlled outputs
- Reduced output swing of 0-3.5V
- Military product compliant to MIL-STD-883, Class B

FCT-T 573T

- JEDEC-FCT spec compatible
- Std, A, and C speed grades with 4.2ns t_{PD} for C
- I_{OL} = 48mA Ind., 32mA Mil.

FCT-T 2573T

- Built-in 25Ω series resistor outputs reduce reflection and other system noise
- Std, A, and C speed grades with 4.2ns t_{PD} for C
- I_{OL} = 12mA Ind.

DESCRIPTION

The QSFCT573T and QSFCT2573T are 8-bit high-speed CMOS TTL-compatible buffered latches with three-state outputs that are ideal for driving high capacitance loads such as memory and address buses. The 2573 devices are 25Ω resistor output versions useful for driving transmission lines and reducing system noise. The 2573 series parts can replace the 573 series to reduce noise in an existing design. All inputs have clamp diodes for undershoot noise suppression. All outputs have ground bounce suppression (see QSI Application Note AN-001), and outputs will not load an active bus when V_{CC} is removed from the device.

Figure 1. Functional Block Diagram

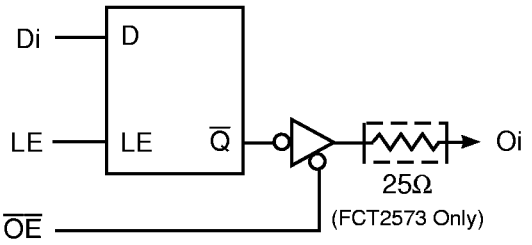
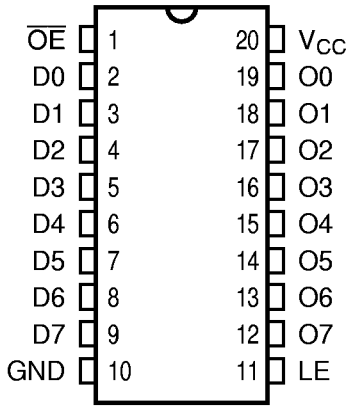


Figure 2. Pin Configurations (All Pins Top View)

PDIP, SOIC, QSOP, HQSOP



ZIP

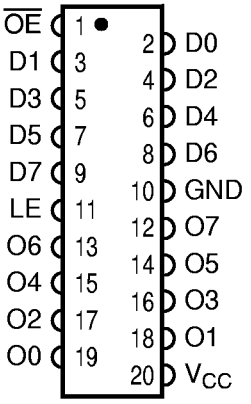


Table 1. Pin Description

Name	I/O	Description
Di	I	Data Inputs
Oi	O	Data Outputs
LE	I	Latch Enable
$\overline{OE}$	I	Output Enable

Table 2. Function Table

Inputs $\overline{OE}$	Inputs LE	Inputs Di	Internal Q Value	Outputs Oi	Function
H	X	X	X	Hi-Z	Disable Outputs
L	L	X	L	L	Enable Outputs
L	L	X	H	H	Enable Outputs
L	H	L	L	L	Pass Inputs
L	H	H	H	H	Pass Inputs
L	L	X	Q	Q	Hold Prior Data

Table 3. Absolute Maximum Ratings

Supply Voltage to Ground	–0.5V to 7.0V
DC Output Voltage V_{OUT}	–0.5V to 7.0V
DC Input Voltage V_{IN}	–0.5V to 7.0V
AC Input Voltage (for a pulse width ≤ 20ns)	–3.0V
DC Input Diode Current with $V_{IN} < 0$	–20mA
DC Output Diode Current with $V_{OUT} < 0$	–50mA
DC Output Current Max. Sink Current/Pin	120mA
Maximum Power Dissipation	0.5 watts
T_{STG} Storage Temperature	–65° to 150°C

Note: Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to QSI devices that result in functional or reliability type failures.

Table 4. Capacitance(1)

T_A = 25°C, f = 1MHz, V_{IN} = 0V, V_{OUT} = 0V

Pins(2)	SOIC	QSOP	PDIP	ZIP	Unit
1-9, 11	4	4	5	7	pF
12-19	6	6	7	9	pF

Notes:
1. Capacitance is characterized but not tested.
2. Pin reference for 20-pin package.

Table 5. Power Supply Characteristics

Symbol	Parameter	Test Conditions(1)	Min	Max	Unit
I_{CC}	Quiescent Power Supply Current	V_{CC} = Max., freq = 0 0V ≤ V_{IN} ≤ 0.2V or V_{CC}-0.2V ≤ V_{IN} ≤ V_{CC}	—	1.5	mA
ΔI_{CC}	Supply Current per Input @ TTL HIGH	V_{CC} = Max., V_{IN} = 3.4V, freq = 0(2)	—	2.0	mA
Q_{CCD}	Supply Current per Input per MHz	V_{CC} = Max., Outputs Open and Enabled One Bit Toggling @ 50% Duty Cycle Other Inputs at GND or V_{CC}(3,4)	—	0.25	mA/ MHz

Notes:
1. For conditions shown as Min. or Max., use the appropriate values specified under DC specifications.
2. Per TTL driven input (V_{IN} = 3.4V).
3. For flip-flops, Q_{CCD} is measured by switching one of the data input pins so that the output changes every clock cycle. This is a measurement of device power consumption only and does not include power to drive load capacitance or tester capacitance. This parameter is guaranteed by design but not tested.
4. I_C can be computed using the above parameters as explained in the Technical Overview section.

Table 6. DC Electrical Characteristics Over Operating Range

Industrial T_A = –40°C to 85°C, V_{CC} = 5.0V ±5% Military T_A = –55°C to 125°C, V_{CC} = 5.0V ±10%

Symbol	Parameter	Test Conditions	Min	Typ(1)	Max	Unit
V_{IH}	Input HIGH Voltage	Logic HIGH for All Inputs	2.0	—	—	V
V_{IL}	Input LOW Voltage	Logic LOW for All Inputs	—	—	0.8	V
ΔV_T	Input Hysteresis	$V_{TLH} - V_{THL}$ for All Inputs	—	0.2	—	V
$\lvert I_{IH} \rvert$ $\lvert I_{IL} \rvert$	Input Current Input HIGH or LOW	V_{CC} = Max., $0 \le V_{IN} < V_{CC}$	—	—	5	µA
$\lvert I_{OZ} \rvert$	Off-State Output Current (Hi-Z)	V_{CC} = Max., $0 \le V_{IN} \le V_{CC}$	—	—	5	µA
I_{OS}	Short Circuit Current (FCT573)	V_{CC} = Max., V_{OUT} = GND(2,3)	–60	—	—	mA
I_{OR}	Current Drive (FCT2573 – 25Ω)	V_{CC} = Min., V_{OUT} = 2.0V(3)	50	—	—	mA
V_{IC}	Input Clamp Voltage	V_{CC} = Min., I_{IN} = –18mA, T_A = 25°C(3)	—	–0.7	–1.2	V
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = –12mA (MIL) I_{OH} = –15mA (IND)	2.4 2.4	— —	— —	V
V_{OL}	Output LOW Voltage (FCT573)	V_{CC} = Min., I_{OL} = 32mA (MIL) I_{OL} = 48mA (IND)	— —	— —	0.50 0.50	V
V_{OL}	Output LOW Voltage (FCT2573 – 25Ω)	V_{CC} = Min., I_{OL} = 12mA (MIL) I_{OL} = 12mA (IND)	— —	— —	0.50 0.50	V
R_{OUT}	Output Resistance (FCT2573 – 25Ω)	V_{CC} = Min., I_{OL} = 12mA (MIL) I_{OL} = 12mA (IND)	— 20	25 28	— 40	Ω

Notes:
1. Typical values indicate V_{CC} = 5.0V and T_A = 25°C.
2. Not more than one output should be shorted and the duration is ≤1 second.
3. These parameters are guaranteed by design but not tested.

Table 7. Switching Characteristics Over Operating Range

Industrial T_A = –40°C to 85°C, V_{CC} = 5.0V ±5% Military T_A = –55°C to 125°C, V_{CC} = 5.0V ±10%
C_{LOAD} = 50pF, R_{LOAD} = 500Ω unless otherwise noted.

Symbol	Description[1]		573 2573 Min	573 2573 Max	573A 2573A Min	573A 2573A Max	573C 2573C Min	573C 2573C Max	Unit
t_{PHL}	Propagation Delay	IND	1.5	8	1.5	5.2	1.5	4.2	ns
t_{PLH}	Data to Oi, 573	MIL	2	8.5	1.5	5.6	1.5	5.1	
t_{PHL}	Propagation Delay	IND	1.5	8	1.5	5.2	1.5	4.2	ns
t_{PLH}	Data to Oi, 2573	MIL	2	8.5	1.5	5.6	1.5	5.1	
t_{PHLE}	Propagation Delay	IND	2	13	2	8.5	2	5.5	ns
t_{PLHE}	LE to Oi, 573	MIL	2	14	2	9.8	2	8	
t_{PHLE}	Propagation Delay	IND	2	13	2	8.5	2	5.5	ns
t_{PLHE}	LE to Oi, 2573	MIL	2	14	2	9.8	2	8	
t_{PZH}	Output Enable Time	IND	1.5	11	1.5	6.5	1.5	5.5	ns
t_{PZL}	$\overline{OE}$ to Yi, 573	MIL	1.5	12.5	1.5	7.5	1.5	6.3	
t_{PZH}	Output Enable Time	IND	1.5	11	1.5	6.5	1.5	6.5	ns
t_{PZL}	$\overline{OE}$ to Yi, 2573	MIL	1.5	12.5	1.5	7.5	1.5	7.5	
t_{PLZ}	Output Disable Time[2]	IND	1.5	7	1.5	5.5	1.5	5.0	ns
t_{PHZ}	$\overline{OE}$ to Yi	MIL	1.5	8.5	1.5	6.5	1.5	5.9	
t_S	Data Setup Time	IND	2		2		2		ns
	Di to LE HIGH to LOW	MIL	2		2				
t_H	Data Hold Time	IND	1.5		1.5		1.5		ns
	Di to LE HIGH to LOW	MIL	1.5		1.5				
t_W	LE Pulse Width[2]	IND	6		5		4		ns
	HIGH to LOW	MIL	6		6				

Notes:
1. Minimums guaranteed but not tested for all parameters except t_S and t_H.
2. This parameter is guaranteed by design but not tested.
3. See Test Circuit and Waveforms.