EVALUATION KIT AVAILABLE

MAX5138/MAX5139

Low-Power, Single, 16-/12-Bit, Buffered Voltage-Output DACs

General Description

The MAX5138/MAX5139 are a family of single-channel pin-compatible and software-compatible 16-bit and 12-bit DACs. The MAX5138/MAX5139 are low-power, 16-bit/12-bit, buffered voltage-output, high-linearity DACs. They use a precision internal reference or a precision external reference for rail-to-rail operation. The MAX5138/MAX5139 accept a wide +2.7V to +5.25V supply-voltage range to accommodate most low-power and low-voltage applications. These devices accept a 3-wire SPI-/QSPI™-/MICROWIRE®-/DSP-compatible serial interface to save board space and reduce the complexity of optically isolated and transformer-isolated applications. The digital interface's double-buffered hardware and software $\overline{LDAC}$ provide simultaneous output update. The serial interface features a $\overline{READY}$ output for easy daisy-chaining of several MAX5138/MAX5139 devices and/or other compatible devices. The MAX5138/MAX5139 include a hardware input to reset the DAC outputs to zero or midscale upon power-up or reset, providing additional safety for applications that drive valves or other transducers that need to be off during power-up. The high linearity of the DACs makes these devices ideal for precision control and instrumentation applications. The MAX5138/MAX5139 are available in an ultra-small (3mm x 3mm), 16-pin TQFN package and are specified over the -40°C to +105°C extended industrial temperature range.

Applications

Automatic Test Equipment

Automatic Tuning

Communication Systems

Data Acquisition

Gain and Offset Adjustment

Portable Instrumentation

Power-Amplifier Control

Process Control and Servo Loops

Programmable Voltage and Current Sources

Functional Diagram and Typical Operating Circuit appear at end of data sheet.

QSPI is a trademark of Motorola Inc.

MICROWIRE is a registered trademark of National Semiconductor Corp.

Features

- **16-/12-Bit Resolution in a 3mm x 3mm, 16-Pin TQFN Package**
- **Hardware-Selectable on Power-Up or Reset-to-Zero/Midscale DAC Output**
- **Double-Buffered Input Registers**
- **$\overline{LDAC}$ Asynchronously Updates DAC Output**
- **$\overline{READY}$ Facilitates Daisy Chaining**
- **High-Performance 10ppm/°C Internal Reference**
- **Guaranteed Monotonic Over All Operating Conditions**
- **Wide +2.7V to +5.25V Supply Range**
- **Rail-to-Rail Buffered Output Operation**
- **Low Gain Error (Less Than ±0.5% FS) and Offset (Less Than ±10mV)**
- **30MHz 3-Wire SPI-/QSPI-/MICROWIRE-/DSP-Compatible Serial Interface**
- **CMOS-Compatible Inputs with Hysteresis**
- **Low Power Consumption (I_{SHDN} = 2µA max)**

Ordering Information

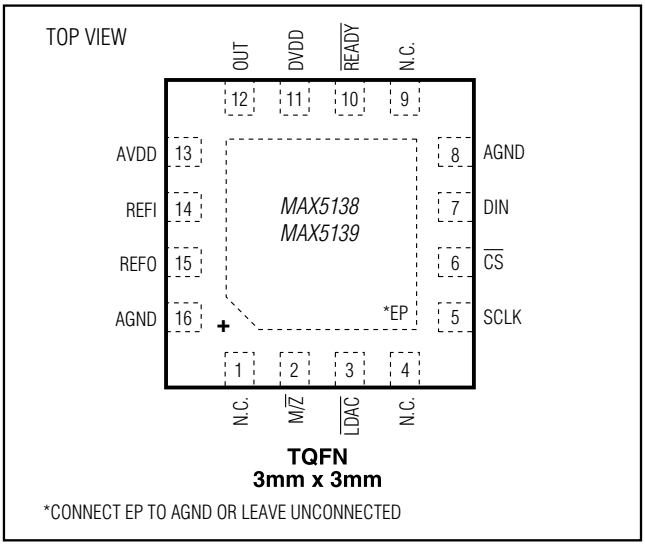
PART	PIN-PACKAGE	RESOLUTION (BITS)
MAX5138BGTE+	16 TQFN-EP*	16
MAX5139GTE+	16 TQFN-EP*	12

Note: *All devices are specified over the -40°C to +105°C operating temperature range.*

+Denotes a lead(Pb)-free/RoHS-compliant package.

**EP = Exposed pad.*

Pin Configuration



TQFN
3mm x 3mm

*CONNECT EP TO AGND OR LEAVE UNCONNECTED

For pricing, delivery, and ordering information, please contact Maxim Direct at 1-888-629-4642, or visit Maxim Integrated's website at www.maximintegrated.com.

19-4428; Rev 2; 10/12

ABSOLUTE MAXIMUM RATINGS

AVDD to AGND .....-0.3V to +6V
DVDD to AGND .....-0.3V to +6V
OUT to AGND.....-0.3V to the lower of (AVDD + 0.3V) and +6V
REFI, REFO, M/$\overline{Z}$ to AGND.....-0.3V to the lower of (AVDD + 0.3V) and +6V
SCLK, DIN, $\overline{CS}$ to AGND.....-0.3V to the lower of (DVDD + 0.3V) and +6V
$\overline{LDAC}$, $\overline{READY}$ to AGND.....-0.3V to the lower of (DVDD + 0.3V) and +6V

Continuous Power Dissipation (T_A = +70°C)
16-Pin TQFN (derate at 14.7mW/°C above +70°C) ..1176.5mW
Maximum Current into Any Input or Output with the Exception of M/$\overline{Z}$ Pin .....±50mA
Maximum Current into M/$\overline{Z}$ Pin .....±5mA
Operating Temperature Range .....-40°C to +105°C
Storage Temperature Range .....-65°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C
Soldering Temperature (reflow) .....+260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{AVDD} = 2.7V to 5.25V, V_{DVDD} = 2.7V to 5.25V, $V_{AVDD} \geq V_{DVDD}$, V_{AGND} = 0V, $V_{REFI} = V_{AVDD}$ - 0.25V, C_{OUT} = 200pF, R_{OUT} = 10kΩ, $T_A = T_{MIN}$ to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
STATIC ACCURACY (Notes 1, 2)							
Resolution	N	MAX5138		16			Bits
		MAX5139		12			
MAX5138 Integral Nonlinearity	INL	V_{REFI} = 5V, V_{AVDD} = 5.25V	(Note 3)	-9	±2	+11	LSB
			T_A = +25°C			±6	
MAX5139 Integral Nonlinearity	INL	V_{REFI} = 5V, V_{AVDD} = 5.25V		-1	±0.25	+1	LSB
Differential Nonlinearity	DNL	Guaranteed monotonic		-1.0		+1.0	LSB
Offset Error	OE	(Note 4)		-10	±1	+10	mV
Offset-Error Drift					±4		µV/°C
Gain Error	GE	(Note 4)		-0.5	±0.2	+0.5	% of FS
Gain Temperature Coefficient					±2		ppm FS/°C
REFERENCE INPUT							
Reference-Input Voltage Range	V_{REFI}	V_{AVDD} = 3V to 5.25V		2		V_{AVDD}	V
		V_{AVDD} = 2.7V to 3V		2		V_{AVDD} - 0.2	
Reference Input Impedance					113		kΩ
INTERNAL REFERENCE							
Reference Voltage	V_{REFO}	T_A = +25°C		2.437	2.440	2.443	V
Reference Temperature Coefficient		(Note 5)			10	25	ppm/°C
Reference Output Impedance					1		Ω
Line Regulation					100		ppm/V
Maximum Capacitive Load	C_R				0.1		nF

ELECTRICAL CHARACTERISTICS (continued)

(V_{AVDD} = 2.7V to 5.25V, V_{DVDD} = 2.7V to 5.25V, $V_{AVDD} \geq V_{DVDD}$, V_{AGND} = 0V, $V_{REFI} = V_{AVDD}$ - 0.25V, C_{OUT} = 200pF, R_{OUT} = 10kΩ, $T_A = T_{MIN}$ to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DAC OUTPUT VOLTAGE (Note 2)						
Output Voltage Range		No load	0.02		V_{AVDD} - 0.02	V
DC Output Impedance				0.1		Ω
Maximum Capacitive Load (Note 5)	C_L	Series resistance = 0Ω		0.2		nF
		Series resistance = 500Ω		15		µF
Resistive Load	R_L		2			kΩ
Short-Circuit Current	I_{SC}	V_{AVDD} = 5.25V		±35		mA
		V_{AVDD} = 2.7V	-40	±20	+40	
Power-Up Time		From power-down mode		25		µs
DIGITAL INPUTS (SCLK, DIN, $\overline{CS}$, $\overline{LDAC}$) (Note 6)						
Input High Voltage	V_{IH}		0.7 x V_{DVDD}			V
Input Low Voltage	V_{IL}				0.3 x V_{DVDD}	V
Input Leakage Current	I_{IN}	V_{IN} = 0V or V_{DVDD}	-1	±0.1	+1	µA
Input Capacitance	C_{IN}				10	pF
DIGITAL OUTPUTS ($\overline{READY}$)						
Output High Voltage	V_{OH}	I_{SOURCE} = 3mA	V_{DVDD} - 0.5			V
Output Low Voltage	V_{OL}	I_{SINK} = 2mA			0.4	V
DYNAMIC PERFORMANCE						
Voltage-Output Slew Rate	SR	Positive and negative		1.25		V/µs
Voltage-Output Settling Time	t_S	1/4 scale to 3/4 scale $V_{REFI} = V_{AVDD}$ = 5V settle to ±2 LSB (Note 5)		5		µs
Digital Feedthrough		Code 0, all digital inputs from 0V to V_{DVDD}		0.5		nV•s
Major Code Transition Analog Glitch Impulse				25		nV•s
Output Noise		10kHz		120		nV/√Hz
Integrated Output Noise		1Hz to 10kHz		18		µV

ELECTRICAL CHARACTERISTICS (continued)

(V_{AVDD} = 2.7V to 5.25V, V_{DVDD} = 2.7V to 5.25V, $V_{AVDD} \geq V_{DVDD}$, V_{AGND} = 0V, $V_{REFI} = V_{AVDD}$ - 0.25V, C_{OUT} = 200pF, R_{OUT} = 10kΩ, $T_A = T_{MIN}$ to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
POWER REQUIREMENTS (Note 7)						
Analog Supply Voltage Range	AVDD		2.7		5.25	V
Digital Supply Voltage Range	DVDD		2.7		V_{AVDD}	V
Supply Current	I_{AVDD}	No load, all digital inputs at 0V or V_{DVDD}		1	1.6	mA
	I_{DVDD}			1	10	µA
Power-Down Supply Current	I_{AVPD}	No load, all digital inputs at 0V or V_{DVDD}		0.2	2	µA
	I_{DVPD}			0.1	2	
TIMING CHARACTERISTICS (Note 8) (Figure 1)						
Serial-Clock Frequency	f_{SCLK}		0		30	MHz
SCLK Pulse-Width High	t_{CH}		13			ns
SCLK Pulse-Width Low	t_{CL}		13			ns
$\overline{CS}$ Fall-to-SCLK Fall Setup Time	t_{CSS}		8			ns
SCLK Fall-to $\overline{CS}$-Rise Hold Time	t_{CSH}		5			ns
DIN-to-SCLK Fall Setup Time	t_{DS}		10			ns
DIN-to-SCLK Fall Hold Time	t_{DH}		2			ns
SCLK Fall to $\overline{READY}$ Transition	t_{SRL}	(Note 9)			30	ns
$\overline{CS}$ Pulse-Width High	t_{CSW}		33			ns
$\overline{LDAC}$ Pulse Width	$t_{LDACPWL}$		33			ns

Note 1: Static accuracy tested without load.
Note 2: Linearity is tested within 20mV of AGND and AVDD, allowing for gain and offset error.
Note 3: Codes above 2047 are guaranteed to be within ±9 LSB.
Note 4: Gain and offset tested within 100mV of AGND and AVDD.
Note 5: Guaranteed by design.
Note 6: Device draws current in excess of the specified supply current when a digital input is driven with a voltage of $V_{VI} < V_{DVDD}$ - 0.6V or $V_{VI} > 0.5V$. At V_{VI} = 2.2V with V_{DVDD} = 5.25V, this current can be as high as 2mA. The SPI inputs are CMOS-input-level compatible. The 30MHz clock frequency cannot be guaranteed for a minimum signal swing.
Note 7: Excess current from AVDD is 10mA when powered without DVDD. Excess current from DVDD is 1mA when powered without AVDD.
Note 8: All timing specifications are with respect to the digital input and output thresholds.
Note 9: Maximum daisy-chain clock frequency is limited to 25MHz.

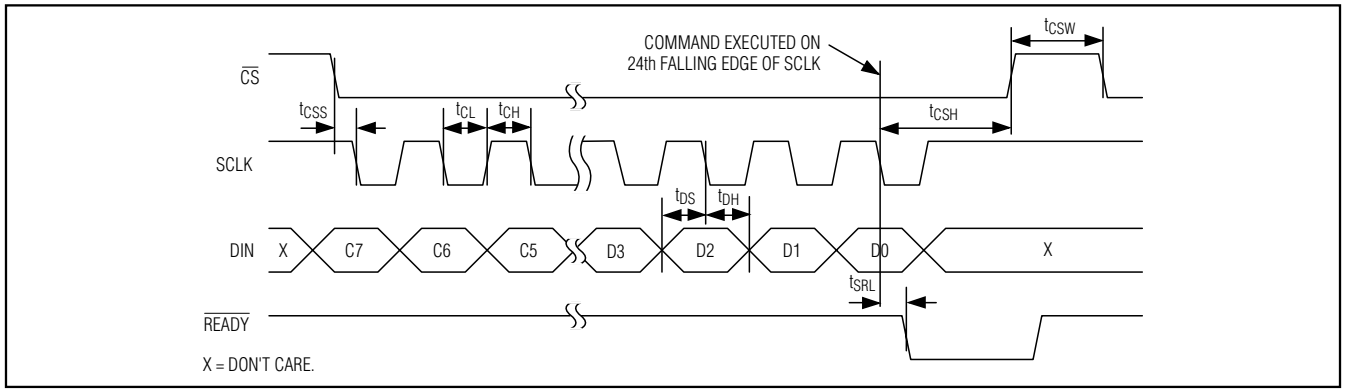
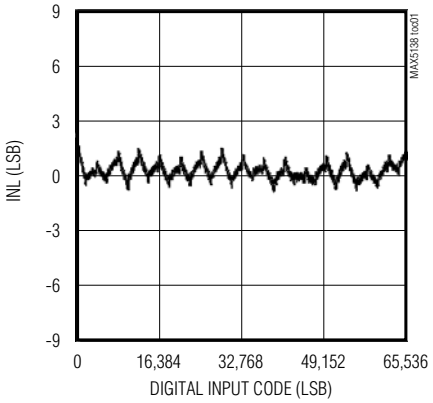


Figure 1. Serial-Interface Timing Diagram

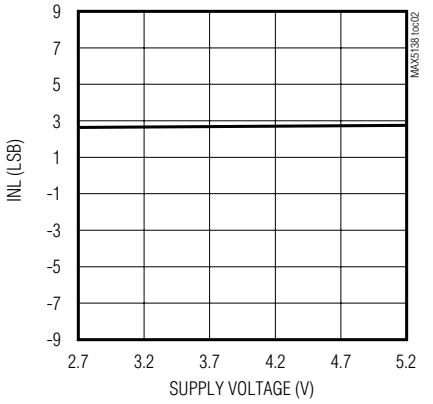
Typical Operating Characteristics

(T_A = +25°C, unless otherwise noted.)

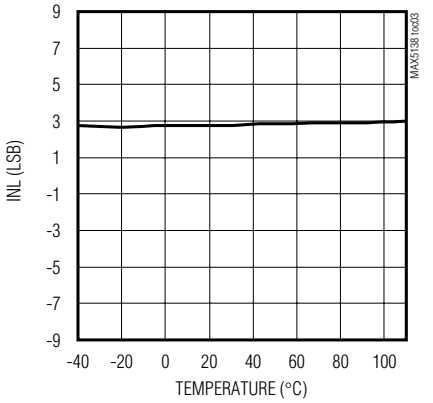
MAX5138 INTEGRAL NONLINEARITY vs. DIGITAL INPUT CODE



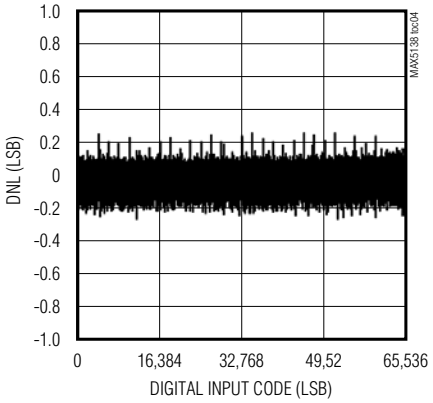
INTEGRAL NONLINEARITY vs. ANALOG SUPPLY VOLTAGE



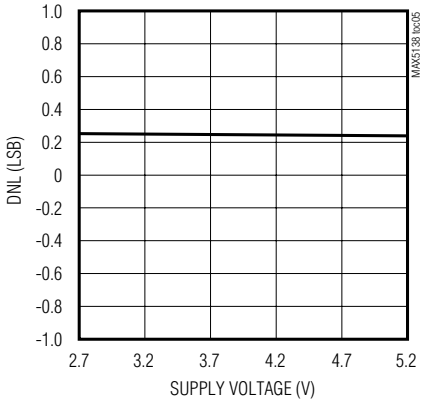
INTEGRAL NONLINEARITY vs. TEMPERATURE



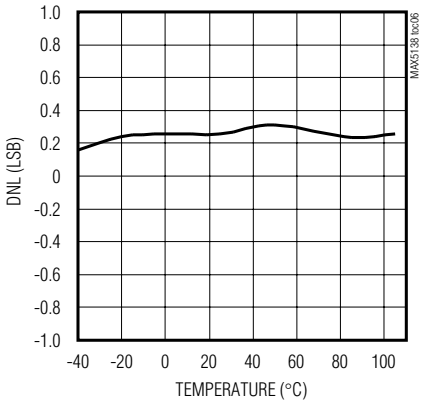
DIFFERENTIAL NONLINEARITY vs. DIGITAL INPUT CODE



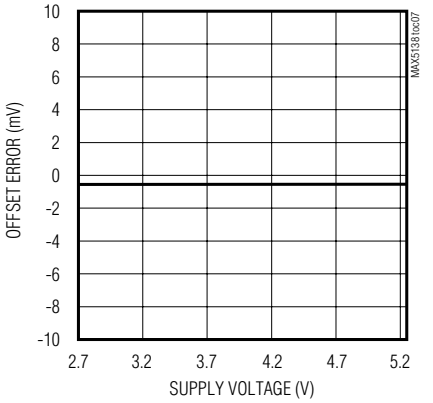
DIFFERENTIAL NONLINEARITY vs. ANALOG SUPPLY VOLTAGE



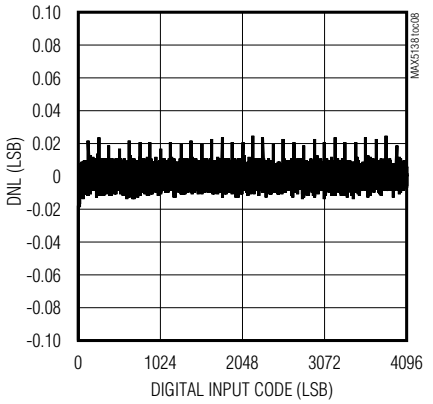
DIFFERENTIAL NONLINEARITY vs. TEMPERATURE



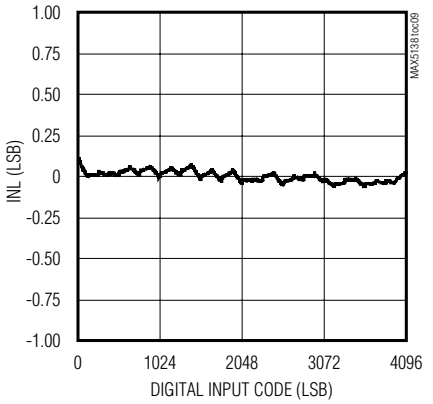
OFFSET ERROR vs. ANALOG SUPPLY VOLTAGE



12-BIT DIFFERENTIAL NONLINEARITY vs. DIGITAL INPUT CODE



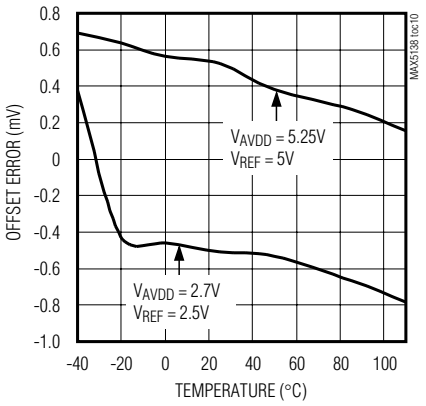
12-BIT INTEGRAL NONLINEARITY vs. DIGITAL INPUT CODE



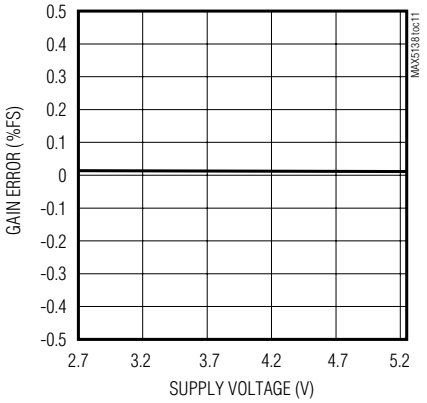
Typical Operating Characteristics (continued)

(T_A = +25°C, unless otherwise noted.)

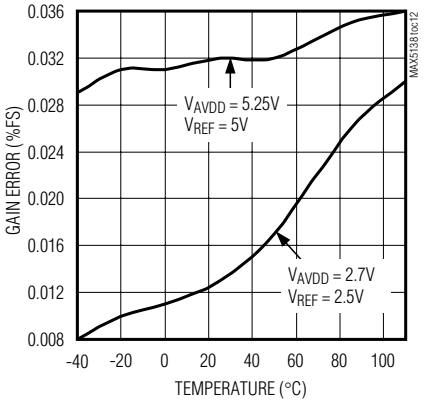
OFFSET ERROR vs. TEMPERATURE



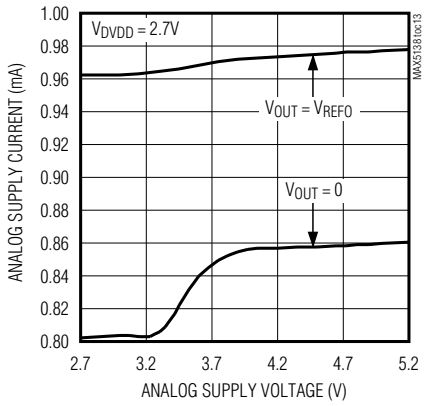
GAIN ERROR vs. ANALOG SUPPLY VOLTAGE



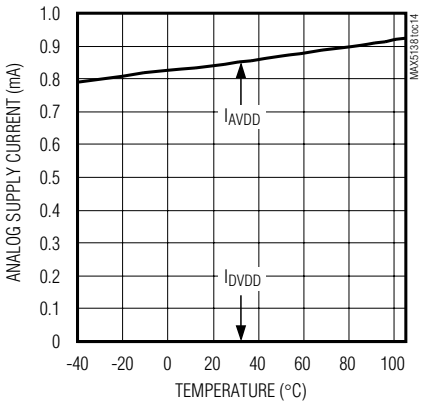
GAIN ERROR vs. TEMPERATURE



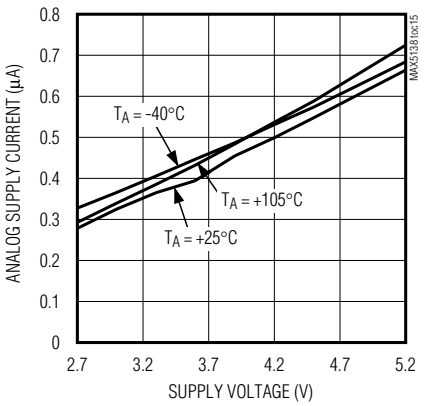
ANALOG SUPPLY CURRENT vs. ANALOG SUPPLY VOLTAGE



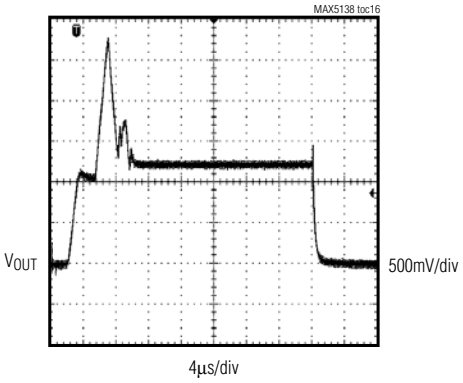
ANALOG SUPPLY CURRENT vs. TEMPERATURE



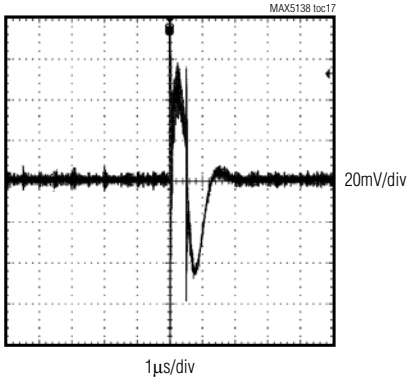
ANALOG SUPPLY CURRENT vs. SUPPLY VOLTAGE (POWER-DOWN MODE)



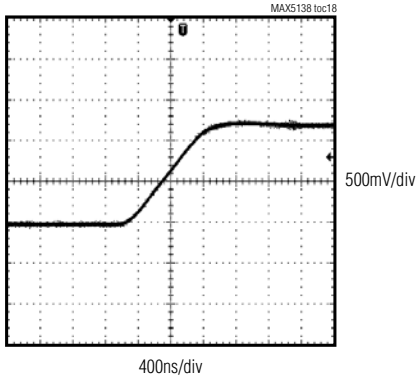
EXITING/ENTERING POWER-DOWN MODE



MAJOR CODE TRANSITION



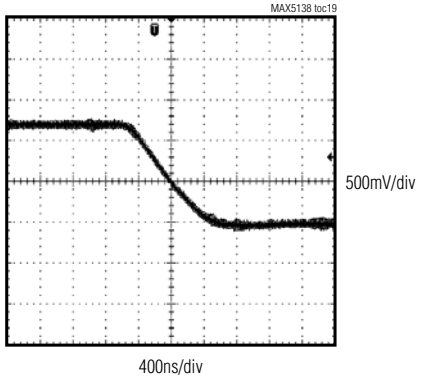
SETTLING TIME UP



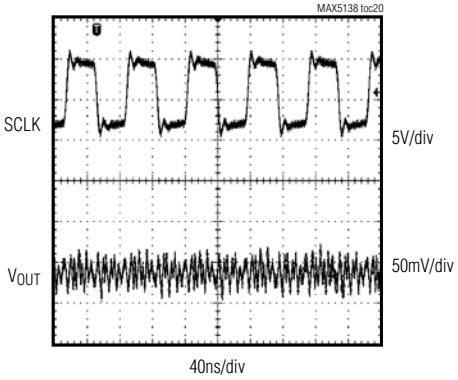
Typical Operating Characteristics (continued)

(T_A = +25°C, unless otherwise noted.)

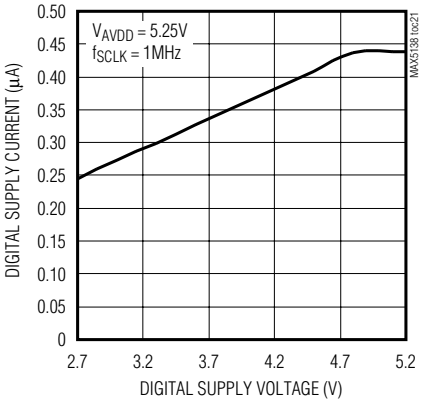
SETTLING TIME DOWN



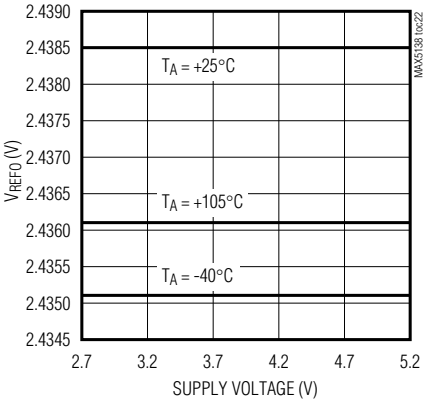
DIGITAL FEEDTHROUGH



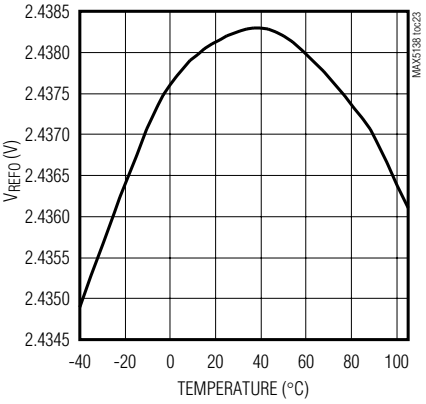
DIGITAL SUPPLY CURRENT vs. DIGITAL SUPPLY VOLTAGE



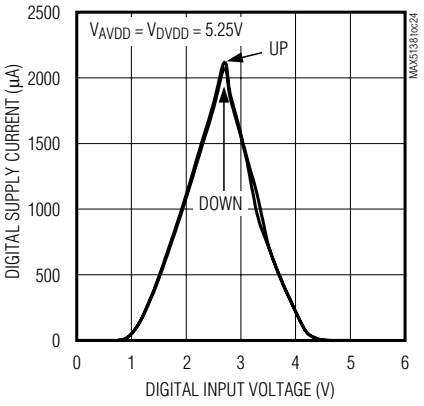
REFERENCE VOLTAGE vs. SUPPLY VOLTAGE



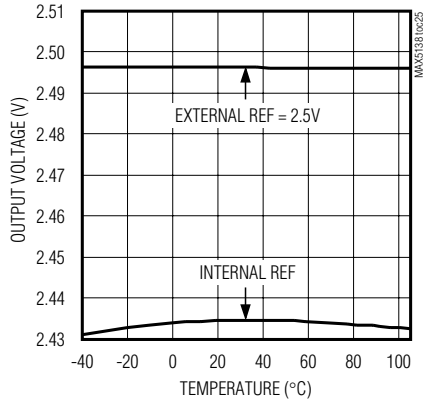
REFERENCE VOLTAGE vs. TEMPERATURE



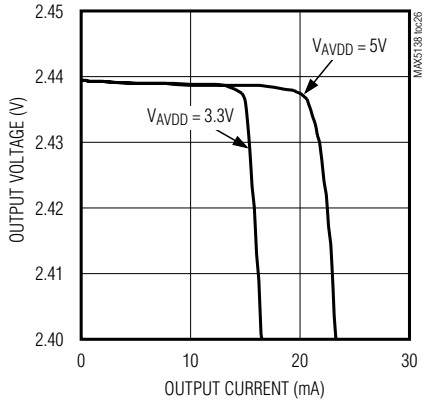
DIGITAL SUPPLY CURRENT vs. DIGITAL INPUT VOLTAGE



FULL-SCALE OUTPUT vs. TEMPERATURE



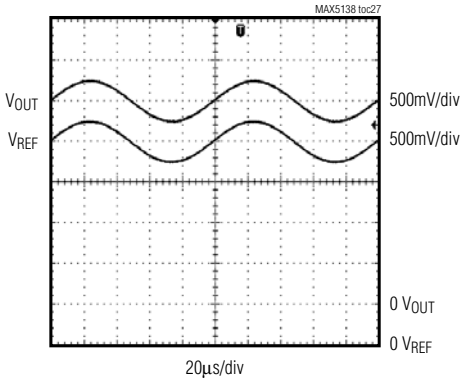
OUTPUT VOLTAGE vs. SUPPLY CURRENT



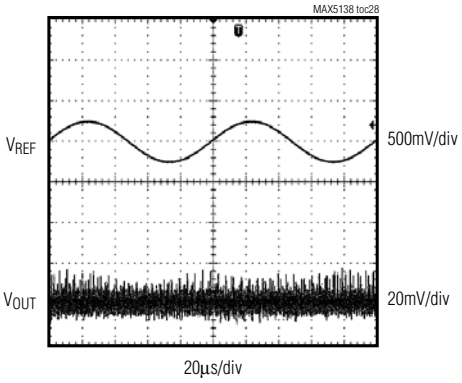
Typical Operating Characteristics (continued)

(T_A = +25°C, unless otherwise noted.)

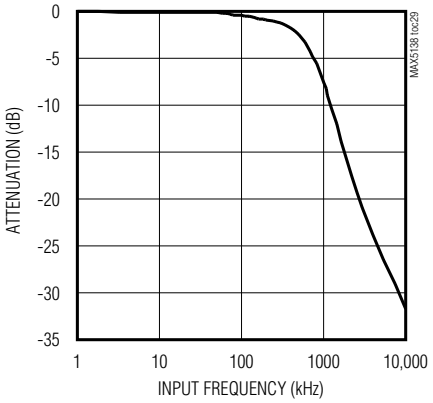
FULL-SCALE REFERENCE FEEDTHROUGH



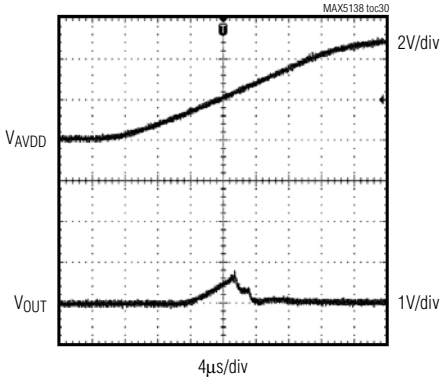
ZERO-SCALE REFERENCE FEEDTHROUGH



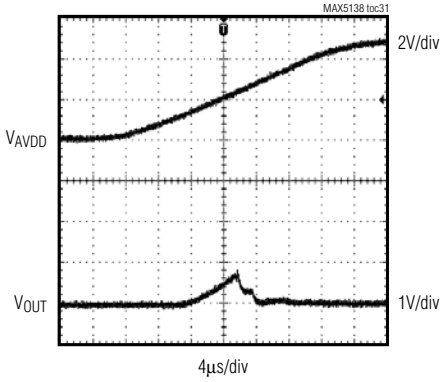
REFERENCE INPUT RESPONSE vs. FREQUENCY



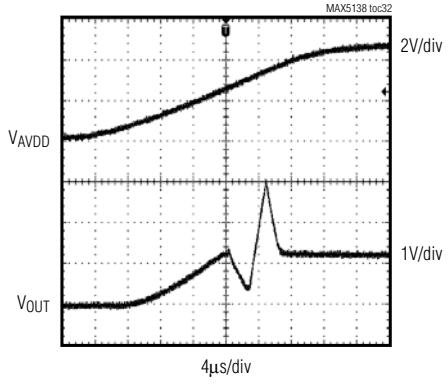
POWER-UP GLITCH, ZERO-SCALE, EXTERNAL REFERENCE



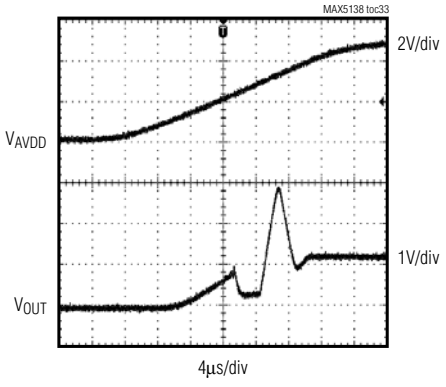
POWER-UP GLITCH, ZERO-SCALE, INTERNAL REFERENCE



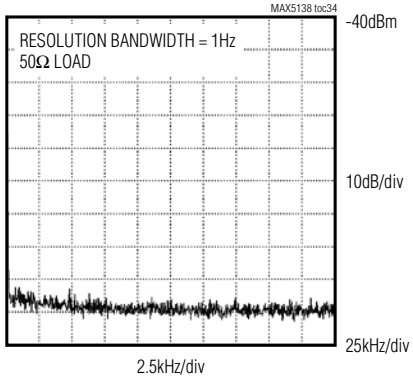
POWER-UP GLITCH, MIDSCALE, EXTERNAL REFERENCE



POWER-UP GLITCH, MIDSCALE, INTERNAL REFERENCE



DC NOISE SPECTRUM, FFT PLOT BUFFERED OUTPUT



Pin Description

PIN	NAME	FUNCTION
1, 4, 9	N.C.	No Connection. Not internally connected.
2	M/$\overline{Z}$	Power-Up Reset Select. Connect M/$\overline{Z}$ low to AGND to power up the DAC output. Connect M/$\overline{Z}$ high to power up the DAC output to midscale.
3	$\overline{LDAC}$	Load DAC. Active-low hardware load DAC input.
5	SCLK	Serial-Clock Input
6	$\overline{CS}$	Active-Low Chip-Select Input
7	DIN	Data In
8	AGND	Analog Ground. Internally connected to AGND. Connect AGND to AGND externally.
10	$\overline{READY}$	Data Output
11	DVDD	Digital Power Supply. Bypass DVDD with a 0.1µF capacitor to AGND.
12	OUT	Buffered DAC Output
13	AVDD	Analog Power Supply. Bypass AVDD with a 0.1µF capacitor to AGND.
14	REFI	Reference Voltage Input. Bypass REFI with a 0.1µF capacitor to AGND.
15	REFO	Reference Voltage Output
16	AGND	DAC Ground. Internally connected to AGND. Connect AGND to AGND externally.
—	EP	Exposed Pad. Not internally connected. Connect EP to AGND or leave unconnected. Not intended as an electrical connection point.

Detailed Description

The MAX5138/MAX5139 are a family of single-channel, pin-compatible and software-compatible, 16-bit and 12-bit DACs. The parts are low-power, buffered voltage-output, high-linearity DACs. The MAX5138/MAX5139 minimize the digital noise feedthrough from input to output by powering down the SCLK and DIN input buffers after completion of each 24-bit serial input. On power-up, the MAX5138/MAX5139 reset the DAC output to zero or midscale, depending on the state of the M/$\overline{Z}$ input, providing additional safety for applications that drive valves or other transducers that need to be off on power-up. The MAX5138/MAX5139 contain a segmented resistor string-type DAC, a serial-in parallel-out shift register, a DAC register, power-on reset (POR) circuit, and control logic. On the falling edge of the clock (SCLK) pulse, the serial input (DIN) data is shifted into the device, MSB first. During power-down, an internal 80kΩ resistor pulls DAC outputs to AGND.

Output Amplifier (OUT)

The MAX5138/MAX5139 include an internal buffer for the DAC output. The internal buffer provides improved load regulation and transition glitch suppression for the DAC output. The output buffer slews at 1.25V/µs and drives up to 2kΩ in parallel with 200pF. The analog supply voltage (AVDD) determines the maximum output voltage range of the device as AVDD powers the output buffer.

DAC Reference

Internal Reference

The MAX5138/MAX5139 feature an internal reference with a nominal +2.44V output. Connect REFO to REFI when using the internal reference. Bypass REFO to AGND with a 47pF (maximum 100pF) capacitor. Alternatively, if heavier decoupling is required, add a 1kΩ resistor in series with a 1µF capacitor in parallel with the existing 100pF capacitor. REFO can deliver up to 100µA of current with no degradation in performance. Configure other reference voltages by applying a resistive potential divider with a total resistance greater than 33kΩ from REFO to AGND.

External Reference

The external reference input features a typical input impedance of 113kΩ and accepts an input voltage from +2V to AVDD. Connect an external voltage supply between REFI and AGND to apply an external reference. Leave REFO unconnected. Visit www.maximintegrated.com/products/references for a list of available external voltage-reference devices.

AVDD as Reference

Connect AVDD to REFI to use AVDD as the reference voltage. Leave REFO unconnected.

Serial Interface

The MAX5138/MAX5139 3-wire serial interface is compatible with MICROWIRE, SPI, QSPI, and DSPs (Figures 2, 3). The interface provides three inputs, SCLK, $\overline{CS}$, and DIN and one output, $\overline{READY}$. Use $\overline{READY}$ to verify communication or to daisy-chain multiple devices (see the *$\overline{READY}$* section). $\overline{READY}$ is capable of driving a 20pF load with a 30ns (max) delay from the falling edge of SCLK. The chip-select input ($\overline{CS}$) frames the serial data loading at DIN. Following a chip-select input's high-to-low transition, the data is shifted synchronously and latched into the input register on each falling edge of the serial-clock input (SCLK). Each serial word is 24 bits. The first 8 bits are the control word followed by 16 data bits (MSB first), as shown in Table 1. The serial input register transfers its contents to the input registers after loading 24 bits of data. To initiate a new data transfer, drive $\overline{CS}$ high and keep $\overline{CS}$ high for a minimum of 33ns before the next write sequence. The SCLK can be either high or low between $\overline{CS}$ write pulses. Figure 1 shows the timing diagram for the complete 3-wire serial-interface transmission.

The MAX5138/MAX5139 digital input is double buffered. Depending on the command issued through the serial interface, the input register can be loaded without affecting the DAC register using the write command. To update the DAC register, either pulse the $\overline{LDAC}$ input low, or use the software $\overline{LDAC}$ command. Use the writethrough commands (see Table 1) to update the DAC output immediately after the data is received. Only use the writethrough command to update the DAC output immediately.

Table 1. Operating Mode Truth Table

24-BIT WORD																		DESC	FUNCTION
CONTROL BITS								DATA BITS											
MSB																	LSB		
C7	C6	C5	C4	C3	C2	C1	C0	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6–D0		
0	0	0	0	0	0	0	0	X	X	X	X	X	X	X	X	X	X	NOP	No operation.
0	0	0	0	0	0	0	1	X	X	X	X	X	X	X	DAC	X	X	LDAC	Set DAC = 1 to move contents of input to DAC register. Setting DAC = 0 results in no operation.
0	0	0	0	0	0	1	0	X	X	X	X	X	X	X	X	X	X	CLR	Software clear.
0	0	0	0	0	0	1	1	X	X	X	X	X	X	X	DAC	READY_EN	X	Power Control	Set DAC = 1 to power down DAC. Set READY_EN = 1 to enable $\overline{READY}$. Setting DAC = 0 results in no operation.
0	0	0	0	0	1	0	1	0	0	0	0	0	0	LIN	0	0	0	Linearity	Optimize DAC linearity.
0	0	0	1	X	X	X	DAC	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	Write	Write to selected input registers (DAC output not affected). Setting DAC = 0 results in no operation.
0	0	1	1	X	X	X	DAC	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	Write-through	Write to selected input and DAC register, DAC output updated (writethrough). Setting DAC = 0 results in no operation.
0	0	1	0	0	0	0	0	X	X	X	X	X	X	X	X	X	X	NOP	No operation.

**For the MAX5139, D3–D0 are X = don't-care bits.*

The MAX5138's DAC code is unipolar binary with V_{OUT} = (code/65536) x V_{REF}. See Table 1 for the serial interface commands.

The MAX5139's DAC code is unipolar with V_{OUT} = (code/4096) x V_{REF}. See Table 1 for the serial interface commands.

Connect the MAX5138/MAX5139 DVDD supply to the supply of the host DSP or microprocessor. The AVDD supply may be set to any voltage within the 2.7V to 5.25V operating range, but must be greater than or equal to the DVDD supply.

Writing to the MAX5138/MAX5139

Write to the MAX5138/MAX5139 using the following sequence:

1) Drive $\overline{CS}$ low, enabling the shift register.
2) Clock 24 bits of data into DIN (C7 first and D0 last), observing the specified setup and hold times. Bits D15–D0 are the data bits that are written to the internal register.
3) After clocking in the last data bit, drive $\overline{CS}$ high. $\overline{CS}$ must remain high for 33ns before the next transmission is started.

Figure 1 shows a write operation for the transmission of 24 bits. If $\overline{CS}$ is driven high at any point prior to receiving 24 bits, the transmission is discarded.

$\overline{READY}$

Connect $\overline{READY}$ to a microcontroller (µC) input to monitor the serial interface for valid communications. The $\overline{READY}$ pulse appears 24 clock cycles after the negative edge of $\overline{CS}$ (Figure 4). Since the MAX5138/MAX5139 look at the first 24 bits of the transmission following the falling edge of $\overline{CS}$, it is possible to daisy chain devices with different command word lengths. $\overline{READY}$ goes high 16ns after $\overline{CS}$ is driven high.

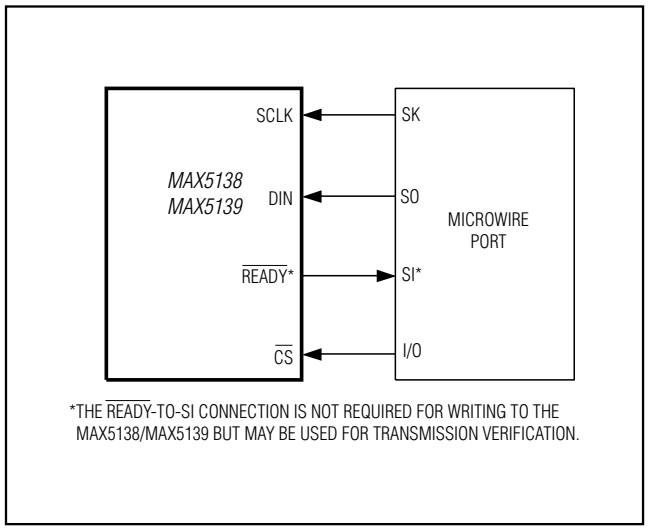


Figure 2. Connections for MICROWIRE

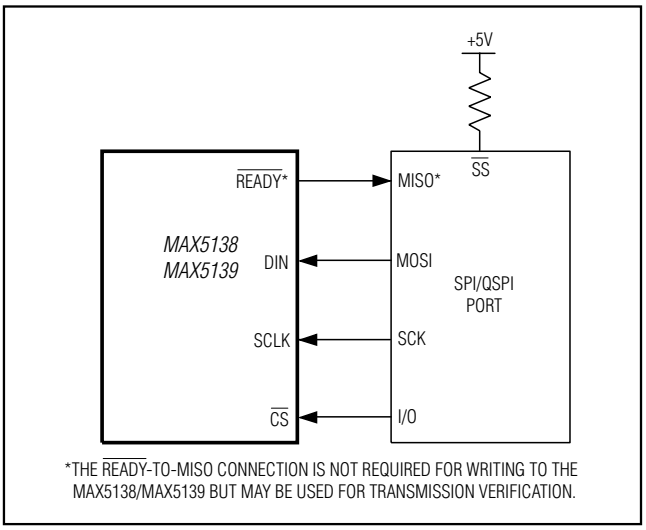


Figure 3. Connections for SPI/QSPI

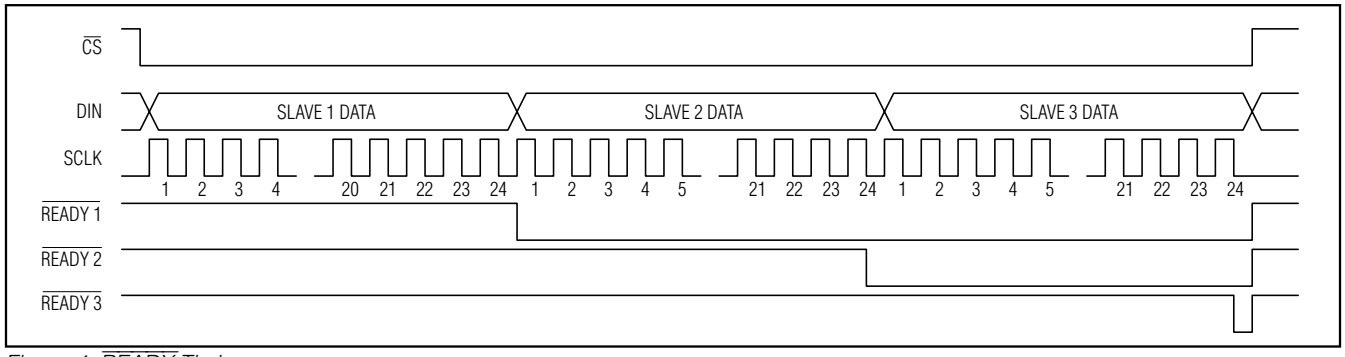


Figure 4. $\overline{READY}$ Timing

Daisy chain multiple MAX5138/MAX5139 devices by connecting the first device conventionally, then connect its READY output to the CS of the following device. Repeat for any other devices in the chain, and drive the SCLK and DIN lines in parallel (Figure 5). When sending commands to daisy-chained MAX5138/MAX5139s, the devices are accessed serially starting with the first device in the chain. The first 24 data bits are read by the first device, the second 24 data bits are read by the second device and so on (Figure 4). Figure 6 shows the configuration when CS is not driven by the µC. These devices can be daisy chained with other compatible devices, such as the MAX5510 and the MAX5511.

To perform a daisy-chain write operation, drive CS low and output the data serially to DIN. The propagation of the READY signal then controls how the data is read by each device. As the data propagates through the daisy chain, each individual command in the chain is executed on the 24th falling clock edge following the falling edge of the respective CS input. To update just one device in a daisy chain, send the no-op command to the other devices in the chain.

If READY is not required, write command 0x03 (power control) and set READY_EN = 0 (see Table 1) to disable the READY output.

Clear Command

The MAX5138/MAX5139 feature a software clear command (0x02). The software clear command acts as a software POR, erasing the contents of all registers. The output returns to the state determined by the M/Z input.

Power-Down Mode

The MAX5138/MAX5139 feature a software-controlled power-down mode. The internal reference and biasing circuits power down to conserve power when powered down. In power-down, the output disconnects from the buffer and is grounded with an internal 80kΩ resistor. The DAC register holds the retained code so that the output is restored when powered up. The serial interface remains active in power-down mode.

Load DAC (LDAC) Input

The MAX5138/MAX5139 feature an active-low LDAC logic input that updates the output. Keep LDAC high during normal operation (when the device is controlled only through the serial interface). Drive LDAC low to update the DAC output with data from the input register. Figure 7 shows the LDAC timing with respect to OUT. Holding LDAC low causes the input register to become transparent and data written to the DAC register to immediately update the DAC output. A software command can also activate the LDAC operation. To activate LDAC by software, set control word 0x01 to load the DAC, and all other data bits to don't care. See Table 1 for the data format. This operation updates the DAC output if it is flagged with a 1. If the DAC output is flagged with a 0 it remains unchanged.

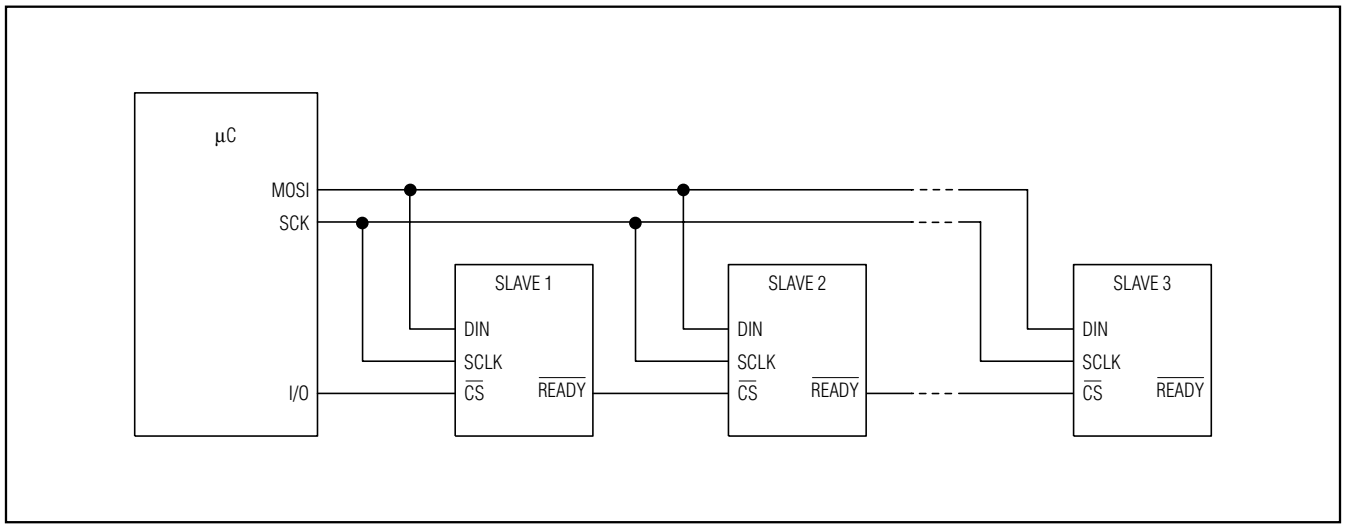


Figure 5. Daisy-Chain Configuration

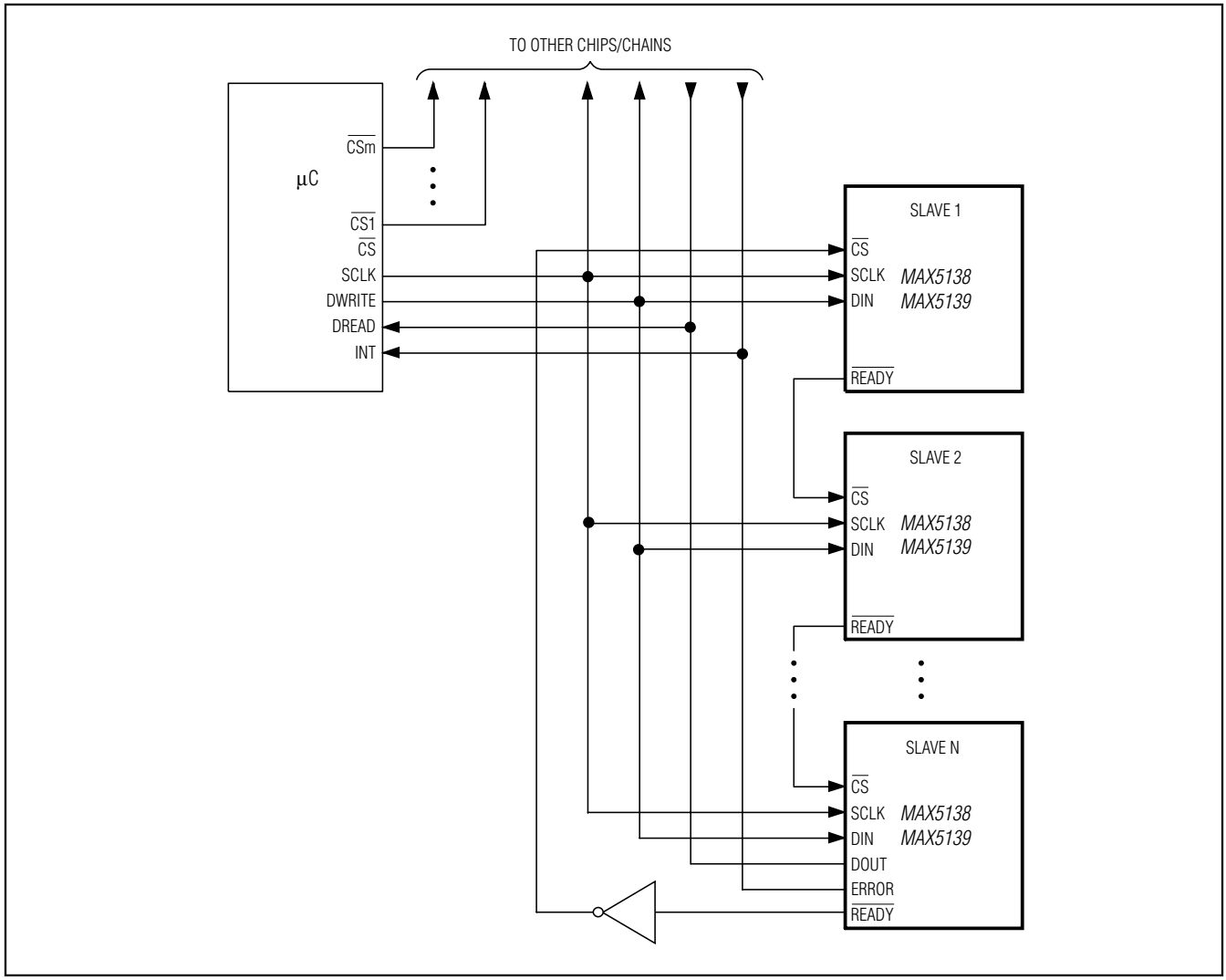


Figure 6. Daisy Chain ($\overline{CS}$ Not Used)

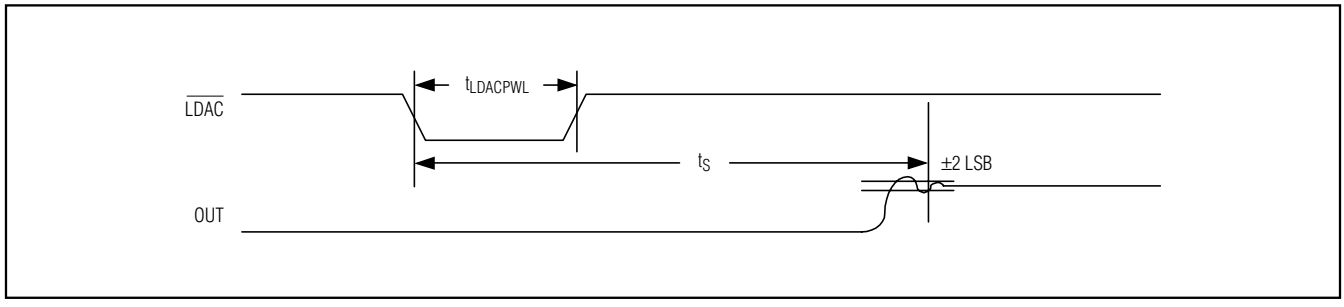


Figure 7. Output Timing

Applications Information

Power-On Reset (POR)

On power-up, the input register is set to zero, and the DAC output powers up to zero or midscale, depending on the configuration of M/$\overline{Z}$. Connect M/$\overline{Z}$ to AGND to power the output to AGND. Connect M/$\overline{Z}$ to AVDD to power the output to midscale.

To guarantee DAC linearity, wait until the supplies have settled. Set the LIN bit in the DAC linearity register; wait 10ms, and clear the LIN bit.

Unipolar Output

The MAX5138/MAX5139 unipolar output voltage range is 0 to V_{REFI}. The output buffer drives a 2kΩ load in parallel with 200pF.

Bipolar Output

Use the MAX5138/MAX5139 in bipolar applications with additional external components (see the *Typical Operating Circuit*).

Power Supplies and Bypassing Considerations

For best performance, use a separate supply for the MAX5138/MAX5139. Bypass both DVDD and AVDD with high-quality ceramic capacitors to a low-impedance ground as close as possible to the device. Minimize lead lengths to reduce lead inductance. Connect both MAX5138/MAX5139 AGND inputs to the analog ground plane.

Layout Considerations

Digital and AC transient signals on AGND inputs can create noise at the outputs. Connect both AGND inputs to form the star ground for the DAC system. Refer remote DAC loads to this system ground for the best possible performance. Use proper grounding techniques, such as a multilayer board with a low-inductance ground plane, or star connect all ground return paths back to the MAX5138/MAX5139 AGND. Do not use wire-wrapped boards and sockets. Use shielding to improve noise immunity. Do not run analog and digital signals parallel to one another (especially clock signals) and avoid routing digital lines underneath the MAX5138/MAX5139 package.

Definitions

Integral Nonlinearity (INL)

INL is the deviation of the measured transfer function from a best fit straight line drawn between two codes. This best fit line for the MAX5138 is a line drawn between codes 3072 and 64,512 of the transfer function and the best fit line for the MAX5139 is a line drawn between codes 192 and 4032 of the transfer function, once offset and gain errors have been nullified.

Differential Nonlinearity (DNL)

DNL is the difference between an actual step height and the ideal value of 1 LSB. If the magnitude of the DNL is greater than -1 LSB, the DAC guarantees no missing codes and is monotonic.

Table 2. MAX5138 Input Code vs. Output Voltage

DAC LATCH CONTENTS MSB LSB	ANALOG OUTPUT, V_{OUT}
1111 1111 1111 1111	V_{REF} x (65,535/65,536)
1000 0000 0000 0000	V_{REF} x (32,768/65,536) = 1/2 V_{REF}
0000 0000 0000 0001	V_{REF} x (1/65,536)
0000 0000 0000 0000	0

Table 3. MAX5139 Input Code vs. Output Voltage

DAC LATCH CONTENTS MSB			LSB	ANALOG OUTPUT, V_{OUT}
1111	1111	1111	XXX	V_{REF} x (4095/4096)
1000	0000	0000	XXX	V_{REF} x (2048/4096)
0000	0000	0001	XXX	V_{REF} x (1/4096)
0000	0000	0000	XXX	0

Offset Error

Offset error indicates how well the actual transfer function matches the ideal transfer function at a single point. Typically, the point at which the offset error is specified is at or near the zero-scale point of the transfer function.

Gain Error

Gain error is the difference between the ideal and the actual full-scale output voltage on the transfer curve, after nullifying the offset error. This error alters the slope of the transfer function and corresponds to the same percentage error in each step.

Settling Time

The settling time is the amount of time required from the start of a transition, until the DAC output settles to the new output value within the converter's specified accuracy.

Digital Feedthrough

Digital feedthrough is the amount of noise that appears on the DAC output when the DAC digital control lines are toggled.

Digital-to-Analog Glitch Impulse

A major carry transition occurs at the midscale point where the MSB changes from low to high and all other bits change from high to low, or where the MSB changes from high to low and all other bits change from low to high. The duration of the magnitude of the switching glitch during a major carry transition is referred to as the digital-to-analog glitch impulse.

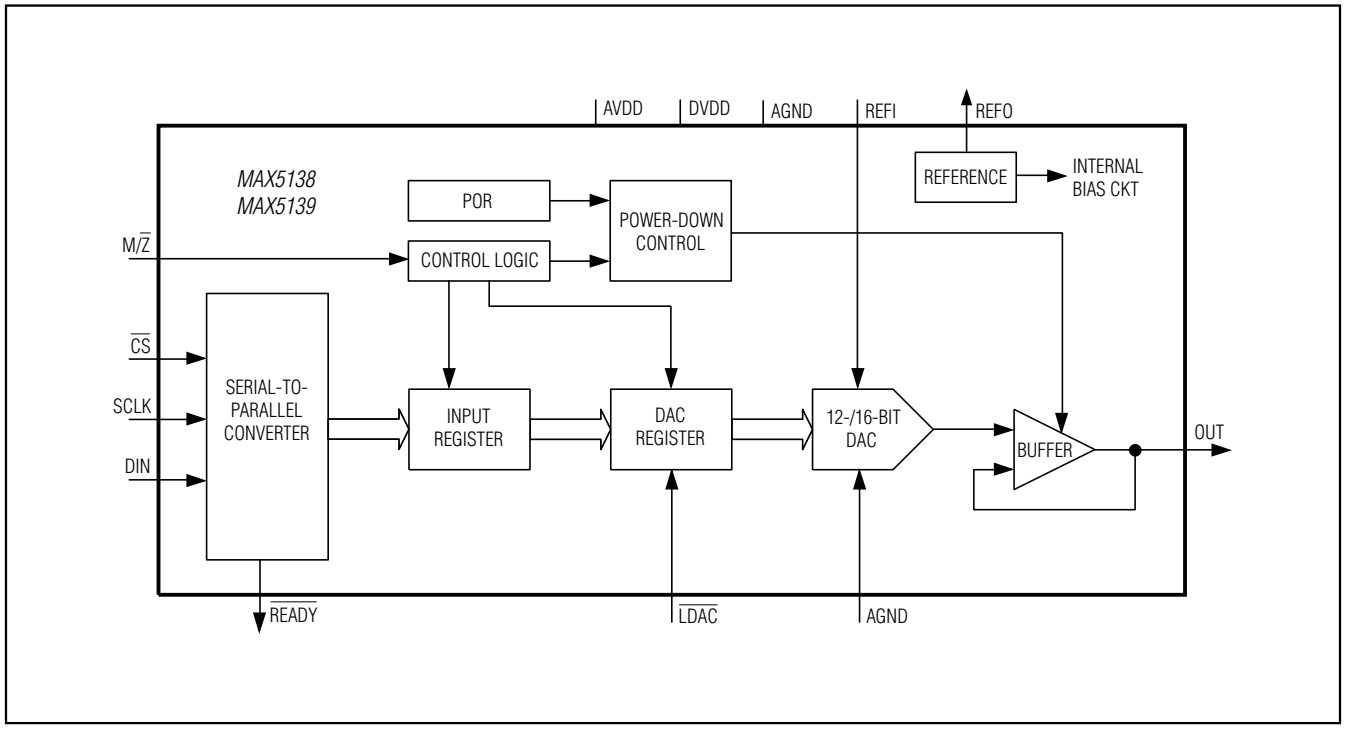
Digital-to-Analog Power-Up Glitch Impulse

The digital-to-analog power-up glitch is the duration of the magnitude of the switching glitch that occurs as the device exits power-down mode.

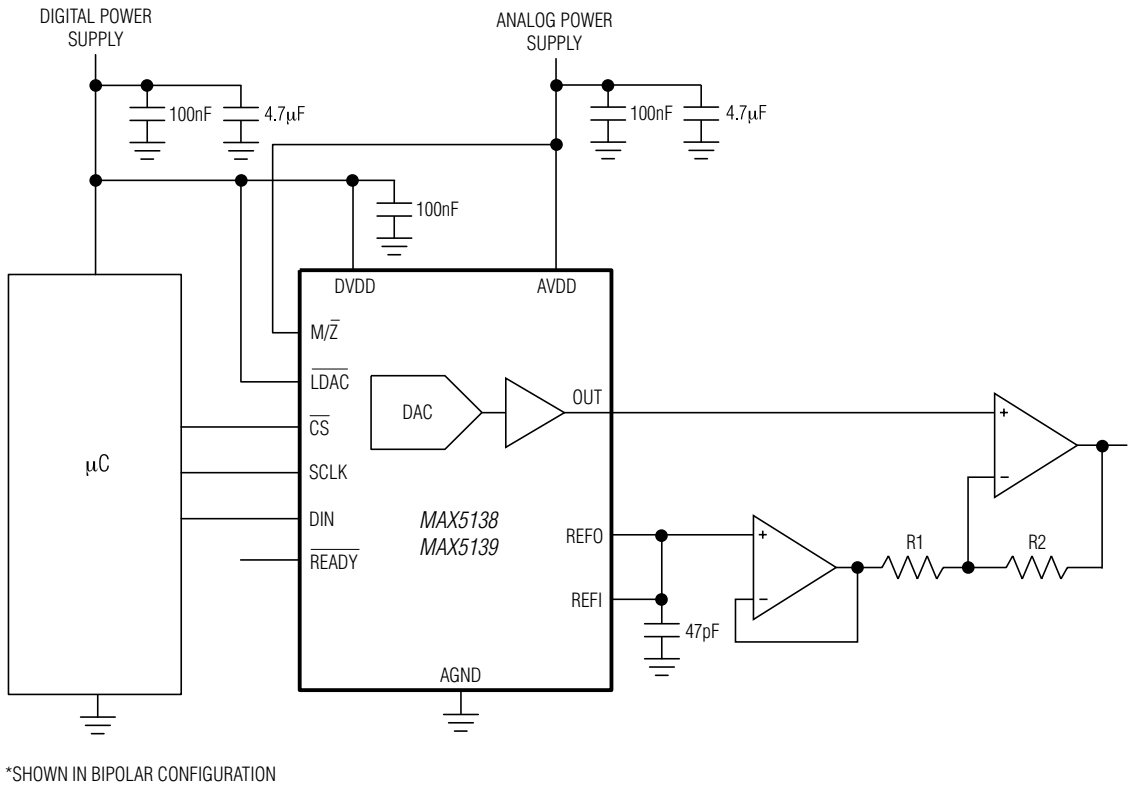
Chip Information

PROCESS: BiCMOS

Functional Diagram



Typical Operating Circuit



Package Information

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
16 TQFN-EP	T1633+5	21-0136	90-0032

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	3/09	Initial release	—
1	4/09	Removed future product reference for MAX5139	1
2	10/12	Correct errors in data sheet	1–4, 9, 10