IH6116

High Reliability 16-Channel CMOS Analog Multiplexer

GENERAL DESCRIPTION

The IH6116 is a CMOS one of 16 multiplexer. The part is a plug-in replacement for the DG506. Four line binary decoding is used so that the 16 channels can be controlled by 4 Address inputs; additionally a fifth input is provided to be used as a system enable. When the ENable input is high (5V) the channels are sequenced by the 4 line Address inputs, and when low (0V), all channels are off. The 4 Address inputs are controlled by TTL logic or CMOS logic elements with a "0" corresponding to any voltage less than 0.8V and a "1" corresponding to any voltage greater than 2.4V. Note that the ENable input must be taken to 5V to enable the system and less than 0.8V to disable the system.

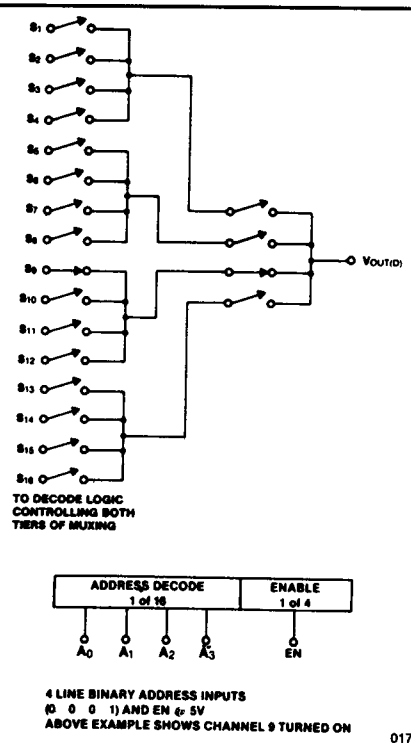
ORDERING INFORMATION

Part Number	Temperature Range	Package
IH6116MJI	−55°C to +125°C	28 pin CERDIP

Ceramic package available as special order only (IH6116MDI/CDI)

FEATURES

- Pin Compatible With DG506A, HI-506 & AD7506
- Ultra Low Leakage — $I_{D(off)} \leq 100pA$ Typical
- ±11 Analog Signal Range
- $r_{DS(on)} < 700$ Ohms Over Full Signal and Temperature Range
- Break-Before-Make Switching
- TTL and CMOS Compatible Address Control
- Binary Address Control (4 Address Inputs Control 16 Channels)
- Two Tier Submultiplexing to Facilitate Expandability
- Power Supply Quiescent Current Less Than 100μA
- No SCR Latchup
- Internal Diode In Series With V^+ For Fault Protection



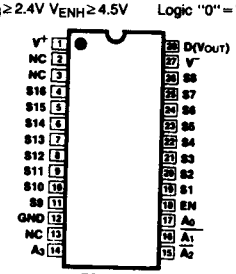
0176-1

Figure 1: Functional Diagram

DECODE TRUTH TABLE

A_3	A_2	A_1	A_0	EN	ON SWITCH
X	X	X	X	0	NONE
0	0	0	0	1	1
0	0	0	1	1	2
0	0	1	0	1	3
0	0	1	1	1	4
0	1	0	0	1	5
0	1	0	1	1	6
0	1	1	0	1	7
0	1	1	1	1	8
1	0	0	0	1	9
1	0	0	1	1	10
1	0	1	0	1	11
1	0	1	1	1	12
1	1	0	0	1	13
1	1	0	1	1	14
1	1	1	0	1	15
1	1	1	1	1	16

Logic "1" = $V_{AH} \geq 2.4V$ $V_{ENH} \geq 4.5V$ Logic "0" = $V_{AL} \leq 0.8V$



0176-2

Figure 2: Pin Configuration

ABSOLUTE MAXIMUM RATINGS

V_{IN} (A, EN) to Ground ..... −15V to 15V
V_S or V_D to V+ ..... 0, −36V
V_S or V_D to V− 0, 36V
V+ to Ground 16V
V− to Ground ..... −16V
Current (Any Terminal) 30mA
Current (Analog Source or Drain) 20mA
Operating Temperature ..... −55 to 125°C
Storage Temperature ..... −65 to 150°C
Lead Temperature (Soldering, 10sec) ..... 300°C
Power Dissipation (Package)* 1200mW

* All leads soldered or welded to PC board. Derate 10mW/°C above 70°C.

NOTE: *Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

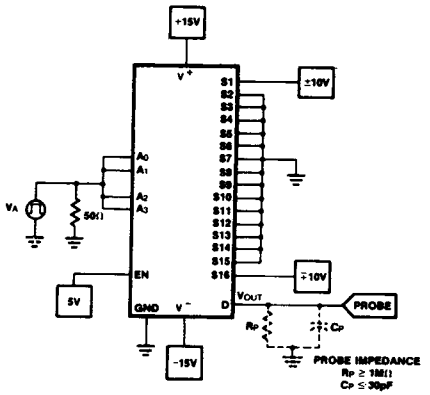
ELECTRICAL CHARACTERISTICS

V+ = 15V, V− = −15V, V_{EN} = +5V (Note 1), Ground = 0V, unless otherwise specified.

Characteristic	Measured Terminal	No Tests Per Temp	Typ 25°C	Test Conditions		Max Limits M Suffix −55°C	Max Limits M Suffix 25°C	Max Limits M Suffix 125°C	Units
SWITCH									
$r_{DS(ON)}$	S to D	16	480	V_D = 10V, I_S = −1mA	Sequence each switch on V_{AL} = 0.8V, V_{AH} = 3V	600	600	700	Ω
		16	300	V_D = −10V, I_S = 1mA		600	600	700	
$\Delta r_{DS(ON)}$			20	$\Delta r_{DS(on)} = \frac{r_{DS(on)max} - r_{DS(on)min}}{r_{DS(on)avg.}} V_S = \pm 10V$					%
$I_{S(OFF)}$	S	16	0.01	V_S = 10V, V_D = −10V	V_{EN} = 0.8V		±.5	50	nA
		16	0.01	V_S = −10V, V_D = 10V			±.5	50	
$I_{D(OFF)}$	D	1	0.1	V_D = 10V, V_S = −10V			±1	100	
		1	0.1	V_D = −10V, V_S = 10V			±2	100	
$I_{D(ON)}$	D	16	0.1	$V_{S(ALL)}$ = V_D = 10V	Sequence each switch on V_{AL} = 0.8V, V_{AH} = 3V		±2	100	
		16	0.1	$V_{S(ALL)}$ = V_D = −10V			±2	100	
INPUT									
$I_{A(on)}$ or $I_{A(off)}$		4	0.01	V_A = 2.4V			−10	−30	μA
		4	0.01	V_A = 14V			10	30	
I_A	A_0 A_1 A_2 A_3	4		V_{EN} = 5V	All V_A = 0		−10	−30	
	EN	1		V_{EN} = 0			−10	−30	
DYNAMIC									
t_{trans}	D		0.6	See Fig. 3					μs
t_{open}	D		0.2	See Fig. 4					
$t_{EN(on)}$	D		0.8	See Fig. 5			1.5		
$t_{EN(off)}$	D		0.3				1		
"OFF" Isolation	D		60	V_{EN} = 0, R_L = 200Ω, C_L = 3pF, V_S = 3VRMS, f = 500kHz					dB
$C_{s(OFF)}$	S		5	V_S = 0	V_{EN} = 0, f = 140kHz to 1MHz				pF
$C_{d(OFF)}$	D		40	V_D = 0					
$C_{ds(OFF)}$	D to S		1	V_S = 0, V_D = 0					
SUPPLY									
Supply Current	+ V+	1	55	V_{EN} = 5V	All V_A = 0 or 5V		200		μA
	− V−	1	2				100		
Standby Current	+ V+	1	1	V_{EN} = 0			100		
	− V−	1	1				100		

NOTE 1: See Section V. Enable Input Strobing Levels.

IH6116



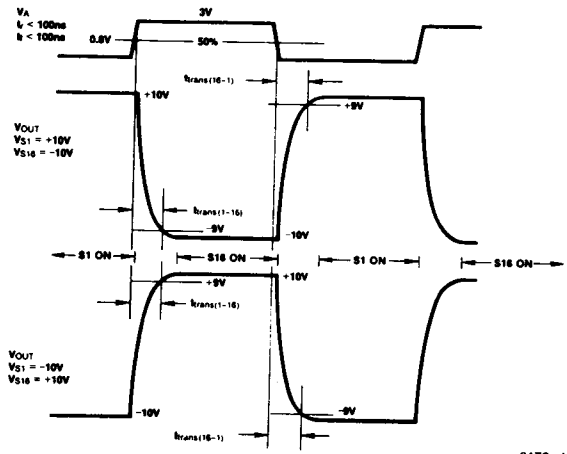
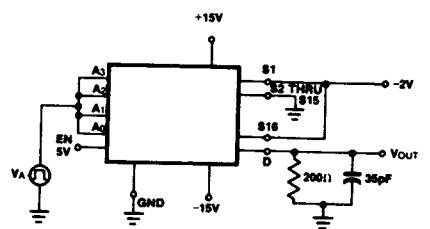


Figure 3: Switching Information



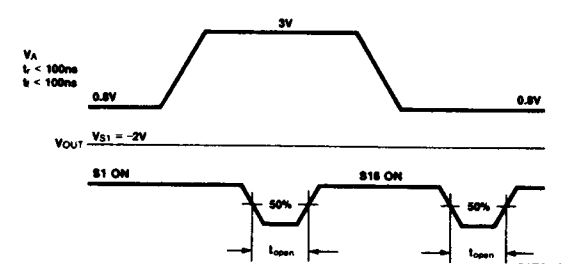
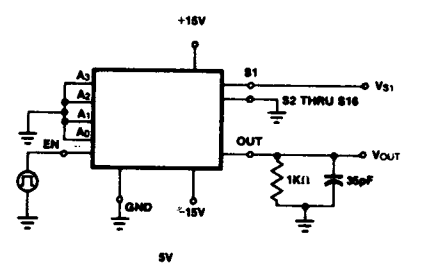


Figure 4: Switching Information



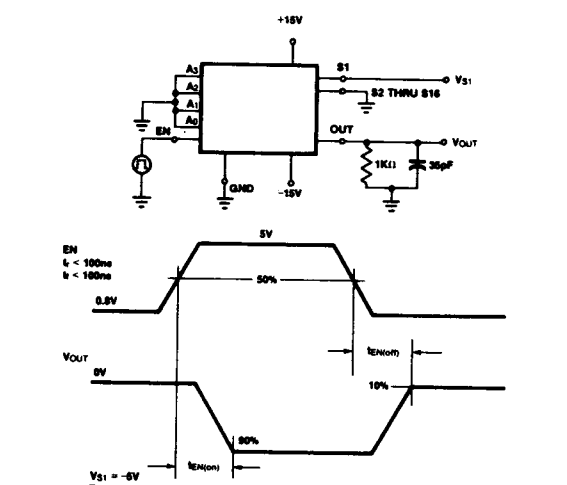
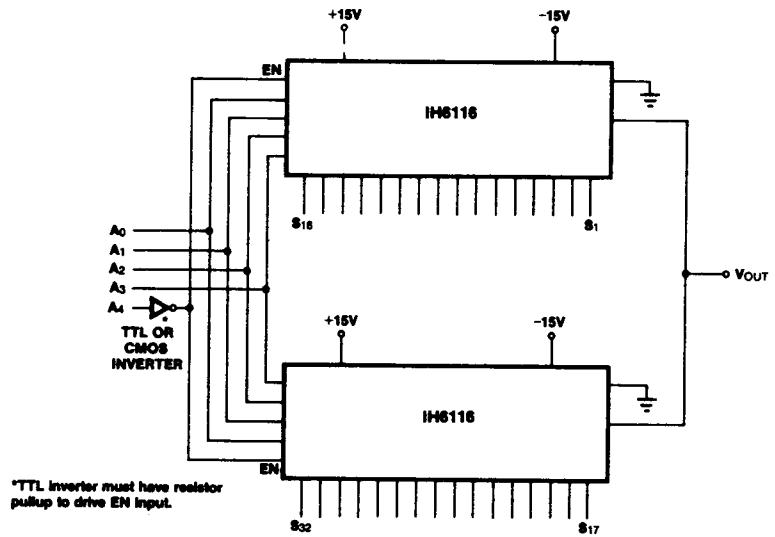


Figure 5: Switching Information

IH6116 APPLICATIONS



DECODE TRUTH TABLE

A_4	A_3	A_2	A_1	A_0	On Switch
0	0	0	0	0	S1
0	0	0	0	1	S2
0	0	0	1	0	S3
0	0	0	1	1	S4
0	0	1	0	0	S5
0	0	1	0	1	S6
0	0	1	1	0	S7
0	0	1	1	1	S8
0	1	0	0	0	S9
0	1	0	0	1	S10
0	1	0	1	0	S11
0	1	0	1	1	S12
0	1	1	0	0	S13
0	1	1	0	1	S14
0	1	1	1	0	S15
0	1	1	1	1	S16

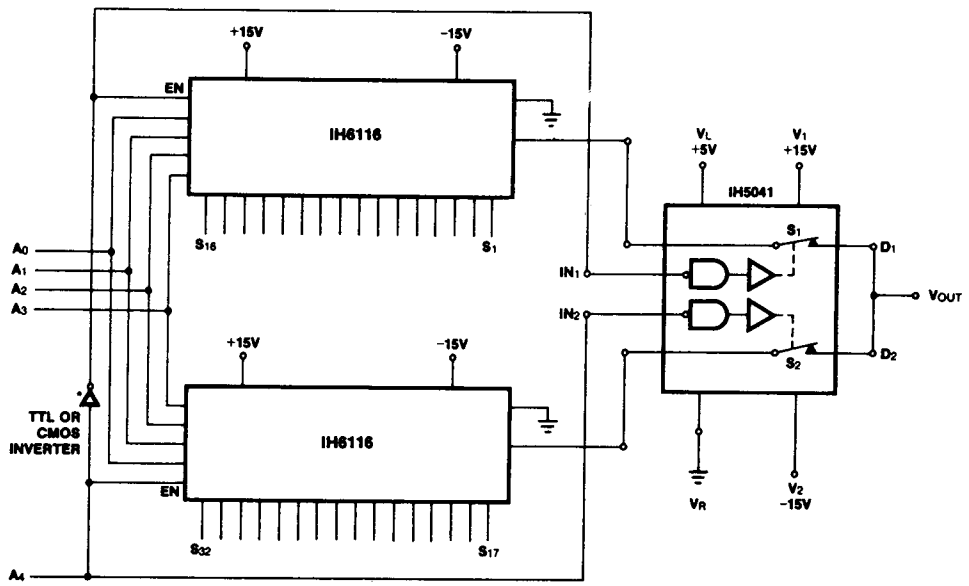
DECODE TRUTH TABLE

A_4	A_3	A_2	A_1	A_0	On Switch
1	0	0	0	0	S17
1	0	0	0	1	S18
1	0	0	1	0	S19
1	0	0	1	1	S20
1	0	1	0	0	S21
1	0	1	0	1	S22
1	0	1	1	0	S23
1	0	1	1	1	S24
1	1	0	0	0	S25
1	1	0	0	1	S26
1	1	0	1	0	S27
1	1	0	1	1	S28
1	1	1	0	0	S29
1	1	1	0	1	S30
1	1	1	1	0	S31
1	1	1	1	1	S32

Figure 6: 1 Out of 32 Channel Multiplexer Using 2 IH6116s

IH6116

IH6116 APPLICATIONS (Continued)



*TTL gate must have pullup resistor to +5V to drive EN inputs

0176-10

DECODE TRUTH TABLE

A_4	A_3	A_2	A_1	A_0	ON SWITCH
0	0	0	0	0	S1
0	0	0	0	1	S2
0	0	0	1	0	S3
0	0	0	1	1	S4
0	0	1	0	0	S5
0	0	1	0	1	S6
0	0	1	1	0	S7
0	0	1	1	1	S8
0	1	0	0	0	S9
0	1	0	0	1	S10
0	1	0	1	0	S11
0	1	0	1	1	S12
0	1	1	0	0	S13
0	1	1	0	1	S14
0	1	1	1	0	S15
0	1	1	1	1	S16

DECODE TRUTH TABLE

A_4	A_3	A_2	A_1	A_0	ON SWITCH
1	0	0	0	0	S17
1	0	0	0	1	S18
1	0	0	1	0	S19
1	0	0	1	1	S20
1	0	1	0	0	S21
1	0	1	0	1	S22
1	0	1	1	0	S23
1	0	1	1	1	S24
1	1	0	0	0	S25
1	1	0	0	1	S26
1	1	0	1	0	S27
1	1	0	1	1	S28
1	1	1	0	0	S29
1	1	1	0	1	S30
1	1	1	1	0	S31
1	1	1	1	1	S32

Figure 7: 1 Out of 32 Channel Multiplexer Using 2 IH6116s; Using An IH5041 for Submultiplexing

IH6116 APPLICATIONS (Continued)

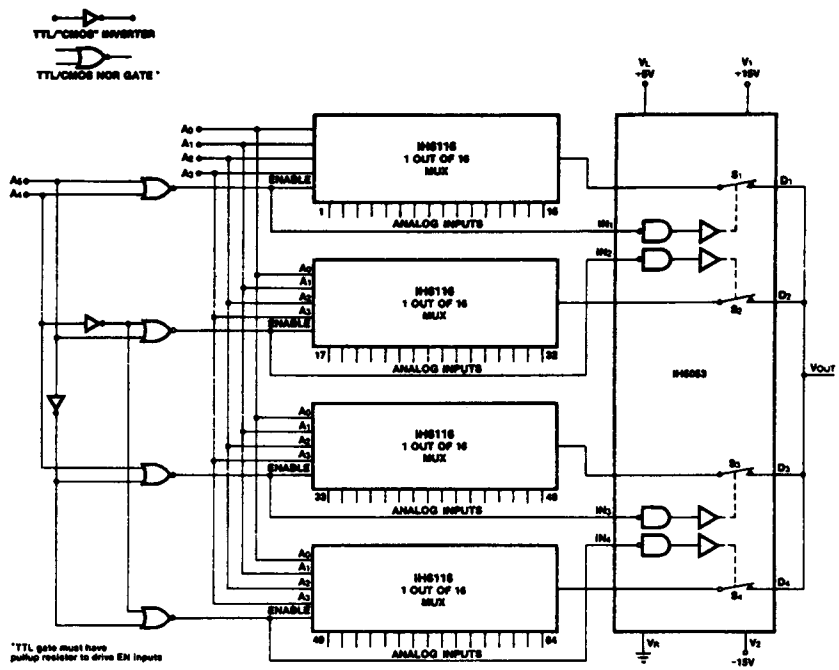


Figure 8: 1 Out of 64 Multiplexer Using 4 1/16s and IH5053 As Submultiplexer

General note on expandability of IH6116

The IH6116 is a two tier multiplexer, where sixteen input channels are routed to a common output in blocks of 4. Each block of 4 input channels is routed to one common output channel, and thus the submultiplexed system looks like 4 blocks of 4 inputs routed to 4 different outputs with the 4 outputs tied together. Thus 20 switches are needed to handle the 16 channels of information. The advantage of this is lower output capacitance and leakage than would be possible with a system using all 16 channels tied to one common output. Also the expandability into 32, 64, 128, channels etc. is facilitated. Figures 6, 7, and 8 show how the IH6116 can be expanded.

Figure 6 shows a 1 of 32 multiplexer, using 2 IH6116s. Since the 6116 is itself a 2 tier MUX, the system as shown is basically a 2 tier system. The four output channels of each 6116 are tied together so that 8 channels are tied to the V_{OUT} common point. Since only one channel of information is on at a time, the common output will consist of 7 OFF channels and 1 ON channel. Thus the output leakage will correspond to 7 $I_{D(offs)}$ and 1 $I_{D(on)}$, or about 1.0nA of typical leakage at room temperature. Throughput speed will be typically 0.8μs for t_{on} and 0.3μs for t_{off}. Throughput channel resistance will be in the 500Ω area.

Figure 7 shows the 1 of 32 MUX of Figure 6, with a third tier of submultiplexing added to further reduce leakage and output capacitance. The IH5041 has typical ON resistances of 50Ω (max. is 75Ω) so it only increases thruput channel resistance from the 500 ohms of Figure 6 to about 550 ohms for Figure 7. Throughput channel speed is a little slower by about 0.5μs for both ON and OFF time, and output leakage is about 0.2nA.

Figure 8 shows a 1 of 64 MUX using 3 tier MUXing (similar to Figure 7). The Intersil IH5053 is used to get the third tier of MUXing. The V_{OUT} point will see 3 OFF channels and 1 ON channel at any one time, so that the typical leakages will be about 0.4 nA. Throughput channel resistance will be in the 550 ohm area with throughput switching speeds about 1.3μs for ON time and 0.8μs for OFF time.

The IH5053 was chosen as the third tier of the MUX because it will switch the same AC signals as the IH6116 (typically plus and minus 15V) and uses break before make switching. Also power supply quiescent currents are on the order of 1-2μA, so that no excessive system power is dissipated. Note that the logic of the 5053 is such that it can be tied directly to the ENable input (as shown in the figures) with no extra circuitry being required.

Enable input strobing levels

The enable input (EN) acts as an enabling or disabling pin for the IH6116 when used as a 16 channel MUX. However, when expanding the MUX to more than 16 channels, the EN pin acts as another address input. Figures 6 and 7 show the EN pin used as the A4 input.

For the system to function properly the EN input (pin 18) must go to 5V $\pm$5% for the high state and less than 0.8V for the low state. When using TTL logic, a pull-up resistor of 1kΩ or less should be used to pull the output voltage up to 5V. When using CMOS logic, the high state goes to the power supply so no pull-up is required.

If used on high voltage logic supplies, EN should be at least 0.7V below V^+ at all times. See IH6108 data sheet for details.

APPLICATION NOTES

Further information may be found in:

A003 "Understanding and Applying the Analog Switch"

A006 "A New CMOS Analog Gate Technology"

A020 "A Cookbook Approach to High Speed Data Acquisition and Microprocessor Interfacing"

R009 "Reduce CMOS Multiplexer Troubles Through Proper Device Selection"

NOTE: This multiplexer does not require external resistors and/or diodes to eliminate what is commonly known as a latch up or SCR action. Because of this fact, the $r_{DS(ON)}$ of the switch is maintained at specified values.