

## Ultra-Precision Differential LVPECL 2:1 MUX with Internal Termination

### Features

- Guaranteed AC Performance over Temperature and Voltage:
  - DC to 5 Gbps Throughput
  - DC to >4 GHz  $f_{MAX}$  (Clock)
  - <240 ps Propagation Delay (IN-to-Q)
  - <110 ps Rise/Fall Times
- Ultra-Low Jitter Design
- Unique Input Termination and VT Pin Accepts DC- and AC-Coupled Inputs (CML, PECL, LVDS)
- 800 mV (100k) LVPECL Output Swing
- 2.5V  $\pm 5\%$  or 3.3V  $\pm 10\%$  Power Supply Operation
- Industrial Temperature Range:  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$
- Available in 16-lead (3 mm x 3 mm) QFN Package

### Applications

- Redundant Clock Distribution
- SONET/SDH Clock/Data Distribution
- Loopback
- Fibre Channel Distribution

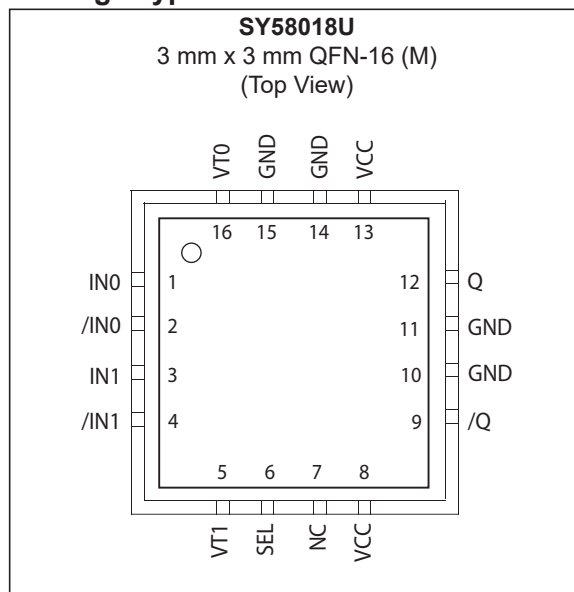
### General Description

The SY58018U is a 2.5V/3.3V precision, high-speed, 2:1 differential MUX capable of handling clocks up to 4 GHz and data up to 5 Gbps.

The differential input includes Microchip's unique, 3-pin input termination architecture that allows customers to interface to any differential signal (AC- or DC-coupled) as small as 100 mV without any level shifting or termination resistor networks in the signal path. The outputs are 800 mV, 100k compatible, LVPECL, with extremely fast rise/fall times guaranteed to be less than 110 ps.

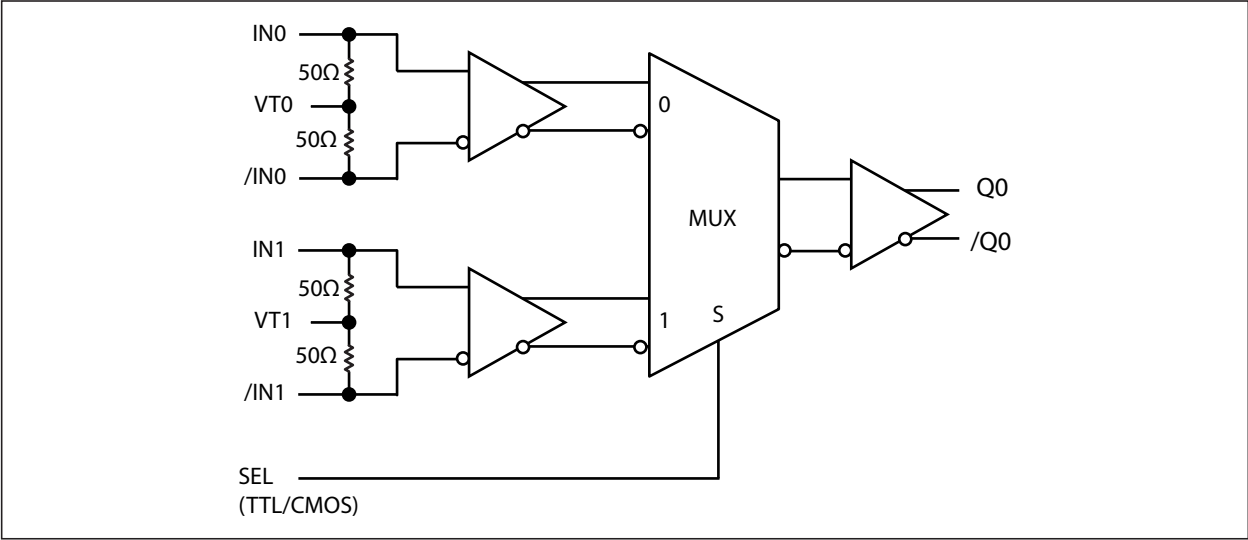
The SY58018U operates from a 2.5V  $\pm 5\%$  supply or a 3.3V  $\pm 10\%$  supply and is guaranteed over the full industrial temperature range of  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$ . For applications that require CML outputs, consider the SY58017U or for 400 mV LVPECL outputs the SY58019U. The SY58018U is part of Microchip's high-speed, Precision Edge<sup>®</sup> product line.

### Package Type



# SY58018U

Functional Block Diagram



## 1.0 ELECTRICAL CHARACTERISTICS

### Absolute Maximum Ratings †

|                                     |                   |
|-------------------------------------|-------------------|
| Supply Voltage ( $V_{CC}$ )         | –0.5V to +4.0V    |
| Input Voltage ( $V_{IN}$ )          | –0.5V to $V_{CC}$ |
| LVPECL Output Current ( $I_{OUT}$ ) |                   |
| Continuous                          | 50 mA             |
| Surge                               | 100 mA            |
| Termination Current ( $I_{VT}$ )    |                   |
| Source or Sink on VT Pin            | ±100 mA           |
| Input Current                       |                   |
| Source or Sink Current on IN, /IN   | ±50 mA            |

### Operating Ratings ††

|                             |                    |
|-----------------------------|--------------------|
| Supply Voltage ( $V_{CC}$ ) | +2.375V to +2.625V |
| Supply Voltage ( $V_{CC}$ ) | +2.97V to +3.63V   |

† **Notice:** Permanent device damage may occur if absolute maximum ratings are exceeded. This is a stress rating only and functional operation is not implied at conditions other than those detailed in the operational sections of this data sheet. Exposure to absolute maximum ratings conditions for extended periods may affect device reliability.

†† **Notice:** The data sheet limits are not guaranteed if the device is operated beyond the operating ratings.

## DC ELECTRICAL CHARACTERISTICS

**Electrical Characteristics:**  $T_A = -40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$ , unless otherwise stated. [Note 1](#)

| Parameters                                                          | Sym.           | Min.           | Typ.       | Max.           | Units    | Conditions                     |
|---------------------------------------------------------------------|----------------|----------------|------------|----------------|----------|--------------------------------|
| Power Supply Voltage Range                                          | $V_{CC}$       | 2.375<br>2.97  | 2.5<br>3.3 | 2.625<br>3.63  | V        | —                              |
| Power Supply Current                                                | $I_{CC}$       | —              | 50         | 65             | mA       | No load, max. $V_{CC}$         |
| Differential Input Resistance (IN0-to-/IN0, IN1-to-/IN1)            | $R_{DIFF\_IN}$ | 80             | 100        | 120            | $\Omega$ | —                              |
| Input Resistance (IN0-to-VT0, /IN0-to-VT0, IN1-to-VT1, /IN1-to-VT1) | $R_{IN}$       | 40             | 50         | 60             | $\Omega$ | —                              |
| Input HIGH Voltage (IN0, /IN0, IN1, /IN1)                           | $V_{IH}$       | $V_{CC} - 1.6$ | —          | $V_{CC}$       | V        | <a href="#">Note 2</a>         |
| Input LOW Voltage (IN0, /IN0, IN1, /IN1)                            | $V_{IL}$       | 0              | —          | $V_{IH} - 0.1$ | V        | —                              |
| Input Voltage Swing (IN0, /IN0, IN1, /IN1)                          | $V_{IN}$       | 0.1            | —          | 1.7            | V        | See <a href="#">Figure 4-1</a> |
| Differential Input Voltage Swing  IN0, /IN0 ,  IN1, /IN1            | $V_{DIFF\_IN}$ | 0.2            | —          | —              | V        | See <a href="#">Figure 4-2</a> |
| Voltage from Input to VT (IN0, /IN0, IN1, /IN1)                     | $V_{T\_IN}$    | —              | —          | 1.28           | V        | —                              |

**Note 1:** The circuit is designed to meet the DC specifications shown in the above table after thermal equilibrium has been established.

**2:**  $V_{IH(MIN)}$  not lower than 1.2V.

## LVPECL OUTPUT DC ELECTRICAL CHARACTERISTICS

**Electrical Characteristics:**  $V_{CC} = +2.5\text{V} \pm 5\%$  or  $+3.3\text{V} \pm 10\%$ ,  $R_L = 50\Omega$  to  $V_{CC} - 2\text{V}$ ;  $T_A = -40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$ , unless otherwise stated. [Note 1](#)

| Parameter                               | Symbol          | Min.             | Typ. | Max.             | Units | Condition                      |
|-----------------------------------------|-----------------|------------------|------|------------------|-------|--------------------------------|
| Output High Voltage Q, /Q               | $V_{OH}$        | $V_{CC} - 1.145$ | —    | $V_{CC} - 0.895$ | V     | —                              |
| Output Low Voltage Q, /Q                | $V_{OL}$        | $V_{CC} - 1.945$ | —    | $V_{CC} - 1.695$ | V     | —                              |
| Output Differential Swing Q, /Q         | $V_{OUT}$       | 550              | 800  | —                | mV    | See <a href="#">Figure 4-1</a> |
| Differential Output Voltage Swing Q, /Q | $V_{DIFF\_OUT}$ | 1100             | 1600 | —                | mV    | See <a href="#">Figure 4-2</a> |

**Note 1:** The circuit is designed to meet the DC specifications shown in the above table after thermal equilibrium has been established.

## LVTTL/CMOS DC ELECTRICAL CHARACTERISTICS

**Electrical Characteristics:**  $V_{CC} = 2.5V \pm 5\%$  or  $3.3V \pm 10\%$ ;  $T_A = -40^\circ C$  to  $+85^\circ C$ . [Note 1](#)

| Parameter          | Symbol   | Min. | Typ. | Max. | Units   | Condition |
|--------------------|----------|------|------|------|---------|-----------|
| Input HIGH Voltage | $V_{IH}$ | 2.0  | —    | —    | V       | —         |
| Input LOW Voltage  | $V_{IL}$ | —    | —    | 0.8  | V       | —         |
| Input HIGH Current | $I_{IH}$ | —    | —    | 40   | $\mu A$ | —         |
| Input LOW Current  | $I_{IL}$ | -300 | —    | —    | $\mu A$ | —         |

**Note 1:** The circuit is designed to meet the DC specifications shown in the above table after thermal equilibrium has been established.

## AC ELECTRICAL CHARACTERISTICS

**Electrical Characteristics:**  $V_{CC} = +2.5V \pm 5\%$  or  $+3.3V \pm 10\%$ ,  $R_L = 50\Omega$  to  $V_{CC} - 2V$ ;  $T_A = -40^\circ C$  to  $+85^\circ C$ , unless otherwise stated. [Note 1](#)

| Parameter                                              | Symbol          | Min. | Typ. | Max. | Units          | Condition                                         |
|--------------------------------------------------------|-----------------|------|------|------|----------------|---------------------------------------------------|
| Maximum Frequency                                      | $f_{MAX}$       | 5    | —    | —    | Gbps           | NRZ (Data)                                        |
|                                                        |                 | —    | 4    | —    | GHz            | $V_{OUT} > 400$ mV (Clock)                        |
| Propagation Delay                                      | $t_{PD}$        | 110  | 190  | 240  | ps             | (IN0 or IN1-to-Q)                                 |
|                                                        |                 | 50   | 180  | 350  | ps             | (SEL-to-Q)                                        |
| Differential Propagation Delay Temperature Coefficient | $t_{PD}$ Tempco | —    | 75   | —    | fs/ $^\circ C$ | —                                                 |
| Input-to-Input Skew                                    | $t_{SKEW}$      | —    | 4    | 15   | ps             | <a href="#">Note 2</a>                            |
| Part-to-Part Skew                                      |                 | —    | —    | 100  | ps             | <a href="#">Note 3</a>                            |
| Additive Phase Jitter                                  | $t_{JITTER}$    | —    | 50   | —    | fs             | 622 MHz<br>Integration Range: 12 kHz to 20 MHz    |
|                                                        |                 | —    | 104  | —    |                | 156.25 MHz<br>Integration Range: 12 kHz to 20 MHz |
|                                                        |                 | —    | 173  | —    |                | 100 MHz<br>Integration Range: 12 kHz to 20 MHz    |
| Output Rise/Fall Time                                  | $t_r/t_f$       | 35   | 75   | 110  | ps             | 20% to 80% at full swing                          |

**Note 1:** High frequency AC parameters are guaranteed by design and characterization.

**2:** Input-to-input skew is the difference in time from and input-to-output in comparison to any other input-to-output.

**3:** Part-to-Part skew is defined for two parts with identical power supply voltages at the same temperature and no skew at the edges at the respective inputs.

## TEMPERATURE SPECIFICATIONS

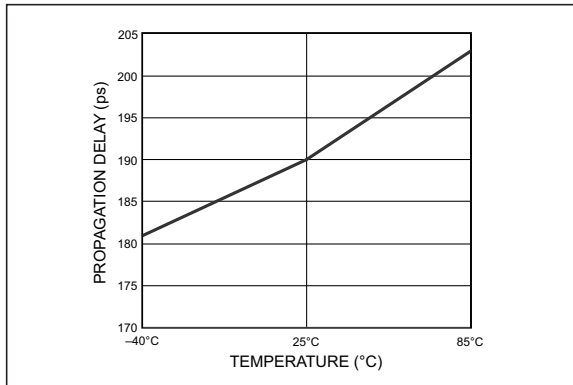
| Parameters                                  | Sym.          | Min. | Typ. | Max. | Units | Conditions         |
|---------------------------------------------|---------------|------|------|------|-------|--------------------|
| <b>Temperature Ranges</b>                   |               |      |      |      |       |                    |
| Operating Ambient Temperature Range         | $T_A$         | -40  | —    | +85  | °C    | —                  |
| Lead Temperature                            | —             | —    | —    | +260 | °C    | Soldering, 20 sec. |
| Storage Temperature Range                   | $T_S$         | -65  | —    | +150 | °C    | —                  |
| <b>Package Thermal Resistances (Note 1)</b> |               |      |      |      |       |                    |
| Thermal Resistance, 3x3 QFN-16Ld            | $\theta_{JA}$ | —    | 60   | —    | °C/W  | Still-air          |
|                                             | $\psi_{JB}$   | —    | 38   | —    | °C/W  | Junction-to-board  |

**Note 1:** Package thermal resistance assumes exposed pad is soldered (or equivalent) to the device's most negative potential on the PCB.  $\psi_{JB}$  and  $\theta_{JA}$  values are determined for a 4-layer board in still-air number, unless otherwise stated.

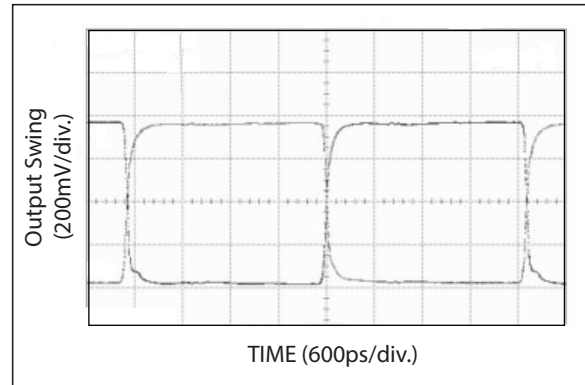
## 2.0 TYPICAL PERFORMANCE CURVES

**Note:** The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

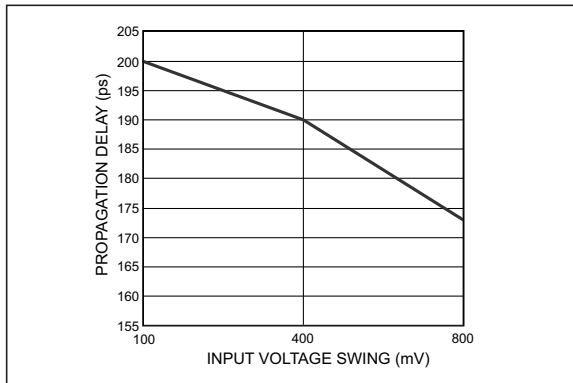
$V_{CC} = 3.3V$ ,  $V_{IN} = 400\text{ mV}$ ,  $T_A = +25^\circ C$ , unless otherwise stated.



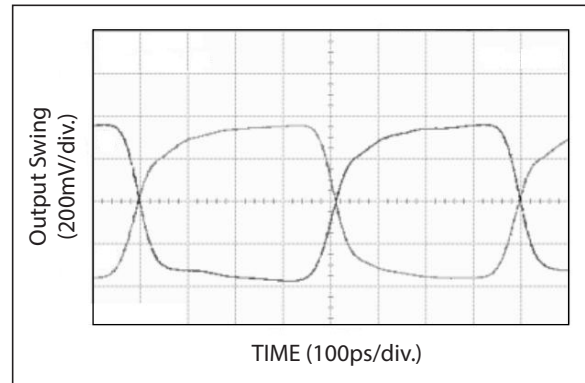
**FIGURE 2-1:** Propagation Delay vs. Temperature.



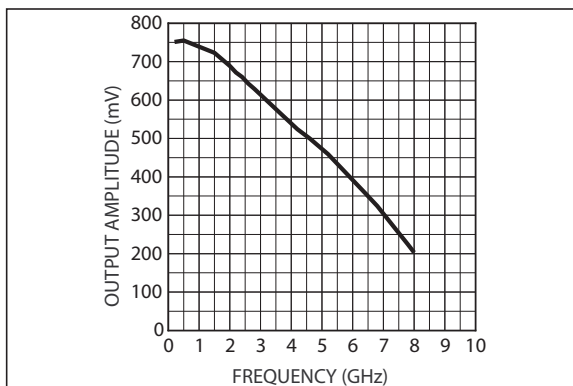
**FIGURE 2-4:** 200 MHz Output.



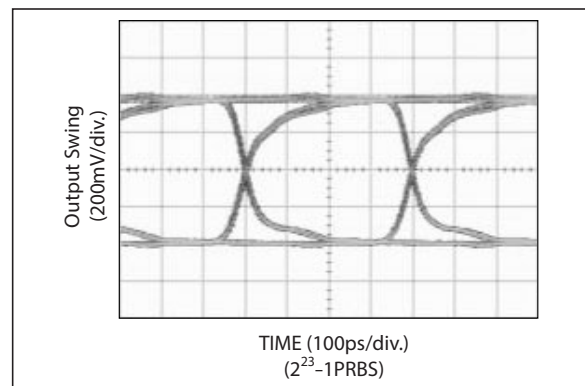
**FIGURE 2-2:** Propagation Delay vs. Input Voltage Swing.



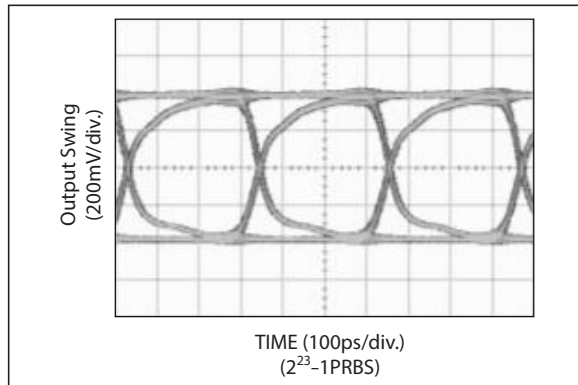
**FIGURE 2-5:** 1.25 GHz Output.



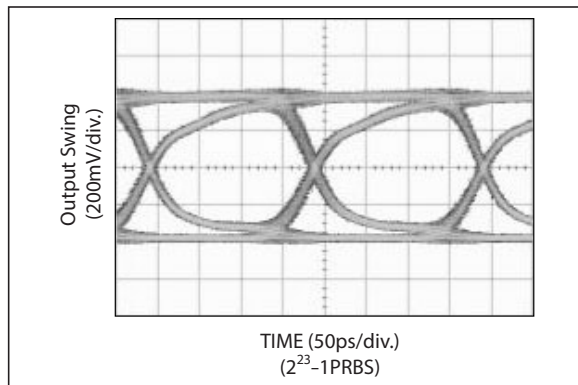
**FIGURE 2-3:** Output Amplitude vs. Frequency.



**FIGURE 2-6:** 2.5 Gbps Output.



**FIGURE 2-7:** 3.2 Gbps Output.



**FIGURE 2-8:** 5 Gbps Output.

### 3.0 PHASE NOISE PLOTS

$V_{CC} = +3.3V$ ,  $T_A = +25^\circ C$ .

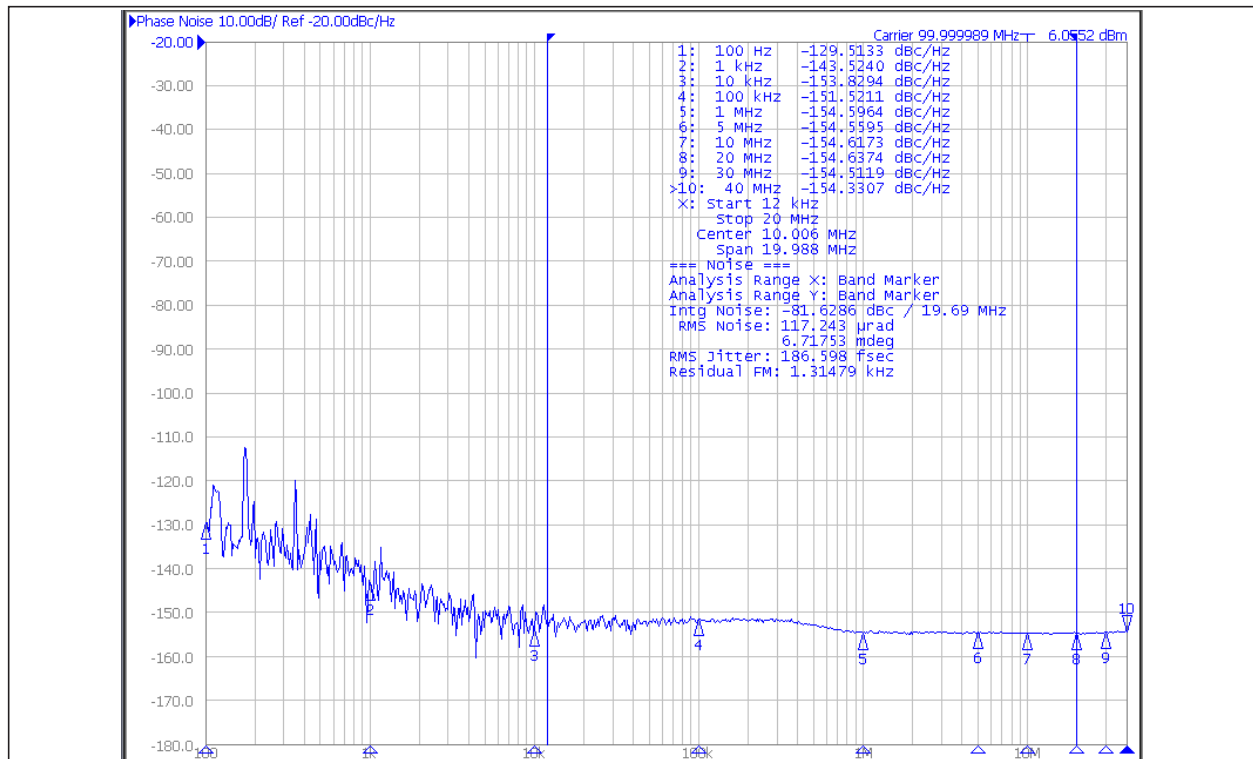


FIGURE 3-1: 100 MHz Phase Jitter, Device.

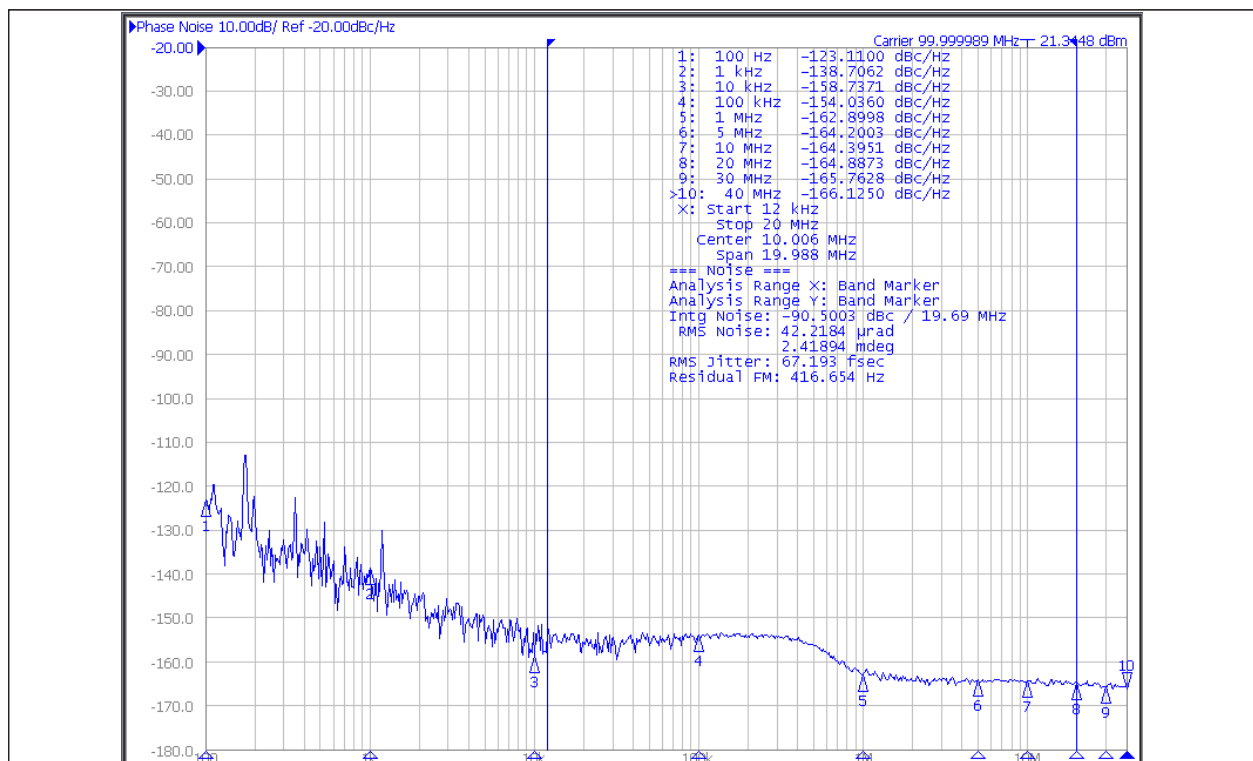
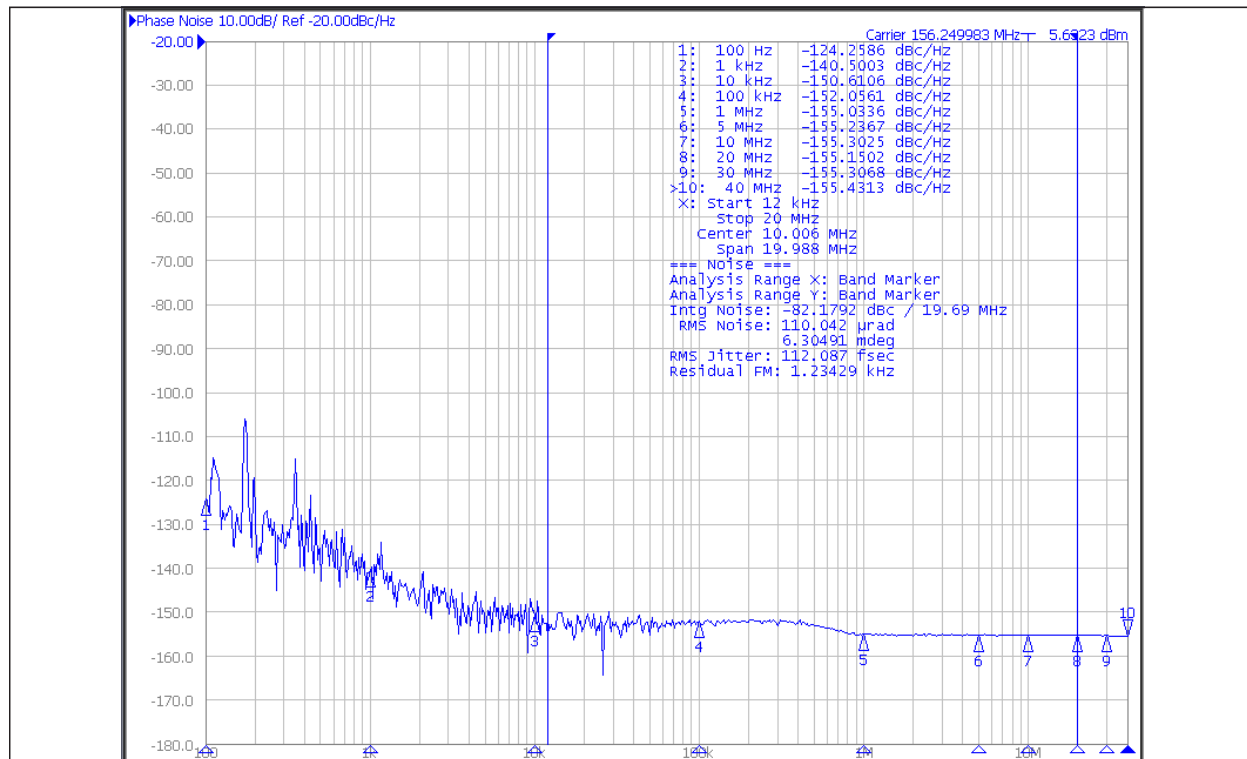
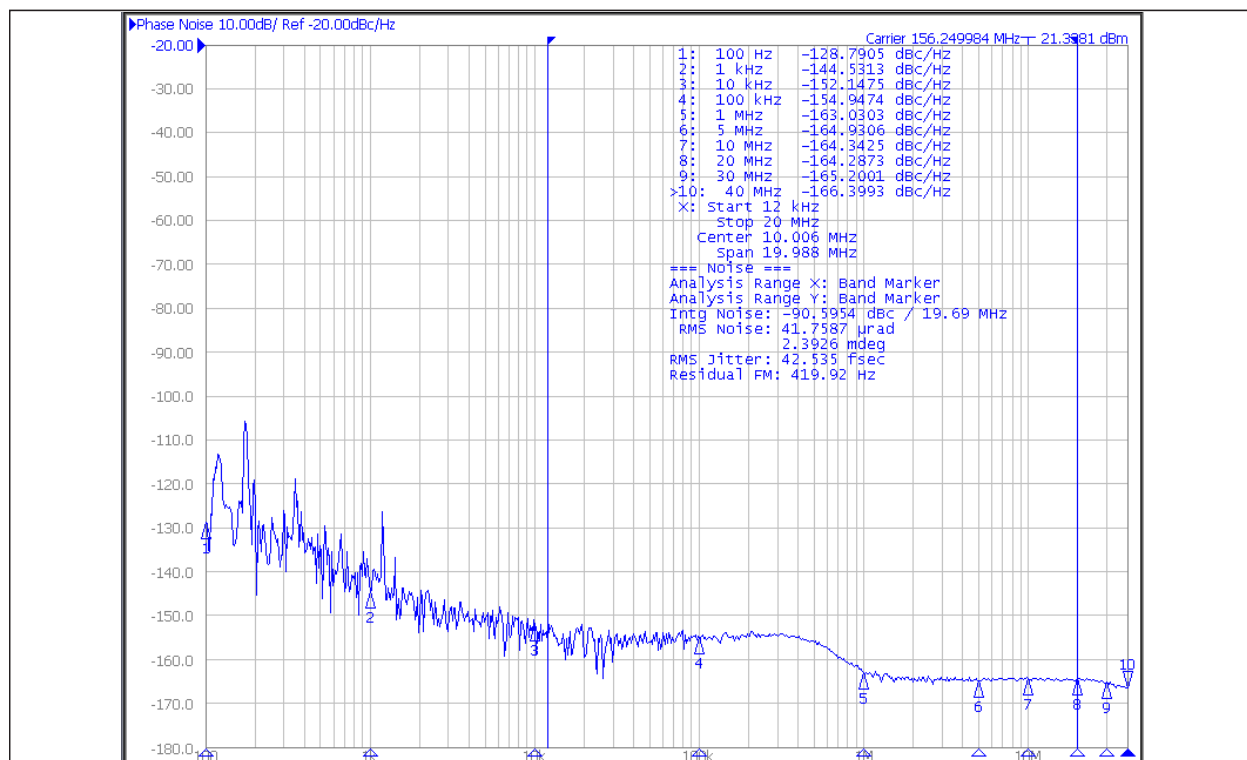


FIGURE 3-2: 100 MHz Phase Jitter, Source.



**FIGURE 3-3:** 156.25 MHz Phase Jitter, Device.



**FIGURE 3-4:** 156.25 MHz Phase Jitter, Source.

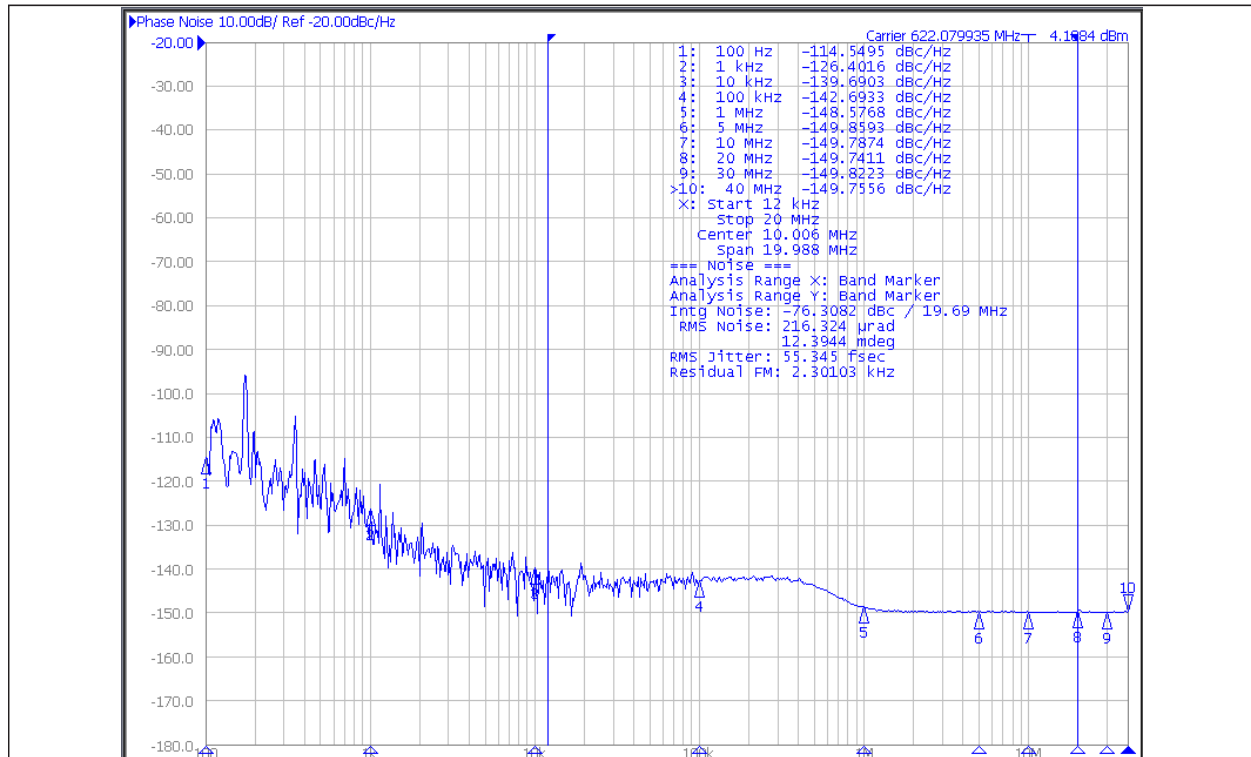


FIGURE 3-5: 622 MHz Phase Jitter, Device.

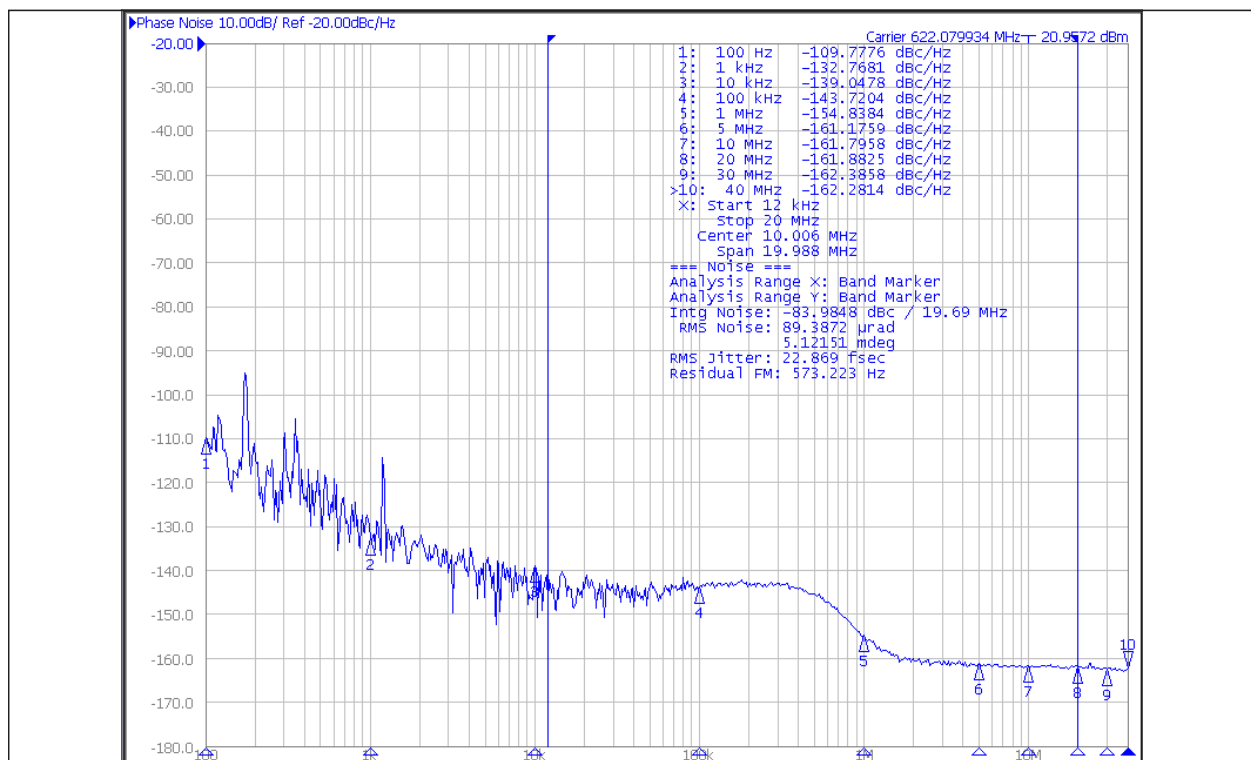


FIGURE 3-6: 622 MHz Phase Jitter, Source.

## 4.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in [Table 4-1](#).

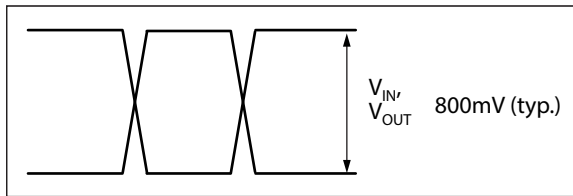
**TABLE 4-1: PIN FUNCTION TABLE**

| Pin Number     | Symbol                 | Description                                                                                                                                                                                                                                                                                                                                                                               |
|----------------|------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 1, 2<br>3, 4   | IN0, /IN0<br>IN1, /IN1 | Differential Input: These input pairs are the differential signal inputs to the device. They accept differential AC- or DC-coupled signals as small as 100 mV. Each pin of a pair internally terminates to a VT pin through 50Ω. Note that these inputs will default to an indeterminate state if left open. Please refer to the “Input Interface Applications” section for more details. |
| 16, 5          | VT0, VT1               | Input Termination Center-Tap: Each side of the differential input pair terminates to a VT pin. The VT0 and VT1 pins provide a center-tap to a termination network for maximum interface flexibility. See “Input Interface Applications” section for more details.                                                                                                                         |
| 6              | SEL                    | This single-ended TTL/CMOS compatible input selects the inputs to the multiplexer. Note that this input is internally connected to a 25 kΩ pull-up resistor and will default to a logic HIGH state if left open.                                                                                                                                                                          |
| 7              | NC                     | No connect.                                                                                                                                                                                                                                                                                                                                                                               |
| 8, 13          | VCC                    | Positive Power Supply: Bypass with 0.1 μF//0.01 μF low ESR capacitors. 0.01 μF capacitor should be as close to VCC pin as possible.                                                                                                                                                                                                                                                       |
| 12, 9          | Q, /Q                  | Differential Outputs: This 100k compatible LVPECL output pair is the output of the device. Normally terminate with 50Ω to $V_{CC} - 2V$ . See “Output Interface Applications” section. It is a logic function of the IN0, IN1, and SEL inputs. Please refer to the “Truth Table” for details.                                                                                             |
| 10, 11, 14, 15 | GND,<br>Exposed Pad    | Ground. Ground pins and exposed pad must be connected to the same ground plane.                                                                                                                                                                                                                                                                                                           |

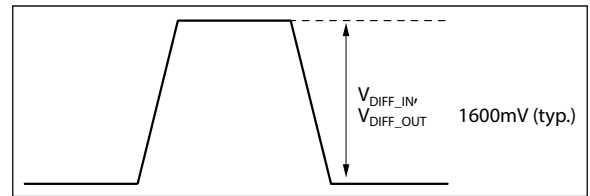
**TABLE 4-2: TRUTH TABLE**

| SEL | Output             |
|-----|--------------------|
| 0   | CH0 Input Selected |
| 1   | CH1 Input Selected |

## Single-Ended and Differential Swings

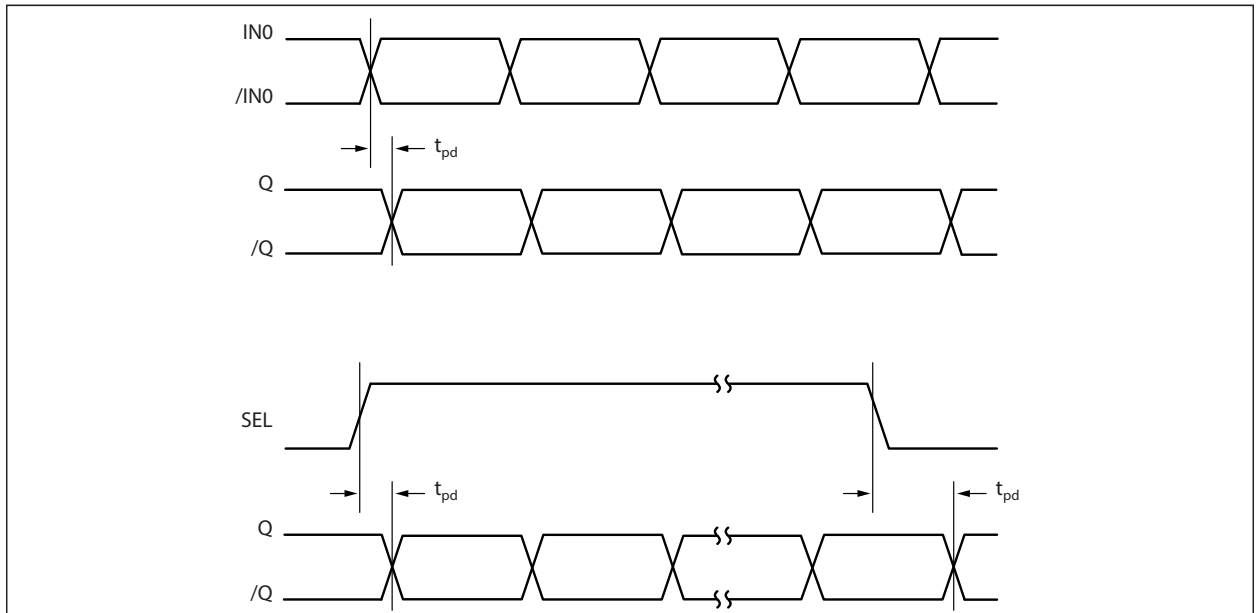


**FIGURE 4-1:** Single-Ended Voltage Swing.

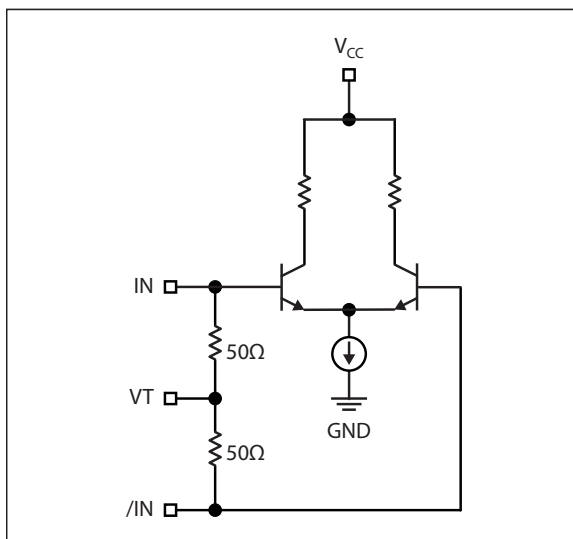


**FIGURE 4-2:** Differential Voltage Swing.

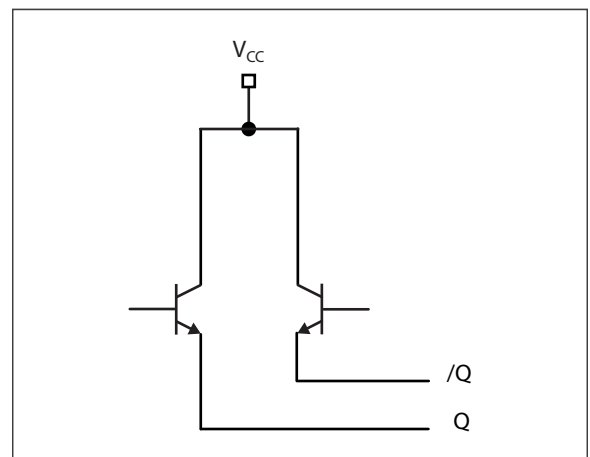
## Timing Diagrams



## Input and Output Stages

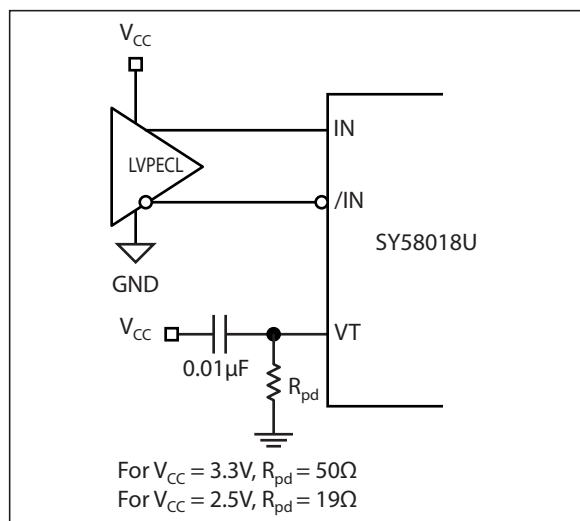


**FIGURE 4-3:** Simplified Differential Input Stage.

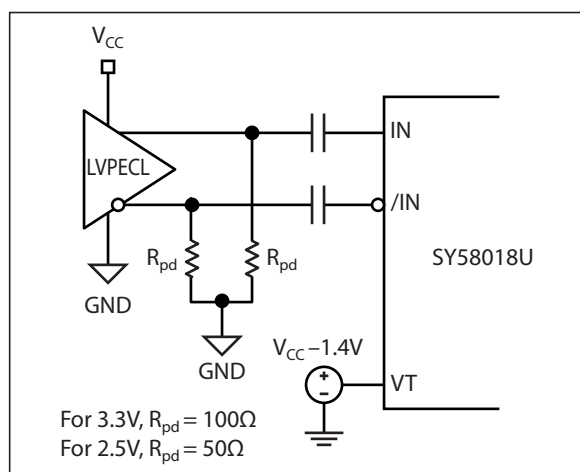


**FIGURE 4-4:** Simplified LVPECL Output Stage.

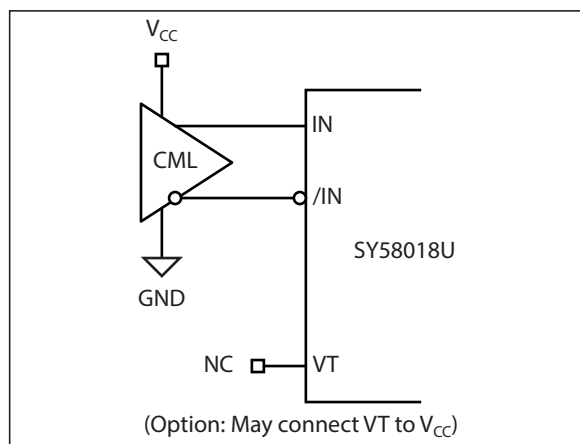
## 5.0 INPUT INTERFACE APPLICATIONS



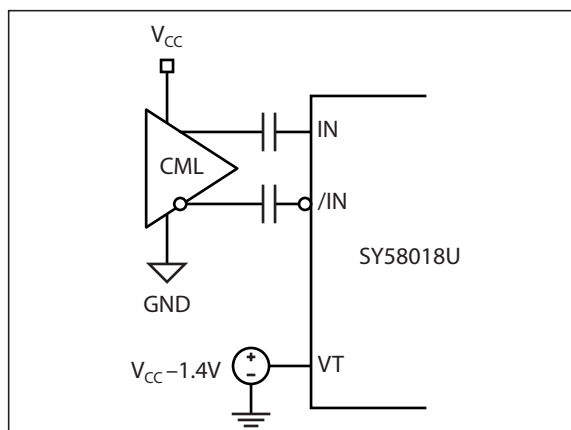
**FIGURE 5-1:** DC-Coupled LVPECL Interface.



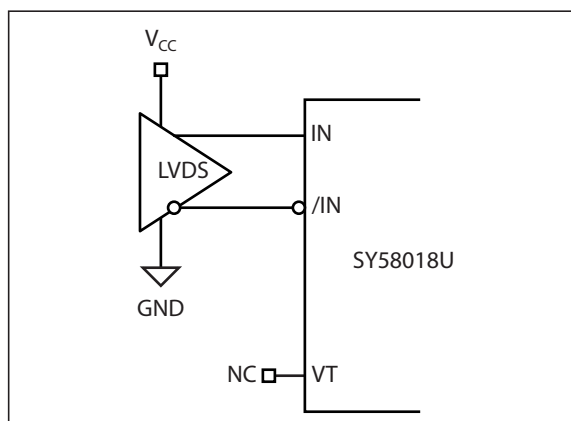
**FIGURE 5-2:** AC-Coupled LVPECL Interface.



**FIGURE 5-3:** DC-Coupled CML Interface.

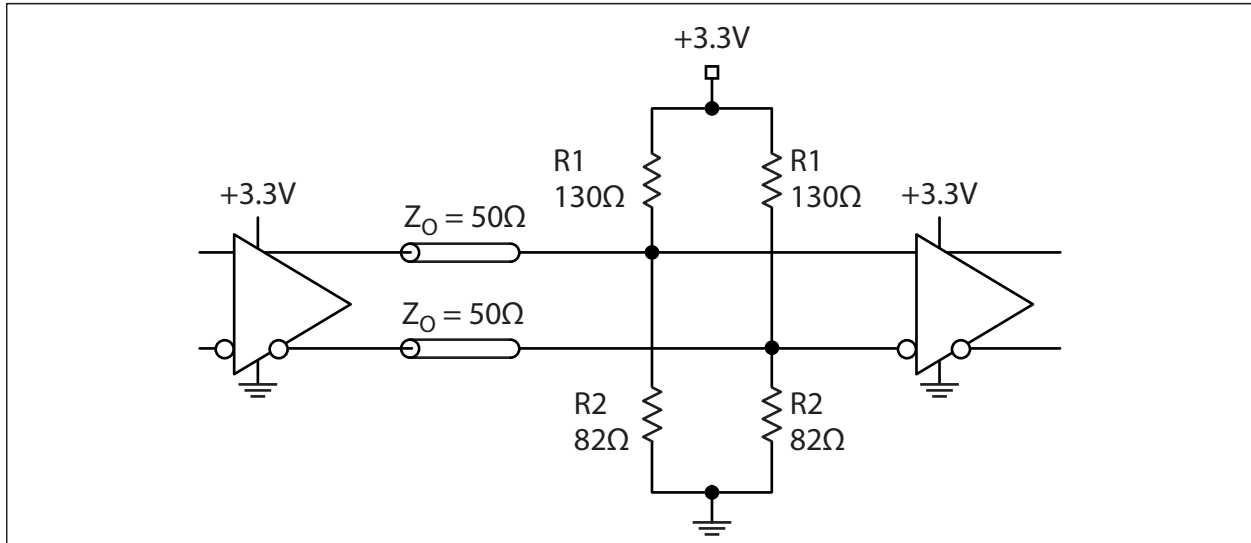


**FIGURE 5-4:** AC-Coupled CML Interface.

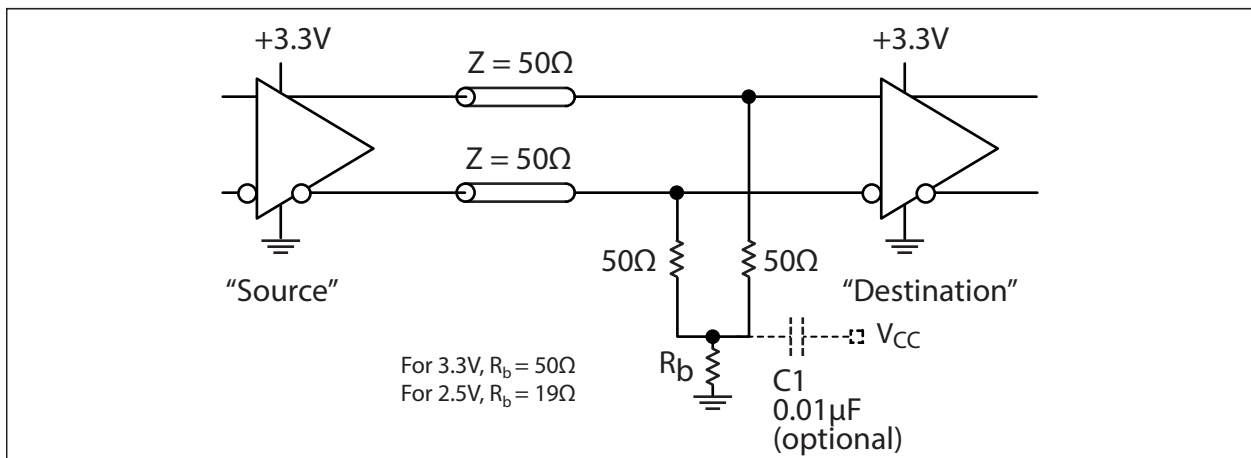


**FIGURE 5-5:** LVDS Interface.

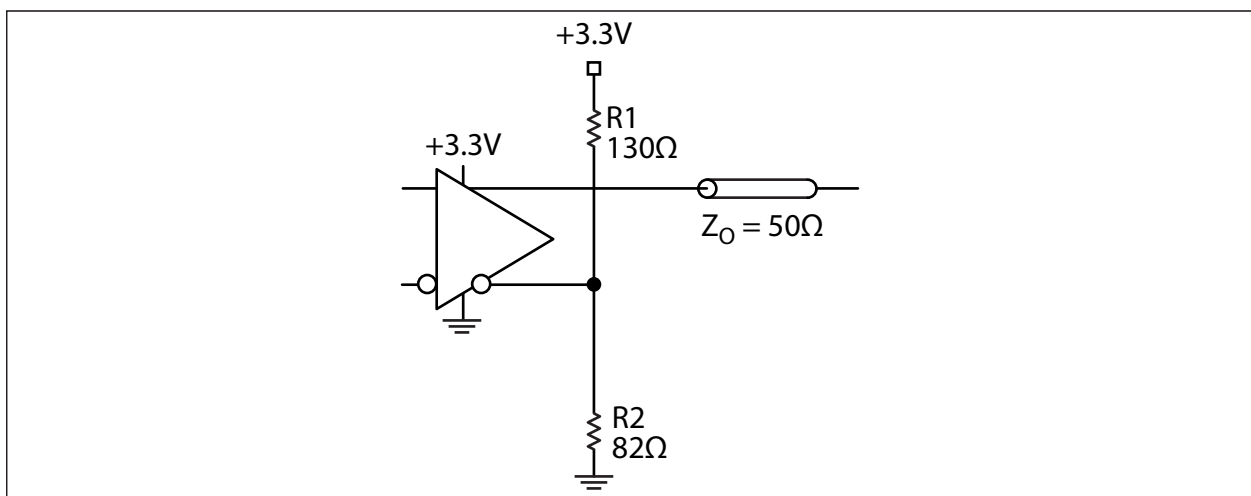
## 6.0 OUTPUT INTERFACE APPLICATIONS



**FIGURE 6-1:** Parallel Termination: Thevenin Equivalent.



**FIGURE 6-2:** Three-Resistor "Y-Termination".

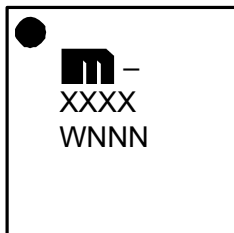


**FIGURE 6-3:** Terminating Unused I/O.

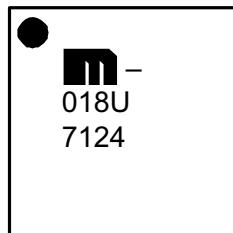
## 7.0 PACKAGING INFORMATION

### 7.1 Package Marking Information

16-Lead QFN\*



Example



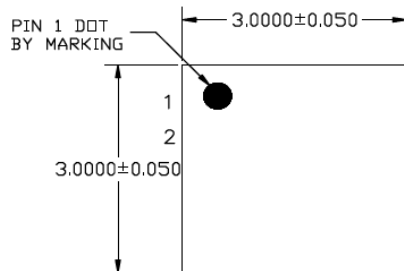
|                |                                                                                                                                                                                                                                                            |                                                                                                                    |
|----------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------------------------------------------------------------------------------------------------------------------|
| <b>Legend:</b> | XX...X                                                                                                                                                                                                                                                     | Product code or customer-specific information                                                                      |
|                | Y                                                                                                                                                                                                                                                          | Year code (last digit of calendar year)                                                                            |
|                | YY                                                                                                                                                                                                                                                         | Year code (last 2 digits of calendar year)                                                                         |
|                | WW                                                                                                                                                                                                                                                         | Week code (week of January 1 is week '01')                                                                         |
|                | NNN                                                                                                                                                                                                                                                        | Alphanumeric traceability code                                                                                     |
|                | (e3)                                                                                                                                                                                                                                                       | Pb-free JEDEC® designator for Matte Tin (Sn)                                                                       |
|                | *                                                                                                                                                                                                                                                          | This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package. |
|                | •, ▲, ▼                                                                                                                                                                                                                                                    | Pin one index is identified by a dot, delta up, or delta down (triangle mark).                                     |
| <b>Note:</b>   | In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information. Package may or may not include the corporate logo. |                                                                                                                    |
|                | Underbar ( _ ) and/or Overbar ( ¯ ) symbol may not be to scale.                                                                                                                                                                                            |                                                                                                                    |

## 16-Lead QFN 3 mm x 3 mm Package Outline and Recommended Land Pattern

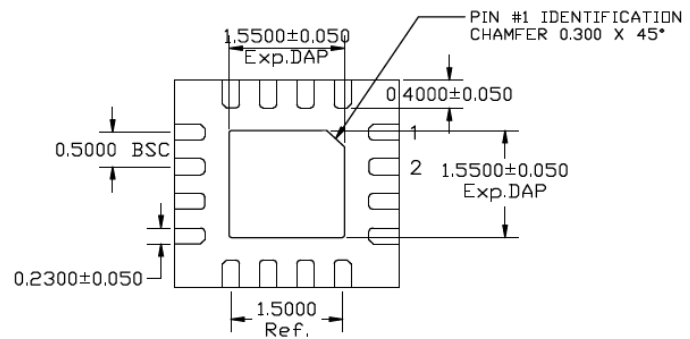
**TITLE**

16 LEAD QFN 3x3mm PACKAGE OUTLINE &amp; RECOMMENDED LAND PATTERN

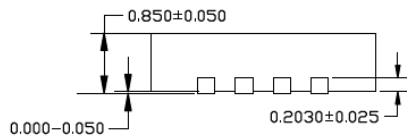
| DRAWING # | QFN33-16LD-PL-1 | UNIT | MM |
|-----------|-----------------|------|----|
|-----------|-----------------|------|----|

TOP VIEW

NOTE: 1, 2, 3

BOTTOM VIEW

NOTE: 1, 2, 3

SIDE VIEW

NOTE: 1, 2, 3

**NOTE:**

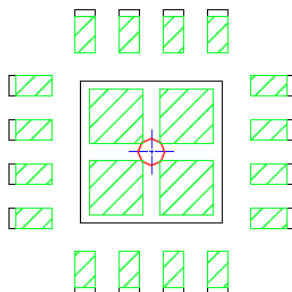
1. MAX PACKAGE WARPAGE IS 0.05 MM
2. MAX ALLOWABLE BURR IS 0.076 MM IN ALL DIRECTIONS
3. PIN #1 IS ON TOP WILL BE LASER MARKED
4. RED CIRCLE IN LAND PATTERN INDICATE THERMAL VIA. SIZE SHOULD BE 0.30-0.35 MM IN DIAMETER AND SHOULD BE CONNECTED TO GND FOR MAX THERMAL PERFORMANCE
5. GREEN RECTANGLES (SHADED AREA) indicate SOLDER STENCIL OPENING ON EXPOSED PAD AREA. SIZE SHOULD BE 0.60x0.60 MM IN SIZE, 0.20 MM SPACING.

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>.

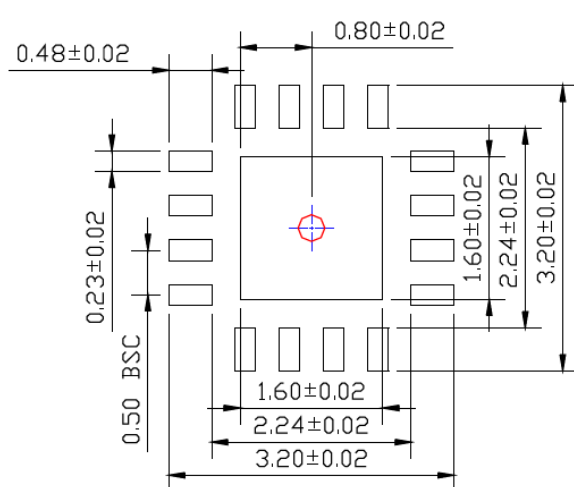
POD-Land Pattern drawing # QFN33-16LD-PL-1

## RECOMMENDED LAND PATTERN

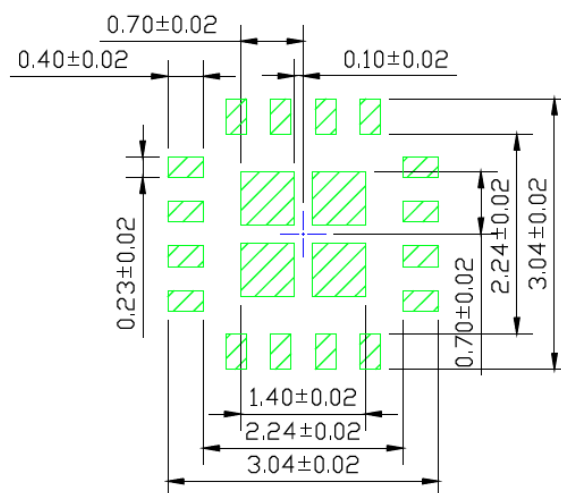
NOTE: 4, 5



STACKED-UP



EXPOSED METAL TRACE



SOLDER STENCIL OPENING

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>.

## APPENDIX A: REVISION HISTORY

### Revision A (December 2019)

- Converted Micrel document SY58018U to Microchip data sheet template DS20006286A.
- Minor text changes throughout.

NOTES:

## PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, contact your local Microchip representative or sales office.

| <u>PART NO.</u>     |          | <u>X</u>                                                              | <u>X</u>                              | <u>X</u>          | <u>XX</u>     |
|---------------------|----------|-----------------------------------------------------------------------|---------------------------------------|-------------------|---------------|
| Device              |          | Supply Voltage                                                        | Package                               | Temperature Range | Tape and Reel |
| Device:             | SY58018: | Ultra-Precision Differential LVPECL 2:1 MUX with Internal Termination |                                       |                   |               |
| Supply Voltage:     | U        | =                                                                     | 2.5V/3.3V                             |                   |               |
| Package:            | M        | =                                                                     | 3 mm x 3 mm QFN-16 (NiPdAu Lead-Free) |                   |               |
| Temperature Range:  | G        | =                                                                     | -40°C to 85°C                         |                   |               |
| Special Processing: | <blank>  | =                                                                     | 100/Tube                              |                   |               |
|                     | TR       | =                                                                     | 1,000/Reel                            |                   |               |

**Examples:**  
a) SY58018UMG: SY58018, 2.5V/3.3V Supply Voltage, 3 mm x 3 mm 16-Lead QFN, -40°C to +85°C Temperature Range, 100/Tube  
b) SY58018UMG-TR: SY58018, 2.5V/3.3V Supply Voltage, 3 mm x 3 mm 16-Lead QFN, -40°C to +85°C Temperature Range, 1,000/Reel  
  
**Note 1:** Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.

NOTES:

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