HV2818/HV2918

No High-Voltage Bias, Low Harmonic Distortion, 32-Channel, High-Voltage Analog Switch

Features

- 32-channel (16 2:1 MUX) High-Voltage Analog Switch
- Only +5V Bias Supply Required
- 3.3V and 5V CMOS Input Logic Level
- Asymmetric Switch Topology for Small Size
- 66 MHz Data Shift Clock Frequency
- Low-Parasitic Capacitance
- Low Harmonic Distortion
- DC to 50 MHz Analog Small-Signal Frequency
- 200 kHz to 50 MHz Large Signal Frequency
- -70 dB Typical Off Isolation at 5.0 MHz
- Excellent Noise Immunity
- Cascadable Serial Data Register with Latches
- Integrated Bleed Resistors on the SW Outputs (HV2918 only)

Applications

- Medical Ultrasound Imaging
- Non-Destructive Testing (NDT) Metal Flaw Detection
- Piezoelectric Transducer Drivers
- Inkjet Printer Head
- Optical MEMS Modules

General Description

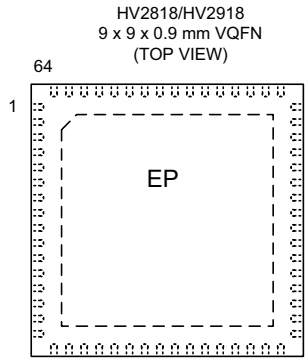
The HV2818/HV2918 are low harmonic distortion, low charge injection, 16 2:1 multiplexer/demultiplexer, high -voltage analog switches without high-voltage bias supplies. They are intended for use in applications requiring high-voltage switching controlled by low-voltage control signals, such as medical ultrasound imaging, driving piezoelectric transducers and printers.

The HV2818/HV2918 are pin-to-pin compatible to high-voltage bias HV2801/HV2901, except for bias voltage pins. HV2818/HV2918 are available in a 64-pin, 9 x 9 mm QFN package. HV2818/HV2918 have asymmetric topology to implement a small size in low voltage bias high-voltage switches while keeping performance such as peak current. The SW pin can pass high-voltage pulsed signals when the switch is ON. During the OFF state, high-voltage should not be applied to the SW pin due to its asymmetric topology. In medical ultrasound systems, the Y pin should be connected to the AFE (analog front end) and the SW pin should be connected to a single piezoelectric transducer element to avoid high-voltage in the SW pin during the switch OFF state.

HV2818 and HV2918 are identical, except for bleed resistors at SW pins. HV2818 does not have the bleed resistors at SW pins like HV2801. HV2918 has the bleed resistors at SW pins like HV2901. The bleed resistors eliminate possible voltage build-up on capacitive loads such as piezoelectric transducers. The ON/OFF state of the 32 switches is programmed individually through a digital serial interface.

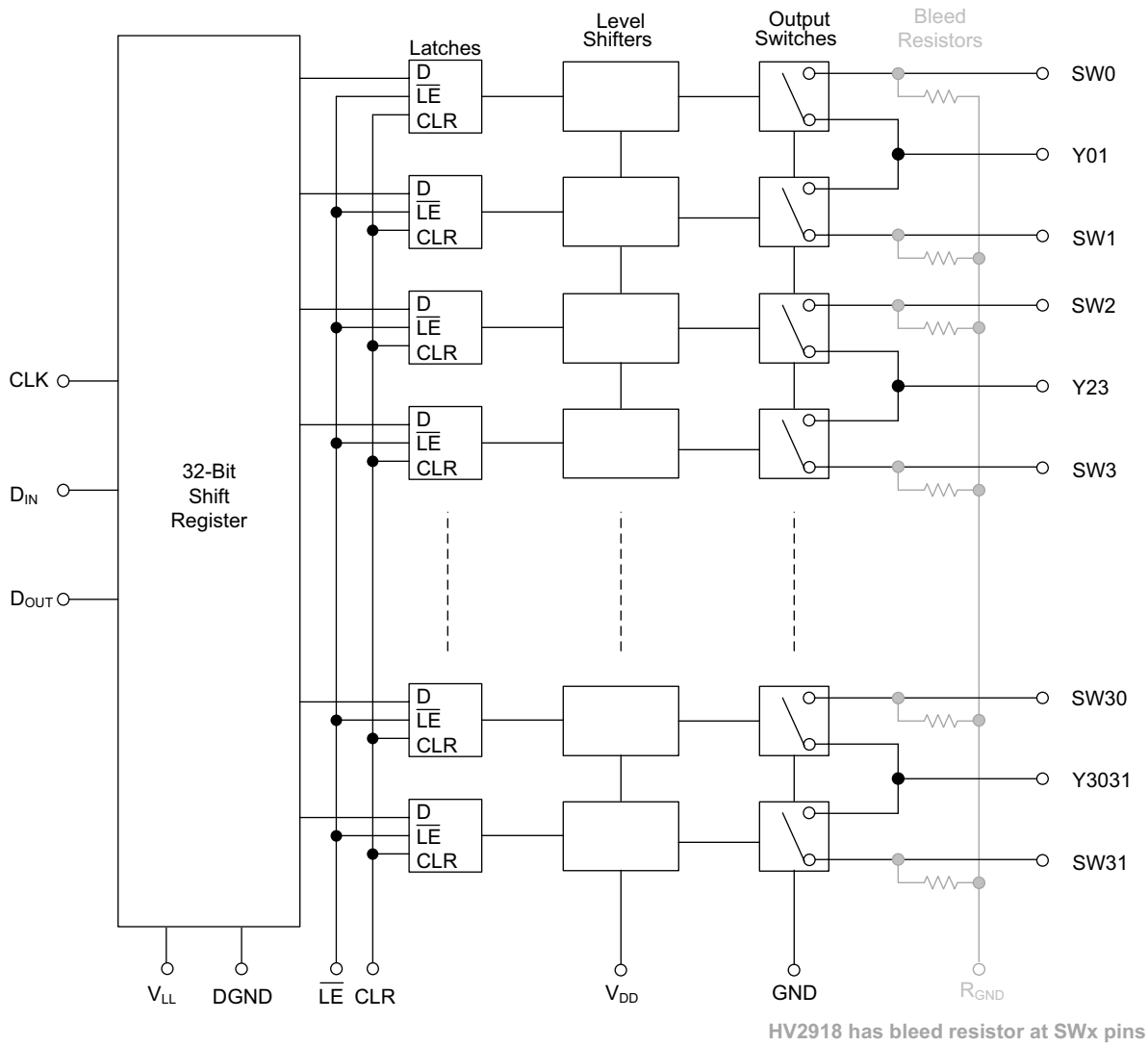
The devices only need a +5V low voltage bias supply. However, all of the analog switches can pass up to ±100V high-voltage pulsed signals. Like other low voltage bias switches, the HV2818/HV2918 cannot pass high-voltage DC signals. They can only pass high -voltage pulsed signals up to 2.5 µs pulse width. These devices have typical 6Ω ON resistance and 50 MHz bandwidth for small signals.

Package Type



*Includes Exposed Thermal Pad (EP); see Table 2-1.

Functional Block Diagram



1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings †

Logic Supply Voltage (V_{LL}) ..... -0.5V to 6.6V
Positive Supply Voltage (V_{DD})..... -0.5V to 6.6V
Logic Input Voltage (V_{IN})..... -0.5V to V_{LL} +0.3V
Analog Signal Voltage Y Pin (V_Y)..... -110V to +110V
Analog Signal Voltage SW Pin (V_{SW}) when Switch ON..... -110V to +110V
Analog Signal Voltage SW Pin (V_{SW}) when Switch OFF ..... -2V to +2V
Peak Analog Signal Current/Channel (I_{PK}) 2.7A

† Notice: Stresses above those listed under Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational sections of this specification is not intended. Exposure to maximum rating conditions for extended periods may affect device reliability.

Note 1: Devices are ESD-sensitive. Handling precautions are recommended.

RECOMMENDED OPERATING CONDITIONS

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Logic Supply Voltage	V_{LL}	3	—	5.5	V	
Positive Supply Voltage	V_{DD}	4.5	—	6.3	V	
Analog Signal Voltage Y Pin Peak-to-Peak	V_Y	-100	—	100	V	
High-Level Input Voltage	V_{IH}	$0.9V_{LL}$	—	V_{LL}	V	
Low-Level Input Voltage	V_{IL}	0	—	$0.1V_{LL}$	V	

Note 1: Power up/down sequence is V_{LL} first and then V_{DD}. Powered-down sequence is reverse of power-up.
2: V_Y and V_{SW} must be within V_{DD} and GND or floating during power-up/down transition.
3: Rise and fall times of power supplies, V_{LL} and V_{DD} should be greater than 1.0 ms.

DC ELECTRICAL CHARACTERISTICS

Unless otherwise specified, V_{DD}=+5V, V_{LL}=+5V, T_A = 25°C. **Boldface** specifications apply over the full operating temperature range.

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Small-Signal Switch On-Resistance	R_{ONS}	—	6	**9**	Ω	I_{SIG} = 5 mA
		—	6	**9**	Ω	I_{SIG} = 200 mA
Small Signal Switch On-Resistance Matching	ΔR_{ONS}	—	—	**20**	%	I_{SIG} = 5 mA,
Large signal switch ON-resistance	R_{ONL}	—	5	—	Ω	V_{SIG} = 90V, R_{LOAD} = 80Ω [Note 1]
Value of Output Bleed Resistor (**HV2918** only)	R_{INT}	20	35	50	kΩ	Output switch to RGND I_{RINT} = 20 µA
Switch Off Leakage per SW Pin	I_{SOL}	—	—	**3**	µA	V_{SIG} = +100V, 500 µs pulse, See Figure 3-1
		—	—	**3**	µA	V_{SIG} = -100V, 100µs pulse, See Figure 3-1 [Note 1]

Note 1: Specification is obtained by characterization and is not 100% tested.
2: Design guidance only.

DC ELECTRICAL CHARACTERISTICS (CONTINUED)

Unless otherwise specified, V_{DD}=+5V, V_{LL}=+5V, T_A = 25°C. **Boldface** specifications apply over the full operating temperature range.

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Switch Off Bias per Y Pin	I_{SOB}	—	—	**3**	µA	V_{SIG} = +100V, 500 µs pulse, See Figure 3-2
		—	—	**3**	mA	V_{SIG} = -100V, 100 µs pulse, See Figure 3-2 [Note 1]
		HV2818				
Switch Off Bias per SW Pin		—	—	**3**	µA	V_{SIG} = +300 mV,-300 mV, See Figure 3-3
		HV2918				
Switch Off Bias of All SW Pins		—	—	**10**	µA	V_{SIG} = +300 mV,-300 mV, See Figure 3-3
DC Offset Switch Off	V_{OS}	—	1	**10**	mV	R_{LOAD} = 50 kΩ (HV2818), No load (HV2918) See Figure 3-4
DC Offset Switch On		—	1	**10**		
Quiescent V_{DD} Supply Current	I_{DDQ}	—	—	**10**	µA	All switches OFF
		—	—	**10**	µA	All switches ON, V_{SW} = 1V
Quiescent V_{LL} Supply Current	I_{LLQ}	—	—	**10**	µA	All logic inputs are static
Switch Output Peak Current	I_{SW}	**2**	2.7	—	A	V_{SIG} duty cycle <0.1% [Note 1]
Output Switching Frequency	f_{SW}	—	—	**50**	kHz	Duty cycle = 50% [Note 1]
Average V_{DD} Supply Current	I_{DD}	—	7	**10**	mA	All output switches are turning ON and OFF at 50 kHz with no load
Average V_{LL} Supply Current	I_{LL}	—	1.3	**2.5**	mA	f_{CLK} = 5.0 MHz
Data Out Source Current	I_{SOR}	**10**	—	—	mA	V_{OUT} = V_{LL} - 0.7V
Data Out Sink Current	I_{SINK}	**10**	—	—	mA	V_{OUT} = 0.7V
Logic Input Capacitance	C_{IN}	-	8	—	pF	[Note 2]

Note 1: Specification is obtained by characterization and is not 100% tested.
2: Design guidance only.

AC ELECTRICAL CHARACTERISTICS

Unless otherwise specified, V_{DD}=+5V, V_{LL}=+5V, T_{AMB} = 25°C. **Boldface** specifications apply over the full operating temperature range.

Parameters	Sym,	Min.	Typ.	Max.	Units.	Conditions
Setup Time before $\overline{LE}$ Rises	t_{SD}	**25**	—	—	ns	[Note 1]
Time Width of $\overline{LE}$	t_{WLE}	**12**	—	—	ns	[Note 1]
Clock Delay Time to Data Out	t_{DO}	—	—	**13.5**	ns	
Time Width of CLR	t_{WCLR}	**55**	—	—	ns	[Note 1]

Note 1: Specification is obtained by characterization and is not 100% tested.
2: Design guidance only.

AC ELECTRICAL CHARACTERISTICS (CONTINUED)

Unless otherwise specified, V_{DD}=+5V, V_{LL}=+5V, T_{AMB} = 25°C. **Boldface** specifications apply over the full operating temperature range.

Parameters	Sym,	Min.	Typ.	Max.	Units.	Conditions
Setup Time Data to Clock	t_{SU}	**1.5**	—	—	ns	[Note 1]
Hold Time Data from Clock	t_H	**1.5**	—	—	ns	[Note 1]
Clock Frequency	f_{CLK}	—	—	**66**	MHz	50% duty cycle, $f_{DIN} = (1/2)f_{CLK}$, C_{DOUT} = 20 pF [Note 1]
Clock Rise and Fall Times	t_R, t_F	—	—	**50**	ns	
Turn-On Time	t_{ON}	—	—	**5**	µs	V_{SIG} = 5V, R_{LOAD} = 550Ω See Figure 3-5
Turn-Off Time	t_{OFF}	—	—	**5**		
Input Large-Signal Pulse Width	t_{PW}	—	—	**2.5**	µs	V_{PULSE} = 0V to ±100V. Measured at 90% amplitude. See Figure 3-6 [Note 1]
Maximum V_{SIG} Slew Rate	dv/dt	—	—	20	V/ns	[1]
Analog Small-Signal Frequency	f_{BWS}	—	50	—	MHz	[1]
Off Isolation Y to SW	K_O	—	-65	-60	dB	f = 5.0 MHz, 1.0 kΩ//15 pF load. See Figure 3-7 [Note 1]
		—	-70	-65		f = 5.0 MHz, 50Ω load. See Figure 3-7 [Note 1]
Off Isolation SW to Y		—	-65	-60	dB	f = 5.0 MHz, 1.0 kΩ//15 pF load. See Figure 3-8 [Note 1]
		—	-70	-75		f = 5.0 MHz, 50Ω load. See Figure 3-8 [Note 1]
Switch Crosstalk	K_{CR}	—	-70	-60	dB	f = 5.0 MHz, 50Ω load. See Figure 3-9 [Note 1]
Off Capacitance SW to GND	$C_{SG(OFF)}$	—	4	—	pF	V_{SIG} = 50 mV @1 MHz, no load, both SW OFF [Note 1]
Off Capacitance Y to GND		—	21	—		
On Capacitance SW to GND	$C_{SG(ON)}$	—	22	—	pF	V_{SIG} = 50 mV@1 MHz, no load, one SW ON, one SW OFF [Note 1]
On Capacitance Y to GND		—	22	—		
Output Voltage Spike at SW	$+V_{SPK}$	—	—	40	mV	R_{LOAD} = 50Ω. See Figure 3-10 [Note 1]
	$-V_{SPK}$	-10	—	—		
Output Voltage Spike at Y	$+V_{SPK}$	—	—	40	mV	R_{LOAD} = 50Ω. See Figure 3-10 [Note 1]
	$-V_{SPK}$	-10	—	—		
Charge Injection at SW	QC	—	50	—	pC	See Figure 3-11 [Note 1]
Charge Injection at Y		—	100	—	pC	See Figure 3-11 [Note 1]
Second Harmonic Distortion	HD2	—	-65	—	dBc	V_{SIG} = 1.5VPP @5 MHz, 50Ω load [Note 1]
		—	-63	—	dBc	V_{SIG} = 1.5VPP@5 MHz, 1 kΩ//15 pF load [Note 1]

Note 1: Specification is obtained by characterization and is not 100% tested.
2: Design guidance only.

Temperature Specification

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Temperature Range						
Operating Temperature Range	T_A	0	—	+70	°C	
Storage Temperature Range	T_S	-65	—	+150	°C	
Maximum Junction Temperature	T_J	—	—	+125	°C	
Package Thermal Resistance						
Thermal Resistance, 64-Lead QFN	Θ_{JA}	—	21	—	°C/W	

TABLE 1-1: TRUTH TABLE

D0	D1	...	D15	D16	...	D31	Din	$\overline{LE}$	CLR	SW0	SW1	...	SW15	SW16	...	SW31
L	—		—	—		—	X	L	L	OFF	—		—	—		—
H	—		—	—		—	X	L	L	ON	—		—	—		—
—	L		—	—		—	X	L	L	—	OFF		—	—		—
—	H		—	—		—	X	L	L	—	ON		—	—		—
—	—		—	—		—	X	L	L	—	—		—	—		—
—	—		—	—		—	X	L	L	—	—		—	—		—
—	—		L	—		—	X	L	L	—	—		OFF	—		—
—	—	...	H	—	...	—	X	L	L	—	—	...	ON	—	...	—
—	—		—	L		—	X	L	L	—	—		—	OFF		—
—	—		—	H		—	X	L	L	—	—		—	ON		—
—	—		—	—		—	X	L	L	—	—		—	—		—
—	—		—	—		—	X	L	L	—	—		—	—		—
—	—		—	—		L	X	L	L	—	—		—	—		OFF
—	—		—	—		H	X	L	L	—	—		—	—		ON
X	X	X	X	X	X	X	X	H	L	HOLD PREVIOUS STATE						
X	X	X	X	X	X	X	X	X	H	ALL SWITCHES OFF						

Note 1: The 32 switches operate independently.

2: Serial data are clocked in on the L to H transition of the CLK.

3: All 32 switches go to a state retaining their latched condition at the rising edge of $\overline{LE}$. When $\overline{LE}$ is low the shift registers data flow through the latch.

4: DOUT is high when data in Register 31 are high.

5: Shift register clocking has no effect on the switch states if $\overline{LE}$ is high.

6: The CLR (clear) input overrides all the inputs.

1.1 Typical Timing Diagram

Figure 1-1 shows timing of AC characteristic parameters graphically.

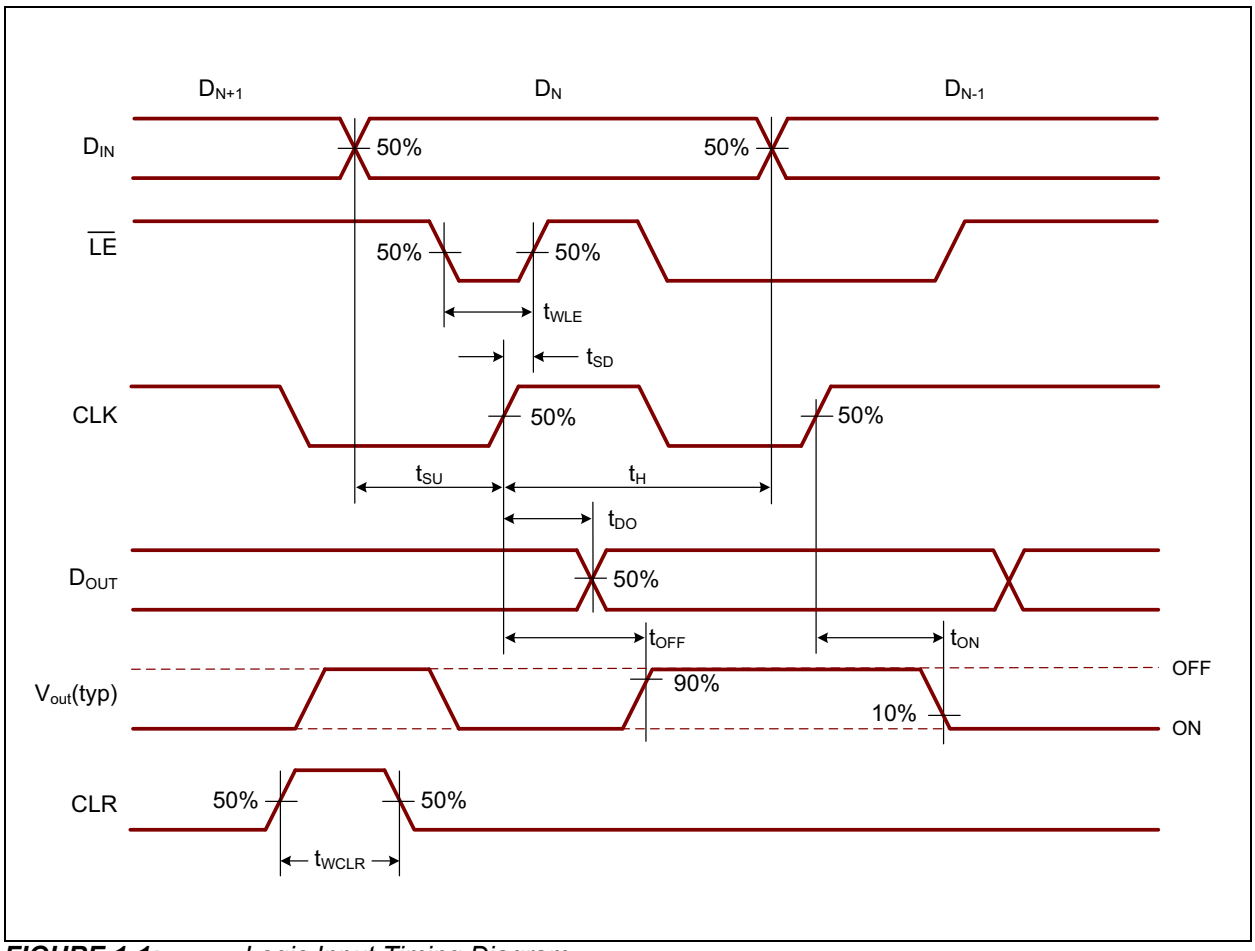
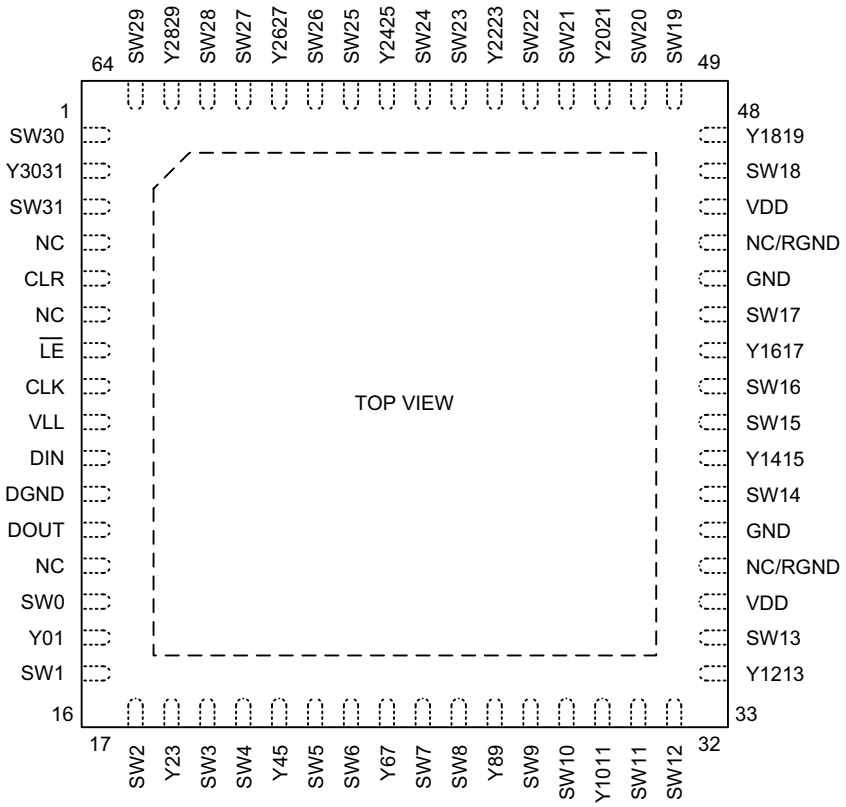


FIGURE 1-1: *Logic Input Timing Diagram.*

2.0 PIN DESCRIPTION

This section details the pin description for 64-Lead QFN package (Figure 2-1).The descriptions of the pins are listed in Table 1-1.



- The central thermal pad on the bottom of package must be connected to GND externally.

FIGURE 2-1: *64-Lead QFN Package - Top View.*

TABLE 2-1: PIN FUNCTION TABLE

Pin Number	Symbol		Description
	HV2818	HV2918	
1	SW30	SW30	Analog Switch 30 SW Terminal; Connect to a Piezoelectric Element
2	Y3031	Y3031	Common Y Terminal of Analog Switch 30 and 31
3	SW31	SW31	Analog Switch 31 SW Terminal; Connect to a Piezoelectric Element
4	NC	NC	No Connection; Keep Floating
5	CLR	CLR	Latch Clear Logic Input
6	NC	NC	No Connection
7	$\overline{LE}$	$\overline{LE}$	Latch Enable Logic Input; Low Active
8	CLK	CLK	Clock Logic Input for Shift Register
9	V_{LL}	V_{LL}	Logic Supply Voltage

TABLE 2-1: PIN FUNCTION TABLE (CONTINUED)

Pin Number	Symbol		Description
	HV2818	HV2918	
10	D_{IN}	D_{IN}	Data in Logic Input
11	DGND	DGND	Digital Ground for Logic Circuitry.
12	D_{OUT}	D_{OUT}	Data Out Logic Output
13	NC	NC	No Connection; Keep Floating
14	SW0	SW0	Analog Switch 0 SW Terminal; Connect to a Piezoelectric Element
15	Y01	Y01	Common Y Terminal of Analog Switch 0 and 1
16	SW1	SW1	Analog Switch 1 SW Terminal; Connect to a Piezoelectric Element
17	SW2	SW2	Analog Switch 2 SW Terminal; Connect to a Piezoelectric Element
18	Y23	Y23	Common Y Terminal of Analog Switch 2 and 3
19	SW3	SW3	Analog Switch 3 SW Terminal; Connect to a Piezoelectric Element
20	SW4	SW4	Analog Switch 4 SW Terminal; Connect to a Piezoelectric Element
21	Y45	Y45	Common Y Terminal of Analog Switch 4 and 5
22	SW5	SW5	Analog Switch 5 SW Terminal; Connect to a Piezoelectric Element
23	SW6	SW6	Analog Switch 6 SW Terminal; Connect to a Piezoelectric Element
24	Y67	Y67	Common Y Terminal of Analog Switch 6 and 7
25	SW7	SW7	Analog Switch 7 SW Terminal; Connect to a Piezoelectric Element
26	SW8	SW8	Analog Switch 8 SW Terminal; Connect to a Piezoelectric Element
27	Y89	Y89	Common Y Terminal of Analog Switch 8 and 9
28	SW9	SW9	Analog Switch 9 SW Terminal; Connect to a Piezoelectric Element
29	SW10	SW10	Analog Switch 10 SW Terminal; Connect to a Piezoelectric Element
30	Y1011	Y1011	Common Y Terminal of Analog Switch 10 and 11
31	SW11	SW11	Analog Switch 11 SW Terminal; Connect to a Piezoelectric Element
32	SW12	SW12	Analog Switch 12 SW Terminal; Connect to a Piezoelectric Element
33	Y1213	Y1213	Common Y Terminal of Analog Switch 12 and 13
34	SW13	SW13	Analog Switch 13 SW Terminal; Connect to a Piezoelectric Element
35	V_{DD}	V_{DD}	Positive Supply Voltage
36	NC	RGND	No Connection/Ground for Bleed Resistor
37	GND	GND	Ground
38	SW14	SW14	Analog Switch 14 SW Terminal; Connect to a Piezoelectric Element
39	Y1415	Y1415	Common Y Terminal of Analog Switch 14 and 15
40	SW15	SW15	Analog Switch 15 SW Terminal; Connect to a Piezoelectric Element
41	SW16	SW16	Analog Switch 16 SW Terminal; Connect to a Piezoelectric Element
42	Y1617	Y1617	Common Y Terminal of Analog Switch 16 and 17
43	SW17	SW17	Analog Switch 17 SW Terminal; Connect to a Piezoelectric Element
44	GND	GND	Ground

TABLE 2-1: PIN FUNCTION TABLE (CONTINUED)

Pin Number	Symbol		Description
	HV2818	HV2918	
45	NC	RGND	No Connection/Ground for Bleed Resistor
46	V_{DD}	V_{DD}	Positive Supply Voltage
47	SW18	SW18	Analog Switch 18 SW Terminal; Connect to a Piezoelectric Element
48	Y1819	Y1819	Common Y Terminal of Analog Switch 18 and 19
49	SW19	SW19	Analog Switch 19 SW Terminal; Connect to a Piezoelectric Element
50	SW20	SW20	Analog Switch 20 SW Terminal; Connect to a Piezoelectric Element
51	Y2021	Y2021	Common Y Terminal of Analog Switch 20 and 21
52	SW21	SW21	Analog Switch 21 SW Terminal; Connect to a Piezoelectric Element
53	SW22	SW22	Analog Switch 22 SW Terminal; Connect to a Piezoelectric Element
54	Y2223	Y2223	Common Y Terminal of Analog Switch 22 and 23
55	SW23	SW23	Analog Switch 23 SW Terminal; Connect to a Piezoelectric Element
56	SW24	SW24	Analog Switch 24 SW Terminal; Connect to a Piezoelectric Element
57	Y2425	Y2425	Common Y Terminal of Analog Switch 24 and 25
58	SW25	SW25	Analog Switch 25 SW Terminal; Connect to a Piezoelectric Element
59	SW26	SW26	Analog Switch 26 SW Terminal; Connect to a Piezoelectric Element
60	Y2627	Y2627	Common Y Terminal of Analog Switch 26 and 27
61	SW27	SW27	Analog Switch 27 SW Terminal; Connect to a Piezoelectric Element
62	SW28	SW28	Analog Switch 28 SW Terminal; Connect to a Piezoelectric Element
63	Y2829	Y2829	Common Y Terminal of Analog Switch 28 and 29
64	SW29	SW29	Analog Switch 29 SW Terminal; Connect to a Piezoelectric Element
EP			The Central Thermal Pad on the Bottom of the Package Must be Connected to GND Externally

3.0 TEST CIRCUIT EXAMPLES

This section details a few examples of test circuits:

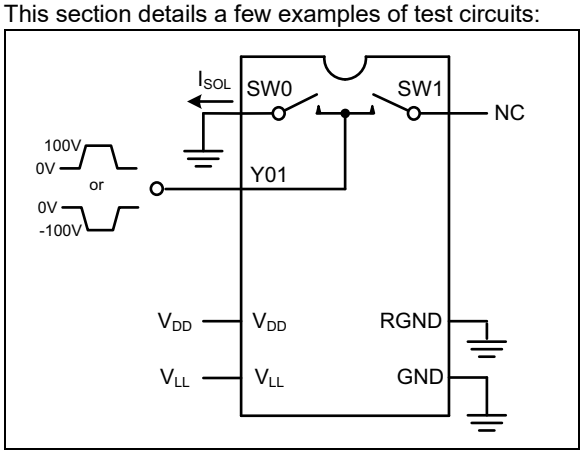


FIGURE 3-1: *Switch-Off Leakage per Switch.*

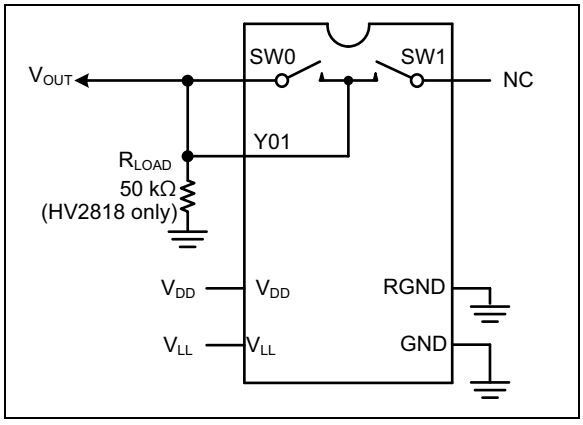


FIGURE 3-4: *Switch DC Offset.*

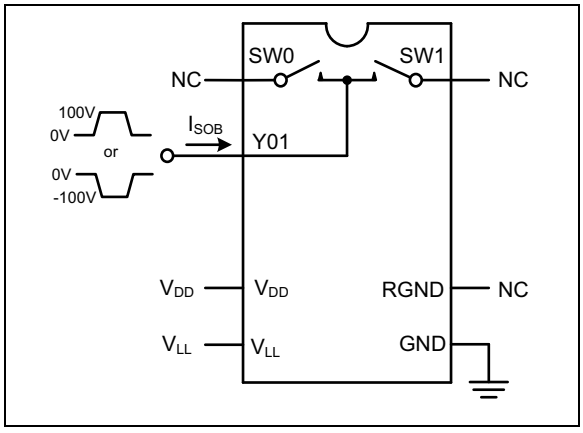


FIGURE 3-2: *Switch-Off Bias Y.*

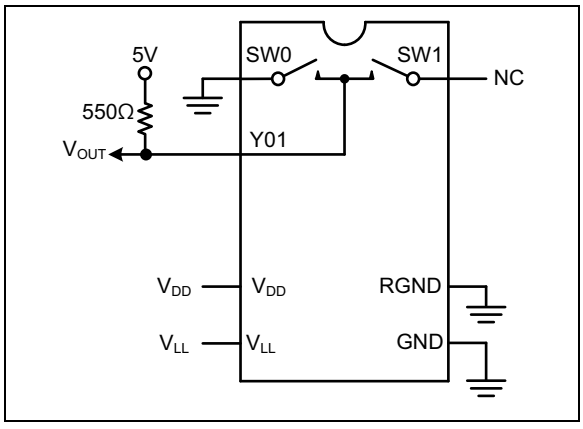


FIGURE 3-5: *T_{ON}/T_{OFF} Test Circuit.*

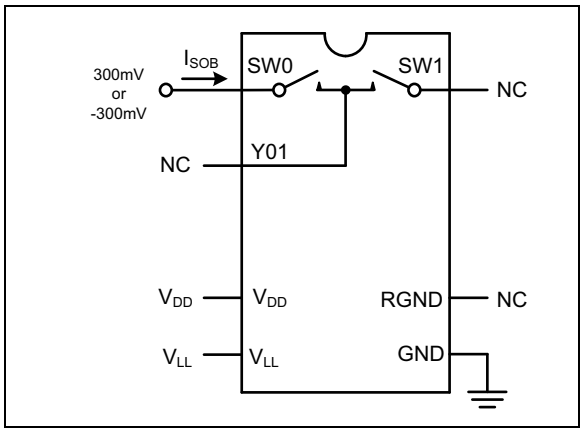


FIGURE 3-3: *Switch-Off Bias SW.*

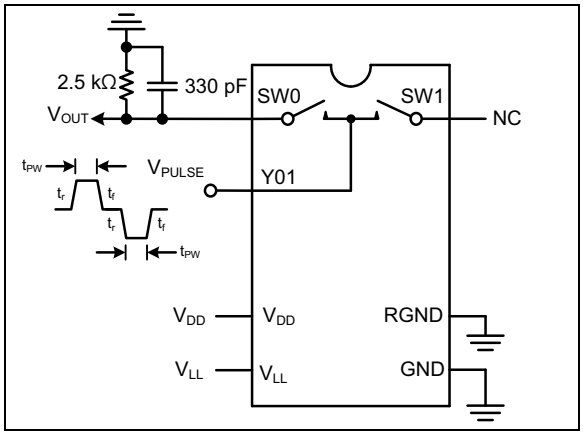


FIGURE 3-6: *Tx Pulse Width.*

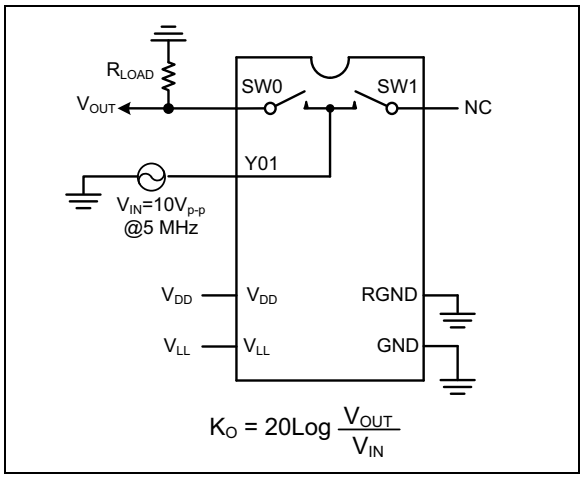


FIGURE 3-7: *Off Isolation Y to SW.*

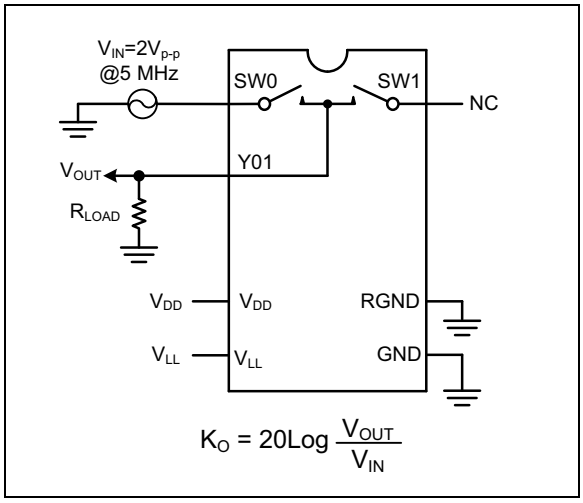


FIGURE 3-8: *Off Isolation SW to Y.*

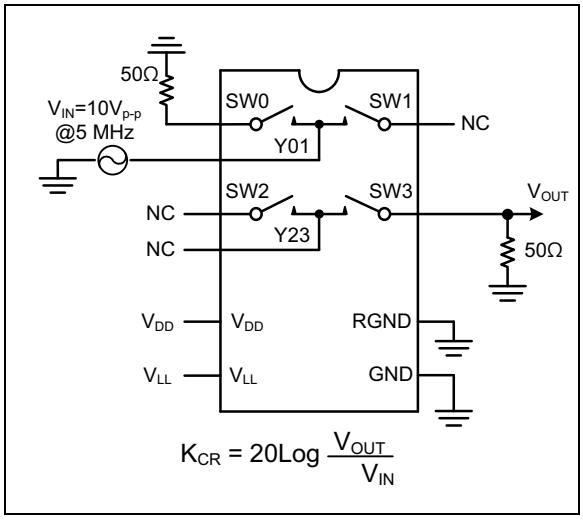


FIGURE 3-9: *Switch Crosstalk.*

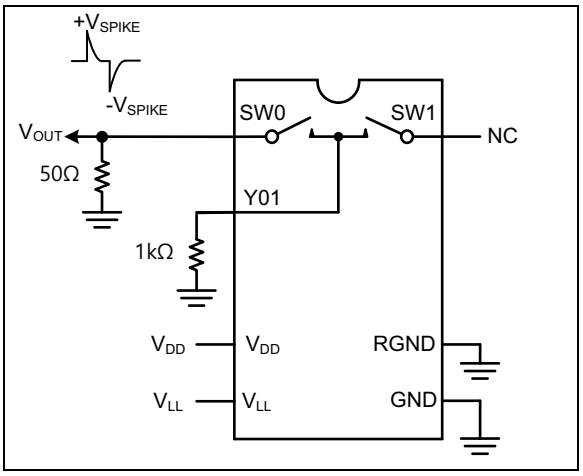


FIGURE 3-10: *Output Voltage Spike.*

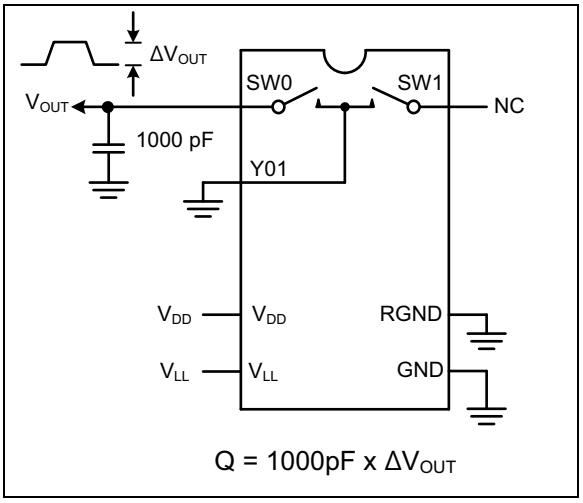


FIGURE 3-11: *Charge Injection.*

4.0 TYPICAL PERFORMANCE CURVES

Note: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

Note: Unless otherwise indicated: V_{DD}=+5V, V_{LL}=+5V, T_A=25°C.

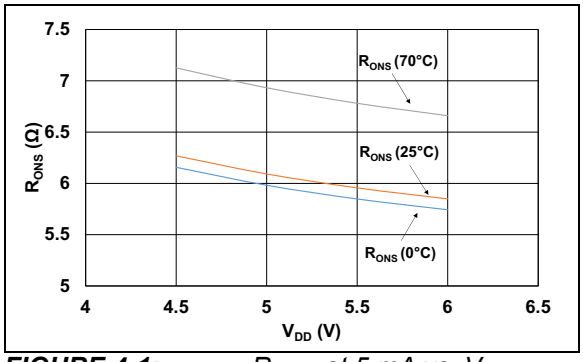


FIGURE 4-1: *R_{ONS} at 5 mA vs. V_{DD}.*

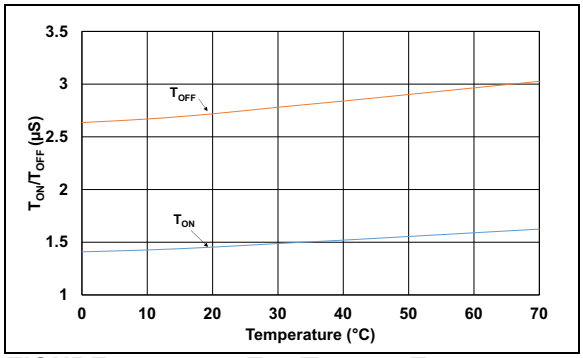


FIGURE 4-4: *T_{ON}/T_{OFF} vs. Temperature.*

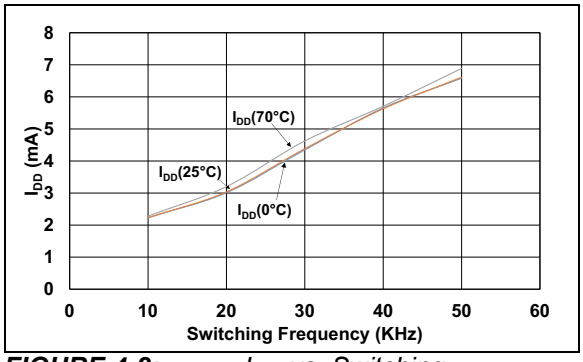


FIGURE 4-2: *I_{DD} vs. Switching Frequency.*

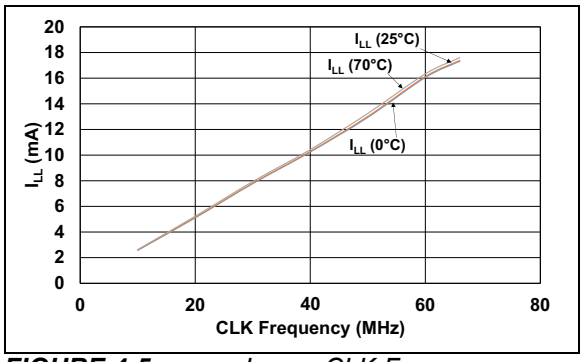


FIGURE 4-5: *I_{LL} vs. CLK Frequency.*

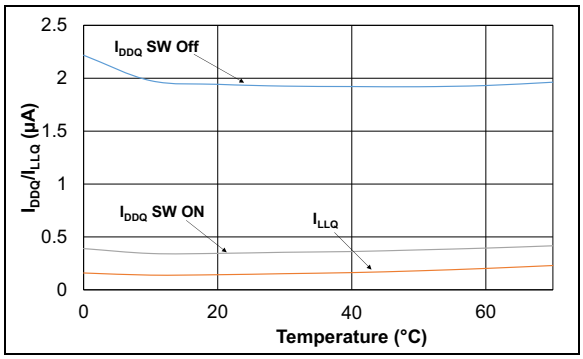


FIGURE 4-3: *I_{DDQ}/I_{LLQ} vs. Temperature.*

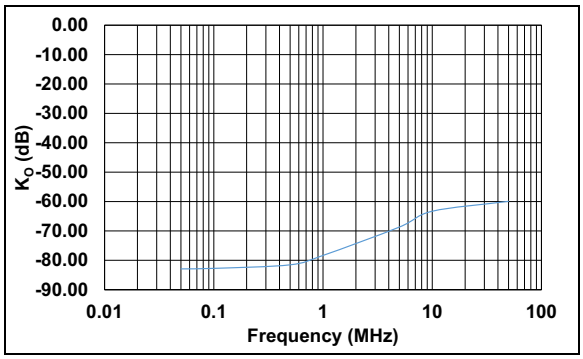


FIGURE 4-6: *K_O Y to SW vs. Frequency with 50Ω Load.*

5.0 DETAILED DESCRIPTION AND APPLICATION INFORMATION

5.1 Device Overview

The HV2818/HV2918 are 200V, low harmonic distortion, low charge injection, 32-channel (16 2:1 multiplexer/demultiplexer), high-voltage analog switches without high-voltage supplies. The devices require only +5V bias voltage for operation. The high-voltage analog switches are used for multiplexing a piezoelectric transducer array in a probe to multiple channel transmitter (Tx) arrays in a medical ultrasound system.

The HV2818/HV2918 are distinguished by bleed resistors that eliminate voltage build-up in capacitance loads such as piezoelectric transducers. These devices can pass ±100V high-voltage pulsed signal without high-voltage bias supplies such as ±100V. These devices have typical 6Ω ON resistance and 50 MHz bandwidth for small signals. Like other low voltage bias switches, HV2818/HV2918 cannot pass high-voltage DC signals. They can only pass high-voltage pulsed signals up to 2.5 µs pulse width.

The HV2818/HV2918 have asymmetric topology to implement smaller size compared to previous low voltage bias high-voltage switches. The SW pin can pass high-voltage pulsed signal applied to Y pin when switch is ON state. When the switch is OFF state, high-voltage signal should not be applied to the SW pin due to the asymmetric topology. In medical ultrasound systems, the Y pin should be connected to AFE (analog front end) and the SW pin should be connected to only one piezoelectric transducer element to avoid high-voltage at the SW pin during switch OFF state in the system.

Figure 5-1 shows a typical medical ultrasound image system consisting of 64 channels of transmit pulsers (Tx), 64 channels of receivers (Rx and ADC) and 64 channels of T/R switches connecting to 256 elements of an ultrasound probe via HV2xxx high-voltage analog switch array.

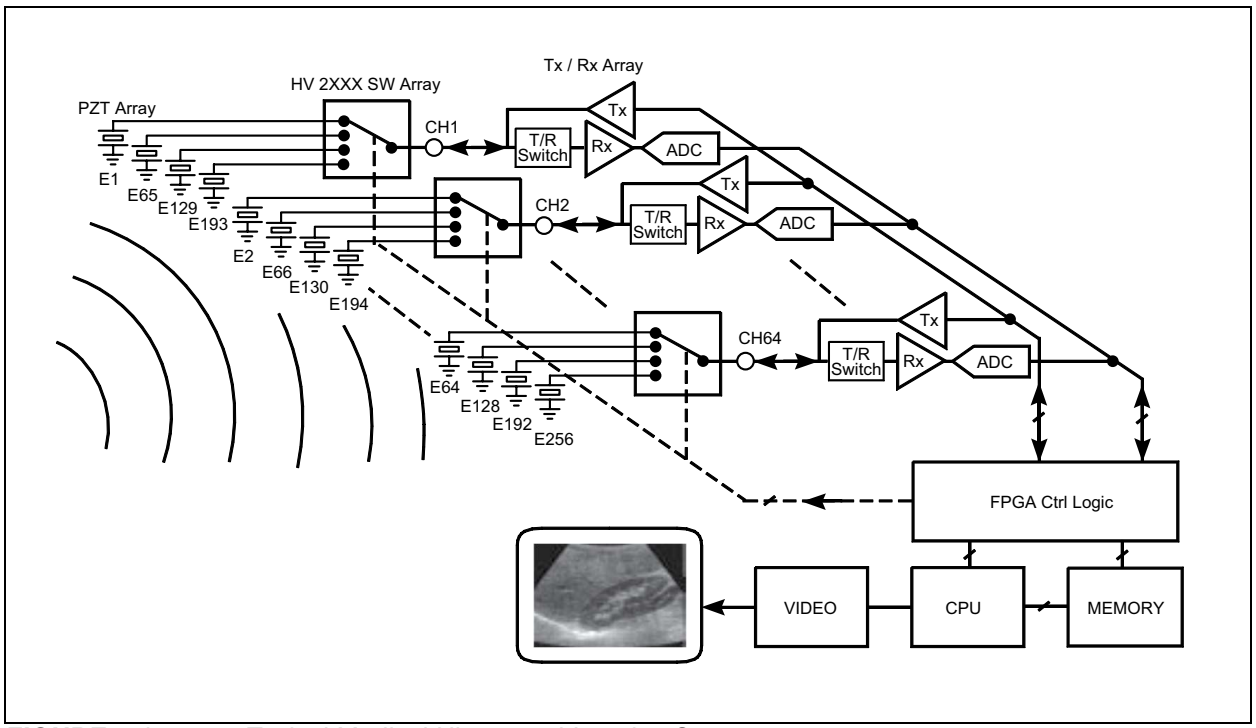


FIGURE 5-1: *Typical Medical Ultrasound Imaging System.*

5.2 Logic Input Timing

The HV2818/HV2918 has a digital serial interface consisting of Data In (D_{IN}), Clock (CLK), Data Out (D_{OUT}), Latch Enable ($\overline{LE}$), and Clear (CLR) to control 32 switches independently. The digital circuits are supplied by V_{LL}. The serial clock frequency is up to 66 MHz.

The switch state configuration data, 32-bit D_{IN} is shifted into the 32 shift registers on the rising edge (low-to-high transition) of the clock. The D_{OUT} has the same logic state of 31th shift register data. The switch Configuration bit of SW31 is shifted in first and the Configuration bit of SW0 is shifted in last. To change all the switch ON/OFF states at the same time, the $\overline{LE}$ should remain high while the 32-bit Data In signal is shifted into the 32-bit register. After the valid 32-bit data completes shifting into the shift registers, the

high-to-low transition of the $\overline{LE}$ signal transfers the contents of the shift registers into the latches. Finally, setting the $\overline{LE}$ back to high allows all the latches to keep the current state while new data can be shifted into the shift registers without disturbing the latches.

It is recommended to change all the latch states at the same time through this method to avoid possible clock feed through noise (see Figure 5-2 for details).

When the CLR input is set high, it resets the data of all 32 latches to low. Consequently, all the high voltage switches are set to OFF state. However, the CLR signal does not affect the contents of the shift register, so the shift register can operate independently of the CLR signal. Therefore, the shift register still retains the previous data when the CLR input is low (See Table 1-1 for details).

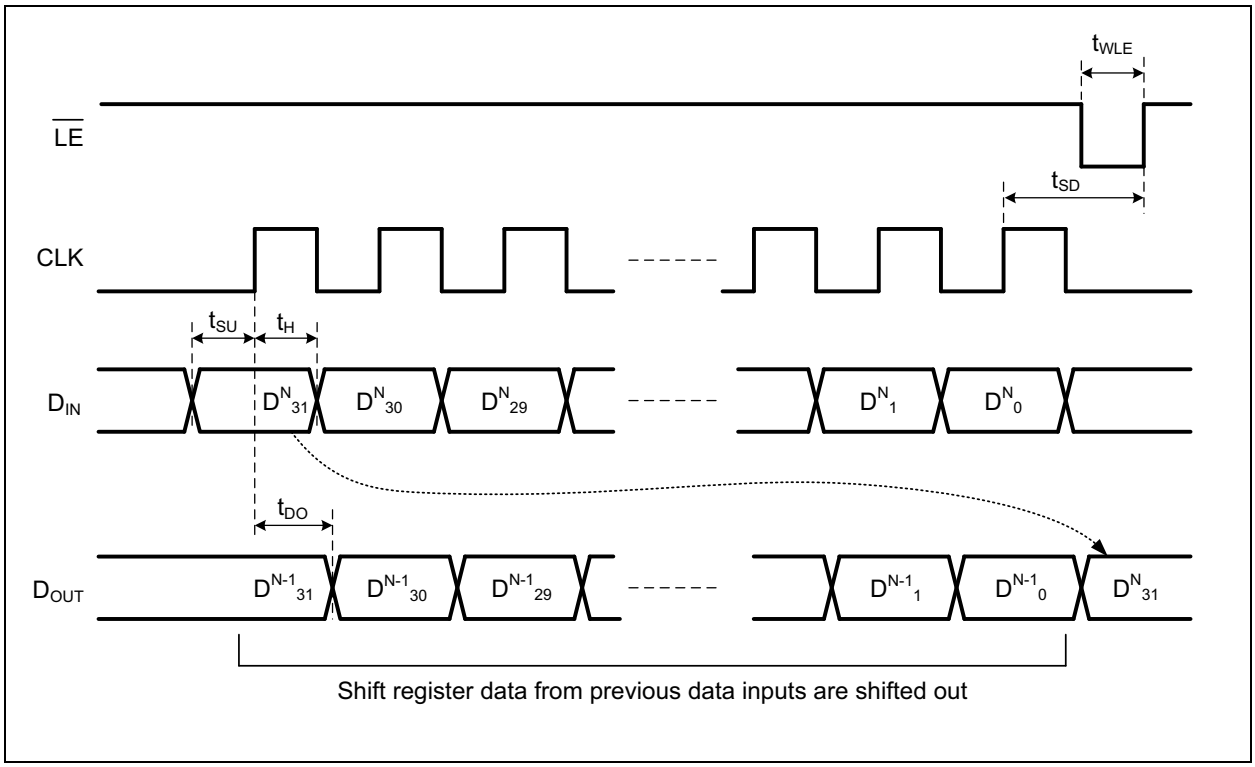


FIGURE 5-2: *Latch Enable Timing Diagram.*

5.3 Multiple Devices Connection

The digital serial interface of the HV2818/HV2918 allows multiple devices to daisy-chain architecture. In daisy-chain architecture, D_{OUT} of the first device is connected to the D_{IN} of the second device, and so forth. The last D_{OUT} of the daisy-chained HV2818/HV2918 can be either floating or fed back to an FPGA to check the previously stored shift register data. CLK, CLR, and $\overline{LE}$ of daisy-chained devices can be connected each other to save number of control signal from FPGA.

To control all the high-voltage analog switch states in daisy-chained N devices, Nx32 bits of data are shifted into shift registers along with Nx32 clocks, while $\overline{LE}$ remains high and CLR remains low. After all the data finishes shifting in, one single negative pulse of $\overline{LE}$ transfers the data from shift registers to latches simultaneously. Consequently, all Nx32 high-voltage analog switches change states simultaneously.

5.4 Power Up/Down Sequence

The recommended power-up sequence of HV2818/HV2918 is V_{LL} first then V_{DD}. The power-down sequence is in reverse order of power-up. During the power up/down period, all the analog switch inputs should be within V_{DD} and GND or floating.

5.5 Layout Considerations

The HV2818/HV2918 devices have two separate ground connections. DGND is the ground connection for digital circuitry and GND is the ground connection for substrate and analog switches. High-transient current passes though the switches and returns through GND in the ultrasound system. The high-current path needs to be designed as short as possible to avoid ground bouncing.

It is recommended to use two separate ground planes in the PCB, connected together at the return terminal of the input power line, as shown in Figure 5-3. It is

recommended that 0.1 µF or larger ceramic decoupling capacitors, with low Equivalent Series Resistance (ESR) and appropriate voltage rating, be connected between DGND and power supplies, V_{LL} and V_{DD}. These decoupling capacitors should be placed as close as possible to the device in the PCB layout.

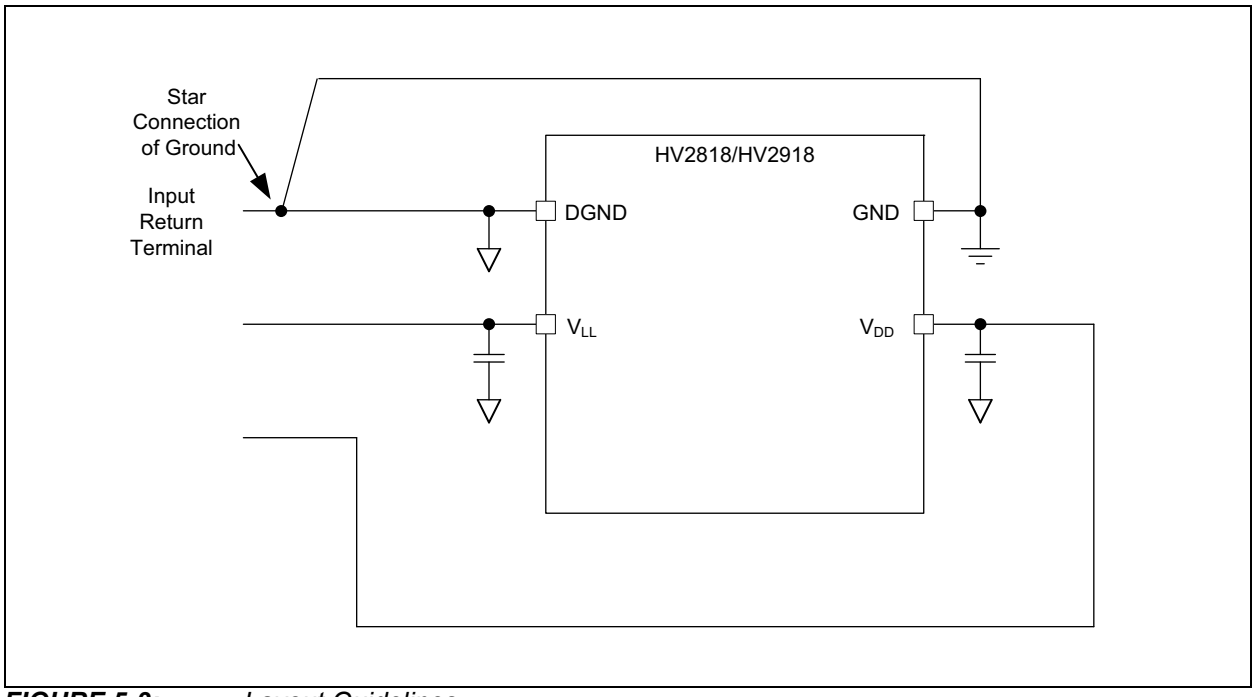
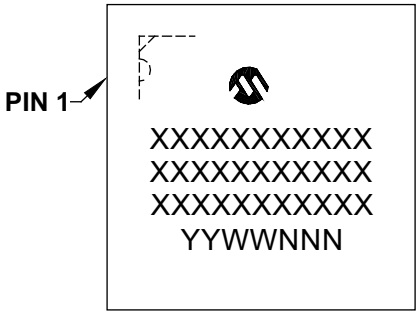


FIGURE 5-3: *Layout Guidelines.*

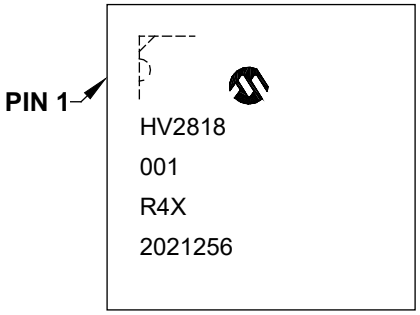
6.0 PACKAGING INFORMATION

6.1 Package Marking Information

64-Lead QFN (9x9x0.9 mm)



Example

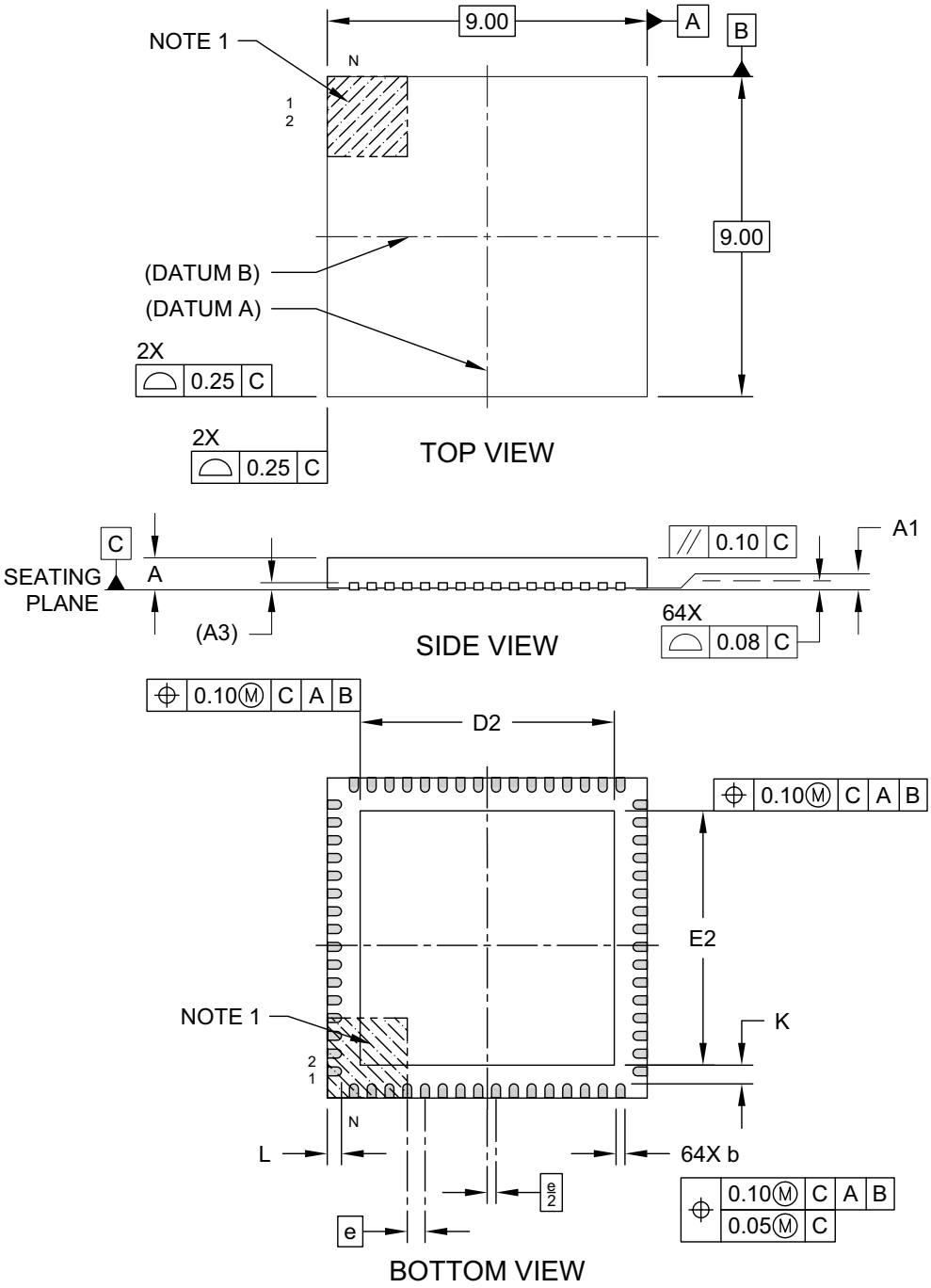


Legend:	XX...X	Product Code or Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information. Package may or may not include the corporate logo.

64-Lead Very Thin Plastic Quad Flat, No Lead Package (R4X) – 9x9x0.9 mm Body [VQFN]
With 7.15 x 7.15 Exposed Pad [Also called QFN]

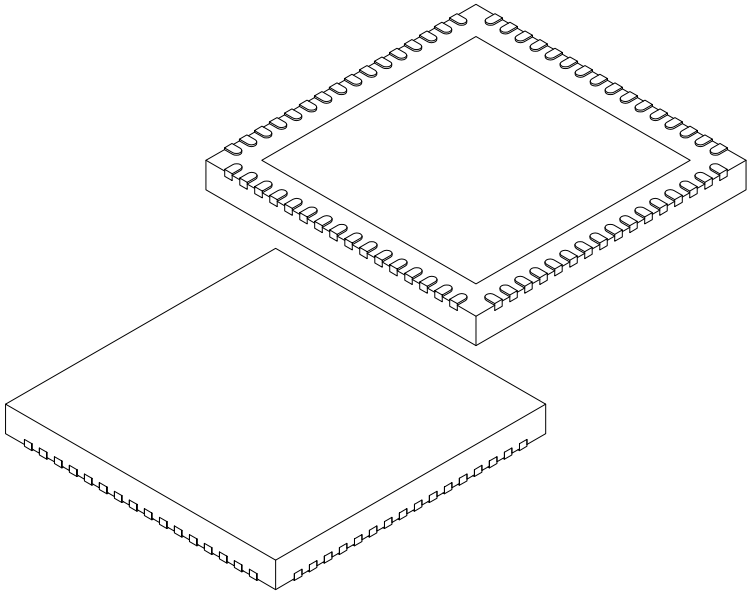
Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing C04-149D [R4X] Sheet 1 of 2

64-Lead Very Thin Plastic Quad Flat, No Lead Package (R4X) – 9x9x0.9 mm Body [VQFN] With 7.15 x 7.15 Exposed Pad [Also called QFN]

Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		64	
Pitch	e		0.50 BSC	
Overall Height	A	0.80	0.90	1.00
Standoff	A1	0.00	0.02	0.05
Contact Thickness	A3		0.20 REF	
Overall Width	E		9.00 BSC	
Exposed Pad Width	E2	7.05	7.15	7.25
Overall Length	D		9.00 BSC	
Exposed Pad Length	D2	7.05	7.15	7.25
Contact Width	b	0.18	0.25	0.30
Contact Length	L	0.30	0.40	0.50
Contact-to-Exposed Pad	K	0.20	-	-

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated
3. Dimensioning and tolerancing per ASME Y14.5M

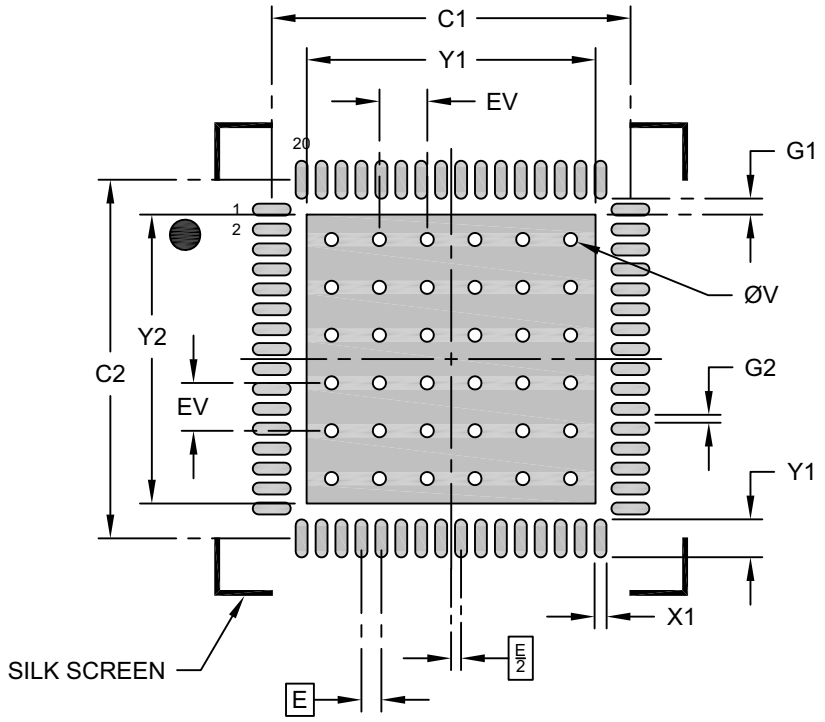
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-149D [R4X] Sheet 2 of 2

64-Lead Very Thin Plastic Quad Flat, No Lead Package (R4X) – 9x9x0.9 mm Body [VQFN]
With 7.15 x 7.15 Exposed Pad [Also called QFN]

Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.50 BSC	
Optional Center Pad Width	X2			7.25
Optional Center Pad Length	Y2			7.25
Contact Pad Spacing	C1		9.00	
Contact Pad Spacing	C2		9.00	
Contact Pad Width (X64)	X1			0.30
Contact Pad Length (X64)	Y1			0.95
Contact Pad to Center Pad (X64)	G1	0.40		
Spacing Between Contact Pads (X60)	G2	0.20		
Thermal Via Diameter	V		0.33	
Thermal Via Pitch	EV		1.20	

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
2. For best soldering results, thermal vias, if used, should be filled or tented to avoid solder loss during reflow process

Microchip Technology Drawing C04-2149C [R4X]

APPENDIX A: REVISION HISTORY

Revision A (June 2020)

- Initial release of this document.

NOTES:

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	/XX
Device	Package Type

Device:	HV2818:	No High-Voltage Bias, Low Harmonic Distortion, 32-Channel, High-Voltage Analog Switch
	HV2918:	No High-Voltage Bias, Low Harmonic Distortion, 32-Channel, High-Voltage Analog Switch with Bleed Resistor
Temperature:	N =	0°C to +70°C (Commercial)
Package Type:	R4X =	Very Thin Plastic Quad Flat Pack, No Lead Package

Examples:

a) HV2818/R4X: Commercial temperature, Very Thin Plastic Quad Flat Pack, 64-LD QFN package

b) HV2918/R4X: Commercial temperature, Very Thin Plastic Quad Flat Pack, 64-LD QFN package

NOTES:

Note the following details of the code protection feature on Microchip devices:

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