

CD54/74HC4316

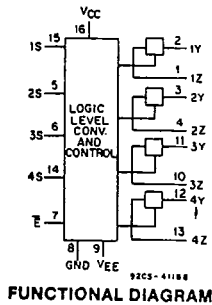
CD54/74HCT4316

HARRIS SEMICONDUCTOR

27E D 4302271 0018126 7 HAS

High-Speed CMOS Logic

T-51-11-00



Quad Analog Switch with Level Translation

Type Features:

- Wide analog-input-voltage range ($V_{CC}-V_{EE}$): 0-10 V
- Low "ON" resistance: 45 Ω typ. @ $V_{CC}=4.5$ V
35 Ω typ. @ $V_{CC}=6$ V
30 Ω typ. @ $V_{CC}-V_{EE}=9$ V
- Fast switching and propagation delay times
- Low "OFF" leakage current
- Built-in "Break-before-make" switching
- Logic-level translation to enable 5 V logic to accommodate ± 5 V analog signals

The RCA CD54/74HC/HCT4316 contains four independent digitally controlled analog switches that use silicon-gate CMOS technology to achieve operating speeds similar to LSTTL with the low power consumption of standard CMOS integrated circuits.

In addition these devices contain logic-level translation circuits that provide for analog signal switching of voltages between ± 5 V via 5 V logic. Each switch is turned on by a high-level voltage on its select input (S) when the common Enable (E) is Low. A High E disables all switches. The digital inputs can swing between V_{CC} and Gnd; the analog inputs/outputs can swing between V_{CC} as a positive limit and V_{EE} as a negative limit. Voltage ranges are shown in Figs. 2 and 3.

The CD54HC4316 and CD54HCT4316 are supplied in 16-lead hermetic dual-in-line ceramic packages (F suffix). The CD74HC4316 and CD74HCT4316 are supplied in 16-lead dual-in-line plastic packages (E suffix) and in 16-lead dual-in-line surface-mount plastic packages (M suffix). Both types are also available in chip form (H suffix).

Family Features:

- Wide operating temperature range:
CD74HC/HCT: -40 to +125°C
- CD54HC/CD74HC types:
2 V to 10 V operation
High noise immunity:
 $N_{IL} = 30\%$, $N_{IH} = 30\%$ of V_{CC} ; @ $V_{CC} = 5$ V
- CD54HCT/CD74HCT types:
Direct LSTTL input logic compatibility
 $V_{IL} = 0.8$ V max., $V_{IH} = 2$ V min.
CMOS input compatibility
 $I_i \leq 1 \mu A$ @ V_{OL} , V_{OH}
- Alternate Source is Phillips/Signetics

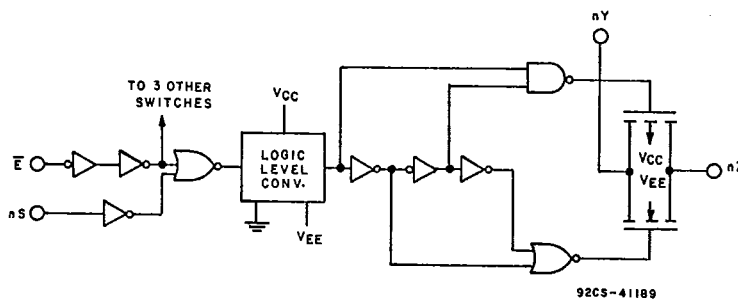


Fig. 1 - Logic diagram (one switch).

TRUTH TABLE

INPUTS		SWITCH
E	S	
L	L	OFF
L	H	ON
H	X	OFF

H = High Level Voltage
L = Low Level Voltage
X = Don't Care

CD54/74HC4316

CD54/74HCT4316

MAXIMUM RATINGS, Absolute-Maximum Values: (All voltages referenced to Gnd unless otherwise shown)

DC SUPPLY-VOLTAGE ($V_{CC}-V_{EE}$)	-0.5 to +10.5 V
DC SUPPLY-VOLTAGE (V_{CC})	-0.5 to +7 V
DC SUPPLY-VOLTAGE (V_{EE})	+0.5 to -7 V
DC INPUT DIODE CURRENT, I_{IK} (FOR $V_i < -0.5$ V OR $V_i > V_{CC} + 0.5$ V)	± 20 mA
DC SWITCH DIODE CURRENT, I_{OK} (FOR $V_i < V_{EE} - 0.5$ V OR $V_i > V_{CC} + 0.5$ V)	± 20 mA
DC SWITCH CURRENT (FOR $V_i > V_{EE} - 0.5$ V OR $V_i < V_{CC} + 0.5$ V)	± 25 mA
DC V_{CC} OR GROUND CURRENT (I_{CC})	± 50 mA
DC V_{EE} CURRENT (I_{EE})	-20 mA
POWER DISSIPATION PER PACKAGE (P_D):	
For $T_A = -40$ to $+100^\circ\text{C}$ (PACKAGE TYPE E)	500 mW
For $T_A = +100$ to $+125^\circ\text{C}$ (PACKAGE TYPE E)	Derate Linearly at 8 mW/ $^\circ\text{C}$ to 300 mW
For $T_A = -55$ to $+100^\circ\text{C}$ (PACKAGE TYPE F, H)	500 mW
For $T_A = +100$ to $+125^\circ\text{C}$ (PACKAGE TYPE F, H)	Derate Linearly at 8 mW/ $^\circ\text{C}$ to 300 mW
For $T_A = -40$ to $+70^\circ\text{C}$ (PACKAGE TYPE M)	400 mW
For $T_A = +70$ to $+125^\circ\text{C}$ (PACKAGE TYPE M)	Derate Linearly at 6 mW/ $^\circ\text{C}$ to 70 mW

OPERATING-TEMPERATURE RANGE (T_A):

PACKAGE TYPE F, H	-55 to $+125^\circ\text{C}$
PACKAGE TYPE E, M	-40 to $+125^\circ\text{C}$
STORAGE TEMPERATURE (T_{stg})	-65 to $+150^\circ\text{C}$

LEAD TEMPERATURE (DURING SOLDERING):

At distance $1/16 \pm 1/32$ in. (1.59 ± 0.79 mm) from case for 10 s max.	$+265^\circ\text{C}$
Unit inserted into a PC Board (min. thickness $1/16$ in., 1.59 mm) with solder contacting lead tips only	$+300^\circ\text{C}$

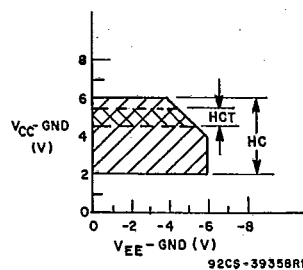
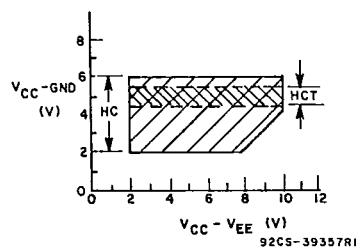
RECOMMENDED OPERATING CONDITIONS

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range (For T_A =Full Package-Temperature Range) V_{CC} *			
CD54/74HC Types	2	6	V
CD54/74HCT Types	4.5	5.5	
Supply-Voltage Range (For T_A =Full Package-Temperature Range) $V_{CC}-V_{EE}$	2	10	V
CD54/74HC Types, CD54/74HCT Types, See Fig. 2			
Supply-Voltage Range (For T_A =Full Package-Temperature Range) V_{EE} *	0	-6	V
CD54/74HC Types, CD54/74HCT, See Fig. 3			
DC Input Control Voltage, V_i	Gnd	V_{CC}	V
Analog Switch I/O Voltage, V_{is}	V_{EE}	V_{CC}	V
Operating Temperature, T_A :			$^\circ\text{C}$
CD74 Types	-40	+125	
CD54 Types	-55	+125	
Input Rise and Fall Times, t_r, t_f :			ns
at 2 V	0	1000	
at 4.5 V	0	500	
at 6 V	0	400	

*Unless otherwise specified, all voltages are referenced to Ground.

Recommended Operating Area as a Function of Supply Voltages



HARRIS SEMICONDUCTOR 27E D 430227J 0018128 0 HAS

T-51-11

New Data

CD54/74HC4316
CD54/74HCT4316

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	TEST CONDITIONS				74HC/54HC			74HC		54HC -55/ +125°C		TEST CONDITIONS				74HCT/54HCT			74HCT		54HCT -55/ +125°C		UNITS			
	V _{IS} V	V _I V	V _{EE} V	V _{CC} V	+25°C			-40/ +85°C		74HC -40/ +125°C		V _{IS} V	V _I V	V _{EE} V	V _{CC} V	+25°C			-40/ +85°C		74HCT -40/ +125°C					
					Min	Typ	Max	Min	Max	Min	Max					Min	Typ	Max	Min	Max						
High-Level Input Voltage V _{HI}					2	1.5	—	—	1.5	—	1.5	—				4.5	2	—	—	2	—	2	—	V		
					4.5	3.15	—	—	3.15	—	3.15	—				to										
					8	4.2	—	—	4.2	—	4.2	—				5.5										
Low-Level Input Voltage V _{LI}					2	—	—	0.5	—	0.5	—	0.5	—				4.5	—	—	0.8	—	0.8	—	0.8	V	
					4.5	—	—	1.35	—	1.35	—	1.35	—				to									
					8	—	—	1.8	—	1.8	—	1.8	—				5.5									
"On" Resistance I _O = 1 mA (Fig. 4 & 5)	V _{CC} or V _{EE} to V _{EH}	V _{IL} or V _{ILH}			0	4.5	—	45	180	—	225	—	270				0	4.5	—	45	180	—	225	—	270	Ω
					0	8	—	35	160	—	200	—	240				—	—	—	—	—	—	—	—	—	
					-4.5	4.5	—	30	135	—	170	—	205				-4.5	4.5	—	30	135	—	170	—	205	Ω
					0	4.5	—	85	320	—	400	—	480				0	4.5	—	85	320	—	400	—	480	Ω
					0	8	—	55	240	—	300	—	360	Same as HC	Same as HC		—	—	—	—	—	—	—	—	—	Ω
					-4.5	4.5	—	35	170	—	215	—	255	as HC	as HC		-4.5	4.5	—	35	170	—	215	—	255	Ω
Maximum "On" Resistance between any two channels ΔR _{on}					0	4.5	—	10	—	—	—	—	—				0	4.5	—	10	—	—	—	—	—	Ω
					0	8	—	8.5	—	—	—	—	—				—	—	—	—	—	—	—	—	—	Ω
					-4.5	4.5	—	5	—	—	—	—	—				-4.5	4.5	—	5	—	—	—	—	—	Ω
Switch Off Leakage Current I _{LZ}	V _{CC} -V _{EE}	V _{IL} or V _{ILH}			0	8	—	—	±0.1	—	±1	—	±1				0	8	—	—	±0.1	—	±1	—	±1	μA
					-5	5	—	—	±0.1	—	±1	—	±1				-5	5	—	—	±0.1	—	±1	—	±1	μA
Control Input Leakage Current I _{LC}	—	V _{CC} or Gnd			0	8	—	—	±0.1	—	±1	—	±1	—	**		5.5	—	—	±0.1	—	±1	—	±1	—	μA
Quiescent Device Current I _{CC} I _O = 0	When V _{IS} = V _{EH} , V _{OE} = V _{CC} , When V _{IS} = V _{CC} , V _{OE} = V _{EH}	V _{CC} or Gnd			0	8	—	—	8	—	80	—	160	Same as HC	Same as HC		0	5.5	—	—	8	—	80	—	160	μA
					-5	5	—	—	16	—	160	—	320	as HC	as HC		-4.5	5.5	—	—	16	—	160	—	320	μA
Additional Quiescent Device Current per input pin: 1 unit load ΔI _{CC} *															V _{CC} -2.1		4.5 to 5.5	—	100	360	—	450	—	490	μA	

*For dual-supply systems theoretical worst case (V_I = 2.4 V, V_{CC} = 5.5 V) specification is 1.8 mA.
**Any voltage between V_{CC} and Gnd.

HCT Input Loading Table

Input	Unit Loads*
All	0.5

*Unit Load is ΔI_{CC} limit specified in Static Characteristics Chart, e.g., 360 μA max. @ 25°C.

CD54/74HC4316

CD54/74HCT4316

SWITCHING CHARACTERISTICS ($V_{CC}=5\text{ V}$, $T_A=25^\circ\text{C}$, Input $t_i, t_f=6\text{ ns}$)

CHARACTERISTIC		Cl (pF)	TYPICAL VALUES		UNITS
			HC	HCT	
Turn "ON" Time E to Out nS to Out	tPZH	15	17	18	ns
			14	17	
Turn "ON" Time E to Out nS to Out	tPZL		17	24	
			14	18	
Turn "OFF" Time E to Out nS to Out	tPLZ, tPHZ		17	21	
			14	18	
Power Dissipation Capacitance*		—	42	47	pF

* C_{PD} is used to determine the dynamic power consumption, per package.

$$P_D = C_{PD} V_{CC}^2 f_i + \Sigma (C_L + C_S) V_{CC}^2 f_o \text{ where}$$

 f_i = input frequency f_o = output frequency C_L = output load capacitance C_S = switch capacitance V_{CC} = supply voltage.SWITCHING CHARACTERISTICS ($C_L=50\text{ pF}$, Input $t_i, t_f=6\text{ ns}$)

CHARACTERISTIC		V _{EE}	V _{CC}	LIMITS												UNITS	
				25° C				-40° C to +85° C				-55° C to +125° C					
				HC		HCT		74HC		74HCT		54HC		54HCT			
				Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
Propagation Delay Switch In to Out	t _{PLH}	0	2	—	60	—	—	—	75	—	—	—	90	—	—	ns	
	t _{PHL}	0	4.5	—	12	—	12	—	15	—	15	—	18	—	18		
		0	6	—	10	—	—	—	13	—	—	—	15	—	—		
		-4.5	4.5	—	8	—	8	—	10	—	10	—	12	—	12		
Turn "ON" Time E̅ to Out	t _{PZH}	0	2	—	205	—	—	—	255	—	—	—	310	—	—		
		0	4.5	—	41	—	44	—	51	—	55	—	62	—	66		
		0	6	—	35	—	—	—	43	—	—	—	53	—	—		
		-4.5	4.5	—	37	—	42	—	47	—	53	—	56	—	63		
	t _{PZL}	0	2	—	205	—	—	—	255	—	—	—	310	—	—		
		0	4.5	—	41	—	56	—	51	—	70	—	62	—	85		
		0	6	—	35	—	—	—	43	—	—	—	53	—	—		
		-4.5	4.5	—	37	—	42	—	47	—	53	—	56	—	63		
	Turn "ON" Time nS to Out	t _{PZH}	0	2	—	175	—	—	—	220	—	—	—	265	—		—
			0	4.5	—	35	—	40	—	44	—	53	—	53	—		60
			0	6	—	30	—	—	—	37	—	—	—	45	—		—
			-4.5	4.5	—	34	—	34	—	43	—	43	—	51	—		51
		t _{PZL}	0	2	—	175	—	—	—	220	—	—	—	265	—		—
			0	4.5	—	35	—	50	—	44	—	63	—	53	—		75
			0	6	—	30	—	—	—	37	—	—	—	45	—		—
			-4.5	4.5	—	34	—	34	—	43	—	43	—	51	—		51
Turn "OFF" Time E̅ to Out	t _{PLZ} , t _{PHZ}	0	2	—	205	—	—	—	255	—	—	—	310	—	—		
		0	4.5	—	41	—	50	—	51	—	63	—	62	—	75		
		0	6	—	35	—	—	—	43	—	—	—	53	—	—		
		-4.5	4.5	—	37	—	46	—	47	—	58	—	56	—	69		
Turn "OFF" Time nS to Out	t _{PHZ}	0	2	—	175	—	—	—	220	—	—	—	265	—	—		
		0	4.5	—	35	—	44	—	44	—	55	—	53	—	66		
		0	6	—	30	—	—	—	37	—	—	—	45	—	—		
		-4.5	4.5	—	34	—	40	—	43	—	50	—	51	—	60		
Input (Control) Capacitance	C _I	—	—	—	10	—	10	—	10	—	10	—	10	—	10	pF	

T -51-11

New Data

CD54/74HC4316
CD54/74HCT4316

ANALOG CHANNEL CHARACTERISTICS - Typical Values at $T_A = 25^\circ\text{C}$

CHARACTERISTIC	TEST CONDITIONS	V_{CC} V	HC	HCT	UNITS
Switch Frequency Response Bandwidth at -3 dB (Fig. 15)	Fig. 6 Notes 1 and 2	4.5	>200	>200	MHz
Crosstalk Between Any Two Switches (Fig. 16)	Fig. 7 Notes 2 and 3	4.5	TBE	TBE	dB
Total Harmonic Distortion	1 kHz, $V_{IS}=4 V_{PP}$ Fig. 8 $V_{IS}=8 V_{PP}$	4.5	0.078	0.078	%
		9	0.018	0.018	
Control to Switch Feedthrough Noise	Fig. 9	4.5	TBE	TBE	mV
		9	TBE	TBE	
Switch "OFF" Signal Feedthrough (Fig. 16)	Fig. 10 Notes 2 and 3	4.5	-62	-62	dB
Switch Input Capacitance C_s	—	—	5	5	pF

Notes:

1. Adjust input level for 0 dBm at output, $f = 1$ MHz.
2. V_{IS} is centered at $V_{CC}/2$.
3. Adjust input for 0 dBm at V_{IS} .

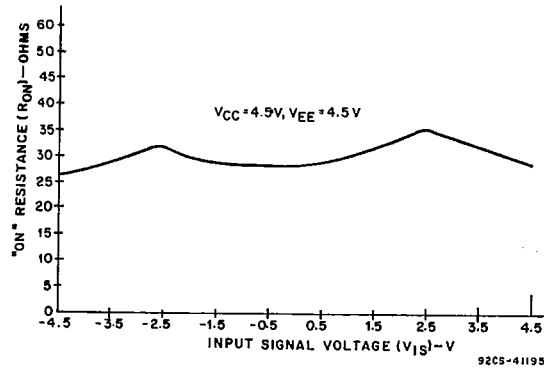


Fig. 4 - Typical "ON" resistance vs. input signal voltage.

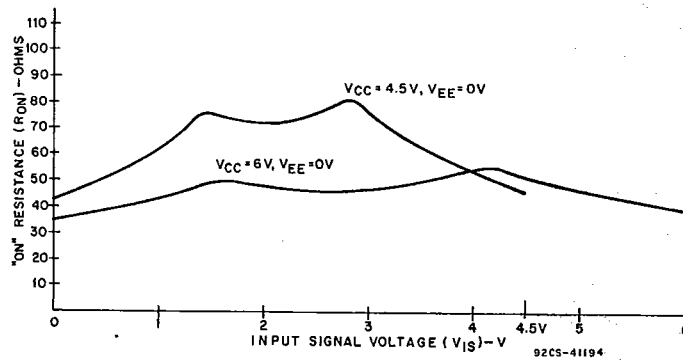


Fig. 5 - Typical "ON" resistance vs. input signal voltage.

CD54/74HC4316

CD54/74HCT4316

T-51-11

ANALOG TEST CIRCUITS

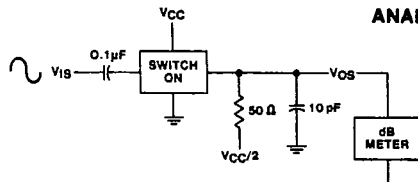


Fig. 6 - Frequency response test circuit.

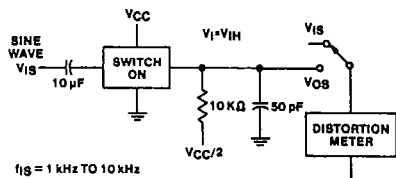


Fig. 8 - Total harmonic distortion test circuit.

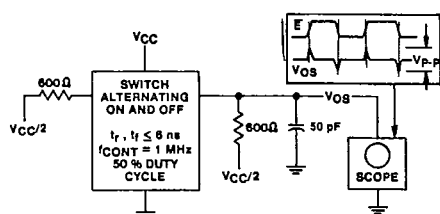


Fig. 9 - Control-to-switch feedthrough noise test circuit.

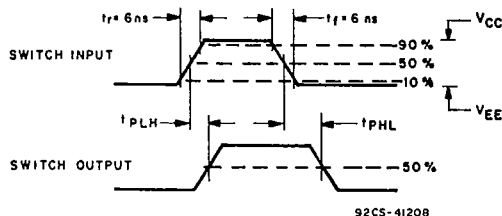


Fig. 11 - Switch propagation - delay times waveforms.

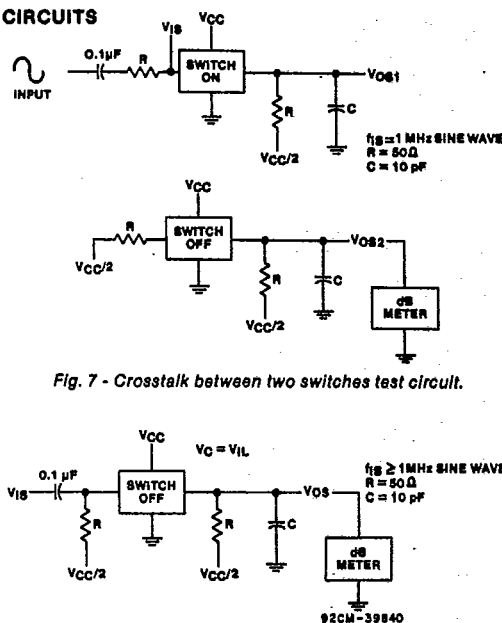


Fig. 7 - Crosstalk between two switches test circuit.

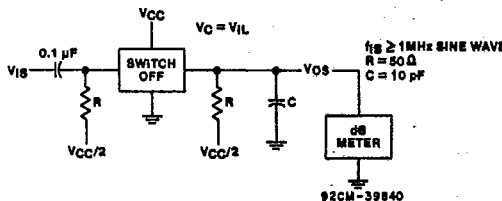


Fig. 10 - Switch off signal feedthrough.

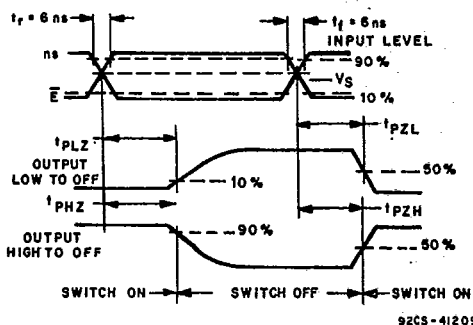


Fig. 12 - Switch turn-on and turn-off propagation delay times waveforms.

	54/74HC	54/74HCT
Input Level	V _{CC}	3 V
Switching Voltage, V _S	50% V _{CC}	1.3 V

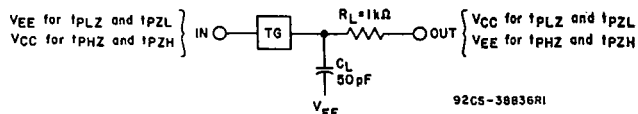


Fig. 13 - Switch on/off propagation delay time test circuit.

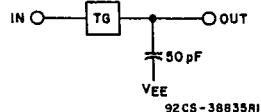


Fig. 14 - Switch-in to switch-out propagation delay time test circuit.

T-51-1/ — New Data

CD54/74HC4316
CD54/74HCT4316

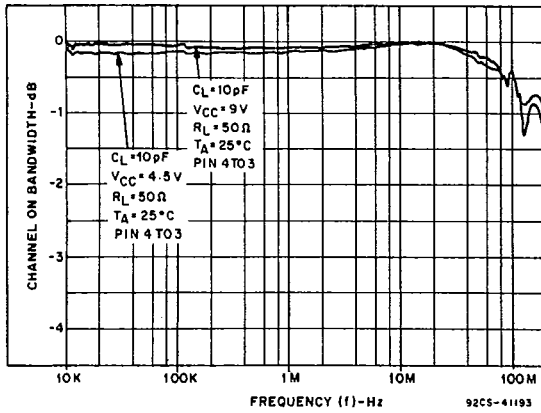


Fig. 15 - Switch frequency response.

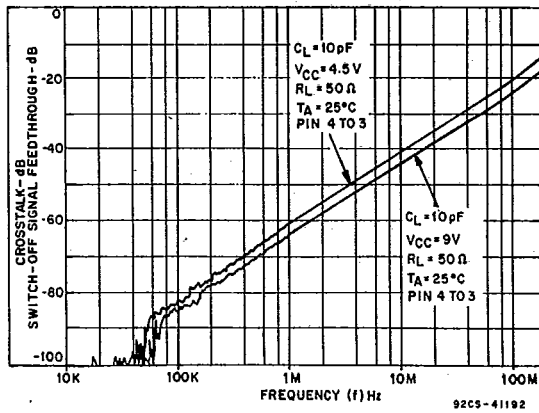


Fig. 16 - Switch-off signal feedthrough and crosstalk vs. frequency.