Two-Stage Hysteretic LED Driver

General Description

The RT8415 is a two-stage LED driver controller with the 2nd stage MOSFET integrated inside. It consists of a Boost controller on the first stage and a Buck converter on the second stage. By adapting two-stage topology, RT8415 is highly compatible with ET (Electronic Transformer) and performs extremely high Power Factor in specific MR16 / AR111 LED lighting applications.

The Boost converter on the first stage provides constant output voltage with well inductor current control. The Buck converter on the second stage provides constant LED output current by hysteretic peak current regulation.

The RT8415 is available in the SOP-8 (Exposed Pad) package.

Ordering Information

RT8415 □□

Package Type
SP : SOP-8 (Exposed Pad-Option 2)

Lead Plating System
G : Green (Halogen Free and Pb Free)

Note :

Richtek products are :

- ▶ RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
- ▶ Suitable for use in SnPb or Pb-free soldering processes.

Features

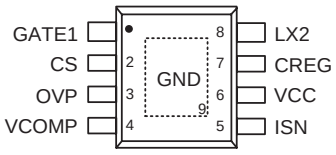
- **Two-Stage Topology (Boost + Buck)**
- **2nd Stage MOSFETs Inside**
- **Wide Input Voltage Range : 4.5V to 36V**
- **Excellent Power Factor**
- **Programmable Boost Output Voltage**
- **Independent Dual Stage Function**
- **Programmable LED Current with ±6% LED Current Accuracy**
- **Flicker-Free LED**
- **Wide Electronic Transformer Compatibility**
- **Input Under Voltage Lockout Detection**
- **Thermal Shutdown Protection**
- **SOP-8 (Exposed Pad) Package**

Applications

- MR16 Lighting
- Signage and Decorative LED Lighting
- Architectural Lighting
- High Power LED Lighting
- Low Voltage Industrial Lighting
- Indicator and Emergency Lighting
- Automotive LED Lighting

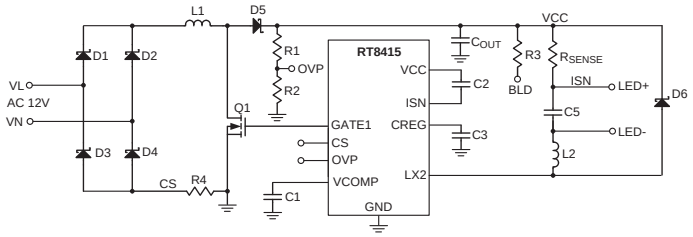
Pin Configuration

(TOP VIEW)

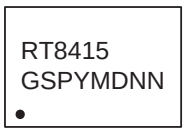


SOP-8 (Exposed Pad)

Simplified Application Circuit



Marking Information

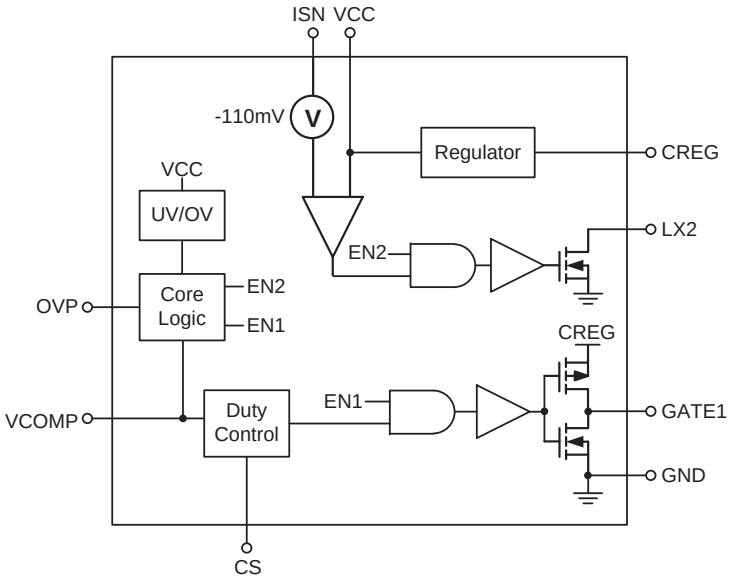


RT8415GSP : Product Number
YMDNN : Date Code

Functional Pin Description

Pin No.	Pin Name	Pin Function
1	GATE1	The 1st stage output gate.
2	CS	The 1st stage current sense input.
3	OVP	Over-voltage protection sense input.
4	VCOMP	Compensation node. A compensation network between VCOMP and GND is needed.
5	ISN	LED current sense amplifier negative input.
6	VCC	Power supply. For good bypass, place a ceramic capacitor near the VCC pin.
7	CREG	Internal regulator output. Place a 4.7μF Capacitor between CREG and GND pins.
8	LX2	Switch node. The 2nd Stage Internal MOSFET Drain.
9 (Exposed Pad)	GND	Ground. The Exposed Pad must be soldered to a large PCB and connected to GND for maximum power dissipation.

Functional Block Diagram



Operation

The RT8415 VCC is supplied from the first stage Boost output.

The first stage is a constant output voltage Boost topology that controls the inductor current with excellent Power Factor.

The second stage is a constant output current Buck topology. The current sense voltage threshold between the VCC and ISN pins is only −110mV to minimize the power loss.

Absolute Maximum Ratings (Note 1)

- Supply Voltage, VCC to GND ---------- –0.3V to 40V
- CREG, OVP, VCOMP, CS to GND ---------- –0.3V to 6V
- LX2 to GND ---------- –0.3V to 40V
- VCC to ISN ---------- –0.3V to 3V
- Power Dissipation, P_D @ T_A = 25°C
  SOP-8 (Exposed Pad) ---------- 2.46W
- Package Thermal Resistance (Note 2)
  SOP-8 (Exposed Pad), θ_{JA} ---------- 40.6°C/W
  SOP-8 (Exposed Pad), θ_{JC} ---------- 2°C/W
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Junction Temperature ---------- 150°C
- Storage Temperature Range ---------- –65°C to 150°C
- ESD Susceptibility (Note 3)
  HBM (Human Body Model) ---------- 2kV
  MM (Machine Model) ---------- 200V

Recommended Operating Conditions (Note 4)

- Supply Input Voltage, VCC ---------- 4.5V to 36V
- Ambient Temperature Range ---------- –40°C to 85°C
- Junction Temperature Range ---------- –40°C to 125°C

Electrical Characteristics

(V_{CC} = 20V_{DC}, No Load, C_{LOAD} = 1nF, T_A = 25°C, unless otherwise specified.)

Parameter		Symbol	Test Conditions	Min	Typ	Max	Unit
Supply Voltage							
CREG UVLO_ON		V_{UVLO_ON}	OVP = 0V	--	4.2	--	V
CREG UVLO_OFF		V_{UVLO_OFF}	OVP = 0V	--	3.9	--	V
Supply Current							
VCC Shutdown Current		I_{SHDN}	V_{CC} = 2V	--	10	--	μA
VCC Quiescent Current		I_Q		--	2	--	mA
VCC OVP Trigger Level		V_{CC_OVP}		--	39	--	V
Internal Reference Voltage		V_{CREG}		--	5	--	V
Internal Reference Voltage (I_{CREG} = –20mA)			I_{CREG} = –20mA	--	4.9	--	V
Boost Converter							
Stage 1 OVP	High Level	V_{OVP_H}		--	1.88	--	V
	Low Level	V_{OVP_L}		1.52	1.6	1.68	V
OVP Pin Leakage Current		I_{OVP}		--	1	--	μA
CS Input Impendence			CS = –0.2V	--	50	--	kΩ

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
UGATE1 Drive Sink	RUGATE1sk	Sink = 50mA	--	2	--	Ω
LGATE1 Drive Source	RLGATE1sr	Source = –50mA	--	1.5	--	Ω
GATE1 Default Pull Down Resistor	RLGATE1sr		--	90	--	kΩ
Buck Converter						
ISN Threshold	$V_{CC}-V_{ISN}$		103	110	117	mV
Stage 2 Peak to Peak Sense Voltage		(dV1 + dV2) / 2	--	15	--	%
LX2 Internal Switch $R_{DS(ON)}$	$R_{DS(ON)\_LX2}$	Sink = 100mA	--	0.2	--	Ω
Temperature Protection						
Over-Temperature Threshold	T_{SD}	(Note 5)	--	150	--	°C
Over-Temperature Threshold Hysteresis	ΔT_{SD}	(Note 5)	--	30	--	°C

Note 1. Stresses beyond those listed “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

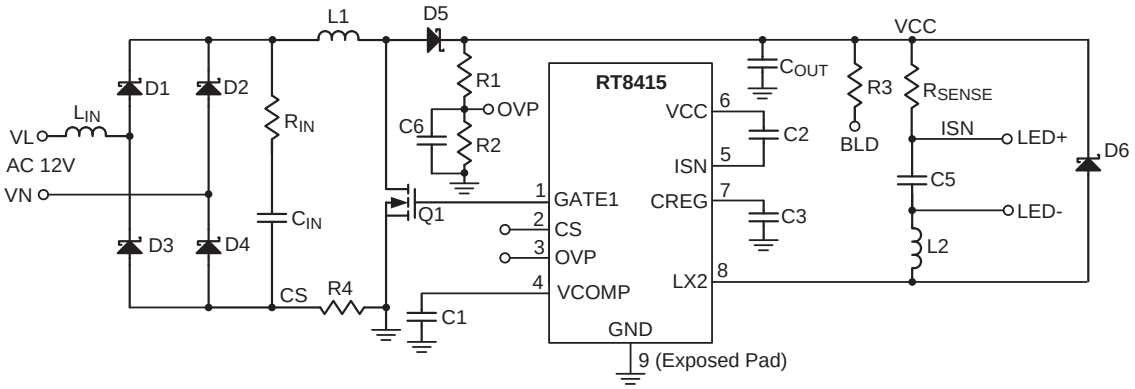
Note 2. θ_{JA} is measured under natural convection (still air) at T_A = 25°C with the component mounted on a low effective-thermal-conductivity two-layer test board on a JEDEC thermal measurement standard. θ_{JC} is measured at the exposed pad of the package.

Note 3. Devices are ESD sensitive. Handling precaution recommended.

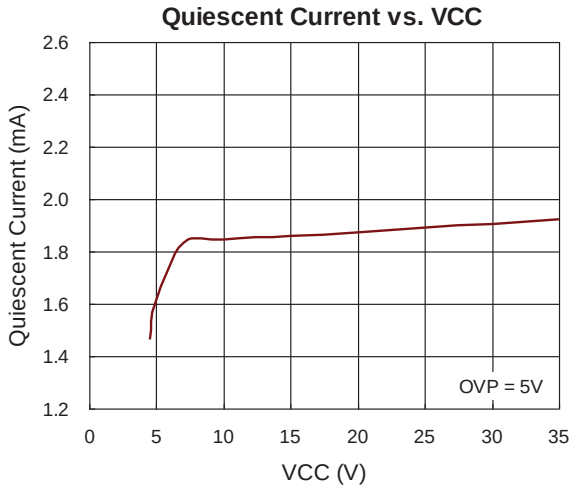
Note 4. The device is not guaranteed to function outside its operating conditions.

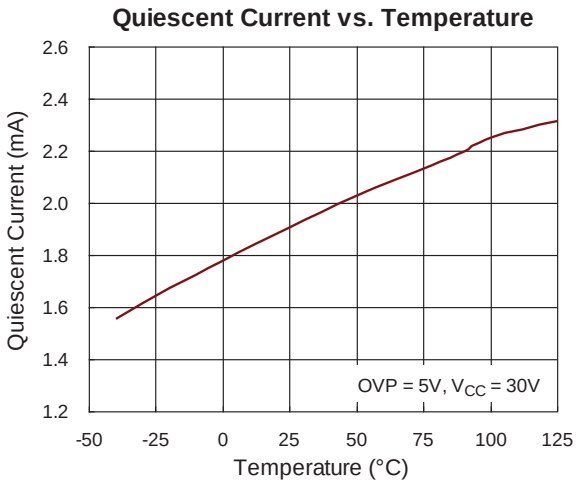
Note 5. Guaranteed by design.

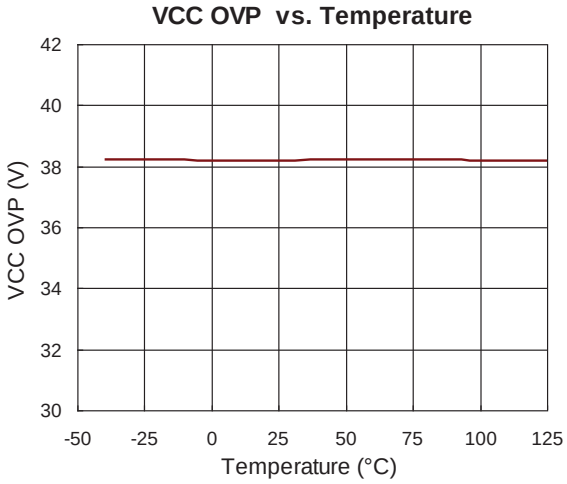
Typical Application Circuit

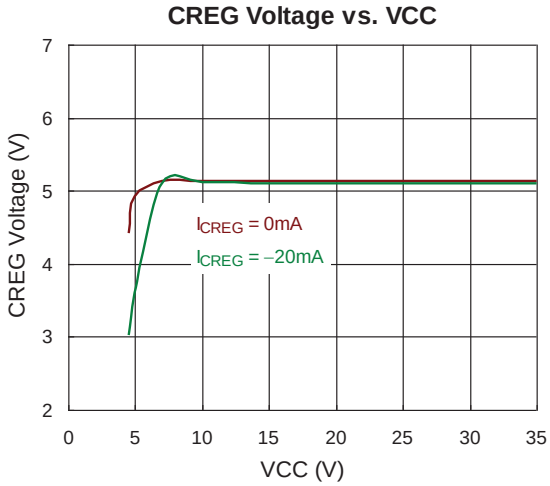


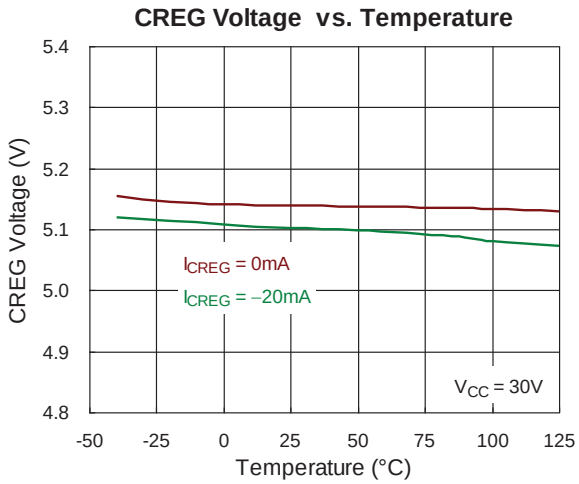
Typical Operating Characteristics

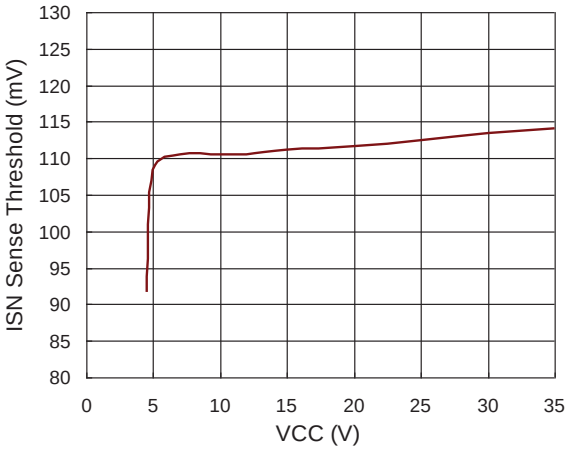


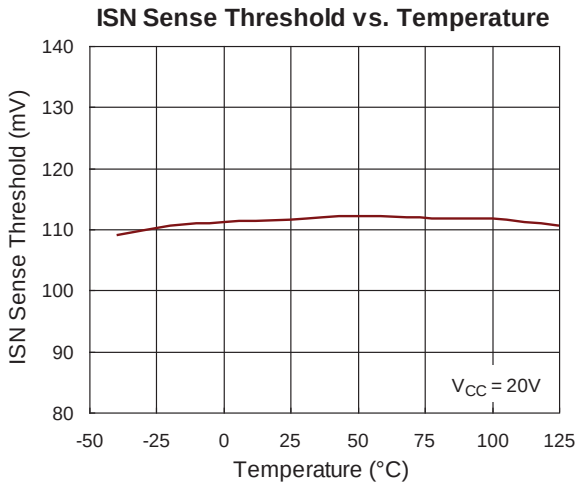


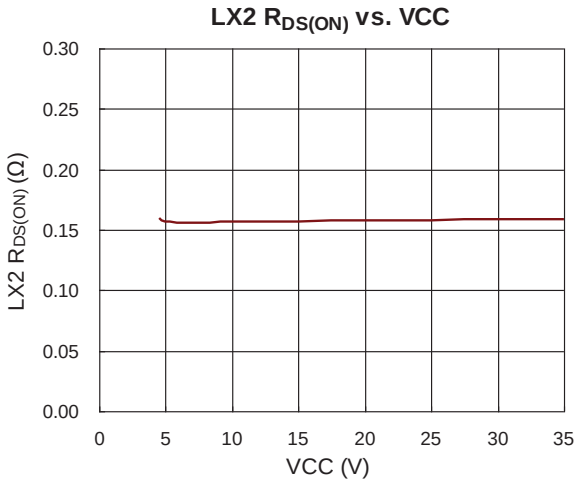


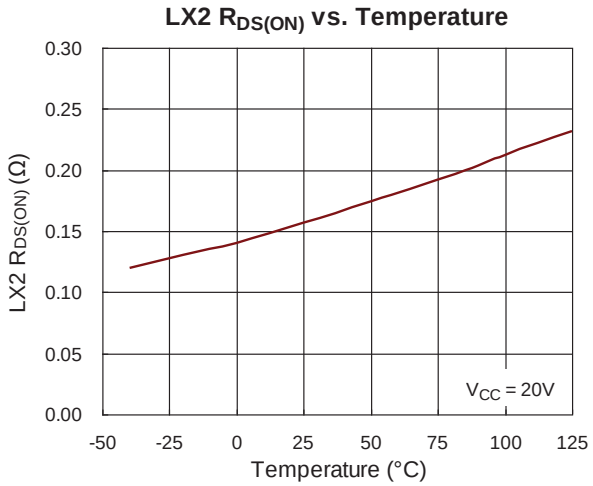












Application Information

The RT8415 consists of a constant voltage Boost controller and a constant output current Buck controller. The Boost controller is based on a peak current, well PFC control architecture, and designed to operate up to 1MHz to use a very small inductor for space constrained applications.

Under-Voltage Lockout (UVLO)

The RT8415 includes an under-voltage lockout function with 300mV hysteresis. The internal MOSFET turns off when VCC falls below 3.9V (typ.).

CREG Regulator

The CREG pin requires a capacitor for stable operation and to store the charge for the large GATE switching currents. Choose a 10V rated low ESR, X7R or X5R, ceramic capacitor for best performance. A 4.7μF capacitor will be adequate for many applications. Place the capacitor close to the IC to minimize the trace length to the CREG pin and to the IC ground. An internal current limit on the CREG output protects the RT8415 from excessive on-chip power dissipation. The CREG pin has set the output to 4.2V (typ.) to protect the internal FETs from excessive power dissipation caused by not being fully enhanced. If the CREG pin is used to drive extra circuits beside RT8415, the extra loads should be limited to less than 10mA.

Average Output Current Setting

The output current that flows through the LED string is set by an external resistor, R_{SENSE}, which is connected between the VCC and ISN terminal. The relationship between output current, I_{OUT}, and R_{SENSE} is shown below :

$$I_{OUT} = \frac{110mV}{R_{SENSE}}$$

LED Current Ripple Reduction

Higher LED current ripple will shorten the LED life time and increase heat accumulation of LED. To reduce the LED current ripple, an output capacitor in parallel with the LED should be added. The typical value of output capacitor is 4.7μF.

VCC Voltage Setting

The VCC voltage setting is equipped with an over-voltage protection (OVP) function. When the voltage at the OVP pin exceeds threshold approximately 1.88V, the power switch is turned off. The power switch can be turned on again once the voltage at the OVP pin drops below 1.6V. For Boost applications, the output voltage can be set by the following equation :

$$V_{CC(MAX)} = 1.88V \times \left(1 + \frac{R1}{R2}\right)$$

R1 and R2 are the voltage divider resistors from VOUT to GND with the divider center node connected to the OVP pin. For MR16 LED lamp application, the minimum voltage of V_{CC} should maintain above 25V for stable operation.

The VCC voltage setting is equipped with an Over-Voltage Protection function. When the voltage at the VCC pin exceeds threshold approximately 39V, the power switch is turned off.

Step-Down Converter Inductor Selection

The RT8415 implemented a simple high efficiency, continuous mode inductive step-down converter. The inductance L2 in Buck converter is determined by the following factors : inductor ripple current, switching frequency, V_{OUT}/V_{CC} ratio, internal MOSFET, topology specifications, and component parameter. The inductance L2 is calculated according to the following equation :

$$L2 \geq \left[V_{CC(MAX)} - V_{OUT} - 0.11 - \left(R_{DS(ON)\_LX2} \times I_{OUT}\right)\right] \times \frac{D2}{\left(f_{SW2} \times \Delta I_{OUT}\right)}$$

where

f_{SW2} is the switching frequency of Buck controller (Hz).

$R_{DS2(ON)\_LX2}$ is the low-side switch on-resistance of internal MOSFET M2. The typical value is 0.2Ω.

D2 is the duty cycle = V_{OUT} / V_{CC}.

I_{OUT} is the required LED current (A).

ΔI_{OUT} is the inductor peak-peak ripple current (internally set to 0.3 x I_{OUT}).

V_{CC} is the Buck input voltage (V).

V_{OUT} is the total LED forward voltage (V).

L2 is the inductance (H).

The selected inductor must have saturation current higher than the peak output LED current and continuous current rating above the required average output LED current. In general, the inductor saturation current should be 1.5 times the LED current. In order to minimize output current ripple, higher values of inductance are recommended at higher supply voltages. Because high values of inductance has high line resistance, it will cause lower efficiency.

Step-Up Converter Inductor Selection

The RT8415 uses a continuous mode and well inductor control to provide wide electronic transformer compatibility step-up converter.

Following the continuous mode mechanism, the inductance L1 is calculated according to the following equation :

$$L1 \geq \left[V_{IN} - V_{FBR} - \left(R_{DS(ON)\_Q1} \times I_{L1}\right) - \left(R4 \times I_{L1}\right) \right] \times \frac{D1}{\left(f_{SW1} \times \Delta I_{L1}\right)}$$

The limit current of first inductor is calculated according to the following equation :

$$I_{L1\_LIMIT} = \frac{V_{CL}}{R4}$$

where

f_{SW1} is the switching frequency of Boost controller (Hz).

$R_{DS(ON)\_Q1}$ is the switch on-resistance of external MOSFET Q1.

D1 is the duty cycle = (V_{CC} – V_{IN}) / V_{CC}.

I_{L1} is the input current. The typical value is 2A for MR16 application.

ΔI_{L1} is the inductor peak-peak ripple current (typically set to 0.055 / R4).

V_{FBR} is the bridge rectifier forward voltage (V).

V_{IN} is the supply input voltage (V).

V_{CC} is the Boost output voltage (V).

V_{CL} is the current limit threshold (0.125V, typ.).

L1 is the inductance (H).

R4 is the CS resistance (Ω).

The selected inductor must have saturation current higher than the limit current of inductance L1. In general, the inductor saturation current should be 1.2 times the limit current of inductance L1. A 10μH to 22μH inductor will meet the demand of most of the RT8415 applications.

1st Stage Current Sense Resistor Selection

The resistor, R4, between CS and GND should be selected to provide adequate switch current to drive the application without exceeding the current limit threshold set by the CS pin sense threshold of the RT8415. The Sense resistor value can be calculated according to the following equation :

$$R4 = \frac{V_{CL}}{I_{L1\_LIMIT}}$$

Where

V_{CL} is the current limit threshold (0.125V, typ.).

I_{L1_LIMIT} is the limit current of first inductor.

Diode Selection

To obtain better efficiency, the Schottky diode is recommended for its low reverse leakage current, low recovery time and low forward voltage. With its low power dissipation, the Schottky diode outperforms other silicon diodes and increases overall efficiency.

Input Capacitor selection

Input capacitor has to supply peak current to the inductor and flatten the current ripple on the input. The low ESR condition is required to avoid increasing power loss. The ceramic capacitor is recommended due to its excellent high frequency characteristic and low ESR, which is suitable for the RT8415. For maximum stability over the entire operating temperature range, capacitors with better dielectric are suggested.

Thermal Protection

A thermal protection feature is to protect the RT8415 from excessive heat damage. When the junction temperature exceeds 150°C, the thermal protection will turn off the GATE1 and LX2 terminals. When the junction temperature drops below 125°C, the RT8415 will turn on the GATE1 and LX2 terminals terminal and return to normal operation.

Thermal Considerations

The junction temperature should never exceed the absolute maximum junction temperature $T_{J(MAX)}$, listed under Absolute Maximum Ratings, to avoid permanent damage to the device. The maximum allowable power dissipation depends on the thermal resistance of the IC package, the PCB layout, the rate of surrounding airflow, and the difference between the junction and ambient temperatures. The maximum power dissipation can be calculated using the following formula :

$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$

where $T_{J(MAX)}$ is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction-to-ambient thermal resistance.

For continuous operation, the maximum operating junction temperature indicated under Recommended Operating Conditions is 125°C. The junction-to-ambient thermal resistance, θ_{JA}, is highly package dependent. For a SOP-8 (Exposed Pad) package, the thermal resistance, θ_{JA}, is 40.6°C/W on a standard JEDEC low effective-thermal-conductivity two-layer test board. The maximum power dissipation at T_A = 25°C can be calculated as below :

$P_{D(MAX)}$ = (125°C – 25°C) / (40.6°C/W) = 2.46W for a SOP-8 (Exposed Pad) package.

The maximum power dissipation depends on the operating ambient temperature for the fixed $T_{J(MAX)}$ and the thermal resistance, θ_{JA}. The derating curves in Figure 1 allows the designer to see the effect of rising ambient temperature on the maximum power dissipation.

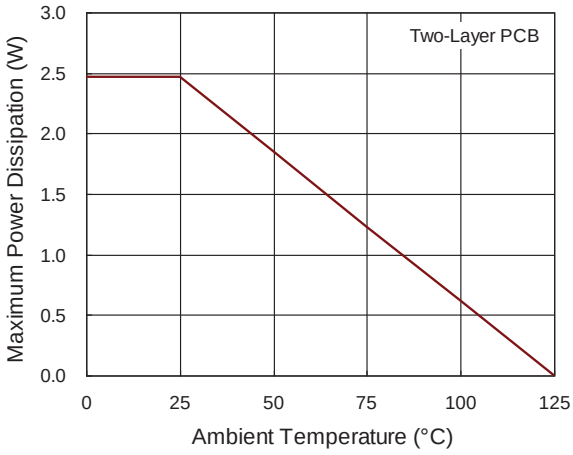


Figure 1. Derating Curve of Maximum Power Dissipation

Layout Consideration

PCB layout is very important to design power switching converter circuits. Some recommended layout guidelines are suggested as follows :

- The power components L1, D5, Q1, C_{IN}, and C_{OUT} must be placed as close to each other as possible to reduce the ac current loop area. The power components L2, D6, and LX2 pin of device must be placed as close to each other as possible to reduce the ac current loop area. The PCB trace between power components must be as short and wide as possible due to large current flow through these traces during operation.
- The capacitor C_{OUT}, C5 and external resistor, R_{SENSE}, must be placed as close as possible to the VCC and ISN pins of the device respectively.
- The GND should be connected to a strong ground plane.
- Keep the main current traces as short and wide as possible.

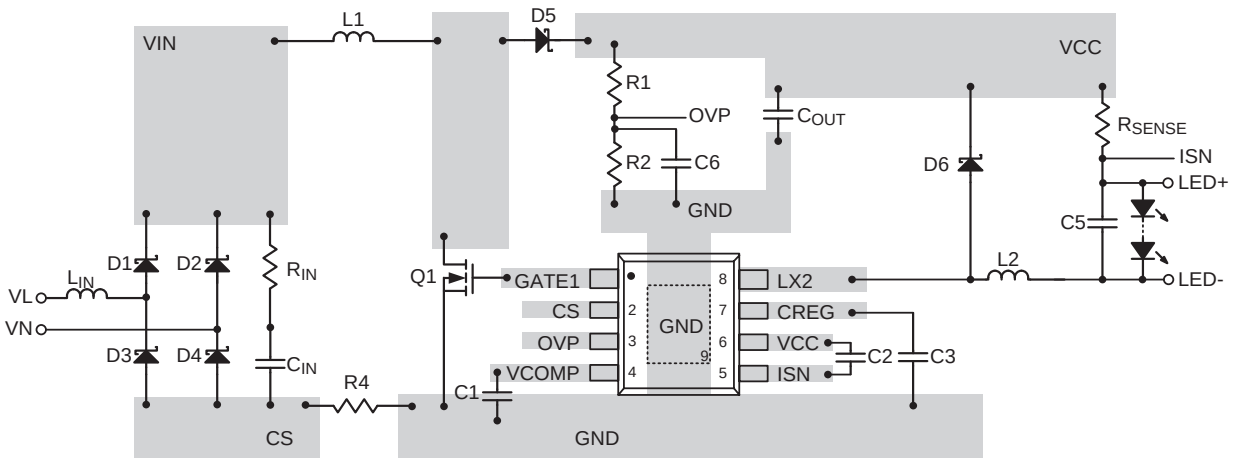
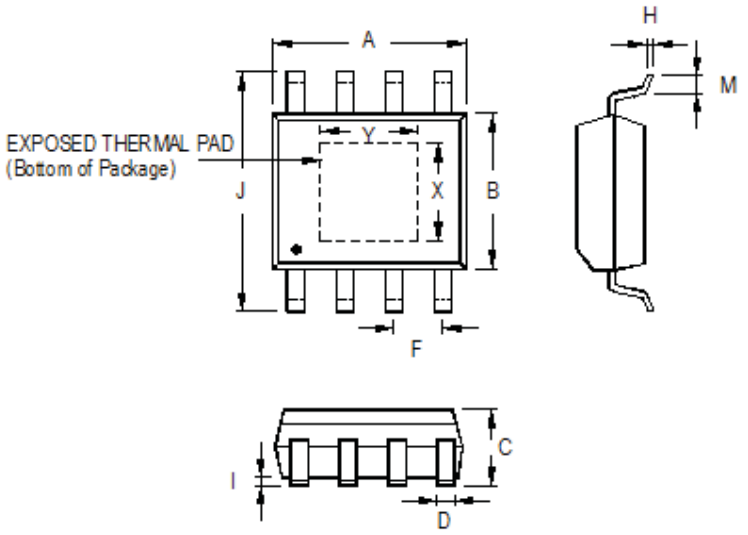


Figure 2. PCB Layout Guide

Outline Dimension



Symbol		Dimensions In Millimeters		Dimensions In Inches	
		Min	Max	Min	Max
A		4.801	5.004	0.189	0.197
B		3.810	4.000	0.150	0.157
C		1.346	1.753	0.053	0.069
D		0.330	0.510	0.013	0.020
F		1.194	1.346	0.047	0.053
H		0.170	0.254	0.007	0.010
I		0.000	0.152	0.000	0.006
J		5.791	6.200	0.228	0.244
M		0.406	1.270	0.016	0.050
Option 1	X	2.000	2.300	0.079	0.091
	Y	2.000	2.300	0.079	0.091
Option 2	X	2.100	2.500	0.083	0.098
	Y	3.000	3.500	0.118	0.138

8-Lead SOP (Exposed Pad) Plastic Package

Richtek Technology Corporation
14F, No. 8, Tai Yuen 1st Street, Chupei City
Hsinchu, Taiwan, R.O.C.
Tel: (8863)5526789