

54AC11175, 74AC11175 QUADRUPLE D-TYPE FLIP-FLOPS WITH CLEAR

SCAS090 – DECEMBER 1989 – REVISED APRIL 1993

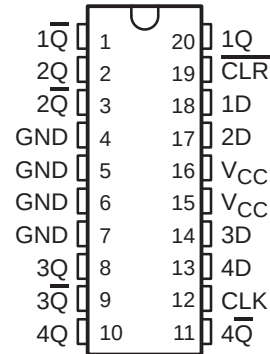
- Applications Include: Buffer/Storage Registers, Shift Registers, Pattern Generators
- Flow-Through Architecture Optimizes PCB Layout
- Center-Pin V_{CC} and GND Configurations Minimize High-Speed Switching Noise
- EPIC™ (Enhanced-Performance Implanted CMOS) 1- μ m Process
- 500-mA Typical Latch-Up Immunity at 125°C
- Package Options Include Plastic Small-Outline Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs

description

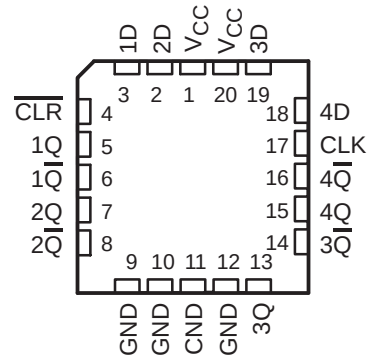
These positive-edge-triggered flipflops implement D-type flip-flop logic with a direct clear input. Information at the D inputs that meets the setup time requirements is transferred to the outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a particular voltage level and is not directly related to the transition time of the positive-going pulse. When the clock input is at either the high or low level, the D input signal has no effect at the output.

The 54AC11175 is characterized for operation over the full military temperature range of – 55°C to 125°C. The 74AC11175 is characterized for operation from – 40°C to 85°C.

54AC11175 . . . J PACKAGE
74AC11175 . . . DW or N PACKAGE
(TOP VIEW)



54AC11014 . . . FK PACKAGE
(TOP VIEW)



FUNCTION TABLE
(each flip-flop)

INPUTS			OUTPUTS	
CLR	CLK	D	Q	$\bar{Q}$
L	X	X	L	H
H	$\uparrow$	H	H	L
H	$\uparrow$	L	L	H
H	L	X	Q_0	$\bar{Q}_0$

EPIC is a trademark of Texas Instruments Incorporated.

UNLESS OTHERWISE NOTED this document contains PRODUCTION DATA information current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

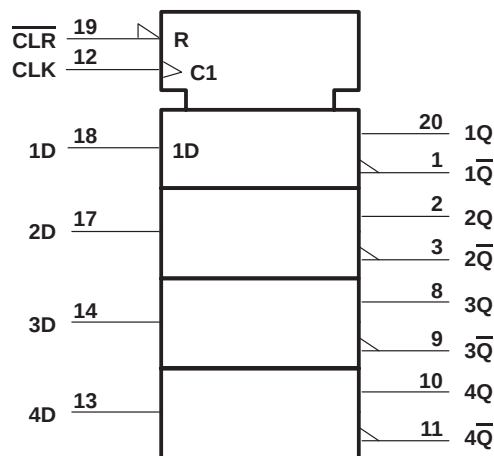
Copyright © 1993, Texas Instruments Incorporated

54AC11175, 74AC11175

QUADRUPLE D-TYPE FLIP-FLOPS WITH CLEAR

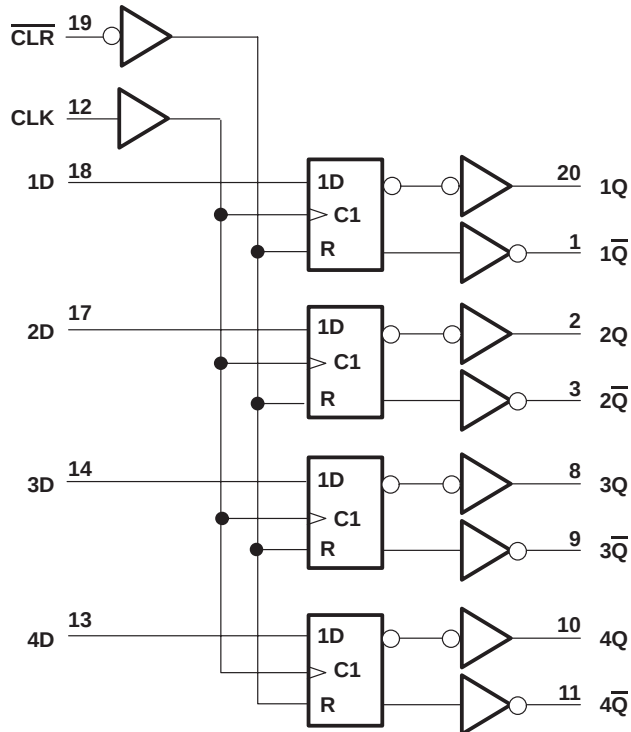
SCAS090 – DECEMBER 1989 – REVISED APRIL 1993

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the DW, J and N packages.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC}	–0.5 V to 7 V
Input voltage range, V_I (see Note 1)	–0.5 V to $V_{CC} + 0.5$ V
Output voltage range, V_O (see Note 1)	–0.5 V to $V_{CC} + 0.5$ V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$)	± 20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	± 50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	± 50 mA
Continuous current through V_{CC} or GND	± 200 mA
Storage temperature range	–65°C to 150°C

‡Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

54AC11175, 74AC11175
QUADRUPLE D-TYPE FLIP-FLOPS
WITH CLEAR

SCAS090 – DECEMBER 1989 – REVISED APRIL 1993

recommended operating conditions

			54AC11175			74AC11175			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V _{CC}	Supply voltage		3	5	5.5	3	5	5.5	V
V _{IH}	High-level input voltage	V _{CC} = 3 V	2.1			2.1			V
		V _{CC} = 4.5 V	3.15			3.15			
		V _{CC} = 5.5 V	3.85			3.85			
V _{IL}	Low-level input voltage	V _{CC} = 3 V	0.9			0.9			V
		V _{CC} = 4.5 V	1.35			1.35			
		V _{CC} = 5.5 V	1.65			1.65			
I _{OH}	High-level output current	V _{CC} = 3 V	−4			−4			mA
		V _{CC} = 4.5 V	−24			−24			
		V _{CC} = 5.5 V	−24			−24			
I _{OL}	Low-level output current	V _{CC} = 3 V	12			12			mA
		V _{CC} = 4.5 V	24			24			
		V _{CC} = 5.5 V	24			24			
V _I	Input voltage		0	V _{CC}		0	V _{CC}		V
V _O	Output voltage		0	V _{CC}		0	V _{CC}		V
Δt/Δv	Input transition rise or fall rate		0	10		0	10		ns/V
T _A	Operating free-air temperature		−55	125		−40	85		°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	T _A = 25°C			54AC11175		74AC11175		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V _{OH}	I _{OH} = – 50 μA	3 V	2.9			2.9		2.9		V
		4.5 V	4.4			4.4		4.4		
		5.5 V	5.4			5.4		5.4		
	I _{OH} = – 4 mA	3 V	2.58			2.4		2.48		
		4.5 V	3.94			3.7		3.8		
		5.5 V	4.94			4.7		4.8		
	I _{OH} = – 50 mA [†]	5.5 V				3.85				
	I _{OH} = – 75 mA [†]	5.5V						3.85		
V _{OL}	I _{OL} = 50 μA	3 V			0.1		0.1		0.1	V
		4.5 V			0.1		0.1		0.1	
		5.5 V			0.1		0.1		0.1	
	I _{OL} = 12 mA	3 V			0.36		0.5		0.44	
		4.5 V			0.36		0.5		0.44	
	I _{OL} = 24 mA	5.5 V			0.36		0.5		0.44	
	I _{OL} = 50 mA	5.5 V					1.65			
	I _{OL} = 75 mA [†]	5.5 V							1.65	
I _I	V _I = V _{CC} or GND	5.5 V			±0.1		±1		±1	μA
I _{CC}	V _I = V _{CC} or GND, I _O = 0	5.5 V			8		160		80	μA
C _i	V _I = V _{CC} or GND	5 V			4					pF

[†] Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.

PRODUCT PREVIEW information concerns products in the formative or design phase of development. Characteristic data and other specifications are design goals. Texas Instruments reserves the right to change or discontinue these products without notice.



POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

54AC11175, 74AC11175 QUADRUPLE D-TYPE FLIP-FLOPS WITH CLEAR

SCAS090 – DECEMBER 1989 – REVISED APRIL 1993

timing requirements over recommended operating free-air temperature range, $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$ (unless otherwise noted) (see Figure 1)

			$T_A = 25^\circ\text{C}$		54AC11175		74AC11175		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency		0	90	0	90	0	90	MHz
t_w	Pulse duration	$\overline{\text{CLR}}$ low	5.5		5.5		5.5		ns
		CLK high or low	5.5		5.5		5.5		
t_{su}	Setup time before CLK $\uparrow$	Data	8		8		8		ns
		$\overline{\text{CLR}}$ inactive	8		8		8		
t_h	Hold time, data after CLK $\uparrow$		0.5		0.5		0.5		ns

timing requirements over recommended operating free-air temperature range, $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$ (unless otherwise noted) (see Figure 1)

			$T_A = 25^\circ\text{C}$		54AC11175		74AC11175		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency		0	125	0	125	0	125	MHz
t_w	Pulse duration	$\overline{\text{CLR}}$ low	4		4		4		ns
		CLK high or low	4		4		4		
t_{su}	Setup time before CLK $\uparrow$	Data	5.5		5.5		5.5		ns
		$\overline{\text{CLR}}$ inactive	5.5		5.5		5.5		
t_h	Hold time, data after CLK $\uparrow$		0.5		0.5		0.5		ns

switching characteristics over recommended operating free-air temperature range, $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$ (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$T_A = 25^\circ\text{C}$			54AC11175		74AC11175		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			90	120		90		90		MHz
t_{PLH}	$\overline{\text{CLR}}$	Any Q	2.6	7	8.7	2.6	9.9	2.6	9.3	ns
		Any $\overline{\text{Q}}$	2.6	7	8.7	2.6	9.9	2.6	9.3	
t_{PHL}	$\overline{\text{CLR}}$	Any Q	2.5	10	11.6	2.5	13	2.5	12.4	ns
		Any $\overline{\text{Q}}$	2.5	10	11.6	2.5	13	2.5	12.4	
t_{PLH}	CLK	Any Q	2.4	6.8	8.7	2.4	9.4	2.4	9.1	ns
		Any $\overline{\text{Q}}$	2.4	6.8	8.7	2.4	9.4	2.4	9.1	
t_{PHL}	CLK	Any Q	1.7	9.4	11.7	1.7	13	1.7	12.5	ns
		Any $\overline{\text{Q}}$	1.7	9.4	11.7	1.7	13	1.7	12.5	

PRODUCT PREVIEW information concerns products in the formative or design phase of development. Characteristic data and other specifications are design goals. Texas Instruments reserves the right to change or discontinue these products without notice.



POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

54AC11175, 74AC11175 QUADRUPLE D-TYPE FLIP-FLOPS WITH CLEAR

SCAS090 – DECEMBER 1989 – REVISED APRIL 1993

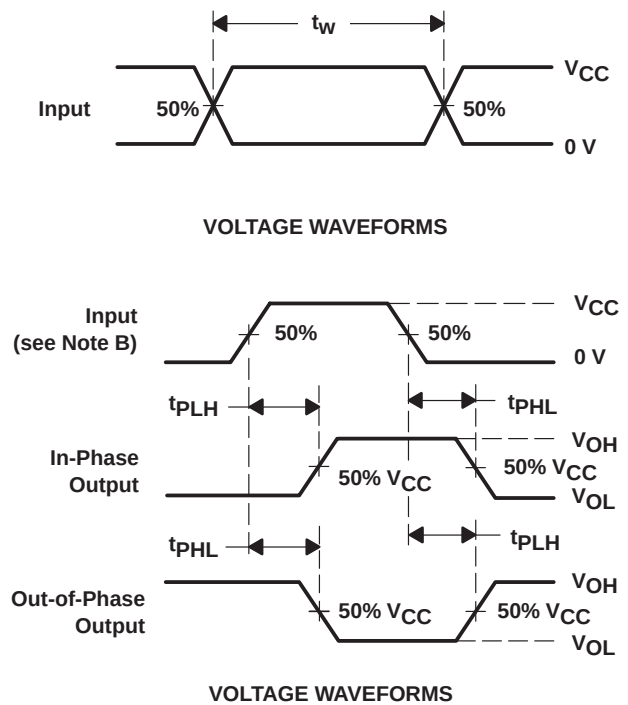
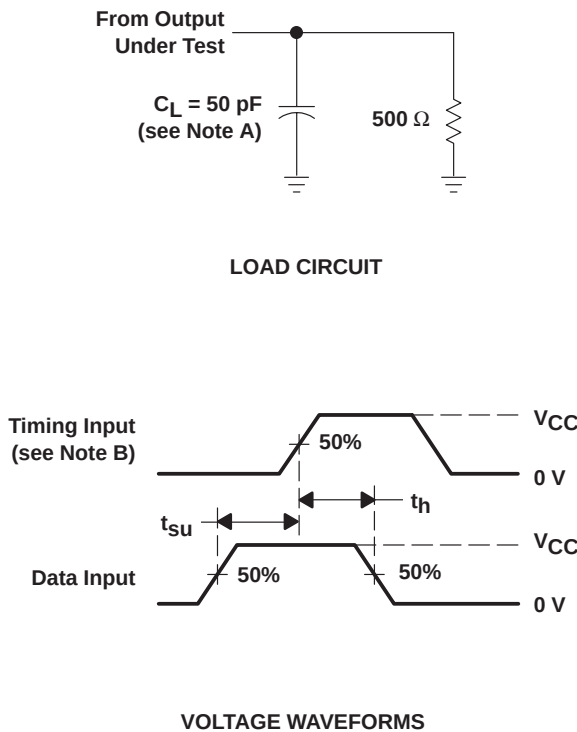
switching characteristics over recommended operating free-air temperature range,
 $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$ (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$T_A = 25^\circ\text{C}$			54AC11175		74AC11175		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
$f_{\max}$			125	150		125		125		MHz
t_{PLH}	CLR	Any Q	2.2	4.5	6.3	2.2	7.1	2.2	6.8	ns
		Any $\overline{Q}$	2.2	4.5	6.3	2.2	7.1	2.2	6.8	
t_{PHL}	$\overline{\text{CLR}}$	Any Q	2.4	6.7	8.5	2.4	9.7	2.4	9.3	ns
		Any $\overline{Q}$	2.4	6.7	8.5	2.4	9.7	2.4	9.3	
t_{PLH}	CLK	Any Q	2.2	4.5	6.3	2.2	7.2	2.2	6.9	ns
		Any $\overline{Q}$	2.2	4.5	6.3	2.2	7.2	2.2	6.9	
t_{PHL}	CLK	Any Q	1.9	6.4	8.5	1.9	9.7	1.9	9.3	ns
		Any $\overline{Q}$	1.9	6.4	8.5	1.9	9.7	1.9	9.3	

operating characteristics, $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	TYP	UNIT
C_{pd} Power dissipation capacitance	$C_L = 50\text{ pF}$, $f = 1\text{ MHz}$	48	pF

PARAMETER MEASUREMENT INFORMATION



NOTES: A. C_L includes probe and jig capacitance.

B. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10\text{ MHz}$, $Z_O = 50\text{ }\Omega$, $t_r = 3\text{ ns}$, $t_f = 3\text{ ns}$.

C. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

PRODUCT PREVIEW information concerns products in the formative or design phase of development. Characteristic data and other specifications are design goals. Texas Instruments reserves the right to change or discontinue these products without notice.



POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

IMPORTANT NOTICE

Texas Instruments and its subsidiaries (TI) reserve the right to make changes to their products or to discontinue any product or service without notice, and advise customers to obtain the latest version of relevant information to verify, before placing orders, that information being relied on is current and complete. All products are sold subject to the terms and conditions of sale supplied at the time of order acknowledgement, including those pertaining to warranty, patent infringement, and limitation of liability.

TI warrants performance of its semiconductor products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are utilized to the extent TI deems necessary to support this warranty. Specific testing of all parameters of each device is not necessarily performed, except those mandated by government requirements.

CERTAIN APPLICATIONS USING SEMICONDUCTOR PRODUCTS MAY INVOLVE POTENTIAL RISKS OF DEATH, PERSONAL INJURY, OR SEVERE PROPERTY OR ENVIRONMENTAL DAMAGE ("CRITICAL APPLICATIONS"). TI SEMICONDUCTOR PRODUCTS ARE NOT DESIGNED, AUTHORIZED, OR WARRANTED TO BE SUITABLE FOR USE IN LIFE-SUPPORT DEVICES OR SYSTEMS OR OTHER CRITICAL APPLICATIONS. INCLUSION OF TI PRODUCTS IN SUCH APPLICATIONS IS UNDERSTOOD TO BE FULLY AT THE CUSTOMER'S RISK.

In order to minimize risks associated with the customer's applications, adequate design and operating safeguards must be provided by the customer to minimize inherent or procedural hazards.

TI assumes no liability for applications assistance or customer product design. TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right of TI covering or relating to any combination, machine, or process in which such semiconductor products or services might be or are used. TI's publication of information regarding any third party's products or services does not constitute TI's approval, warranty or endorsement thereof.