



PI74AVC+16374

2.5V 16-Bit Edge Triggered D-Type Flip-Flop with 3-State Outputs

Product Features

- PI74AVC+16374 is designed for low voltage operation, $V_{CC} = 1.65V$ to $3.6V$
- True $\pm 24mA$ Balanced Drive @ $3.3V$
- Compatible with Philips and T.I. AVC Logic family
- I_{OFF} supports partial power-down operation
- $3.6V$ I/O Tolerant inputs and outputs
- All outputs contain a patented DDC (Dynamic Drive Control) circuit that reduces noise without degrading propagation delay.
- Industrial operation at $-40^{\circ}C$ to $+85^{\circ}C$
- Available Packages:
 - 48-pin 240-mil wide plastic TSSOP
 - 48-pin 173-mil wide plastic TVSOP

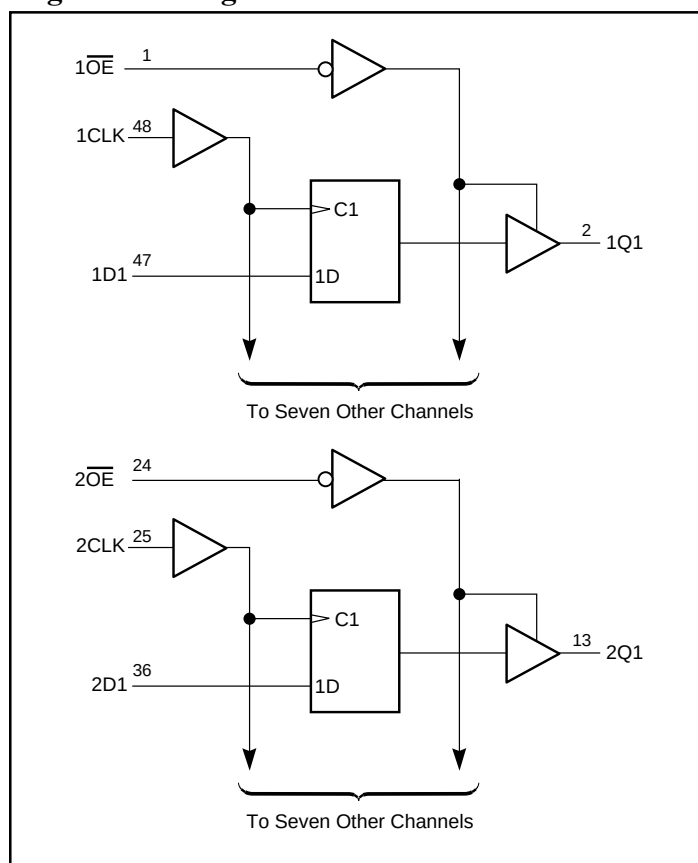
Product Description

Pericom Semiconductor's PI74AVC+ series of logic circuits are produced using the Company's advanced submicron CMOS technology, achieving industry leading speed.

The PI74ALVCH16374 is particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers. This device can be used as two 8-bit flip-flops or one 16-bit flip-flop. On the positive transition of the Clock (CLK) input, the Q outputs of the flip-flop take on the logic levels set up at the data (D) inputs. $\overline{OE}$ can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In that state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and the increased drive provide the capability to drive bus lines without need for interface or pullup components. $\overline{OE}$ does not affect internal operations of the flip-flop. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

Logic Block Diagram



Maximum Ratings (Above which the useful life may be impaired. For user guidelines, not tested.)

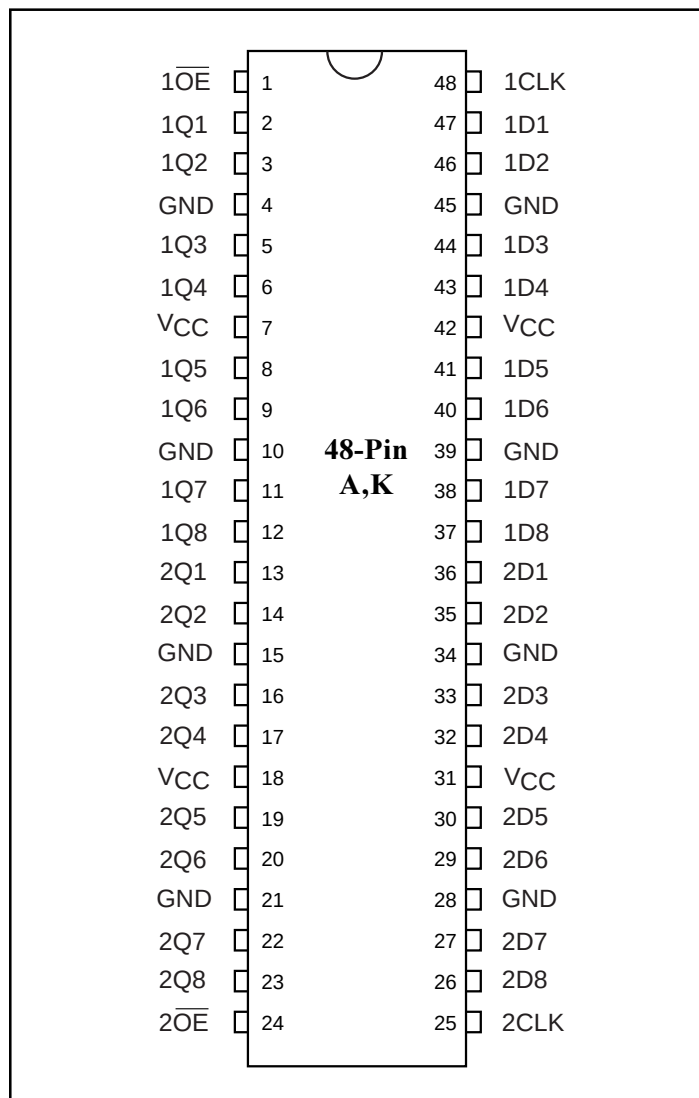
Supply voltage range, V_{CC}	−0.5V to +4.6V
Input voltage range, V_I	−0.5V to +4.6V
Voltage range applied to any output in the high-impedance or power-off state, $V_O^{(1)}$	−0.5V to +4.6V
Voltage range applied to any output in the high or low state, $V_O^{(1,2)}$	−0.5V to $V_{CC}+0.5V$
Input clamp current, I_{IK} ($V_I < 0$)	−50mA
Output clamp current, I_{OK} ($V_O < 0$)	−50mA
Continuous output current, I_O	±50mA
Continuous current through each V_{CC} or GND	±100mA
Package thermal impedance, $\theta_{JA}^{(3)}$: package A	64°C/W
package K	48°C/W
Storage Temperature range, T_{stg}	−65°C to 150°C

Notes:

Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

1. Input & output negative-voltage ratings may be exceeded if the input and output current rating are observed.
2. Output positive-voltage rating may be exceeded up to 4.6V maximum if the output current rating is observed.
3. The package thermal impedance is calculated in accordance with JESD 51.

Product Pin Configuration



Product Pin Description

Pin Name	Description
$\overline{OE}$	3-State Output Enable Inputs (Active LOW)
CLK	Clock Input (Active HIGH)
Dx	Data Inputs
Qx	3-State Outputs
GND	Ground
VCC	Power

Truth Table⁽¹⁾

Inputs			Outputs
$\overline{OE}$	CLK	D	Q
L	↑	H	H
L	↑	L	L
L	H or L	X	Q_0
H	X	X	Z

Notes:

1. H = High Signal Level
L = Low Signal Level
X = Don't Care or Irrelevant
Z = High Impedance

Recommended Operating Conditions⁽¹⁾

		Min.	Max.	Units
V _{CC} Supply Voltage	Operating	1.4	3.6	V
	Data retention only	1.2		
V _{IH} High-level Input Voltage	V _{CC} = 1.2V	V _{CC}		
	V _{CC} = 1.4V to 1.6V	0.65 x V _{CC}		
	V _{CC} = 1.65V to 1.95V	0.65 x V _{CC}		
	V _{CC} = 2.3V to 2.7V	1.7		
	V _{CC} = 3V to 3.6V	2		
V _{IL} Low-level Input Voltage	V _{CC} = 1.2V		GND	
	V _{CC} = 1.4V to 1.6V		0.35 x V _{CC}	
	V _{CC} = 1.65V to 1.95V		0.35 x V _{CC}	
	V _{CC} = 2.3V to 2.7V		0.7	
	V _{CC} = 3V to 3.6V		0.8	
V _I Input Voltage		0	3.6	
V _O Output Voltage	Active State	0	V _{CC}	
	3-State	0	3.6	
I _{OHS} High-level output current	V _{CC} = 1.4V to 1.6V		– 4	mA
	V _{CC} = 1.65V to 1.95V		– 6	
	V _{CC} = 2.3V to 2.7V		– 12	
	V _{CC} = 3V to 3.6V		– 24	
I _{OLS} Low-level output current	V _{CC} = 1.4V to 1.6V		4	
	V _{CC} = 1.65V to 1.95V		6	
	V _{CC} = 2.3V to 2.7V		12	
	V _{CC} = 3V to 3.6V		24	
ΔtΔv Input transition rise or fall rate	V _{CC} = 1.4V to 3.6V		5	ns/V
T _A Operating free-air temperature		–40	85	°C

Notes:

1. All unused inputs must be held at V_{CC} or GND to ensure proper device operation.

DC Electrical Characteristics (Over the Operating Range, $T_A = -40^\circ\text{C} + 85^\circ\text{C}$)

Parameters		Test Conditions ⁽¹⁾	V _{CC}	Min.	Typ.	Max.	Units	
V _{OH}		I _{OH} = −100μA	1.4V to 3.6V	V _{CC} −0.2V			V	
		I _{OHS} = −4mA V _{IH} = 0.91V	1.4V	1.05				
		I _{OHS} = −6mA V _{IH} = 1.07V	1.65V	1.2				
		I _{OHS} = −12mA V _{IH} = 1.7V	2.3V	1.75				
		I _{OHS} = −24mA V _{IH} = 2V	3V	2.0				
V _{OL}		I _{OLS} = 100μA	1.4V to 3.6V			0.2		
		I _{OLS} = 4mA V _{IL} = 0.49V	1.4V			0.4		
		I _{OLS} = 6mA V _{IL} = 0.57V	1.65V			0.45		
		I _{OLS} = 12mA V _{IL} = 0.7V	2.3V			0.55		
		I _{OLS} = 24mA V _{IL} = 0.8V	3V			0.75		
I _I	Control Inputs	V _I = V _{CC} or GND	3.6V			±2.5	μA	
I _{OFF}		V _I or V _O = 3.6V	0			±10		
I _{OZ}		V _O = V _{CC} or GND	3.6V			±10		
I _{CC}		V _I = V _{CC} or GND I _O = 0	3.6V			40		
C _I	Control Inputs	V _I = V _{CC} or GND	2.5V		3.5		pF	
			3.3V		3.5			
	Data Inputs		2.5V		6			
			3.3V		6			
C _O	Outputs		V _O = V _{CC} or GND	2.5V		6.5		
				3.3V		6.5		

Note: Typical values are measured at $T_A = 25^\circ\text{C}$.

Timing requirements over recommended operating free-air temperature range

(unless otherwise noted, see Figures 1 thru 4)

	$V_{CC} = 1.2V$		$V_{CC} = 1.5V \pm 0.1V$		$V_{CC} = 1.8V \pm 0.15V$		$V_{CC} = 2.5V \pm 0.2V$		$V_{CC} = 3.3V \pm 0.3V$		Units
	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
f_{clock} Clock frequency						160		200		200	ns
t_w Pulse duration, CLK high or low					3.1		2.5		2.5		
t_{su} Setup time, data before CLK $\uparrow$	4.1		2.7		1.9		1.4		1.4		
t_h Hold time, data after CLK $\uparrow$	1.7		1.3		1.2		1.1		1.1		

Switching Characteristics over recommended operating free-air temperature range

(unless otherwise noted, see Figures 1 thru 4)

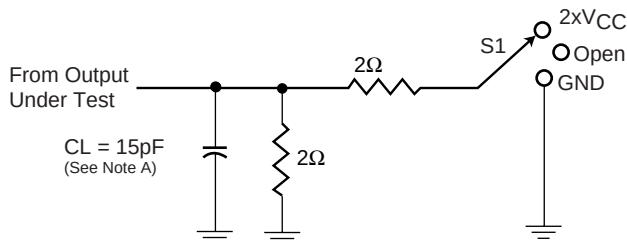
Parameters	From (Input)	To (Output)	$V_{CC} = 1.2V$	$V_{CC} = 1.5V \pm 0.1V$		$V_{CC} = 1.8V \pm 0.15V$		$V_{CC} = 2.5V \pm 0.2V$		$V_{CC} = 3.3V \pm 0.3V$		Units
			Typ.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
f_{max}						160		200		200		ns
t_{pd}	CLK	Q	7.3	1.5	8.4	1.2	6.7	0.8	4.1	0.7	3.3	
t_{en}	$\overline{OE}$	Q	7.4	1.6	8.5	1.6	6.7	0.9	4.3	0.7	3.4	
t_{ds}	$\overline{OE}$	Q	8.4	2.5	9.4	2.3	7.8	1	4.2	1.5	3.9	

Operating Characteristics, $T_A = 25^\circ C$

Parameters		Test Conditions	$V_{CC} = 1.8V \pm 0.15V$	$V_{CC} = 2.5V \pm 0.2V$	$V_{CC} = 3.3V \pm 0.3V$	Units
			Typical	Typical	Typical	
Cpd Power Dissipation Capacitance	Outputs Enabled	$C_L = 0pF$, $f = 10 MHz$ 2 outputs switching	74	81	89	pF
	Outputs Disabled		52	57	63	

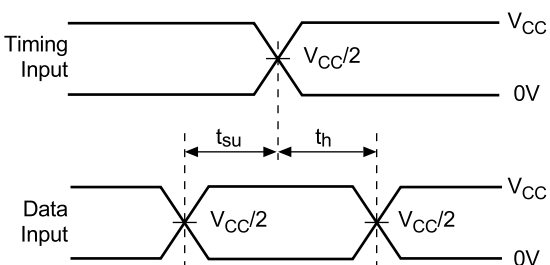
PARAMETER MEASUREMENT INFORMATION

$V_{CC} = 1.2V \text{ AND } 1.5V \pm 0.1V$

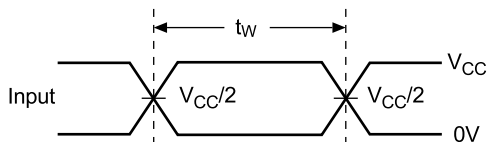


Load Circuit

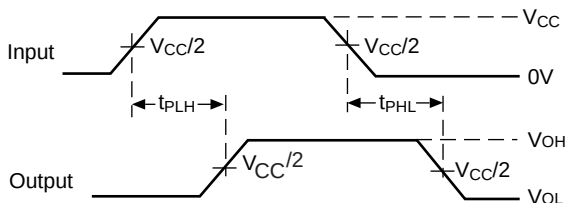
Test	S1
t_{pd} t_{PLZ}/t_{PZL} t_{PHZ}/t_{PZH}	Open $2 \times V_{CC}$ GND



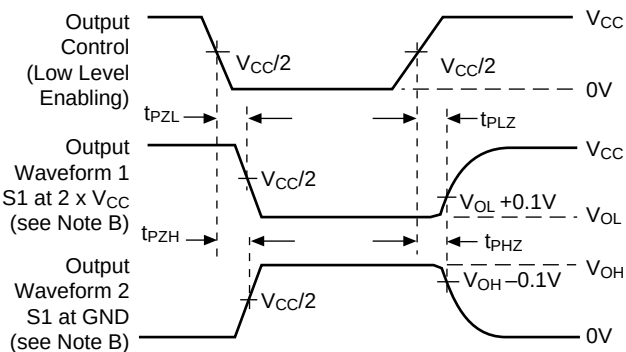
**Voltage Waveforms
Setup and Hold Times**



**Voltage Waveforms
Pulse Duration**



**Voltage Waveforms
Propagation Delay Times**



**Voltage Waveforms
Enable and Disable Times**

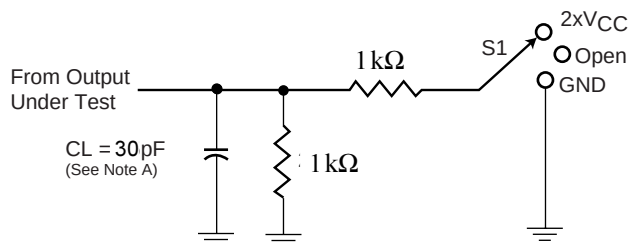
Figure 1. Load Circuit and Voltage Waveforms

Notes:

- C_L includes probe and jig capacitance.
- Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.
Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- All input impulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50\Omega$, $t_R \leq 2.0ns$, $t_F \leq 2.0ns$.
- The outputs are measured one at a time with one transition per measurement.
- t_{PLZ} and t_{PHZ} are the same as t_{dis}
- t_{PZL} and t_{PZH} are the same as t_{en}
- t_{PLH} and t_{PHL} are the same as t_{pd}

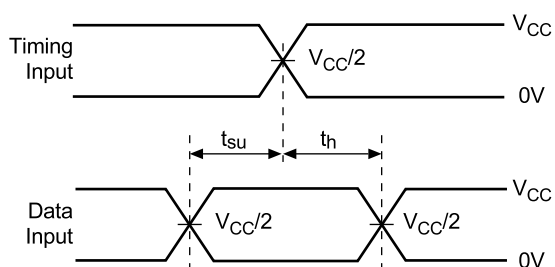
PARAMETER MEASUREMENT INFORMATION

$$V_{CC} = 1.8V \pm 0.15V$$

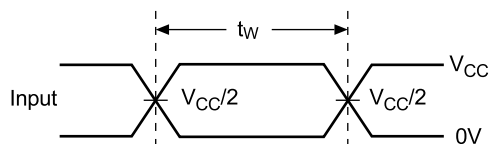


Load Circuit

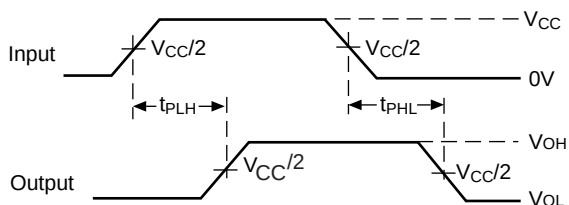
Test	S1
t _{pd} t _{PLZ} /t _{PZL} t _{PHZ} /t _{PZH}	Open 2 x V _{CC} GND



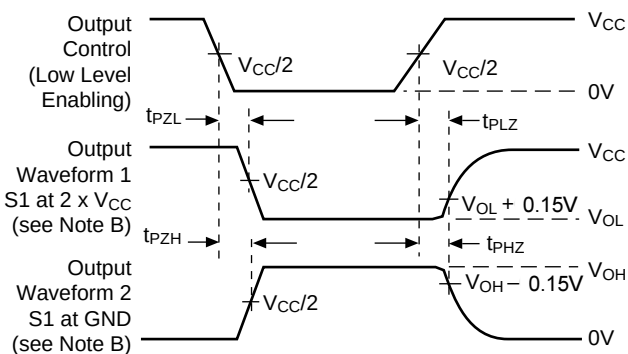
**Voltage Waveforms
Setup and Hold Times**



**Voltage Waveforms
Pulse Duration**



**Voltage Waveforms
Propagation Delay Times**



**Voltage Waveforms
Enable and Disable Times**

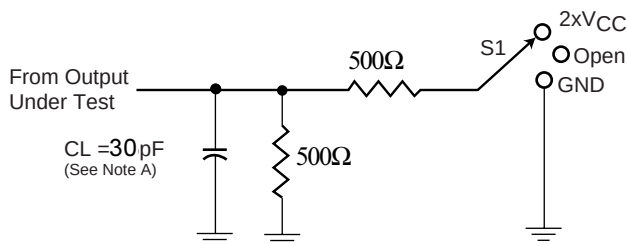
Figure2. Load Circuit and Voltage Waveforms

Notes:

- C_L includes probe and jig capacitance.
- Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- All input impulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50Ω, t_R ≤ 2.0ns, t_F ≤ 2.0ns.
- The outputs are measured one at a time with one transition per measurement.
- t_{PLZ} and t_{PHZ} are the same as t_{dis}
- t_{PZL} and t_{PZH} are the same as t_{en}
- t_{PLH} and t_{PHL} are the same as t_{pd}

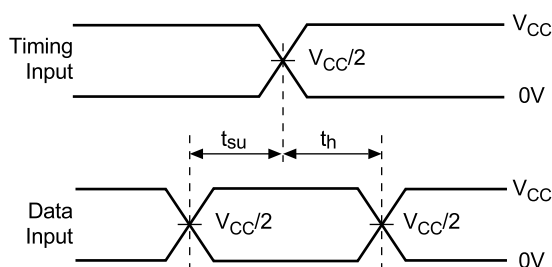
PARAMETER MEASUREMENT INFORMATION

$$V_{CC} = 2.5V \pm 0.2V$$

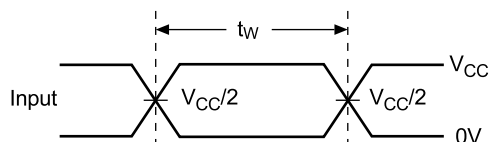


Load Circuit

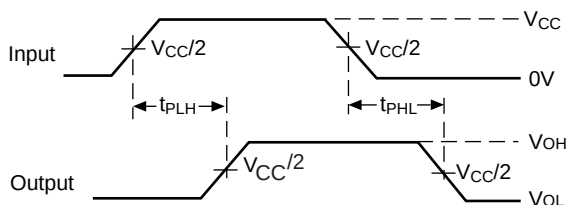
Test	S1
t _{pd} t _{PLZ} /t _{PZL} t _{PHZ} /t _{PZH}	Open 2 x V _{CC} GND



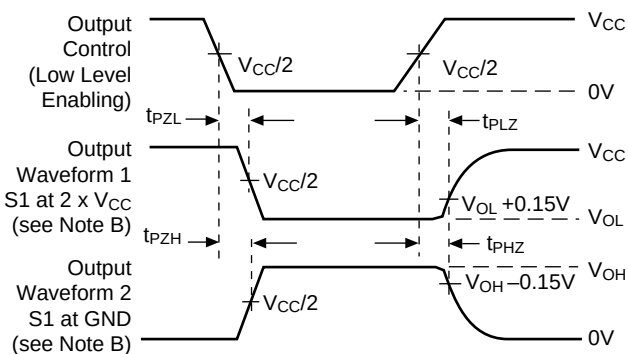
**Voltage Waveforms
Setup and Hold Times**



**Voltage Waveforms
Pulse Duration**



**Voltage Waveforms
Propagation Delay Times**



**Voltage Waveforms
Enable and Disable Times**

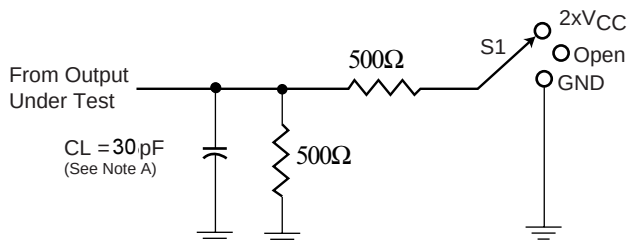
Figure3. Load Circuit and Voltage Waveforms

Notes:

- C_L includes probe and jig capacitance.
- Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- All input impulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50Ω, t_R ≤ 2.0ns, t_F ≤ 2.0ns.
- The outputs are measured one at a time with one transition per measurement.
- t_{PLZ} and t_{PHZ} are the same as t_{dis}
- t_{PZL} and t_{PZH} are the same as t_{en}
- t_{PLH} and t_{PHL} are the same as t_{pd}

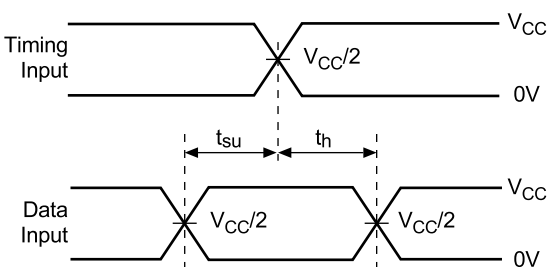
PARAMETER MEASUREMENT INFORMATION

$$V_{CC} = 3.3V \pm 0.3V$$

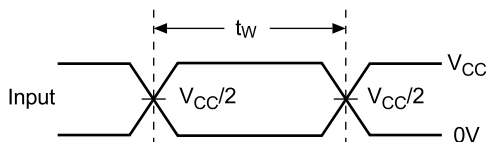


Load Circuit

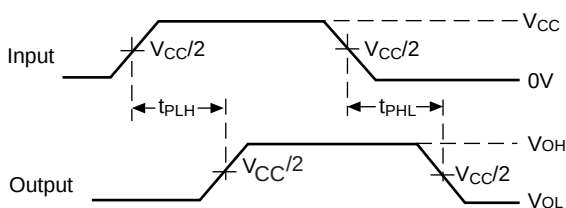
Test	S1
t_{pd} t_{PLZ}/t_{PZL} t_{PHZ}/t_{PZH}	Open 2 x VCC GND



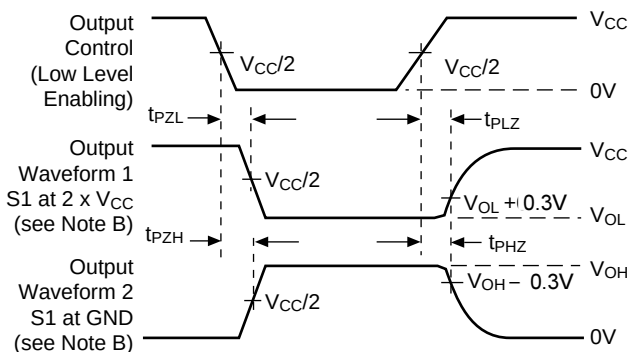
**Voltage Waveforms
Setup and Hold Times**



**Voltage Waveforms
Pulse Duration**



**Voltage Waveforms
Propagation Delay Times**



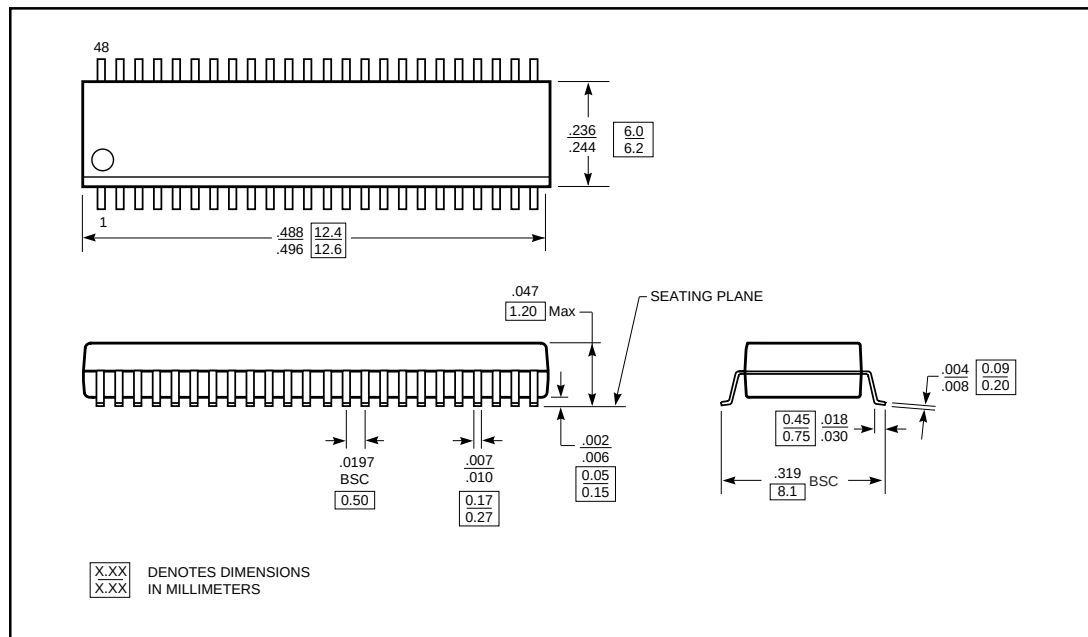
**Voltage Waveforms
Enable and Disable Times**

Figure 4. Load Circuit and Voltage Waveforms

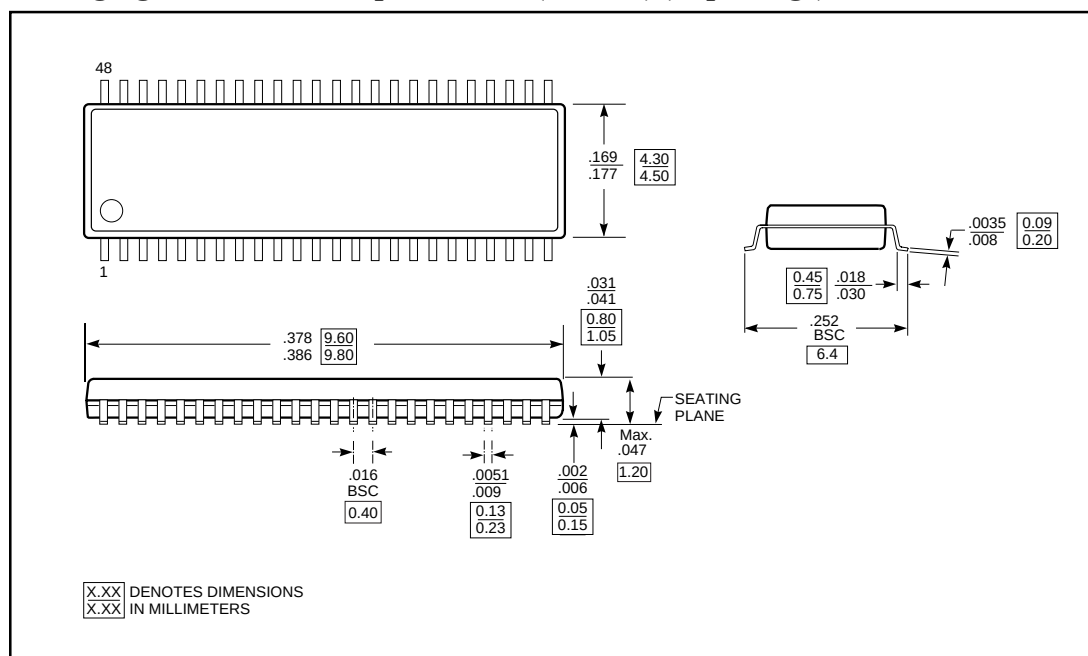
Notes:

- C_L includes probe and jig capacitance.
- Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- All input impulses are supplied by generators having the following characteristics: $PRR \leq 10\text{ MHz}$, $Z_O = 50\Omega$, $t_R \leq 2.0\text{ns}$, $t_F \leq 2.0\text{ns}$.
- The outputs are measured one at a time with one transition per measurement.
- t_{PLZ} and t_{PHZ} are the same as t_{dis}
- t_{PZL} and t_{PZH} are the same as t_{en}
- t_{PLH} and t_{PHL} are the same as t_{pd}

Packaging Mechanical - 48-pin TSSOP (A-package)



Packaging Mechanical - 48-pin TVSOP (TSSOP) (K-package)



Ordering Information	Description
PI74AVC+16374A	48-pin, 240-mil wide plastic TSSOP
PI74AVC+16374K	48-pin, 173-mil wide plastic TVSOP