

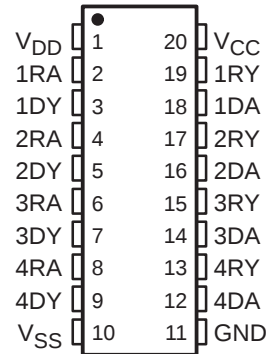
SN75C1154

QUADRUPLE LOW-POWER DRIVERS/RECEIVERS

SLLS151C – DECEMBER 1988 – REVISED MARCH 1997

- Meets or Exceeds the Requirements of ANSI EIA/TIA-232-E and ITU Recommendation V.28
- Very Low Power Consumption
5 mW Typ
- Wide Driver Supply Voltage . . . ± 4.5 V to ± 15 V
- Driver Output Slew Rate Limited to 30 V/ μ s Max
- Receiver Input Hysteresis . . . 1000 mV Typ
- Push-Pull Receiver Outputs
- On-Chip Receiver 1- μ s Noise Filter
- Functionally interchangeable With Motorola MC145404

DW OR N PACKAGE
(TOP VIEW)



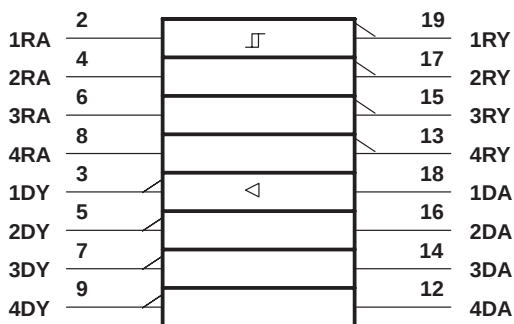
description

The SN75C1154 is a low-power BiMOS device containing four independent drivers and receivers that are used to interface data terminal equipment (DTE) with data circuit-terminating equipment (DCE). This device has been designed to conform to ANSI EIA/TIA-232-E. The drivers and receivers of the SN75C1154 are similar to those of the SN75C188 quadruple driver and SN75C189A quadruple receiver, respectively. The drivers have a controlled output slew rate that is limited to a maximum of 30 V/ μ s and the receivers have filters that reject input noise pulses of shorter than 1 μ s. Both these features eliminate the need for external components.

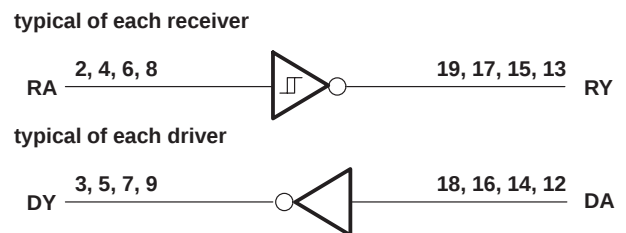
The SN75C1154 is designed using low-power techniques in a BiMOS technology. In most applications, the receivers contained in these devices interface to single inputs of peripheral devices such as ACEs, UARTs, or microprocessors. By using sampling, such peripheral devices are usually insensitive to the transition times of the input signals. If this is not the case or for other uses, it is recommended that the SN75C1154 receiver outputs be buffered by single Schmitt input gates or single gates of the HCMOS, ALS, or 74F logic families.

The SN75C1154 is characterized for operation from 0°C to 70°C.

logic symbol†



logic diagram (positive logic)



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

**TEXAS
INSTRUMENTS**

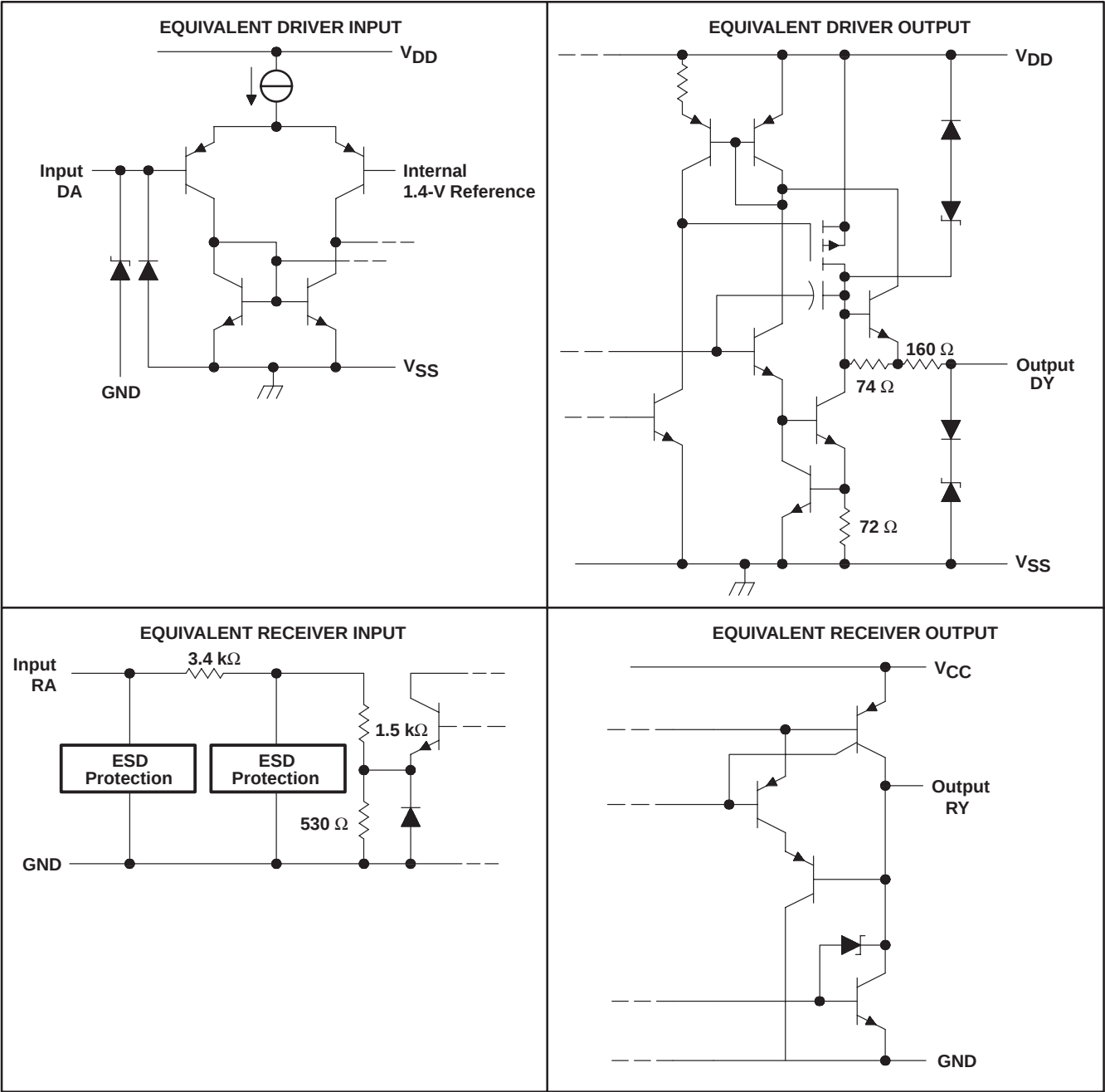
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

Copyright © 1997, Texas Instruments Incorporated

SN75C1154 QUADRUPLE LOW-POWER DRIVERS/RECEIVERS

SLLS151C – DECEMBER 1988 – REVISED MARCH 1997

schematics of inputs and outputs



Resistor values shown are nominal.

SN75C1154

QUADRUPLE LOW-POWER DRIVERS/RECEIVERS

SLLS151C – DECEMBER 1988 – REVISED MARCH 1997

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage, V_{DD} (see Note 1)	15 V
Supply voltage, V_{SS}	–15 V
Supply voltage, V_{CC}	7 V
Input voltage range, V_I : Driver	V_{SS} to V_{DD}
Receiver	–30 V to 30 V
Output voltage range, V_O : Driver	($V_{SS} - 6$ V) to ($V_{DD} + 6$ V)
Receiver	–0.3 V to ($V_{CC} + 0.3$ V)
Continuous total power dissipation	See Dissipation Rating Table
Operating free-air temperature range, T_A : SN75C1154	0°C to 70°C
Storage temperature range, T_{stg}	–65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltages are with respect to the network GND terminal.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25^\circ\text{C}$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25^\circ\text{C}$	$T_A = 70^\circ\text{C}$ POWER RATING
DW	1125 mW	9.0 mW/°C	720 mW
N	1150 mW	9.2 mW/°C	736 mW

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V _{DD}		4.5	12	15	V
Supply voltage, V _{SS}		−4.5	−12	−15	V
Supply voltage, V _{CC}		4.5	5	6	V
Input voltage, V _I	Driver	V _{SS} +2		V _{DD}	V
	Receiver	±25			
High-level input voltage, V _{IH}	Driver	2			V
Low-level input voltage, V _{IL}				0.8	
High-level output current, I _{OH}	Receiver			−1	mA
High-level output current, I _{OL}				3.2	mA
Operating free-air temperature, T _A		0		70	°C

SN75C1154

QUADRUPLE LOW-POWER DRIVERS/RECEIVERS

SLLS151C – DECEMBER 1988 – REVISED MARCH 1997

DRIVER SECTION

electrical characteristics over operating free-air temperature range, $V_{DD} = 12\text{ V}$, $V_{SS} = -12\text{ V}$, $V_{CC} = 5\text{ V} \pm 10\%$ (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP [†]	MAX	UNIT
V_{OH} High-level output voltage	$V_{IL} = 0.8\text{ V}$, $R_L = 3\text{ k}\Omega$, See Figure 1	$V_{DD} = 5\text{ V}$, $V_{SS} = -5\text{ V}$	4	4.5	V
		$V_{DD} = 12\text{ V}$, $V_{SS} = -12\text{ V}$	10	10.8	
V_{OL} Low-level output voltage (see Note 2)	$V_{IH} = 2\text{ V}$, $R_L = 3\text{ k}\Omega$, See Figure 1	$V_{DD} = 5\text{ V}$, $V_{SS} = -5\text{ V}$	-4.4	-4	V
		$V_{DD} = 12\text{ V}$, $V_{SS} = -12\text{ V}$	-10.7	-10	
I_{IH} High-level input current	$V_I = 5\text{ V}$, See Figure 2			1	μA
I_{IL} Low-level input current	$V_I = 0$, See Figure 2			-1	μA
$I_{OS(H)}$ High-level short circuit output current [‡]	$V_I = 0.8\text{ V}$, $V_O = 0$ or V_{SS} , See Figure 1	-7.5	-12	-19.5	mA
$I_{OS(L)}$ Low-level short circuit output current [‡]	$V_I = 2\text{ V}$, $V_O = 0$ or V_{DD} , See Figure 1	7.5	12	19.5	mA
I_{DD} Supply current from V_{DD}	No load, All inputs at 2 V or 0.8 V	$V_{DD} = 5\text{ V}$, $V_{SS} = -5\text{ V}$	115	250	μA
		$V_{DD} = 12\text{ V}$, $V_{SS} = -12\text{ V}$	115	250	
I_{SS} Supply current from V_{SS}	No load, All inputs at 2 V or 0.8 V	$V_{DD} = 5\text{ V}$, $V_{SS} = -5\text{ V}$	-115	-250	μA
		$V_{DD} = 12\text{ V}$, $V_{SS} = -12\text{ V}$	-115	-250	
r_o Output resistance	$V_{DD} = V_{SS} = V_{CC} = 0$, $V_O = -2\text{ V}$ to 2 V , See Note 3	300	400		Ω

[†] All typical values are at $T_A = 25^\circ\text{C}$.

[‡] Not more than one output should be shorted at one time.

NOTES: 2. The algebraic convention, where the more positive (less negative) limit is designated as maximum, is used in this data sheet for logic levels only.

3. Test conditions are those specified by EIA/TIA-232-E.

switching characteristics, $V_{DD} = 12\text{ V}$, $V_{SS} = -12\text{ V}$, $V_{CC} = 5\text{ V} \pm 10\%$, $T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH} Propagation delay time, low- to high-level output [§]	$R_L = 3$ to $7\text{ k}\Omega$, $C_L = 15\text{ pF}$, See Figure 3		1.2	3	μs
t_{PHL} Propagation delay time, high- to low-level output [§]			2.5	3.5	μs
t_{TLH} Transition time, low- to high-level output [¶]		0.53	2	3.2	μs
t_{THL} Transition time, high- to low-level output [¶]		0.53	2	3.2	μs
t_{TLH} Transition time, low- to high-level output [#]	$R_L = 3$ to $7\text{ k}\Omega$, $C_L = 2500\text{ pF}$, See Figure 3		1	2	μs
t_{THL} Transition time, high- to low-level output [#]	$R_L = 3$ to $7\text{ k}\Omega$, $C_L = 2500\text{ pF}$, See Figure 3		1	2	μs
SR Output slew rate	$R_L = 3$ to $7\text{ k}\Omega$, $C_L = 15\text{ pF}$, See Figure 3	4	10	30	V/ μs

[§] t_{PHL} and t_{PLH} include the additional time due to on-chip slew rate control and are measured at the 50% points.

[¶] Measured between 10% and 90% points of output waveform.

[#] Measured between 3 V and -3 V points of output waveform (EIA/TIA-232-E conditions) with all unused inputs tied either high or low.



RECEIVER SECTION

electrical characteristics over operating free-air temperature range, $V_{DD} = 12\text{ V}$, $V_{SS} = -12\text{ V}$, $V_{CC} = 5\text{ V} \pm 10\%$ (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP [†]	MAX	UNIT
V_{IT+} Positive-going input threshold voltage	See Figure 5	1.7	2.1	2.55	V
V_{IT-} Negative-going input threshold voltage	See Figure 5	0.65	1	1.25	V
V_{hys} Input hysteresis voltage ($V_{IT+} - V_{IT-}$)		600	1000		mV
V_{OH} High-level output voltage	$V_I = 0.75\text{ V}$, $I_{OH} = -20\text{ }\mu\text{A}$, See Figure 5 and Note 4	3.5			V
	$V_I = 0.75\text{ V}$, $I_{OH} = -1\text{ mA}$, See Figure 5	$V_{CC} = 4.5\text{ V}$	2.8	4.4	
		$V_{CC} = 5\text{ V}$	3.8	4.9	
		$V_{CC} = 5.5\text{ V}$	4.3	5.4	
V_{OL} Low-level output voltage	$V_I = 3\text{ V}$, $I_{OL} = 3.2\text{ mA}$, See Figure 5		0.17	0.4	V
I_{IH} High-level input current	$V_I = 25\text{ V}$	3.6	4.6	8.3	mA
	$V_I = 3\text{ V}$	0.43	0.55	1	
I_{IL} Low-level input current	$V_I = -25\text{ V}$	-3.6	-5	-8.3	
	$V_I = -3\text{ V}$	-0.43	-0.55	-1	
$I_{OS(H)}$ Short-circuit output at high level	$V_I = 0.75\text{ V}$, $V_O = 0$, See Figure 4		-8	-15	mA
$I_{OS(L)}$ Short-circuit output at low level	$V_I = V_{CC}$, $V_O = V_{CC}$, See Figure 4		13	25	mA
I_{CC} Supply current from V_{CC}	No load, All inputs at 0 or 5 V	$V_{DD} = 5\text{ V}$, $V_{SS} = -5\text{ V}$	400	600	μA
		$V_{DD} = 12\text{ V}$, $V_{SS} = -12\text{ V}$	400	600	

[†] All typical values are at $T_A = 25^\circ\text{C}$.

NOTE 4: If the inputs are left unconnected, the receiver interprets this as an input low and the receiver outputs will remain in the high state.

switching characteristics, $V_{DD} = 12\text{ V}$, $V_{SS} = -12\text{ V}$, $V_{CC} = 5\text{ V} \pm 10\%$, $T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH} Propagation delay time, low- to high-level output	$C_L = 50\text{ pF}$, $R_L = 5\text{ k}\Omega$, See Figure 6		3	4	μs
t_{PHL} Propagation delay time, high- to low-level output			3	4	μs
t_{TLH} Transition time, low- to high-level output			300	450	ns
t_{THL} Transition time, high- to low-level output			100	300	ns
$t_{W(N)}$ Duration of longest pulse rejected as noise [‡]	$C_L = 50\text{ pF}$, $R_L = 5\text{ k}\Omega$	1		4	μs

[‡] The receiver ignores any positive- or negative-going pulse that is less than the minimum value of $t_{W(N)}$ and accepts any positive- or negative-going pulse greater than the maximum of $t_{W(N)}$.

SN75C1154

QUADRUPLE LOW-POWER DRIVERS/RECEIVERS

SLLS151C – DECEMBER 1988 – REVISED MARCH 1997

PARAMETER MEASUREMENT INFORMATION

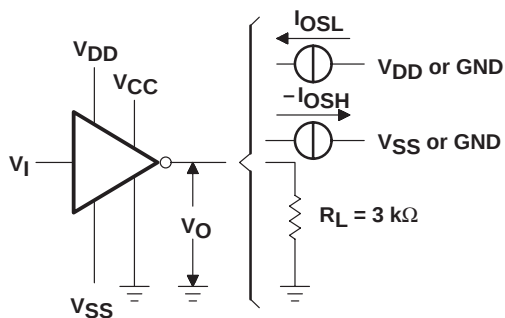


Figure 1. Driver Test Circuit
 V_{OH} , V_{OL} , I_{OSL} , I_{OSH}

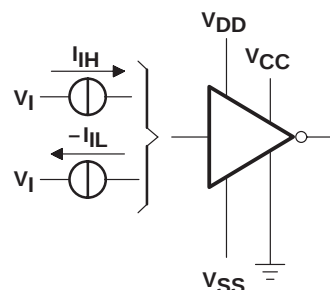
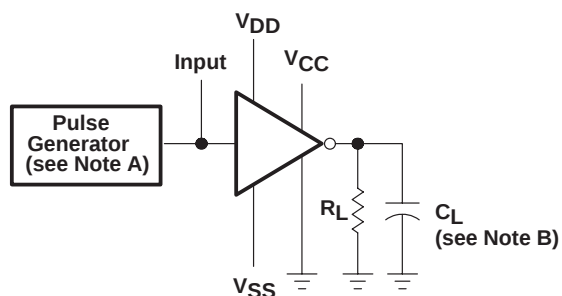
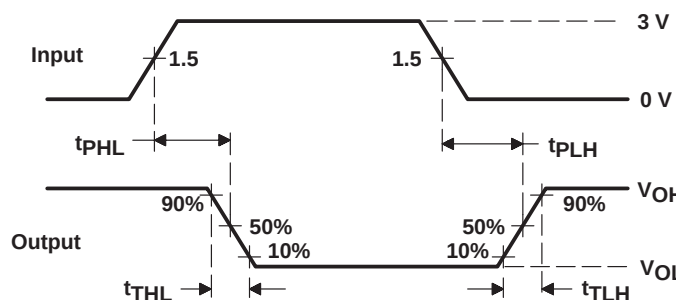


Figure 2. Driver Test Circuit, I_{IL} , I_{IH}



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES: A. The pulse generator has the following characteristics: $t_{WV} = 25 \mu s$, $PRR = 20 \text{ kHz}$, $Z_O = 50 \Omega$, $t_r = t_f < 50 \text{ ns}$.
B. C_L includes probe and jig capacitance.

Figure 3. Driver Test Circuit and Voltage Waveforms

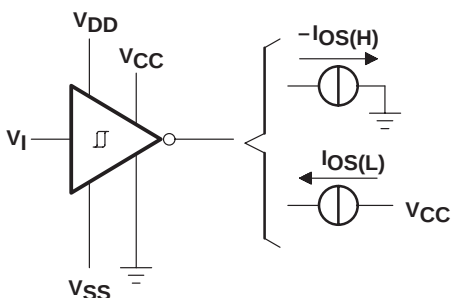


Figure 4. Receiver Test Circuit, I_{OSH} , I_{OSL}

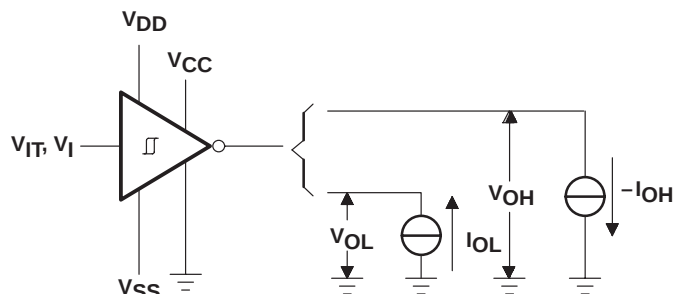
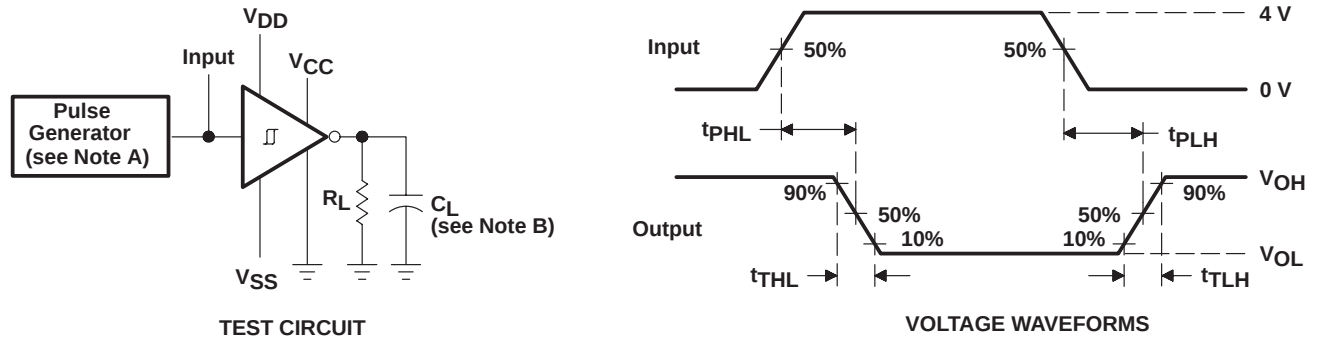


Figure 5. Receiver Test Circuit, V_{IT} , V_{OL} , V_{OH}

PARAMETER MEASUREMENT INFORMATION



- NOTES: A. The pulse generator has the following characteristics: $t_W = 25 \mu s$, $PRR = 20 \text{ kHz}$, $Z_O = 50 \Omega$, $t_r = t_f < 50 \text{ ns}$.
B. C_L includes probe and jig capacitance.

Figure 6. Receiver Test Circuit and Voltage Waveforms

IMPORTANT NOTICE

Texas Instruments and its subsidiaries (TI) reserve the right to make changes to their products or to discontinue any product or service without notice, and advise customers to obtain the latest version of relevant information to verify, before placing orders, that information being relied on is current and complete. All products are sold subject to the terms and conditions of sale supplied at the time of order acknowledgement, including those pertaining to warranty, patent infringement, and limitation of liability.

TI warrants performance of its semiconductor products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are utilized to the extent TI deems necessary to support this warranty. Specific testing of all parameters of each device is not necessarily performed, except those mandated by government requirements.

CERTAIN APPLICATIONS USING SEMICONDUCTOR PRODUCTS MAY INVOLVE POTENTIAL RISKS OF DEATH, PERSONAL INJURY, OR SEVERE PROPERTY OR ENVIRONMENTAL DAMAGE ("CRITICAL APPLICATIONS"). TI SEMICONDUCTOR PRODUCTS ARE NOT DESIGNED, AUTHORIZED, OR WARRANTED TO BE SUITABLE FOR USE IN LIFE-SUPPORT DEVICES OR SYSTEMS OR OTHER CRITICAL APPLICATIONS. INCLUSION OF TI PRODUCTS IN SUCH APPLICATIONS IS UNDERSTOOD TO BE FULLY AT THE CUSTOMER'S RISK.

In order to minimize risks associated with the customer's applications, adequate design and operating safeguards must be provided by the customer to minimize inherent or procedural hazards.

TI assumes no liability for applications assistance or customer product design. TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right of TI covering or relating to any combination, machine, or process in which such semiconductor products or services might be or are used. TI's publication of information regarding any third party's products or services does not constitute TI's approval, warranty or endorsement thereof.



[>> Semiconductor Home](#) > [Products](#) > [Analog & Mixed-Signal](#) > [Interface Products](#) > [Transmitters and Receivers](#) >

SN75C1154, QUADRUPLE LOW-POWER DRIVERS/RECEIVERS

Device Status: Active

- > [Description](#)
- > [Features](#)
- > [Datasheets](#)
- > [Pricing/Samples/Availability](#)
- > [Application Notes](#)
- > [Related Documents](#)
- > [Development Tools](#)
- > [Applications](#)

Description

The SN75C1154 is a low-power BiMOS device containing four independent drivers and receivers that are used to interface data terminal equipment (DTE) with data circuit-terminating equipment (DCE). This device has been designed to conform to ANSI EIA/TIA-232-E. The drivers and receivers of the SN75C1154 are similar to those of the SN75C188 quadruple driver and SN75C189A quadruple receiver, respectively. The drivers have a controlled output slew rate that is limited to a maximum of 30 V/us and the receivers have filters that reject input noise pulses of shorter than 1 us. Both these features eliminate the need for external components.

The SN75C1154 is designed using low-power techniques in a BiMOS technology. In most applications, the receivers contained in these devices interface to single inputs of peripheral devices such as ACEs, UARTs, or microprocessors. By using sampling, such peripheral devices are usually insensitive to the transition times of the input signals. If this is not the case or for other uses, it is recommended that the SN75C1154 receiver outputs be buffered by single Schmitt input gates or single gates of the HCMOS, ALS, or 74F logic families.

The SN75C1154 is characterized for operation from 0°C to 70°C.

Features

- Meets or Exceeds the Requirements of ANSI EIA/TIA-232-E and ITU Recommendation V.28
- Very Low Power Consumption
5 mW Typ
- Wide Driver Supply Voltage . . . ± 4.5 V to ± 15 V
- Driver Output Slew Rate Limited to 30 V/us Max
- Receiver Input Hysteresis . . . 1000 mV Typ
- Push-Pull Receiver Outputs
- On-Chip Receiver 1-us Noise Filter
- Functionally interchangeable With Motorola MC145404

To view the following documents, [Acrobat Reader 3.x](#) is required.

To download a document to your hard drive, right-click on the link and choose 'Save'.

Datasheets

Full datasheet in Acrobat PDF: [slls151c.pdf](#) (139 KB)

Full datasheet in Zipped PostScript: [slls151c.psz](#) (126 KB)

Pricing/Samples/Availability

Orderable Device	Package	Pins	Temp (°C)	Status	Price/unit USD (100-999)	Pack Qty	Availability / Samples
SN75C1154DW	DW	20	0 TO 70	ACTIVE	1.36	25	Check stock or order
SN75C1154DWR	DW	20	0 TO 70	ACTIVE	1.17	2000	Check stock or order
SN75C1154N	N	20	0 TO 70	ACTIVE	1.36	20	Check stock or order
SN75C1154NS	NS	20	0 TO 70	ACTIVE			Check stock or order

Application Reports

- [422 AND 485 OVERVIEW AND SYSTEM CONFIGURATIONS](#) (SLLA070 - Updated: 02/15/2000)
- [ANALOG APPLICATIONS JOURNAL, FEBRUARY 2000](#) (SLYT012A - Updated: 03/23/2000)
- [ANALOG APPLICATIONS JOURNAL, NOVEMBER 1999](#) (SLYT010A - Updated: 03/23/2000)
- [COMPARING BUS SOLUTIONS](#) (SLLA067 - Updated: 03/06/2000)
- [ELECTROSTATIC DISCHARGE APPLICATION NOTE](#) (SSYA008 - Updated: 05/05/1999)
- [JITTER ANALYSIS](#) (SLLA075 - Updated: 03/31/2000)
- [SKEW DEFINITIONS](#) (SLLA060 - Updated: 08/13/1999)
- [THERMAL CHARACTERISTICS OF LINEAR AND LOGIC PACKAGES USING JEDEC PCB DESIGNS](#) (SZZA017A - Updated: 09/15/1999)

Related Documents

- [A STATISTICAL SURVEY OF COMMON-MODE NOISE](#) (SLLA057, 131 KB - Updated: 12/23/1999)

Table Data Updated on: 6/2/2000

• [Search](#) • [Tech Support](#) • [Comments](#) • [Site Map](#) • [TI&ME](#) • [Home](#)

[\(c\) Copyright](#) 2000 Texas Instruments Incorporated. All rights reserved.
[Trademarks](#), [Important Notice!](#), [Privacy Policy](#)