NOTICE OF REVISION (NOR) THIS REVISION DESCRIBED BELOW HAS BEEN AUTHORIZED FOR THE DOCUMENT LISTED.	1. DATE *(YYMMDD)* 96-06-14	*Form Approved* *OMB No. 0704-0188*

2. PROCURING ACTIVITY NO.

3. DODAAC

4. ORIGINATOR a. TYPED NAME *(First, Middle Initial, Last)*	b. ADDRESS *(Street, City, State, Zip Code)* Defense Electronics Supply Center 1507 Wilmington Pike Dayton, OH 45444-5765	5. CAGE CODE 67268 7. CAGE CODE 67268	6. NOR NO. 5962-R149-96 8. DOCUMENT NO. **5962-94601**

9. TITLE OF DOCUMENT	10. REVISION LETTER		11. ECP NO.
MICROCIRCUIT, DIGITAL, ADVANCED BIPOLAR CMOS, SCAN TEST DEVICE WITH 18-BIT BUS TRANSCEIVER, THREE-STATE OUTPUTS, TTL COMPATIBLE INPUTS, MONOLITHIC SILICON	a. CURRENT A	b. NEW B	N/A

12. CONFIGURATION ITEM (OR SYSTEM) TO WHICH ECP APPLIES
All

13. DESCRIPTION OF REVISION

Sheet 1: Revisions ltr column; add "B".
Revisions description column; add "Changes in accordance with NOR 5962-R149-96".
Revisions date column; add "96-06-14".
Revision level block; change from "A" to "B".
Rev status of sheets; for sheets 1 and 6, change from "A" to "B".

Sheet 6: Table I, off-state leakage current, I_{OFF}; delete and replace as follows:

"

Off-state leakage current	I_{OFF}	For inputs or outputs under test V_{IN} or V_{OUT} ≤ 4.5 V All other pins at 0.0 V	device type 01	0.0 V	1		±100	µA
			device type 02				±450	

"

Revision level block; change from "A" to "B".

14. THIS SECTION FOR GOVERNMENT USE ONLY

a. *(X one)*		
	X	(1) Existing document supplemented by the NOR may be used in manufacture.
		(2) Revised document must be received before manufacturer may incorporate this change.
		(3) Custodian of master document shall make above revision and furnish revised document.

b. ACTIVITY AUTHORIZED TO APPROVE CHANGE FOR GOVERNMENT	c. TYPED NAME *(First, Middle Initial, Last)*	
DESC-ELDC	Monica L. Poelking	
d. TITLE	e. SIGNATURE	f. DATE SIGNED *(YYMMDD)*
Chief, Custom Microelectronics	Monica L. Poelking	96-06-14
15a. ACTIVITY ACCOMPLISHING REVISION	b. REVISION COMPLETED *(Signature)*	c. DATE SIGNED *(YYMMDD)*
DESC-ELDC	Joseph A. Kerby	96-06-14

REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Add device 02. Editorial changes throughout.	95-11-20	Monica Poelking

REV																				
SHEET																				
REV	A	A	A	A	A	A	A	A	A											
SHEET	15	16	17	18	19	20	21	22	23											
REV STATUS OF SHEETS			REV		A	A	A	A	A	A	A	A	A	A	A	A	A	A		
			SHEET		1	2	3	4	5	6	7	8	9	10	11	12	13	14		

PMIC N/A

STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

PREPARED BY
Thanh V. Nguyen

CHECKED BY
Thanh V. Nguyen

APPROVED BY
Monica L. Poelking

DRAWING APPROVAL DATE

REVISION LEVEL
A

DEFENSE ELECTRONICS SUPPLY CENTER
DAYTON, OHIO 45444

MICROCIRCUIT, DIGITAL, ADVANCED BIPOLAR CMOS, SCAN TEST DEVICE WITH 18-BIT BUS TRANSCEIVER, THREE-STATE OUTPUTS, TTL COMPATIBLE INPUTS, MONOLITHIC SILICON

SIZE	CAGE CODE	
A	**67268**	5962-94601

SHEET 1 OF 24

1. SCOPE

1.1 Scope. This drawing forms a part of a one part - one part number documentation system (see 6.6 herein). Two product assurance classes consisting of military high reliability (device classes Q and M) and space application (device class V, and a choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). Device class M microcircuits represent non-JAN class B microcircuits in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices". When available, a choice of Radiation Hardness Assurance (RHA) levels are reflected in the PIN.

1.2 PIN. The PIN shall be as shown in the following example:

```
 5962          -          94601    01        Q        X        X
   |           |                   |         |        |        |
 Federal      RHA               Device    Device     Case     Lead
 stock class  designator         type     class      outline  finish
 designator   (see 1.2.1)     (see 1.2.2) designator (see 1.2.4) (see 1.2.5)
                                          (see 1.2.3)
\_____________    ______________/
              \/
        Drawing number
```

1.2.1 RHA designator. Device class M RHA marked devices shall meet the MIL-I-38535 appendix A specified RHA levels and shall be marked with the appropriate RHA designator. Device classes Q and V RHA marked devices shall meet the MIL-I-38535 specified RHA levels and shall be marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) shall identify the circuit function as follows:

Device type	Generic number	Circuit function
01	54ABT18245	Scan test device with 18-bit bus transceiver, three-state outputs, TTL compatible inputs
02	54ABT18245A	Scan test device with 18-bit bus transceiver, three-state outputs, TTL compatible inputs

1.2.3 Device class designator. The device class designator shall be a single letter identifying the product assurance level as follows:

Device class	Device requirements documentation
M	Vendor self-certification to the requirements for non-JAN class B microcircuits in accordance with 1.2.1 of MIL-STD-883
Q or V	Certification and qualification to MIL-I-38535

1.2.4 Case outline(s). The case outline(s) shall be as designated in MIL-STD-1835, and as follows:

Outline letter	Descriptive designator	Terminals	Package style
X	GDFP1-F56	56	Flat pack

1.2.5 Lead finish. The lead finish shall be as specified in MIL-STD-883 (see 3.1 herein) for class M or MIL-I-38535 for classes Q and V. Finish letter "X" shall not be marked on the microcircuit or its packaging. The "X" designation is for use in specifications when lead finishes A, B, and C are considered acceptable and interchangeable without preference.

1.3 Absolute maximum ratings. 1/ 2/ 3/

Supply voltage range (V_{CC})	-0.5 V dc to +7.0 V dc
DC input voltage range (I/O ports) (V_{IN})	-0.5 V dc to +5.5 V dc 4/
DC input voltage range (except I/O ports) (V_{IN})	-0.5 V dc to +7.0 V dc 4/
DC output voltage range (V_{OUT})	-0.5 V dc to +5.5 V dc 4/
DC output current (I_{OL}) (per output)	+96 mA
DC input clamp current (I_{IK}) (V_{IN} < 0.0 V)	-18 mA
DC output clamp current (I_{OK}) (V_{OUT} < 0.0 V)	-50 mA
V_{CC} current (I_{VCC})	
Device 01	+581 mA
Device 02	+576 mA
Ground current (I_{GND})	
Device 01	+1190 mA
Device 02	+1152 mA
Storage temperature range (T_{STG})	-65°C to +150°C
Lead temperature (soldering, 10 seconds)	+300°C
Thermal resistance, junction-to-case (Θ_{JC})	See MIL-STD-1835
Junction temperature (T_J)	+175°C
Maximum power dissipation T_A = +55°C(P_D)	950 mW 5/

1.4 Recommended operating conditions. 2/ 3/

Supply voltage range (V_{CC})	+4.5 V dc to +5.5 V dc
Input voltage range (V_{IN})	+0.0 V dc to V_{CC}
Output voltage range (V_{OUT})	+0.0 V dc to V_{CC}
Maximum low level input voltage (V_{IL})	0.8 V
Minimum high level input voltage (V_{IH})	2.0 V
Maximum high level output current (I_{OH})	-24 mA
Maximum low level output current (I_{OL})	+48 mA
Maximum input rise or fall rate ($\Delta t/\Delta V$)	10 ns/V
Minimum setup time (t_s):	
mAn, mBn, mDIR, or mOE before TCK↑	9.5 ns
TDI before TCK↑	4.5 ns
TMS before TCK↑	3.6 ns
Minimum hold time (t_h):	
mAn, mBn, mDIR, or mOE after TCK↑	0.7 ns
TDI after TCK↑	0.0 ns
TMS after TCK↑	0.5 ns
Minimum pulse width, TCK high or low (t_w)	8.1 ns
Minimum delay time, power-up to TCK↑ (t_d)	50.0 ns 6/
Minimum rise time, V_{CC} power-up (t_r)	1.0 µs 6/
Maximum TCK frequency (f_{CLK})	50 MHz
Case operating temperature range (T_C)	-55°C to +125°C

1.5 Digital logic testing for device classes Q and V.

Fault coverage measurement of manufacturing logic tests (MIL-STD-883, test method 5012)	XX percent 7/

1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.
2/ Unless otherwise noted, all voltages are referenced to GND.
3/ The limits for the parameters specified herein shall apply over the full specified V_{CC} range and case temperature range of -55°C to +125°C.
4/ The input negative voltage rating may be exceeded provided that the input clamp current rating is observed.
5/ The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 75 mils.
6/ These parameters are not production tested.
7/ Values will be added when they become available.

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, bulletin, and handbook. Unless otherwise specified, the following specification, standards, bulletin, and handbook of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this drawing to the extent specified herein.

SPECIFICATION

MILITARY

MIL-I-38535 - Integrated Circuits, Manufacturing, General Specification for.

STANDARDS

MILITARY

MIL-STD-883 - Test Methods and Procedures for Microelectronics.
MIL-STD-973 - Configuration Management.
MIL-STD-1835 - Microcircuit Case Outlines

BULLETIN

MILITARY

MIL-BUL-103 - List of Standardized Military Drawings (SMD's).

HANDBOOK

MILITARY

MIL-HDBK-780 - Standardized Military Drawings.

(Copies of the specification, standards, bulletin, and handbook required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity.)

2.2 Non-Government publications. The following document(s) form a part of this document to the extent specified herein. Unless otherwise specified, the issues of the documents which are DOD adopted are those listed in the issue of the DODISS cited in the solicitation. Unless otherwise specified, the issues of documents not listed in the DODISS are the issues of the documents cited in the solicitation.

INSTITUTE OF ELECTRICAL AND ELECTRONICS ENGINEERS (IEEE)

IEEE Standard 1149.1 - IEEE Standard Test Access Port and Boundary Scan Architecture.

(Applications for copies should be addressed to the Institute of Electrical and Electronics Engineers, 445 Hoes Lane, Piscataway, NJ 08854-4150.)

(Non-Government standards and other publications are normally available from the organizations that prepare or distribute the documents. These documents may also be available in or through libraries or other informational services.)

2.3 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device class M shall be in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices" and as specified herein. The individual item requirements for device classes Q and V shall be in accordance with MIL-I-38535, the device manufacturer's Quality Management (QM) plan, and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-STD-883 (see 3.1 herein) for device class M and MIL-I-38535 for device classes Q and V and herein.

3.2.1 Case outline. The case outline shall be in accordance with 1.2.4 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Truth table. The truth table shall be as specified on figure 2.

3.2.4 Block diagram. The block diagram shall be as specified on figure 3.

3.2.5 Test access port controller and scan test registers. The test access port (TAP) controller and scan test registers shall be as specified on figure 4.

3.2.6 Ground bounce load circuit and waveforms. The ground bounce load circuit and waveforms shall be as specified on figure 5.

3.2.7 Switching waveforms and test circuit. The switching waveforms and test circuit shall be as specified on figure 6.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table I and shall apply over the full case operating temperature range. Test conditions for these specified characteristics and limits are as specified in table I.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are defined in table I.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. Marking for device class M shall be in accordance with MIL-STD-883 (see 3.1 herein). In addition, the manufacturer's PIN may also be marked as listed in MIL-BUL-103. Marking for device classes Q and V shall be in accordance with MIL-I-38535.

3.5.1 Certification/compliance mark. The compliance mark for device class M shall be a "C" as required in MIL-STD-883 (see 3.1 herein). The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-I-38535.

3.6 Certificate of compliance. For device class M, a certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-BUL-103 (see 6.7.2 herein). For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.7.1 herein). The certificate of compliance submitted to DESC-EC prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device class M the requirements of MIL-STD-883 (see 3.1 herein), or for device classes Q and V, the requirements of MIL-I-38535 and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required for device class M in MIL-STD-883 (see 3.1 herein) or for device classes Q and V in MIL-I-38535 shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change for device class M. For device class M, notification to DESC-EC of change of product (see 6.2 herein) involving devices acquired to this drawing is required for any change as defined in MIL-STD-973.

3.9 Verification and review for device class M. For device class M, DESC, DESC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

3.10 Microcircuit group assignment for device class M. Device class M devices covered by this drawing shall be in microcircuit group number 126 (see MIL-I-38535, appendix A).

3.11 IEEE 1149.1 compliance. This device shall be compliant with IEEE 1149.1.

TABLE I. Electrical performance characteristics.

Test and MIL-STD-883 test method 1/	Symbol	Test conditions 2/ $-55°C \le T_C \le +125°C$ $+4.5\ V \le V_{CC} \le +5.5\ V$ unless otherwise specified		V_{CC}	Group A subgroups	Limits 3/ Min	Limits 3/ Max	Unit
High level output voltage 3006	V_{OH}	For all inputs affecting output under test V_{IN} = 2.0 V or 0.8 V	I_{OH} = -3.0 mA	4.5 V	1, 2, 3	2.5		V
				5.0 V	1, 2, 3	3.0		
			I_{OH} = -24.0 mA	4.5 V	1, 2, 3	2.0		
Low level output voltage 3007	V_{OL}	For all inputs affecting output under test, V_{IN} = 2.0 V or 0.8 V I_{OL} = 48 mA		4.5 V	1, 2, 3		0.55	V
Negative input clamp voltage 3022	V_{IC-}	For input under test I_{IN} = -18 mA		4.5 V	1, 2, 3		-1.2	V
Input current high 3010	I_{IH} 4/	For input under test $V_{IN} = V_{CC}$	mDIR, mOE, TCK	5.5 V	1, 2, 3		1.0	µA
			A or B ports		1, 2, 3		100	
			TDI, TMS		1, 2, 3		10.0	
Input current low 3009	I_{IL} 4/	For input under test V_{IN} = GND	mDIR, mOE, TCK	5.5 V	1, 2, 3		-1.0	µA
			A or B ports		1, 2, 3		-100	
			TDI, TMS		1, 2, 3		-150	
Three-state output leakage current high 3021	I_{OZH} 5/	V_{OUT} = 2.7 V		5.5 V	1, 2, 3		50	µA
Three-state output leakage current low 3020	I_{OZL} 5/	V_{OUT} = 0.5 V		5.5 V	1, 2, 3		-50	µA
Off-state leakage current	I_{OFF}	For input or output under test V_{IN} or $V_{OUT} \le 4.5$ V All other pins at 0.0 V		0.0 V	1		±100	µA
High-state leakage current	I_{CEX}	For output under test, V_{OUT} = 5.5 V Outputs at high logic state		5.5 V	1, 2, 3		50	µA
Output current 3011	I_O 6/	V_{OUT} = 2.5 V		5.5 V	1, 2, 3	-50	-200	mA
Quiescent supply current delta, TTL input level 3005	ΔI_{CC} 7/	For input under test, V_{IN} = 3.4 V For all other inputs $V_{IN} = V_{CC}$ or GND		5.5 V	1, 2, 3		50	µA

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test and MIL-STD-883 test method 1/	Symbol	Test conditions 2/ $-55°C \le T_C \le +125°C$ $+4.5\ V \le V_{CC} \le +5.5\ V$ unless otherwise specified		V_{CC}	Device type	Group A subgroups	Limits 3/		Unit
							Min	Max	
Quiescent supply current, outputs high 3005	I_{CCH}	For all inputs, $V_{IN} = V_{CC}$ or GND $I_{OUT} = 0$ A A or B ports		5.5 V	All	1, 2, 3		5.0	mA
Quiescent supply current, outputs low 3005	I_{CCL}			5.5 V	All	1, 2, 3		38	mA
Quiescent supply current, outputs disabled 3005	I_{CCZ}			5.5 V	All	1, 2 ,3		4.5	mA
Input capacitance 3012	C_{IN}	$T_C = +25°C$ See 4.4.1b	Control inputs	5.0 V	All	4		9.8	pF
I/O capacitance 3012	$C_{I/O}$		A or B ports	5.0 V	All	4		12.6	pF
Output capacitance 3012	C_{OUT}		TDO	5.0 V	All	4		11.4	pF
Low level ground bounce noise	V_{OLP} 8/	$V_{IH} = 3.0$ V, $V_{IL} = 0.0$ V $T_A = +25°C$ See figure 5 See 4.4.1d		5.0 V	All	4		770	mV
	V_{OLV} 8/			5.0 V	All	4		-870	
High level V_{CC} bounce noise	V_{OHP} 8/			5.0 V	All	4		1500	mV
	V_{OHV} 8/			5.0 V	All	4		-480	
Functional test 3014	9/	$V_{IH} = 2.0$ V, $V_{IL} = 0.8$ V Verify output V_O See 4.4.1c		4.5 V	All	7, 8	L	H	
				5.5 V	All	7, 8	L	H	
NORMAL MODE									
Propagation delay time, mAn to mBn or mBn to mAn 3003	t_{PLH1}	$C_L = 50$ pF minimum $R_L = 500\Omega$ See figure 6		5.0 V	All	9	1.5	4.1	ns
				4.5 V and 5.5 V	All	10, 11	1.5	5.1	
	t_{PHL1}			5.0 V	All	9	1.5	4.6	ns
				4.5 V and 5.5 V	All	10, 11	1.5	5.8	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test and MIL-STD-883 test method 1/	Symbol	Test conditions 2/ $-55°C \le T_C \le +125°C$ $+4.5\ V \le V_{CC} \le +5.5\ V$ unless otherwise specified	V_{CC}	Device type	Group A subgroups	Limits 3/		Unit
						Min	Max	
Propagation delay time, output enable, mOE to mAn or mBn 3003	t_{PZH1}	C_L = 50 pF minimum R_L = 500Ω See figure 6	5.0 V	01 02	9	3.0 2.0	7.5 5.8	ns
			4.5 V and 5.5 V	01 02	10, 11	3.0 2.0	9.9 8.1	
	t_{PZL1}		5.0 V	01 02	9	3.0 2.0	8.0 6.2	
			4.5 V and 5.5 V	01 02	10, 11	3.0 2.0	10.1 8.5	
Propagation delay time, output disable, mOE to mAn or mBn 3003	t_{PHZ1}		5.0 V	01 02	9	3.0 2.5	9.6 6.8	ns
			4.5 V and 5.5 V	01 02	10, 11	3.0 2.9	12.2 9.5	
	t_{PLZ1}		5.0 V	01 02	9	3.0 2.5	9.6 6.0	
			4.5 V and 5.5 V	01 02	10, 11	3.0 2.5	10.9 8.5	
TEST MODE								
Propagation delay time, TCK↓ to mAn or mBn 3003	t_{PLH2}	C_L = 50 pF minimum R_L = 500Ω See figure 6	5.0 V	All	9	3.0	10.1	ns
			4.5 V and 5.5 V	All	10, 11	2.8	14.0	
	t_{PHL2}		5.0 V	All	9	3.0	10.1	
			4.5 V and 5.5 V	All	10, 11	3.0	13.8	
Propagation delay time, TCK↓ to TDO 3003	t_{PLH3}		5.0 V	All	9	2.0	5.0	ns
			4.5 V and 5.5 V	All	10, 11	2.0	6.4	
	t_{PHL3}		5.0 V	All	9	2.0	5.6	
			4.5 V and 5.5 V	All	10, 11	2.0	7.0	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test and MIL-STD-883 test method 1/	Symbol	Test conditions 2/ $-55°C \le T_C \le +125°C$ $+4.5\ V \le V_{CC} \le +5.5\ V$ unless otherwise specified	V_{CC}	Device type	Group A subgroups	Limits 3/		Unit
						Min	Max	
Propagation delay time, output enable, TCK↓ to mAn or mBn 3003	t_{PZH2}	C_L = 50 pF minimum R_L = 500Ω See figure 6	5.0 V	01 02	9	4.0 4.0	10.8 10.6	ns
			4.5 V and 5.5 V	All	10, 11	4.0	14.1	
	t_{PZL2}		5.0 V	All	9	4.0	10.5	
			4.5 V and 5.5 V	All	10, 11	4.0	14.3	
Propagation delay time, output enable, TCK↓ to TDO 3003	t_{PZH3}		5.0 V	All	9	2.0	5.5	ns
			4.5 V and 5.5 V	All	10, 11	2.0	7.0	
	t_{PZL3}		5.0 V	All	9	2.5	5.7	
			4.5 V and 5.5 V	01 02	10, 11	2.5 2.3	7.3 7.3	
Propagation delay time, output disable, TCK↓ to mAn or mBn 3003	t_{PHZ2}		5.0 V	01 02	9	3.3 3.5	10.8 10.8	ns
			4.5 V and 5.5 V	All	10, 11	2.9	14.4	
	t_{PLZ2}		5.0 V	All	9	2.5	10.1	
			4.5 V and 5.5 V	All	10, 11	2.5	13.8	
Propagation delay time, output disable, TCK↓ to TDO 3003	t_{PHZ3}		5.0 V	01 02	9	2.0 2.0	5.8 5.7	ns
			4.5 V and 5.5 V	All	10, 11	2.0	7.5	
	t_{PLZ3}		5.0 V	All	9	1.5	5.4	
			4.5 V and 5.5 V	All	10, 11	1.5	6.7	
Maximum TCK frequency	f_{MAX}		5.0 V	All	9	50		MHz
			4.5 V and 5.5 V	All	10, 11	50		

See footnotes on the next sheet.

TABLE I. Electrical performance characteristics - Continued.

1/ For tests not listed in the referenced MIL-STD-883 (e.g. ΔI_{CC}), utilize the general test procedure of 883 under the conditions listed herein.

2/ Each input/output, as applicable, shall be tested at the specified temperature, for the specified limits, to the tests in table I herein. Output terminals not designated shall be high level logic, low level logic, or open, except for all I_{CC} and ΔI_{CC} tests, where the output terminals shall be open. When performing these tests, the current meter shall be placed in the circuit such that all current flows through the meter. For input terminals not designated, V_{IN} = GND or $V_{IN} \geq 3.0$ V.

3/ For negative and positive voltage and current values, the sign designates the potential difference in reference to GND and the direction of current flow, respectively, and the absolute value of the magnitude, not the sign, is relative to the minimum and maximum limits, as applicable, listed herein. All devices shall meet or exceed the limits specified in table I at $4.5 \text{ V} \leq V_{CC} \leq 5.5$ V.

4/ For I/O ports, the limit includes I_{OZH} or I_{OZL} leakage current from the output circuitry.

5/ For I/O ports, the limit includes I_{IH} or I_{IL} leakage current from the input circuitry. Limit will be guaranteed when the control input affecting the output under test is at 2.0 V or 0.8 V.

6/ Not more than one output should be tested at one time, and the duration of the test condition should not exceed one second.

7/ This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or V_{CC}. This test may be performed either one input at a time (preferred method) or with all input pins simultaneously at $V_{IN} = V_{CC} - 2.1$ V (alternate method). When the test is performed using the alternate test method, the maximum limit is equal to the number of inputs at a high TTL input level times 50 µA, and the preferred method and limits are guaranteed.

8/ This test is for qualification only. Ground and V_{CC} bounce tests are performed on a non-switching (quiescent) output and are used to measure the magnitude of induced noise caused by other simultaneously switching outputs. The test is performed on a low noise bench test fixture. For the device under test, all outputs shall be loaded with 500Ω of load resistance and a minimum of 50 pF of load capacitance (see figure 5). Only chip capacitors and resistors shall be used. The output load components shall be located as close as possible to the device outputs. It is suggested, that whenever possible, this distance be kept to less than 0.25 inches. Decoupling capacitors shall be placed in parallel from V_{CC} to ground. The values of these decoupling capacitors shall be determined by the device manufacturer. The low and high level ground and V_{CC} bounce noise is measured at the quiet output using a 1 GHz minimum bandwidth oscilloscope with a 50Ω input impedance.

The device inputs shall be conditioned such that all outputs are at a high nominal V_{OH} level. The device inputs shall then be conditioned such that they switch simultaneously and the output under test remains at V_{OH} as all other outputs possible are switched from V_{OH} to V_{OL}. V_{OHV} and V_{OHP} are then measured from the nominal V_{OH} level to the largest negative and positive peaks, respectively (see figure 5). This is then repeated with the same outputs not under test switching from V_{OL} to V_{OH}.

The device inputs shall be conditioned such that all outputs are at a low nominal V_{OL} level. The device inputs shall then be conditioned such that they switch simultaneously and the output under test remains at V_{OL} as all other outputs possible are switched from V_{OL} to V_{OH}. V_{OLP} and V_{OLV} are then measured from the nominal V_{OL} level to the largest positive and negative peaks, respectively (see figure 5). This is then repeated with the same outputs not under test switching from V_{OH} to V_{OL}.

9/ Tests shall be performed in sequence, attributes data only. Functional tests shall include the truth table and other logic patterns used for fault detection. The test vectors used to verify the truth table shall, at a minimum, test all functions of each input and output. All possible input to output logic patterns per function shall be guaranteed, if not tested, to the truth table in figure 2 herein. Functional tests shall be performed in sequence as approved by the qualifying activity on qualified devices. After incorporating allowable tolerances per MIL-STD-883, V_{IL} = 0.4 V and V_{IH} = 2.4 V. For outputs, L ≤ 0.8 V, H ≥ 2.0 V.

Device type	01 and 02						
Case outline	X						
Terminal number	Terminal symbol	Terminal number	Terminal symbol	Terminal number	Terminal symbol	Terminal number	Terminal symbol
1	1DIR	15	2B2	29	TCK	43	2A1
2	1B1	16	2B3	30	TDI	44	1A9
3	1B2	17	2B4	31	2OE	45	1A8
4	GND	18	GND	32	GND	46	GND
5	1B3	19	2B5	33	2A9	47	1A7
6	1B4	20	2B6	34	2A8	48	1A6
7	V_{CC}	21	2B7	35	V_{CC}	49	1A5
8	1B5	22	V_{CC}	36	2A7	50	V_{CC}
9	1B6	23	2B8	37	2A6	51	1A4
10	1B7	24	2B9	38	2A5	52	1A3
11	GND	25	GND	39	GND	53	GND
12	1B8	26	2DIR	40	2A4	54	1A2
13	1B9	27	TDO	41	2A3	55	1A1
14	2B1	28	TMS	42	2A2	56	1OE

Terminal descriptions	
Terminal symbol	Description
mAn (m = 1 to 2, n = 1 to 8)	Data inputs/outputs, A ports
mBn (m = 1 to 2, n = 1 to 8)	Data inputs/outputs, B ports
mOE (m = 1 to 2)	Output enable control inputs
mDIR (m = 1 to 2)	Direction control inputs
TDI	Test data input
TDO	Test data output
TMS	Test mode select input
TCK	Test clock input

FIGURE 1. Terminal connections.

Device type 01 and 02		
Inputs		Operation
OE	DIR	
L	L	B data to A bus
L	H	A data to B bus
H	X	Isolation

H = High voltage level
L = Low voltage level
X = Irrelevant

FIGURE 2. Truth table.

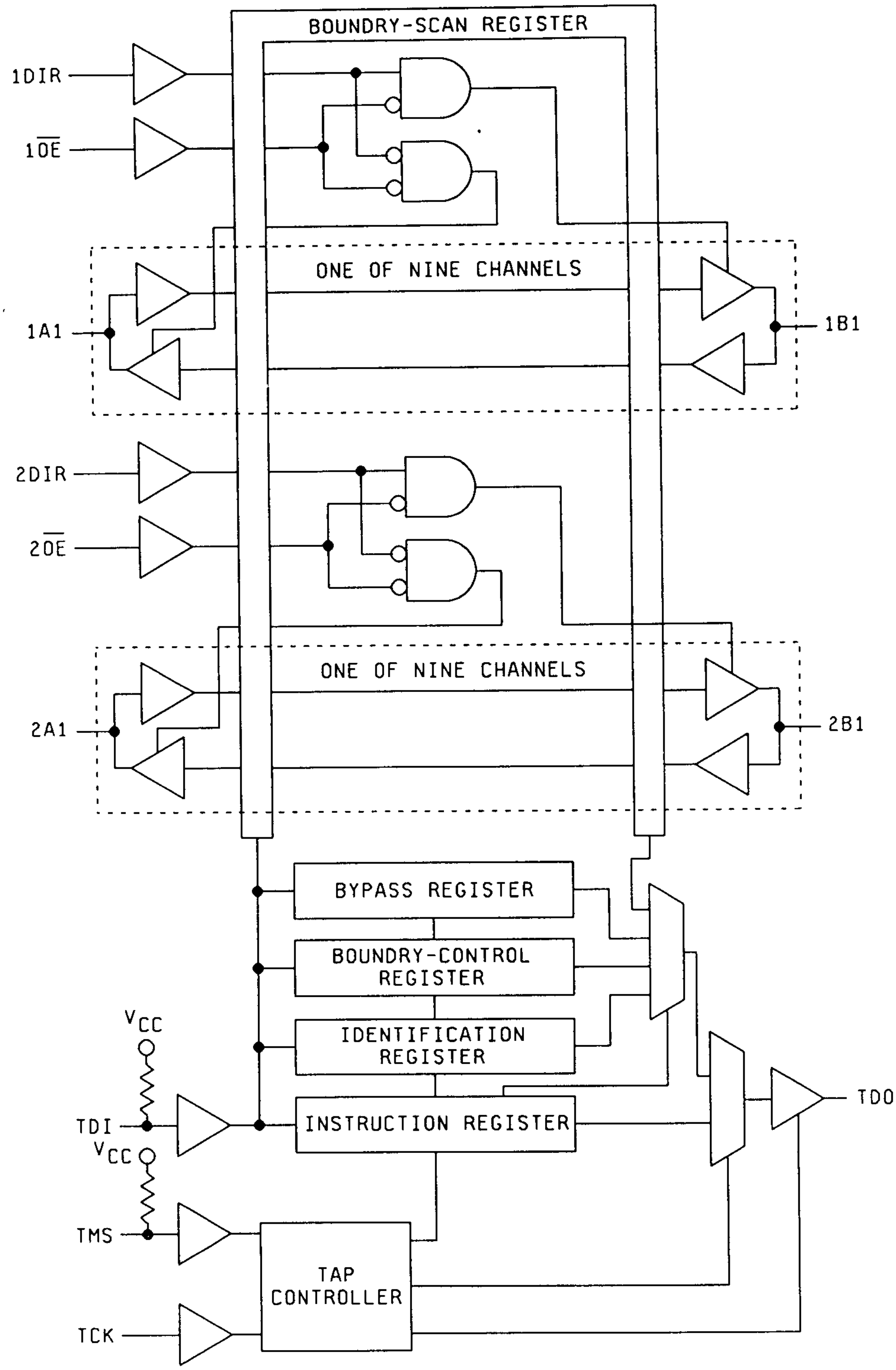


FIGURE 3. Block diagram.

Test access port (TAP) controller state diagram

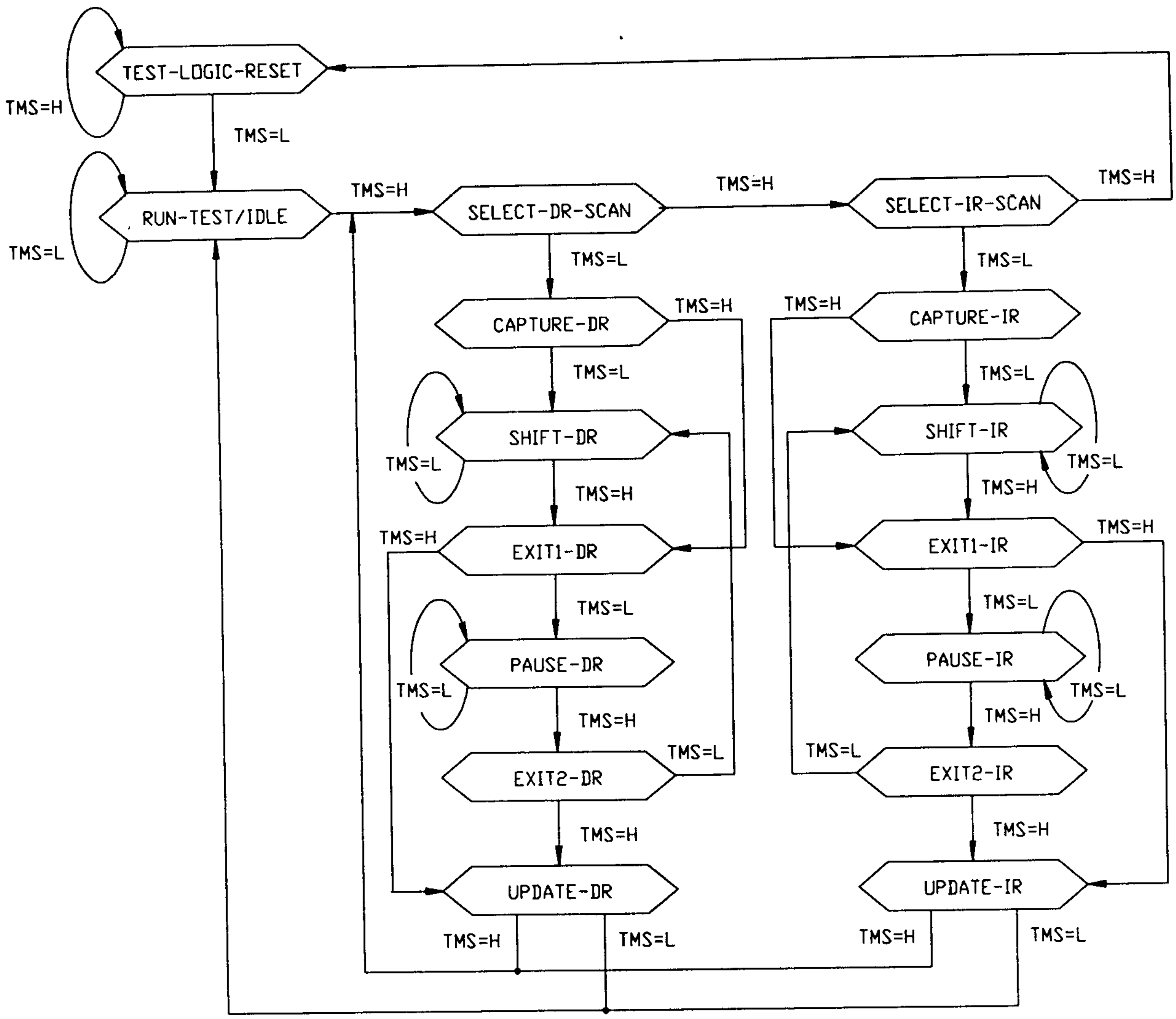


FIGURE 4. Test access port controller and scan test registers.

Instruction register (IR) order of scan

TDI → BIT 7 PARITY (MSB) → BIT 6 → BIT 5 → BIT 4 → BIT 3 → BIT 2 → BIT 1 → BIT 0 (LSB) → TDO

NOTE: During capture-IR, the IR captures the binary value 10000001. At power up or in the test-logic-reset state, the IR is reset to the binary value 10000001, which selects the IDCODE instruction.

Instruction register opcodes

Binary code 1/ Bit 7 - Bit 0 MSB - LSB	opcode	Description	Selected data register	Mode
00000000	EXTEST	Boundary scan	Boundary scan	Test
10000001	CCODE	Certification read	Device identification	Normal
10000010	SAMPLE/PRELOAD	Sample boundary	Boundary scan	Normal
00000011	BYPASS 2/	Bypass scan	Bypass	Normal
10000100	BYPASS 2/	Bypass scan	Bypass	Normal
00000101	BYPASS 2/	Bypass scan	Bypass	Normal
00000110	HIGHZ	Control boundary to high impedance	Bypass	Modified test
10000111	CLAMP	Control boundary to 1/0	Bypass	Test
10001000	BYPASS 2/	Bypass scan	Bypass	Normal
00001001	RUNT	Boundary run test	Bypass	Test
00001010	READBN	Boundary read	Boundary scan	Normal
10001011	READBT	Boundary read	Boundary scan	Test
00001100	CELLTST	Boundary self test	Boundary scan	Normal
10001101	TOPHIP	Boundary toggle outputs	Bypass	Test
10001110	SCANCN	Boundary-control register scan	Boundary control	Normal
00001111	SCANCT	Boundary-control register scan	Boundary control	Test
All others	BYPASS	Bypass scan	Bypass	Normal

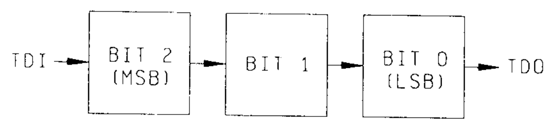
1/ Bit 7 is used to maintain even parity in the 8-bit instruction.
2/ The BYPASS instruction is executed in lieu of a SCOPE™ instruction that is not supported in this device.

FIGURE 4. Test access port controller and scan test registers - Continued.

Boundary-scan register (BSR) configuration

BSR bit number	Device signal	BSR bit number	Device signal	BSR bit number	Device signal	BSR bit number	Device signal	BSR bit number	Device signal
43	2OEB	35	2A9-I/O	26	1A9-I/O	17	2B9-I/O	8	1B9-I/O
42	1OEB	34	2A8-I/O	25	1A8-I/O	16	2B8-I/O	7	1B8-I/O
41	2OEA	33	2A7-I/O	24	1A7-I/O	15	2B7-I/O	6	1B7-I/O
40	1OEA	32	2A6-I/O	23	1A6-I/O	14	2B6-I/O	5	1B6-I/O
39	2DIR	31	2A5-I/O	22	1A5-I/O	13	2B5-I/O	4	1B5-I/O
38	1DIR	30	2A4-I/O	21	1A4-I/O	12	2B4-I/O	3	1B4-I/O
37	2OE	29	2A3-I/O	20	1A3-I/O	11	2B3-I/O	2	1B3-I/O
36	1OE	28	2A2-I/O	19	1A2-I/O	10	2B2-I/O	1	1B2-I/O
---	---	27	2A1-I/O	18	1A1-I/O	9	2B1-I/O	0	1B1-I/O

Boundary-control register (BCR) order of scan



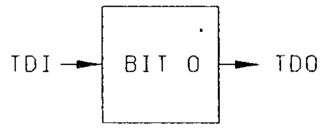
NOTE: During capture-DR (DR stands for data register), the contents of BCR are not changed. At power up or in the test-logic-reset state, the BCR is reset to the binary value 010, which selects the PSA test operation.

Boundary-control register opcodes

Binary code Bit 1 - Bit 0 MSB - LSB	Description
X00	Sample inputs/toggle outputs (TOPSIP)
X01	Pseudo-random pattern generation/36-bit mode (PRPG)
X10	Parallel signature analysis/36-bit mode (PSA)
011	Simultaneous PSA and PRPG/18-bit mode (PSA/PRPG)
111	Simultaneous PSA and binary count up/18-bit mode (PSA/COUNT)

FIGURE 4. Test access port controller and scan test registers - Continued.

Bypass register order of scan



NOTE: During capture-DR, the bypass register captures a logic 0.

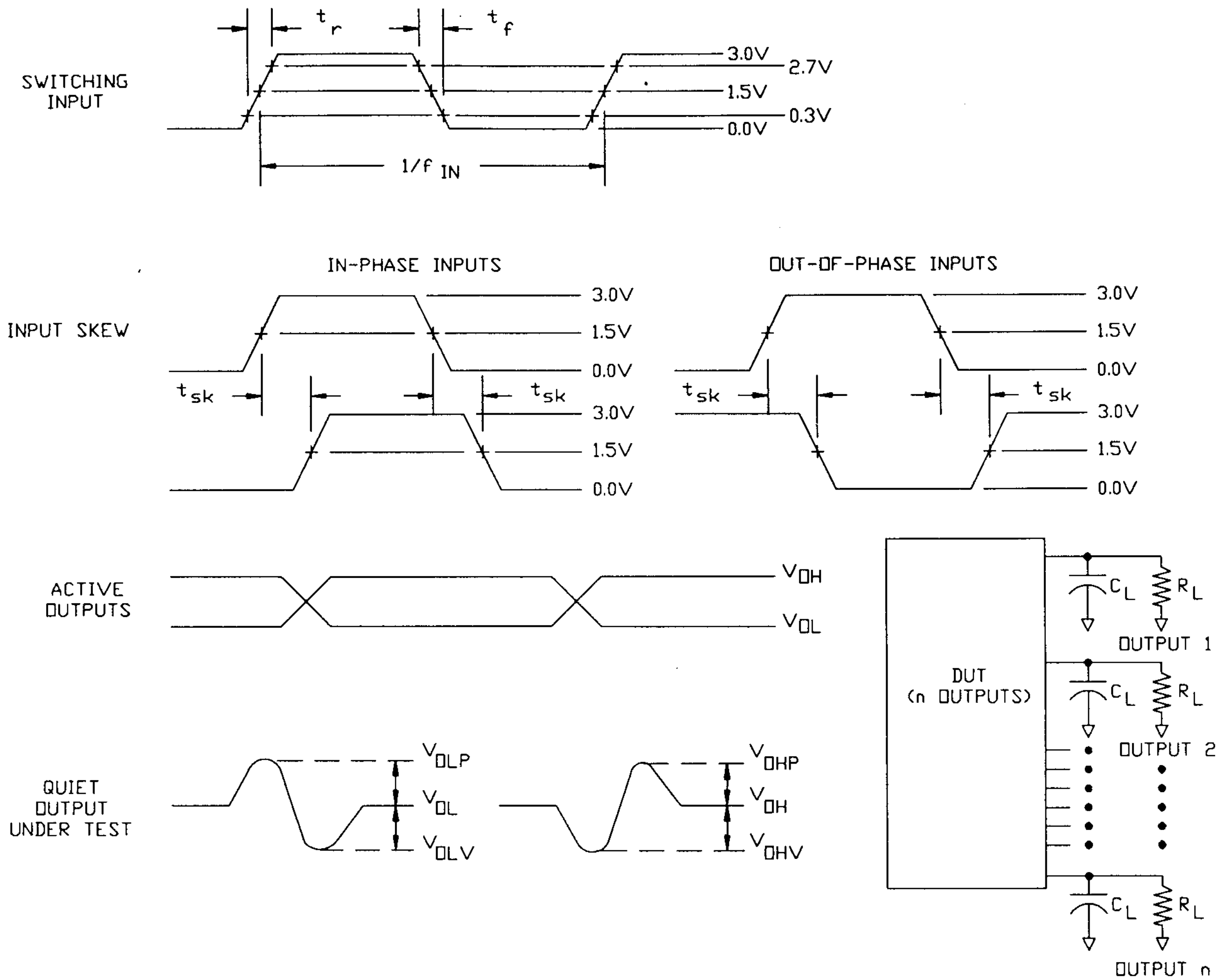
Device identification register (IDR) configuration

IDR bit number	Identification significance	IDR bit number	Identification significance	IDR bit number	Identification significance 1/
31	VERSION3	27	PARTNUMBER15	11	MANUFACTURER10
30	VERSION2	26	PARTNUMBER14	10	MANUFACTURER09
29	VERSION1	25	PARTNUMBER13	9	MANUFACTURER08
28	VERSION0	24	PARTNUMBER12	8	MANUFACTURER07
---	---	23	PARTNUMBER11	7	MANUFACTURER06
---	---	22	PARTNUMBER10	6	MANUFACTURER05
---	---	21	PARTNUMBER09	5	MANUFACTURER04
---	---	20	PARTNUMBER08	4	MANUFACTURER03
---	---	19	PARTNUMBER07	3	MANUFACTURER02
---	---	18	PARTNUMBER06	2	MANUFACTURER01
---	---	17	PARTNUMBER05	1	MANUFACTURER00
---	---	16	PARTNUMBER04	0	LOGIC1
---	---	15	PARTNUMBER03	---	---
---	---	14	PARTNUMBER02	---	---
---	---	13	PARTNUMBER01	---	---
---	---	12	PARTNUMBER00	---	---

1/ For cage code 01295 products, bits 11-0 of the device identification register always contain the binary value 000000101111 (02F, hex).

NOTE: During capture-DR, the binary value 00000000000000000101000000101111 (000502F, hex) is captured in the device identification register to identify this device as the 01 device, version 0 and 00010000000000000101000000101111 (1000502F) to identify the device as the 02 device.

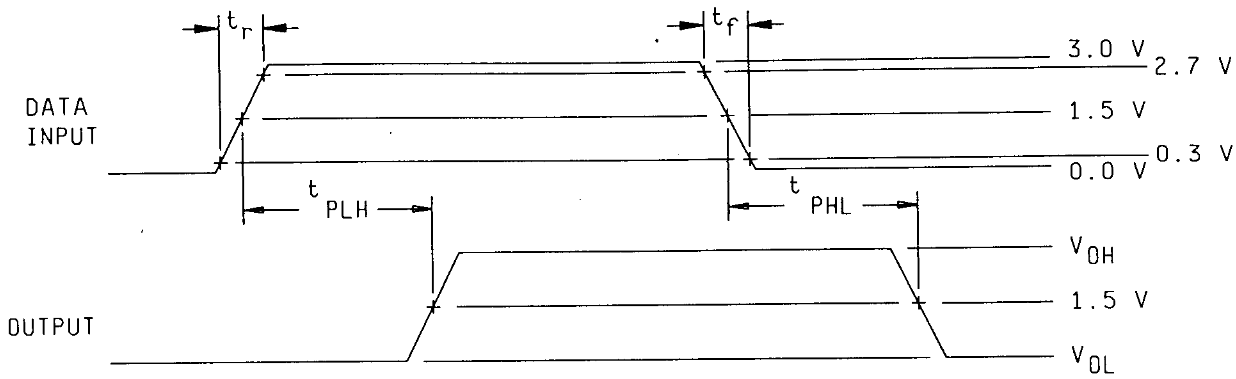
FIGURE 4. Test access port controller and scan test registers - Continued.



NOTES:

1. C_L includes a 47 pF chip capacitor (-0 percent, +20 percent) and at least 3 pF of equivalent capacitance from the test jig and probe.
2. R_L = 450Ω ±1 percent, chip resistor in series with a 50Ω termination. For monitored outputs, the 50Ω termination shall be the 50Ω characteristic impedance of the coaxial connector to the oscilloscope.
3. Input signal to the device under test:
   a. V_{IN} = 0.0 V to 3.0 V; duty cycle = 50 percent; $f_{IN} \geq 1$ MHz.
   b. t_r, t_f = 3 ns ±1.0 ns. For input signal generators incapable of maintaining these values of t_r and t_f, the 3.0 ns limit may be increased up to 10 ns, as needed, maintaining the ±1.0 ns tolerance and guaranteeing the results at 3.0 ns ±1.0 ns; skew between any two switching inputs signals (t_{sk}): ≤ 250 ps.

FIGURE 5. Ground bounce load circuit and waveforms.



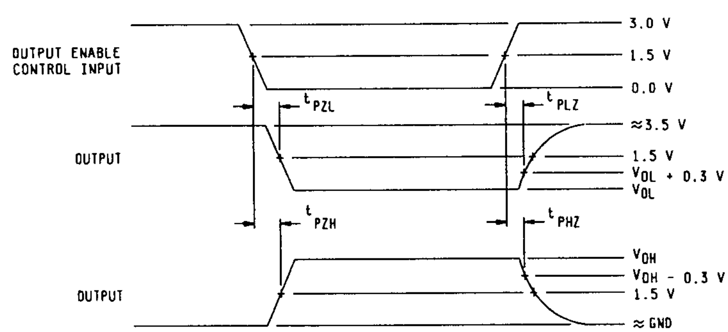


FIGURE 6. Switching waveforms and test circuit.

Boundry scan waveform

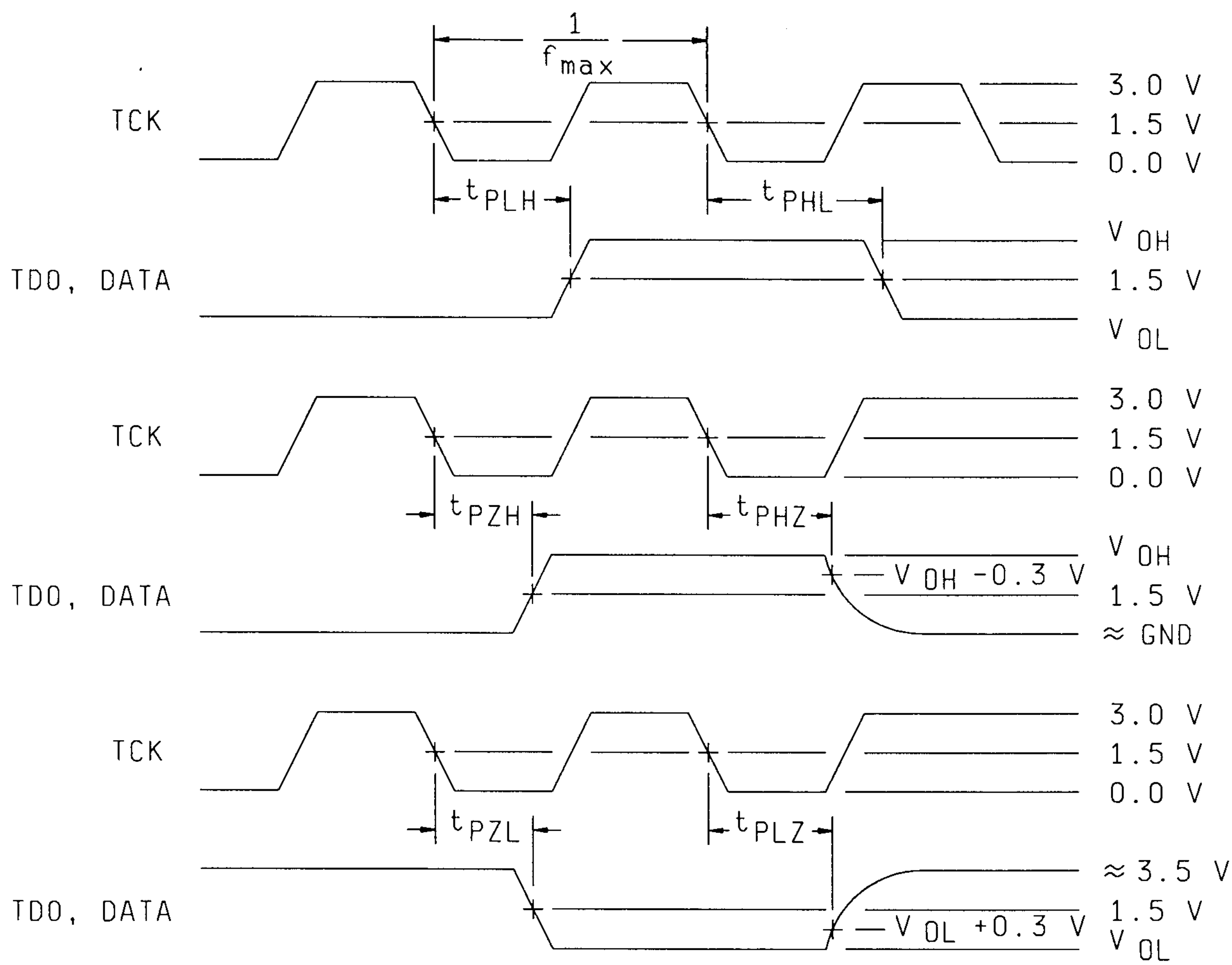
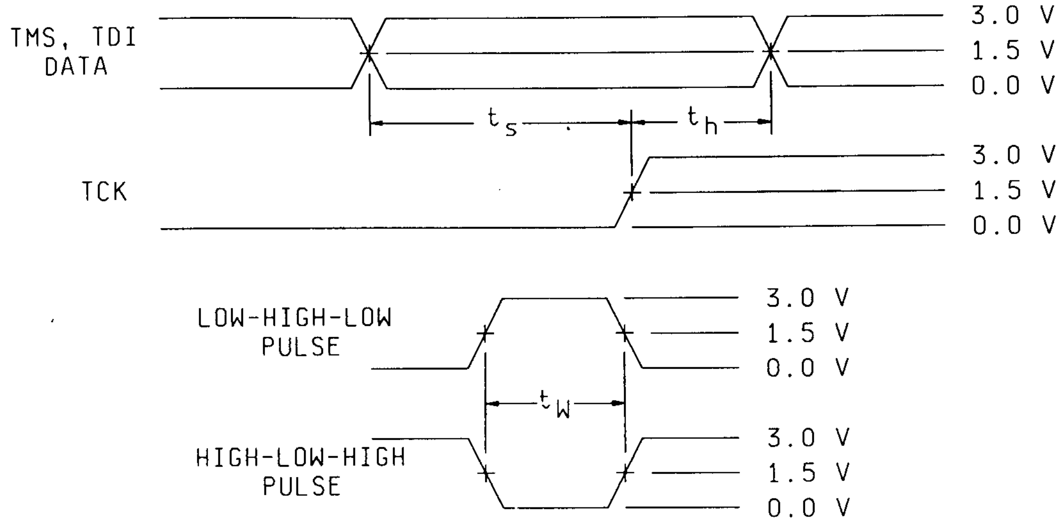
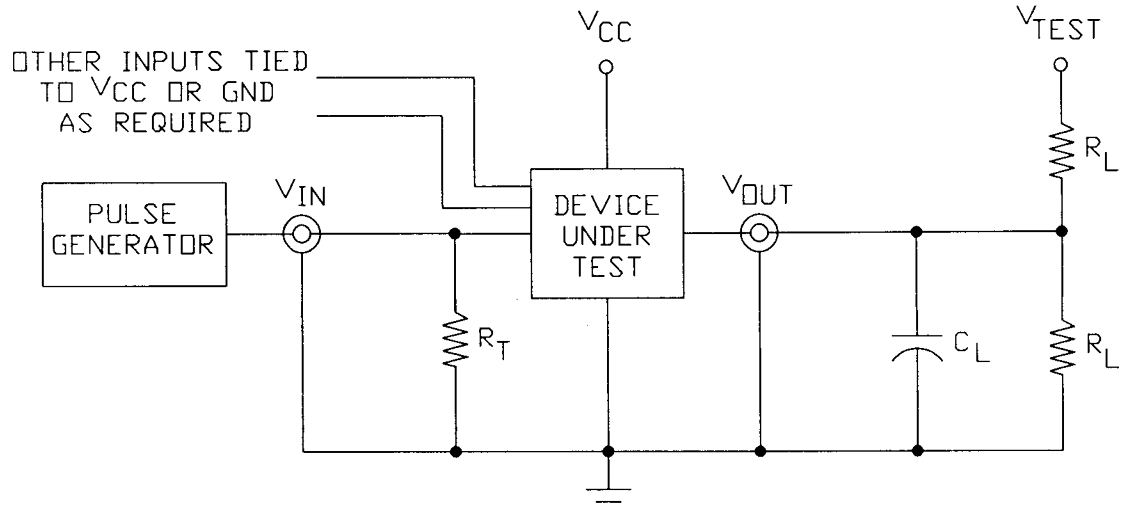


FIGURE 6. Switching waveforms and test circuit - Continued.

Boundry scan waveform





NOTES:

1. When measuring t_{PLZ} and t_{PZL}: V_{TEST} = 7.0 V.
2. When measuring t_{PHZ}, t_{PZH}, t_{PLH}, and t_{PHL}: V_{TEST} = open.
3. The t_{PZL} and t_{PLZ} reference waveform is for the output under test with internal conditions such that the output is at V_{OL} except when disabled by the output enable control. The t_{PZH} and t_{PHZ} reference waveform is for the output under test with internal conditions such that the output is at V_{OH} except when disabled by the output enable control.
4. C_L = 50 pF minimum or equivalent (includes test jig and probe capacitance).
5. R_L = 500Ω or equivalent.
6. R_T = 50Ω or equivalent.
7. Input signal from pulse generator: V_{IN} = 0.0 V to 3.0 V; PRR ≤ 10 MHz; t_r ≤ 2.5 ns; t_f ≤ 2.5 ns; t_r and t_f shall be measured from 0.3 V to 2.7 V and from 2.7 V to 0.3 V, respectively; duty cycle = 50 percent.
8. Timing parameters shall be tested at a minimum input frequency of 1 MHz.
9. The outputs are measured one at a time with one transition per measurement.

FIGURE 6. Switching waveforms and test circuit - Continued.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. For device class M, sampling and inspection procedures shall be in accordance with MIL-STD-883 (see 3.1 herein). For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-I-38535 and the device manufacturer's QM plan.

4.2 Screening. For device class M, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. For device classes Q and V, screening shall be in accordance with MIL-I-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection.

4.2.1 Additional criteria for device class M.

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A, B, C or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015.

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein.

4.2.2 Additional criteria for device classes Q and V.

a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-I-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-I-38535 and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015.

b. Interim and final electrical test parameters shall be as specified in table II herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in appendix B of MIL-I-38535.

4.3 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-I-38535. Inspections to be performed shall be those specified in MIL-I-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.3.1 Electrostatic discharge sensitivity qualification inspection. Electrostatic discharge sensitivity (ESDS) testing shall be performed in accordance with MIL-STD-883, method 3015. ESDS testing shall be measured only for initial qualification and after process or design changes which may affect ESDS classification.

4.4 Conformance inspection. Quality conformance inspection for device class M shall be in accordance with MIL-STD-883 (see 3.1 herein) and as specified herein. Inspections to be performed for device class M shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4). Technology conformance inspection for classes Q and V shall be in accordance with MIL-I-38535 including groups A, B, C, D, and E inspections and as specified herein except where option 2 of MIL-I-38535 permits alternate in-line control testing.

4.4.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. C_{IN}, C_{OUT}, and $C_{I/O}$ shall be measured only for initial qualification and after process or design changes which may affect capacitance. C_{IN}, C_{OUT}, and $C_{I/O}$ shall be measured between the designated terminal and GND at a frequency of 1 MHz. This test may be performed at 10 MHz and guaranteed, if not tested, at 1 MHz. The DC bias for the pin under test (V_{BIAS}) = 2.5 V or 3.0 V. For C_{IN}, C_{OUT}, and $C_{I/O}$, test all applicable pins on five devices with zero failures.

For C_{IN}, C_{OUT}, and $C_{I/O}$, a device manufacturer may qualify devices by functional groups. A specific functional group shall be composed of function types, that by design, will yield the same capacitance values when tested in accordance with table I herein. The device manufacturer shall set a functional group limit for the C_{IN}, C_{OUT}, and $C_{I/O}$ tests. The device manufacturer may then test one device function from a functional group to the limits and conditions specified herein. All other device functions in that particular functional group shall be guaranteed, if not tested, to the limits and conditions specified in table I herein. The device manufacturer shall submit to DESC-EC the device functions listed in each functional group and the test results for each device tested.

c. For device class M, subgroups 7 and 8 tests shall be sufficient to verify the truth table in figure 2 herein. The test vectors used to verify the truth table shall, at a minimum, test all functions of each input and output. All possible input to output logic patterns per function shall be guaranteed, if not tested, to the truth table in figure 2 herein. For device classes Q and V, subgroups 7 and 8 shall include verifying the functionality of the device; these tests shall have been fault graded in accordance with MIL-STD-883, test method 5012 (see 1.5 herein).

d. Ground and V_{CC} bounce tests are required for all device classes. These tests shall be performed only for initial qualification, after process or design changes which may affect the performance of the device, and any changes to the test fixture. V_{OLP}, V_{OLV}, V_{OHP}, and V_{OHV} shall be measured for the worst case outputs of the device. All other outputs shall be guaranteed, if not tested, to the limits established for the worst case outputs. The worst case outputs tested are to be determined by the manufacturer. Test 5 devices assembled in the worst case package type supplied to this document. All other package types shall be guaranteed, if not tested, to the limits established for the worst case package. The package type to be tested shall be determined by the manufacturer. The device manufacturer will submit to DESC-EC data that shall include all measured peak values for each device tested and detailed oscilloscope plots for each V_{OLP}, V_{OLV}, V_{OHP}, and V_{OHV} from one sample part per function. The plot shall contain the waveforms of both a switching output and the output under test.

Each device manufacturer shall test product on the fixtures they currently use. When a new fixture is used, the device manufacturer shall inform DESC-EC of this change and test the 5 devices on both the new and old test fixtures. The device manufacturer shall then submit to DESC-EC data from testing on both fixtures that shall include all measured peak values for each device tested and detailed oscilloscope plots for each V_{OLP}, V_{OLV}, V_{OHP}, and V_{OHV} from one sample part per function. The plot shall contain the waveforms of both a switching output and the output under test.

For V_{OLP}, V_{OLV}, V_{OHP}, and V_{OHV}, a device manufacturer may qualify devices by functional groups. A specific functional group shall be composed of function types, that by design, will yield the same test values when tested in accordance with table I herein. The device manufacturer shall set a functional group limit for the V_{OLP}, V_{OLV}, V_{OHP}, and V_{OHV} tests. The device manufacturer may then test one device function from a functional group to the limits and conditions specified herein. All other device functions in that particular functional group shall be guaranteed, if not tested, to the limits and conditions specified in table I herein. The device manufacturer shall submit to DESC-EC the device functions listed in each functional group and the test results, along with the oscilloscope plots, for each device tested.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table II herein.

4.4.2.1 Additional criteria for device class M. Steady-state life test conditions, method 1005 of MIL-STD-883:

a. Test condition A, B, C or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005.

b. T_A = +125°C, minimum.

c. Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

4.4.2.2 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-I-38535. The test circuit shall be maintained under document revision level control of the device manufacturer's TRB in accordance with MIL-I-38535 and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005.

TABLE II. Electrical test requirements.

Test requirements	Subgroups (in accordance with MIL-STD-883, TM 5005, table I)	Subgroups (in accordance with MIL-I-38535, table III)	
	Device class M	Device class Q	Device class V
Interim electrical parameters (see 4.2)	---	---	1
Final electrical parameters (see 4.2)	1, 2, 3, 7, 8, 9, 10, 11 1/	1, 2, 3, 7, 8, 9, 10, 11 1/	1, 2, 3, 7, 8, 9, 10, 11 2/
Group A test requirements (see 4.4)	1, 2, 3, 4, 7, 8, 9, 10, 11	1, 2, 3, 4, 7, 8, 9, 10, 11	1, 2, 3, 4, 7, 8, 9, 10, 11
Group C end-point electrical parameters (see 4.4)	1, 2, 3	1, 2, 3	1, 2, 3, 7 8, 9, 10, 11
Group D end-point electrical parameters (see 4.4)	1, 2, 3	1, 2, 3	1, 2, 3
Group E end-point electrical parameters (see 4.4)	1, 7, 9	1, 7, 9	1, 7, 9

1/ PDA applies to subgroup 1.
2/ PDA applies to subgroups 1 and 7.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table II herein.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein). RHA levels for device classes Q and V shall be M, D, R, and H and RHA levels for device class M shall be M and D.

a. End-point electrical parameters shall be as specified in table II herein.

b. For device class M, the devices shall be subjected to radiation hardness assured tests as specified in MIL-I-38535, appendix A, for the RHA level being tested. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-I-38535 for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table I at T_A = +25°C ±5°C, after exposure, to the subgroups specified in table II herein.

c. When specified in the purchase order or contract, a copy of the RHA delta limits shall be supplied.

4.5 Methods of inspection. Methods of inspection shall be specified as follows:

4.5.1 Voltage and current. Unless otherwise specified, all voltages given are referenced to the microcircuit GND terminal. Currents given are conventional current and positive when flowing into the referenced terminal.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-STD-883 (see 3.1 herein) for device class M and MIL-I-38535 for device classes Q and V.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.1.2 Substitutability. Device class Q devices will replace device class M devices.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished in accordance with MIL-STD-973 using DD Form 1692, Engineering Change Proposal.

6.3 Record of users. Military and industrial users shall inform Defense Electronics Supply Center when a system application requires configuration control and which SMD's are applicable to that system. DESC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DESC-EC, telephone (513) 296-6047.

6.4 Comments. Comments on this drawing should be directed to DESC-EC, Dayton, Ohio 45444-5270, or telephone (513) 296-5377.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-I-38535 and MIL-STD-1331, and as follows:

GND - - - - - - - - - - - - - - Ground zero voltage potential.
I_{CC} - - - - - - - - - - - - - - Supply current.
I_{IL} - - - - - - - - - - - - - - Input current low.
I_{IH} - - - - - - - - - - - - - - Input current high.
T_C - - - - - - - - - - - - - - Case temperature.
T_A - - - - - - - - - - - - - - Ambient temperature.
V_{CC} - - - - - - - - - - - - - - Positive supply voltage.
V_{IC-} - - - - - - - - - - - - - - Negative input clamp voltage.
C_{IN} - - - - - - - - - - - - - - Input terminal-to-GND capacitance.
C_{OUT} - - - - - - - - - - - - - - Output terminal-to-GND capacitance.
$C_{I/O}$ - - - - - - - - - - - - - - Input/output terminal-to-GND capacitance.

6.6 One part - one part number system. The one part - one part number system described below has been developed to allow for transitions between identical generic devices covered by the three major microcircuit requirements documents (MIL-H-38534, MIL-I-38535, and 1.2.1 of MIL-STD-883) without the necessity for the generation of unique PIN's. The three military requirements documents represent different class levels, and previously when a device manufacturer upgraded military product from one class level to another, the benefits of the upgraded product were unavailable to the Original Equipment Manufacturer (OEM), that was contractually locked into the original unique PIN. By establishing a one part number system covering all three documents, the OEM can acquire to the highest class level available for a given generic device to meet system needs without modifying the original contract parts selection criteria.

Military documentation format	Example PIN under new system	Manufacturing source listing	Document listing
New MIL-H-38534 Standardized Military Drawings	5962-XXXXXZZ(H or K)YY	QML-38534	MIL-BUL-103
New MIL-I-38535 Standardized Military Drawings	5962-XXXXXZZ(Q or V)YY	QML-38535	MIL-BUL-103
New 1.2.1 of MIL-STD-883 Standardized Military Drawings.	5962-XXXXXZZ(M)YY	MIL-BUL-103	MIL-BUL-103

6.7 Sources of supply.

6.7.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DESC-EC and have agreed to this drawing.

6.7.2 Approved sources of supply for device class M. Approved sources of supply for class M are listed in MIL-BUL-103. The vendors listed in MIL-BUL-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DESC-EC.

STANDARDIZED MILITARY DRAWING SOURCE APPROVAL BULLETIN

DATE: 95-11-20

Approved sources of supply for SMD 5962-94601 are listed below for immediate acquisition only and shall be added to QML-38535 during the next revision. QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DESC-EC. This bulletin is superseded by the next dated revision of QML-38535.

Standardized military drawing PIN	Vendor CAGE number	Vendor similar PIN 1/
5962-9460101QXA	01295	SNJ54ABT18245WD
5962-9460102QXA	01295	SNJ54ABT18245AWD

1/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number	Vendor name and address
01295	Texas Instruments Incorporated 13500 N. Central Expressway P.O. Box 655303 Dallas, TX 75265 Point of contact: I-20 at FM 1788 Midland, TX 79711-0448