AMC1400 Precision, ±250-mV Input, Reinforced Isolated Amplifier in a 15-mm Stretched SOIC Package

1 Features

- ±250-mV input voltage range optimized for current measurements using shunt resistors
- Fixed gain: 8.2 V/V
- Low DC errors:
  - Offset error: ±0.2 mV (max)
  - Offset drift: ±0.9 µV/°C (max)
  - Gain error: ±0.3% (max)
  - Gain drift: ±30 ppm/°C (max)
  - Nonlinearity: 0.03% (max)
- 3.3-V or 5-V operation on high-side and low-side
- Missing high-side supply detection feature
- High CMTI: 100 kV/µs (min)
- Low EMI, meets CISPR-11 and CISPR-32 standards
- ≥15.7-mm creepage, stretched SOIC package
- Safety-related certifications:
  - 10600-V_{PK} reinforced isolation per DIN EN IEC 60747-17 (VDE 0884-17)
  - 7500-V_{RMS} isolation for 1 minute per UL1577
- Fully specified over the extended industrial temperature range: –40°C to +125°C

2 Applications

- Shunt-resistor-based current sensing in:
  - Motor drives
  - Frequency inverters
  - Solar inverters
  - Wind turbine inverters
  - Rail transport systems

3 Description

The AMC1400 is a precision, isolated amplifier with an output separated from the input circuitry by an isolation barrier that is highly resistant to magnetic interference. This barrier is certified to provide reinforced galvanic isolation of up to 7.5 kV_{RMS} according to DIN EN IEC 60747-17 (VDE 0884-17) and UL1577, and supports a working voltage of up to 2 kV_{RMS}.

The isolation barrier separates parts of the system that operate on different common-mode voltage levels and protects the low-side from voltage levels that can cause electrical damage and are potentially harmful to an operator.
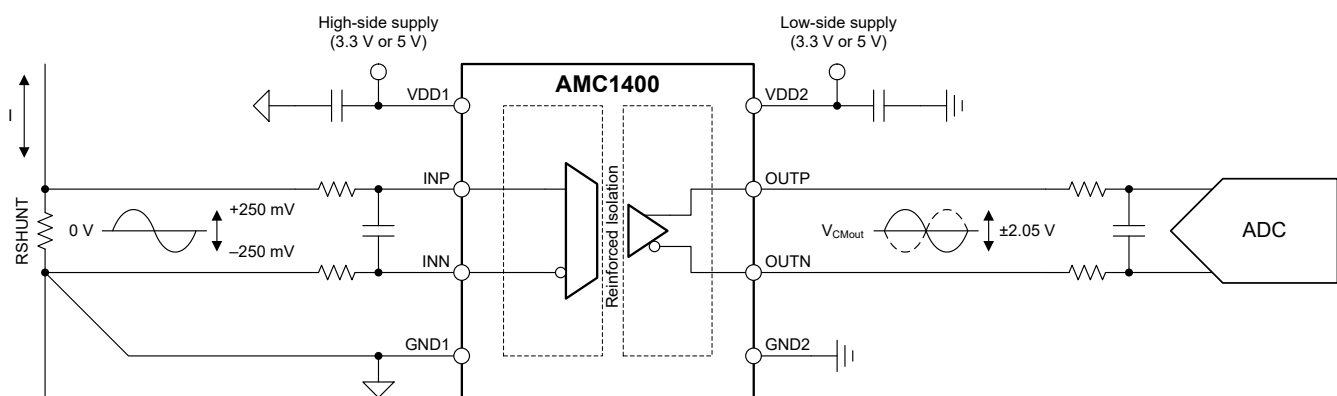
The input of the AMC1400 is optimized for direct connection to a low-impedance shunt resistor or other low-impedance voltage source with low signal levels. The excellent DC accuracy and low temperature drift supports accurate current control in DC/DC converters, frequency inverters, AC motor drives, and other applications that must operate at high voltages, high altitudes, or in environments with high pollution degrees.

The AMC1400 is offered in a stretched SOIC package and is specified over the extended industrial temperature range from –40°C to +125°C .

Package Information[1]

PART NUMBER	PACKAGE	BODY SIZE (NOM)
AMC1400	SOIC (8)	6.4 mm × 14.0 mm

(1)　For all available packages, see the orderable addendum at the end of the data sheet.

Typical Application

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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
July 2022	*	Initial Release

5 Pin Configuration and Functions

Not to scale

Figure 5-1. DWL Package, 8-Pin SOIC (Top View)

Table 5-1. Pin Functions

PIN		TYPE	DESCRIPTION
NO.	NAME		
1	VDD1	High-side power	High-side power supply.[1]
2	INP	Analog input	Noninverting analog input. Either INP or INN must have a DC current path to GND1 to define the common-mode input voltage.[2]
3	INN	Analog input	Inverting analog input. Either INP or INN must have a DC current path to GND1 to define the common-mode input voltage.[2]
4	GND1	High-side ground	High-side analog ground.
5	GND2	Low-side ground	Low-side analog ground.
6	OUTN	Analog output	Inverting analog output.
7	OUTP	Analog output	Noninverting analog output.
8	VDD2	Low-side power	Low-side power supply.[1]

(1)   See the *Power Supply Recommendations* section for power-supply decoupling recommendations.
(2)   See the *Layout* section for details.

6 Specifications

6.1 Absolute Maximum Ratings

see[1]

		MIN	MAX	UNIT
Power-supply voltage	High-side VDD1 to GND1	−0.3	6.5	V
	Low-side VDD2 to GND2	−0.3	6.5	
Analog input voltage	INP, INN	GND1 − 6	VDD1 + 0.5	V
Output voltage	OUTP, OUTN	GND2 − 0.5	VDD2 + 0.5	V
Input current	Continuous, any pin except power-supply pins	−10	10	mA
Temperature	Junction, T_J		150	°C
	Storage, T_{stg}	−65	150	

(1)   Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions* . If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001[1]	±2000	V
		Charged-device model (CDM), per ANSI/ESDA/JEDEC JS-002[2]	±1000	

(1)   JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2)   JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating ambient temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
POWER SUPPLY						
	High-side power supply	VDD1 to GND1	3	5	5.5	V
	Low-side power supply	VDD2 to GND2	3	3.3	5.5	V
ANALOG INPUT						
$V_{Clipping}$	Differential input voltage before clipping output	$V_{IN} = V_{INP} − V_{INN}$		±320		mV
V_{FSR}	Specified linear differential full-scale voltage	$V_{IN} = V_{INP} − V_{INN}$	−250		250	mV
V_{CM}	Operating common-mode input voltage	$(V_{INP} + V_{INN})$ / 2 to GND1	−0.16		VDD1 − 2.1	V
ANALOG OUTPUT						
C_{LOAD}	Capacitive load	On OUTP or OUTN to GND2			500	pF
C_{LOAD}	Capacitive load	OUTP to OUTN			250	pF
R_{LOAD}	Resistive load	On OUTP or OUTN to GND2		10	1	kΩ
TEMPERATURE RANGE						
T_A	Specified ambient temperature		−40	25	125	°C

6.4 Thermal Information

THERMAL METRIC[1]		DWL (SOIC)	UNIT
		8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	63.2	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	26.1	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	28.5	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	7.8	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	26.8	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

6.5 Power Ratings

PARAMETER		TEST CONDITIONS	VALUE	UNIT
P_D	Maximum power dissipation (both sides)	VDD1 = VDD2 = 5.5 V	99	mW
P_{D1}	Maximum power dissipation (high-side)	VDD1 = 3.6 V	31	mW
		VDD1 = 5.5 V	54	
P_{D2}	Maximum power dissipation (low-side)	VDD2 = 3.6 V	26	mW
		VDD2 = 5.5 V	45	

Product Folder Links: *AMC1400*

6.6 Insulation Specifications

over operating ambient temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	VALUE	UNIT
GENERAL				
CLR	External clearance[1]	Shortest pin-to-pin distance through air	≥ 14.7	mm
CPG	External creepage[1]	Shortest pin-to-pin distance across the package surface	≥ 15.7	mm
DTI	Distance through insulation	Minimum internal gap (internal clearance) of the double insulation	≥ 21	μm
CTI	Comparative tracking index	DIN EN 60112 (VDE 0303-11); IEC 60112	≥ 600	V
	Material group	According to IEC 60664-1	I	
	Overvoltage category per IEC 60664-1	Rated mains voltage ≤ 600 V_{RMS}	I-IV	
		Rated mains voltage ≤ 1000 V_{RMS}	I-III	
DIN EN IEC 60747-17 (VDE 0884-17)[2]				
V_{IORM}	Maximum repetitive peak isolation voltage	At AC voltage	2800	V_{PK}
V_{IOWM}	Maximum-rated isolation working voltage	At AC voltage (sine wave)	2000	V_{RMS}
		At DC voltage	2800	V_{DC}
V_{IOTM}	Maximum transient isolation voltage	$V_{TEST} = V_{IOTM}$, t = 60 s (qualification test)	10600	V_{PK}
		$V_{TEST} = 1.2 \times V_{IOTM}$, t = 1 s (100% production test)	12720	
V_{IMP}	Maximum impulse voltage[3]	Tested in air, 1.2/50-μs waveform per IEC 62368-1	9800	V_{PK}
V_{IOSM}	Maximum surge isolation voltage[4]	Tested in oil (qualification test), 1.2/50-μs waveform per IEC 62368-1	12800	V_{PK}
q_{pd}	Apparent charge[5]	Method a, after input/output safety test subgroups 2 and 3, $V_{ini} = V_{IOTM}$, t_{ini} = 60 s, $V_{pd(m)} = 1.2 \times V_{IORM}$, t_m = 10 s	≤ 5	pC
		Method a, after environmental tests subgroup 1, $V_{ini} = V_{IOTM}$, t_{ini} = 60 s, $V_{pd(m)} = 1.6 \times V_{IORM}$, t_m = 10 s	≤ 5	
		Method b1, at routine test (100% production) and preconditioning (type test), $V_{ini} = V_{IOTM}$, t_{ini} = 1 s, $V_{pd(m)} = 1.875 \times V_{IORM}$, t_m = 1 s	≤ 5	
C_{IO}	Barrier capacitance, input to output[6]	$V_{IO} = 0.5 V_{PP}$ at 1 MHz	~1.5	pF
R_{IO}	Insulation resistance, input to output[6]	V_{IO} = 500 V at T_A = 25°C	> 10^{12}	Ω
		V_{IO} = 500 V at 100°C ≤ T_A ≤ 125°C	> 10^{11}	
		V_{IO} = 500 V at T_S = 150°C	> 10^9	
	Pollution degree		2	
	Climatic category		55/125/21	
UL1577				
V_{ISO}	Withstand isolation voltage	$V_{TEST} = V_{ISO}$ = 7500 V_{RMS}, t = 60 s (qualification), $V_{TEST} = 1.2 \times V_{ISO}$ = 9000 V_{RMS}, t = 1 s (100% production test)	7500	V_{RMS}

(1) Apply creepage and clearance requirements according to the specific equipment isolation standards of an application. Care must be taken to maintain the creepage and clearance distance of a board design to ensure that the mounting pads of the isolator on the printed circuit board (PCB) do not reduce this distance. Creepage and clearance on a PCB become equal in certain cases. Techniques such as inserting grooves, ribs, or both on a PCB are used to help increase these specifications.
(2) This coupler is suitable for *safe electrical insulation* only within the safety ratings. Compliance with the safety ratings shall be ensured by means of suitable protective circuits.
(3) Testing is carried out in air to determine the surge immunity of the package.
(4) Testing is carried in oil to determine the intrinsic surge immunity of the isolation barrier.
(5) Apparent charge is electrical discharge caused by a partial discharge (pd).
(6) All pins on each side of the barrier are tied together, creating a two-pin device.

6.7 Safety-Related Certifications

VDE	UL
DIN EN IEC 60747-17 (VDE 0884-17), EN IEC 60747-17, DIN EN IEC 62368-1 (VDE 0868-1), EN IEC 62368-1, IEC 62368-1 Clause : 5.4.3 ; 5.4.4.4 ; 5.4.9	Recognized under 1577 component recognition program
Reinforced insulation	Single protection
Certificate number: 40040142 (pending)	File number: E181974

6.8 Safety Limiting Values

Safety limiting[1] intends to minimize potential damage to the isolation barrier upon failure of input or output circuitry. A failure of the I/O can allow low resistance to ground or the supply and, without current limiting, dissipate sufficient power to over-heat the die and damage the isolation barrier potentially leading to secondary system failures.

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_S	Safety input, output, or supply current	$R_{\theta JA}$ = 63.2°C/W, VDDx = 3.6 V, T_J = 150°C, T_A = 25°C			550	mA
		$R_{\theta JA}$ = 63.2°C/W, VDDx = 5.5 V, T_J = 150°C, T_A = 25°C			360	
P_S	Safety input, output, or total power	$R_{\theta JA}$ = 63.2°C/W, T_J = 150°C, T_A = 25°C			1980	mW
T_S	Maximum safety temperature				150	°C

(1) The maximum safety temperature, T_S, has the same value as the maximum junction temperature, T_J, specified for the device. The I_S and P_S parameters represent the safety current and safety power, respectively. Do not exceed the maximum limits of I_S and P_S. These limits vary with the ambient temperature, T_A.

The junction-to-air thermal resistance, $R_{\theta JA}$, in the *Thermal Information* table is that of a device installed on a high-K test board for leaded surface-mount packages. Use these equations to calculate the value for each parameter:

$T_J = T_A + R_{\theta JA} \times P$, where P is the power dissipated in the device.

$T_{J(max)} = T_S = T_A + R_{\theta JA} \times P_S$, where $T_{J(max)}$ is the maximum junction temperature.

$P_S = I_S \times VDD_{max}$, where VDD_{max} is the maximum supply voltage for high-side and low-side.

6.9 Electrical Characteristics

minimum and maximum specifications apply from T_A = –40°C to +125°C, VDD1 = 3.0 V to 5.5 V, VDD2 = 3.0 V to 5.5 V, INP = –250 mV to +250 mV, and INN = GND1; typical specifications are at T_A = 25°C, VDD1 = 5 V, and VDD2 = 3.3 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ANALOG INPUT						
V_{OS}	Input offset voltage[1] [2]	T_A = 25°C, INP = INN = GND1	–0.2	±0.01	0.2	mV
TCV_{OS}	Input offset drift[1] [2] [4]		–0.9	±0.1	0.9	µV/°C
CMRR	Common-mode rejection ratio	f_{IN} = 0 Hz, $V_{CM\ min}$ ≤ V_{CM} ≤ $V_{CM\ max}$		–100		dB
		f_{IN} = 10 kHz, $V_{CM\ min}$ ≤ V_{CM} ≤ $V_{CM\ max}$		–98		
R_{IN}	Single-ended input resistance	INN = GND1		19		kΩ
R_{IND}	Differential input resistance			22		kΩ
I_{IB}	Input bias current	INP = INN = GND1; I_{IB} = (I_{IBP} + I_{IBN}) / 2	–41	–30	–24	µA
I_{IO}	Input offset current	I_{IO} = I_{IBP} – I_{IBN}; INP = INN = GND1		±5		nA
C_{IN}	Single-ended input capacitance	INN = GND1, f_{IN} = 275 kHz		2		pF
C_{IND}	Differential input capacitance	f_{IN} = 275 kHz		1		pF
ANALOG OUTPUT						
	Nominal gain			8.2		V/V
E_G	Gain error[1]	T_A = 25°C	–0.3%	±0.04%	0.3%	
TCE_G	Gain drift[1] [5]		–30	±5	30	ppm/°C
	Nonlinearity[1]		–0.03%	±0.01%	0.03%	
THD	Total harmonic distortion[3]	f_{IN} = 10 kHz		–85		dB
	Output noise	INP = INN = GND1, f_{IN} = 0 Hz, BW = 100 kHz brickwall filter		230		µV$_{RMS}$
SNR	Signal-to-noise ratio	f_{IN} = 1 kHz, BW = 10 kHz	81.5	85		dB
		f_{IN} = 10 kHz, BW = 100 kHz		72		
PSRR	Power-supply rejection ratio[2]	PSRR vs VDD1, at DC		–100		dB
		PSRR vs VDD1, 100-mV and 10-kHz ripple		–96		
		PSRR vs VDD2, at DC		–106		
		PSRR vs VDD2, 100-mV and 10-kHz ripple		–86		
V_{CMout}	Common-mode output voltage		1.39	1.44	1.49	V
$V_{CLIPout}$	Clipping differential output voltage	V_{OUT} = (V_{OUTP} – V_{OUTN}); $|V_{IN}|$ = $|V_{INP}$ – $V_{INN}|$ > $|V_{Clipping}|$	–2.52	±2.49	2.52	V
$V_{Failsafe}$	Failsafe differential output voltage	VDD1 missing	–2.63	–2.57	–2.53	V
BW	Output bandwidth		250	310		kHz
R_{OUT}	Output resistance	On OUTP or OUTN		< 0.2		Ω
	Output short-circuit current	On OUTP or OUTN, sourcing or sinking, INN = INP = GND1, outputs shorted to either GND2 or VDD2		14		mA
CMTI	Common-mode transient immunity		100	150		kV/µs

6.9 Electrical Characteristics (continued)

minimum and maximum specifications apply from T_A = –40°C to +125°C, VDD1 = 3.0 V to 5.5 V, VDD2 = 3.0 V to 5.5 V, INP = –250 mV to +250 mV, and INN = GND1; typical specifications are at T_A = 25°C, VDD1 = 5 V, and VDD2 = 3.3 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER SUPPLY						
VDD1$_{UV}$	VDD1 undervoltage detection threshold	VDD1 rising	2.5	2.7	2.9	V
		VDD1 falling	2.4	2.6	2.8	
VDD2$_{UV}$	VDD2 undervoltage detection threshold	VDD2 rising	2.2	2.45	2.65	V
		VDD2 falling	1.85	2.0	2.2	
IDD1	High-side supply current	3.0 V ≤ VDD1 ≤ 3.6 V		6.3	8.5	mA
		4.5 V ≤ VDD1 ≤ 5.5 V		7.2	9.8	
IDD2	Low-side supply current	3.0 V ≤ VDD2 ≤ 3.6 V		5.3	7.2	mA
		4.5 V ≤ VDD2 ≤ 5.5 V		5.9	8.1	

(1) The typical value includes one standard deviation (*sigma*) at nominal operating conditions.
(2) This parameter is input referred.
(3) THD is the ratio of the rms sum of the amplitudes of first five higher harmonics to the amplitude of the fundamental.
(4) Offset error temperature drift is calculated using the box method, as described by the following equation:
$TCV_{OS} = (Value_{MAX} - Value_{MIN}) / TempRange$
(5) Gain error temperature drift is calculated using the box method, as described by the following equation:
$TCE_G (ppm) = (Value_{MAX} - Value_{MIN}) / (Value_{(T=25°C)} \times TempRange) \times 10^6$

6.10 Switching Characteristics

over operating ambient temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_r	Output signal rise time			1.3		µs
t_f	Output signal fall time			1.3		µs
	V_{INx} to V_{OUTx} signal delay (50% - 10%)	Unfiltered output		1	1.5	µs
	V_{INx} to V_{OUTx} signal delay (50% - 50%)	Unfiltered output		1.6	2.1	µs
	V_{INx} to V_{OUTx} signal delay (50% - 90%)	Unfiltered output		2.5	3	µs
t_{AS}	Analog settling time	VDD1 step to 3.0 V with VDD2 ≥ 3.0 V, to V_{OUTP}, V_{OUTN} valid, 0.1% settling		500		µs

6.11 Timing Diagram
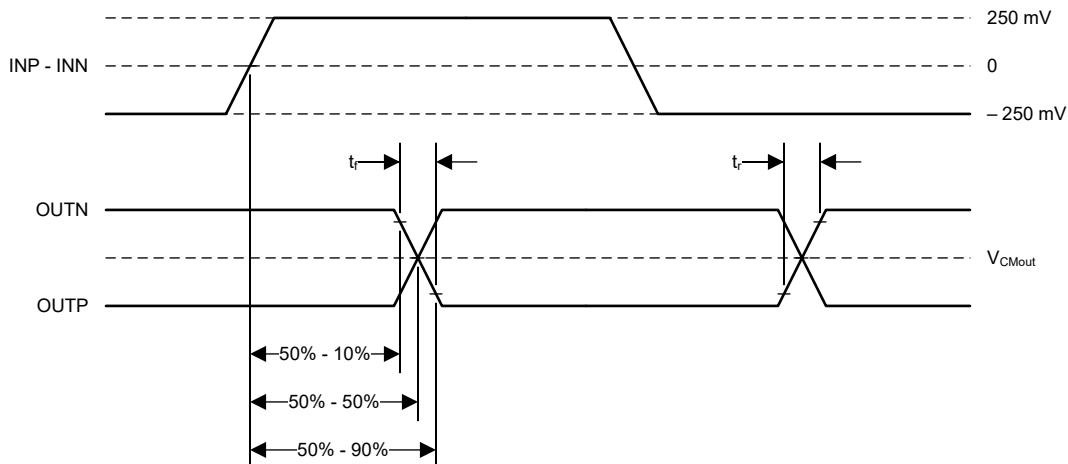
Figure 6-1. Rise, Fall, and Delay Time Definition

Product Folder Links: *AMC1400*

6.12 Insulation Characteristics Curves
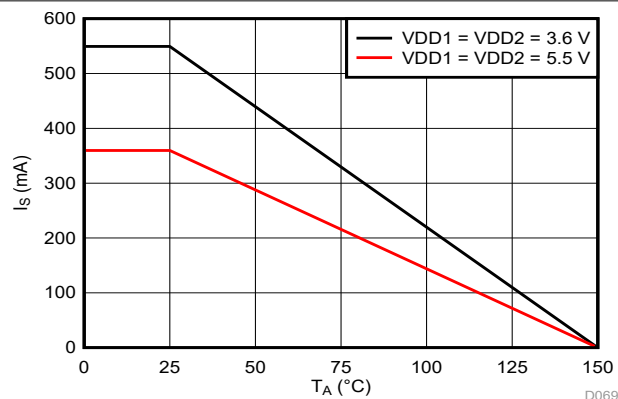
Figure 6-2. Thermal Derating Curve for Safety-Limiting Current per VDE
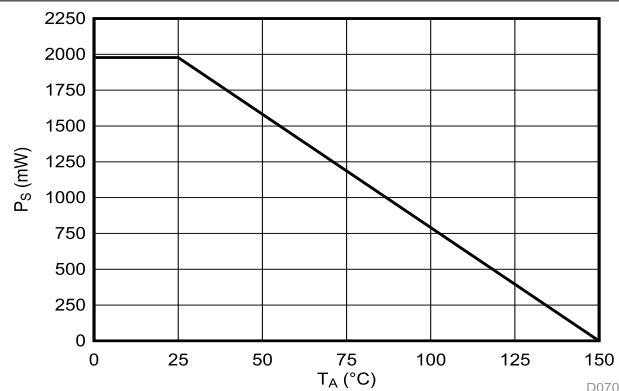
Figure 6-3. Thermal Derating Curve for Safety-Limiting Power per VDE
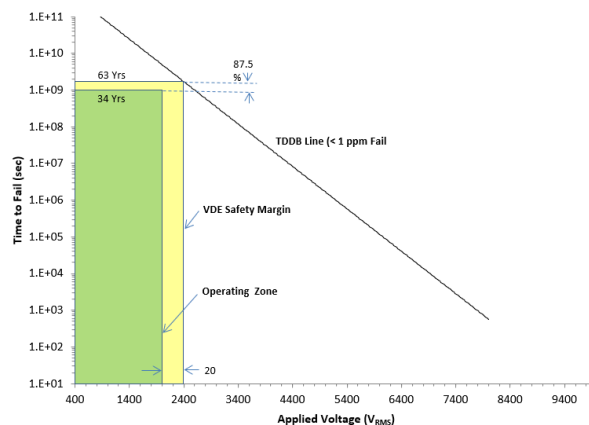
T_A up to 150°C, stress-voltage frequency = 60 Hz, isolation working voltage = 2000 V_{RMS}, operating lifetime = 34 year

Figure 6-4. Reinforced Isolation Capacitor Lifetime Projection

Product Folder Links: *AMC1400*

6.13 Typical Characteristics

at VDD1 = 5 V, VDD2 = 3.3 V, INP = –250 mV to 250 mV, INN = 0 V, and f$_{IN}$ = 10 kHz (unless otherwise noted)
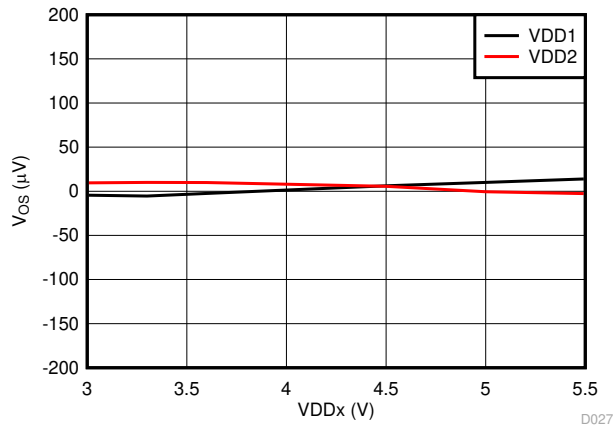
Figure 6-5. Input Offset Voltage vs Supply Voltage
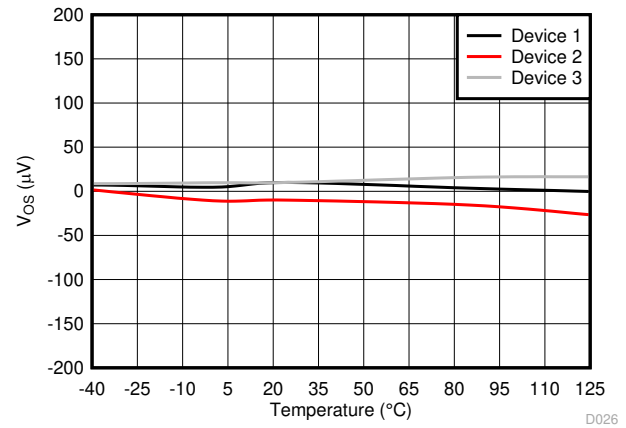
Figure 6-6. Input Offset Voltage vs Temperature
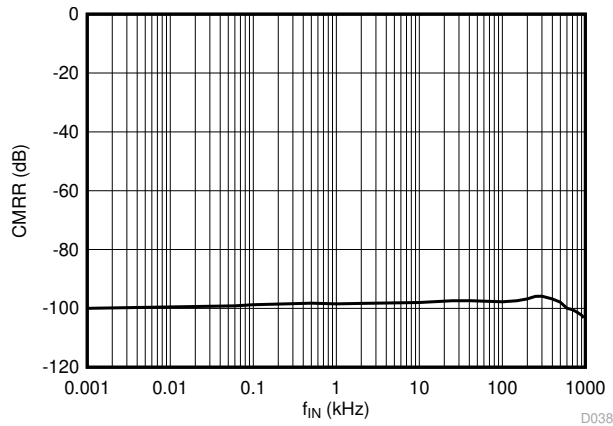
Figure 6-7. Common-Mode Rejection Ratio vs Input Frequency
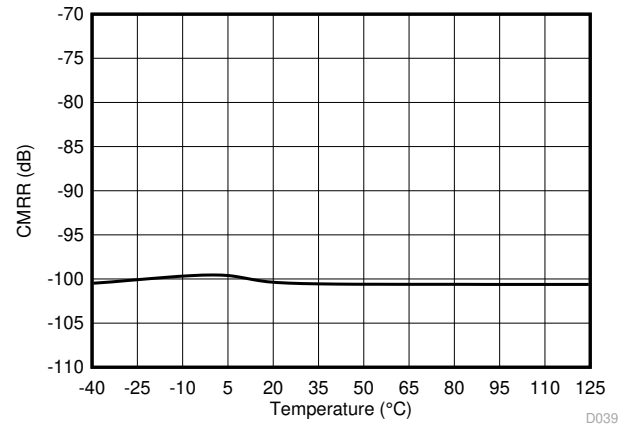
Figure 6-8. Common-Mode Rejection Ratio vs Temperature
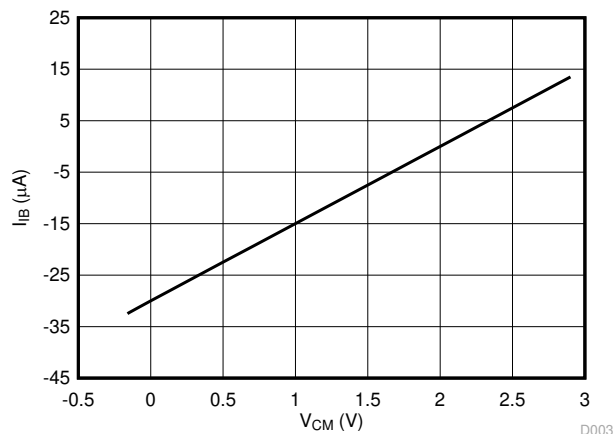
Figure 6-9. Input Bias Current vs Common-Mode Input Voltage
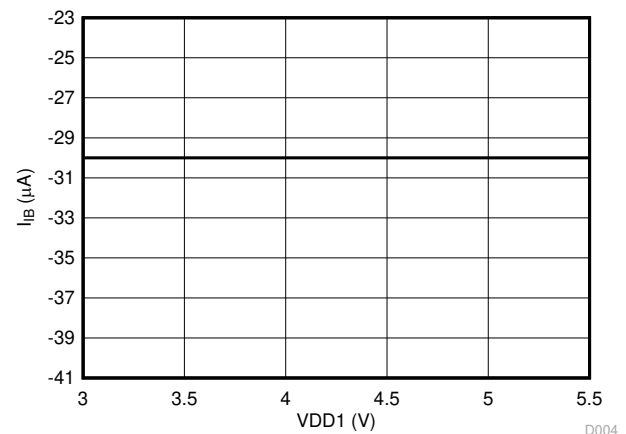
Figure 6-10. Input Bias Current vs High-Side Supply Voltage

Product Folder Links: *AMC1400*

6.13 Typical Characteristics (continued)

at VDD1 = 5 V, VDD2 = 3.3 V, INP = –250 mV to 250 mV, INN = 0 V, and f_{IN} = 10 kHz (unless otherwise noted)
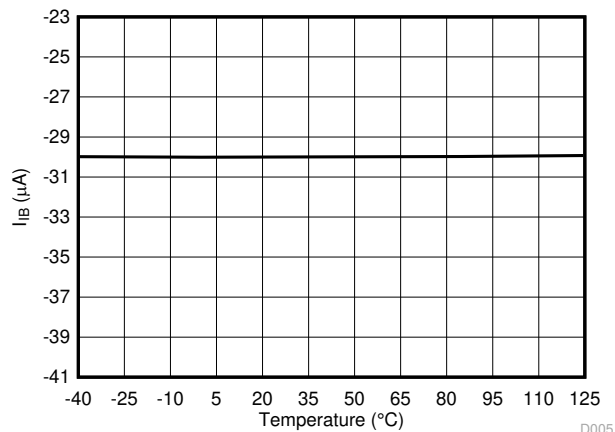
Figure 6-11. Input Bias Current vs Temperature
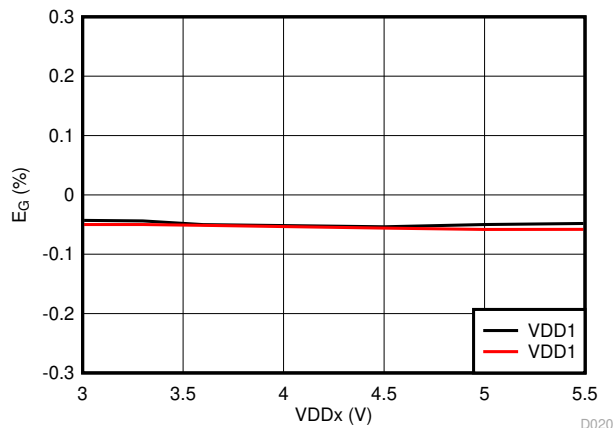
Figure 6-12. Gain Error vs Supply Voltage
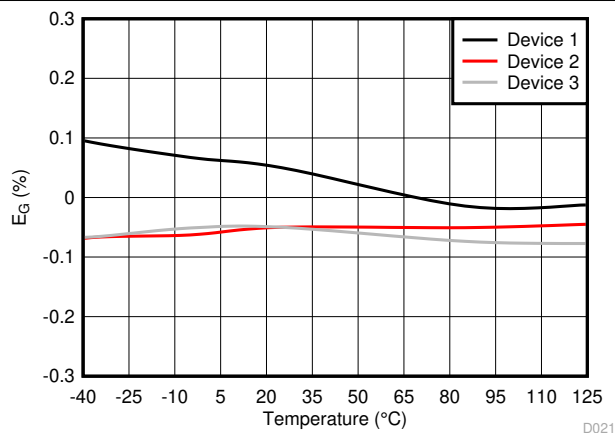
Figure 6-13. Gain Error vs Temperature
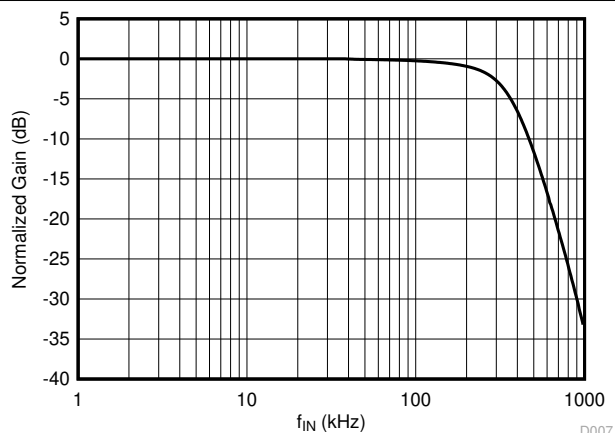
Figure 6-14. Normalized Gain vs Input Frequency
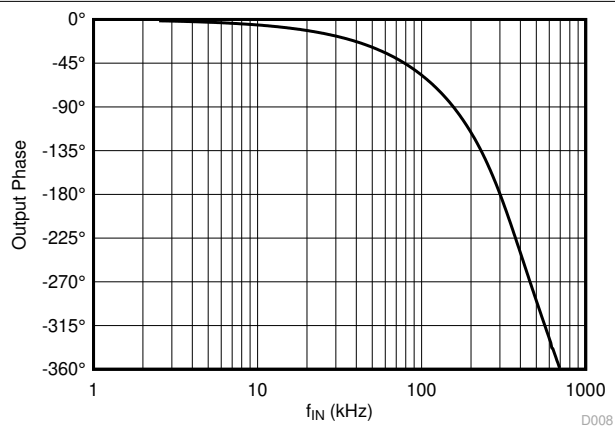
Figure 6-15. Output Phase vs Input Frequency
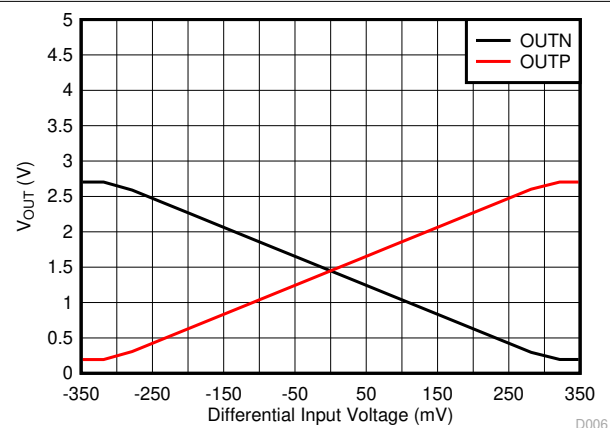
Figure 6-16. Output Voltage vs Input Voltage

Product Folder Links: *AMC1400*

6.13 Typical Characteristics (continued)

at VDD1 = 5 V, VDD2 = 3.3 V, INP = –250 mV to 250 mV, INN = 0 V, and f$_{IN}$ = 10 kHz (unless otherwise noted)
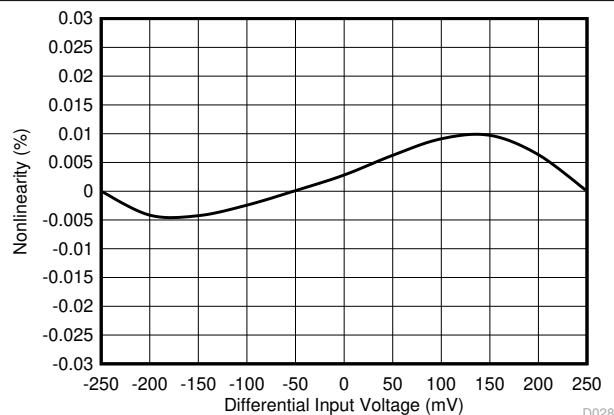
Figure 6-17. Nonlinearity vs Input Voltage
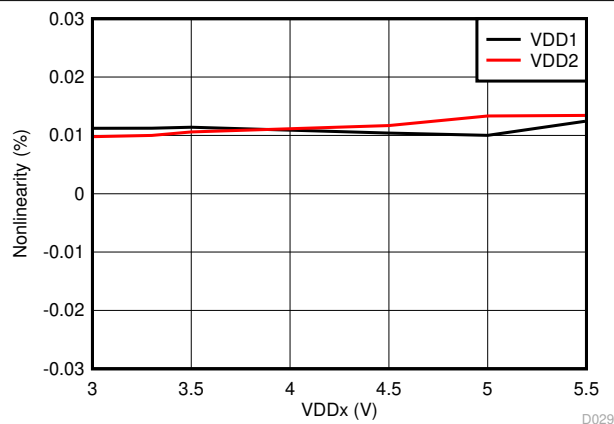
Figure 6-18. Nonlinearity vs Supply Voltage
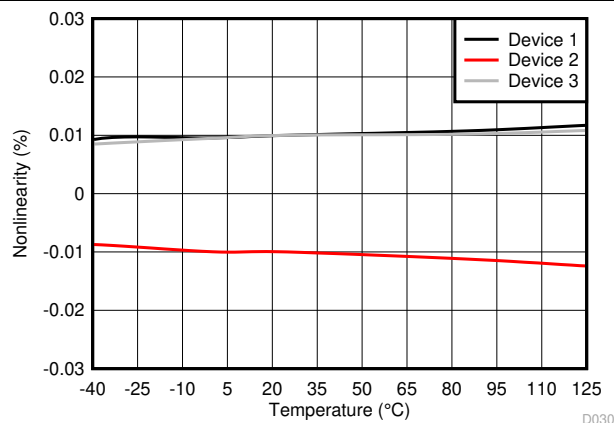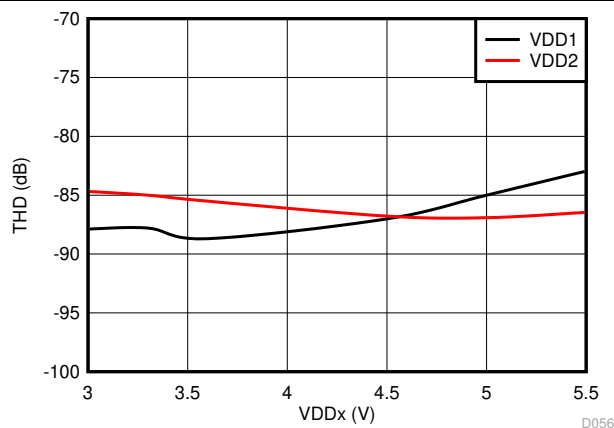

Figure 6-19. Nonlinearity vs Temperature

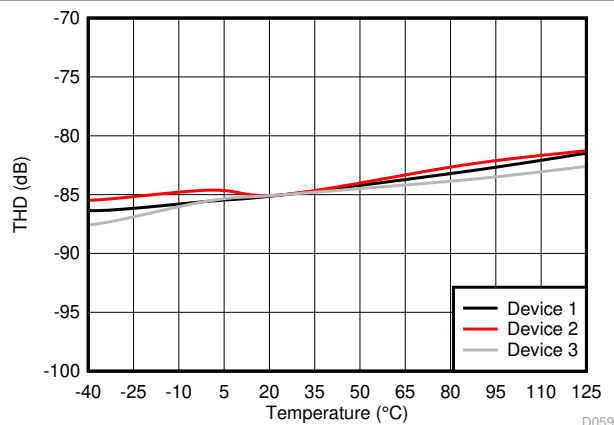
Figure 6-20. Total Harmonic Distortion vs Supply Voltage

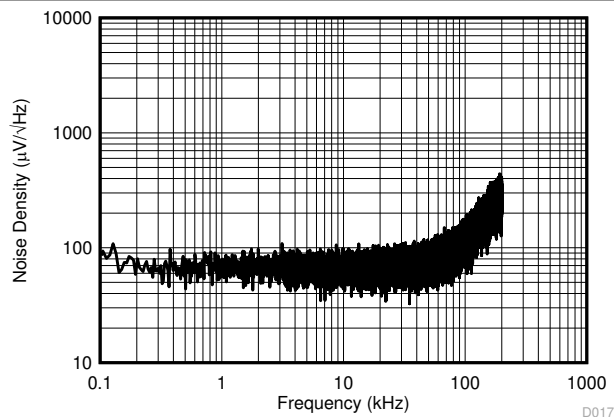**Figure 6-21. Total Harmonic Distortion vs Temperature**

Figure 6-22. Input-Referred Noise Density vs Frequency

6.13 Typical Characteristics (continued)

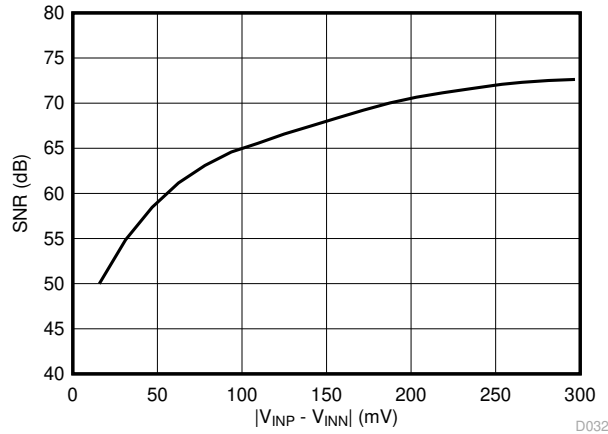at VDD1 = 5 V, VDD2 = 3.3 V, INP = –250 mV to 250 mV, INN = 0 V, and f_{IN} = 10 kHz (unless otherwise noted)
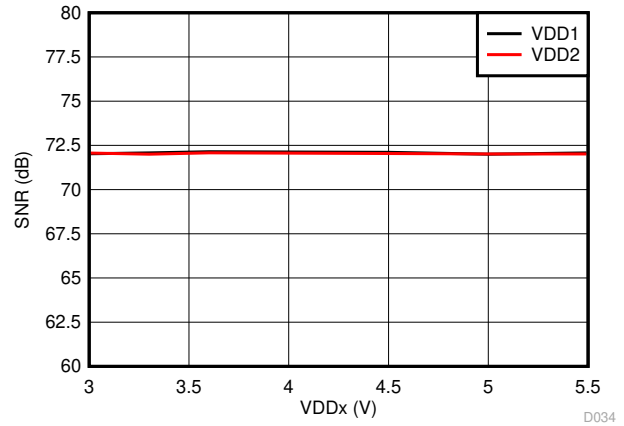

Figure 6-23. Signal-to-Noise Ratio vs Input Voltage

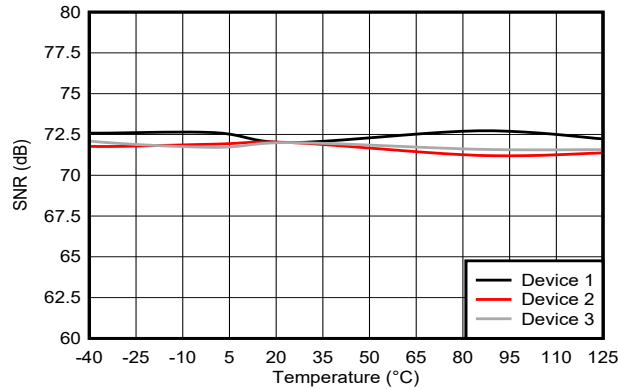**Figure 6-24. Signal-to-Noise Ratio vs Supply Voltage**

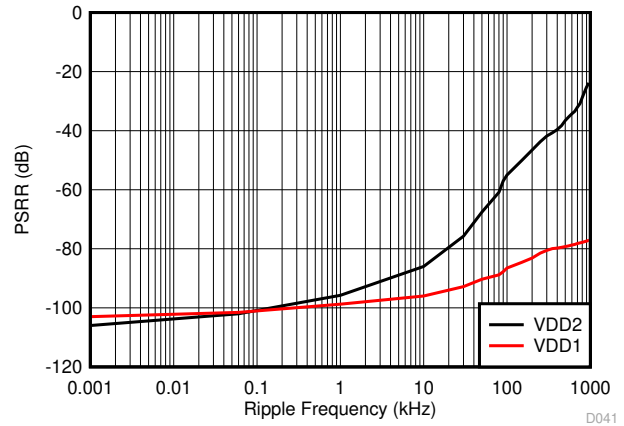**Figure 6-25. Signal-to-Noise Ratio vs Temperature**

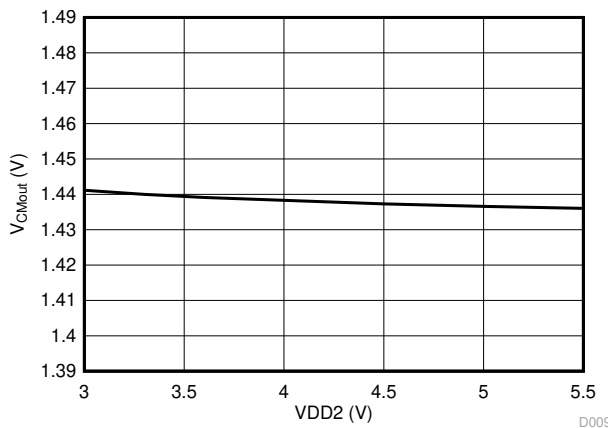**Figure 6-26. Power-Supply Rejection Ratio vs Ripple Frequency**

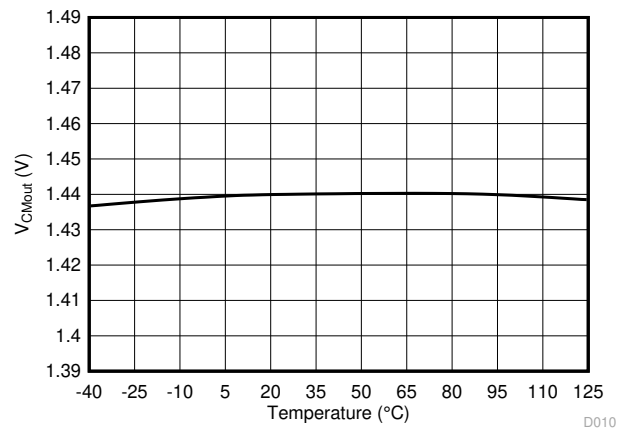**Figure 6-27. Output Common-Mode Voltage vs Low-Side Supply Voltage**

Figure 6-28. Output Common-Mode Voltage vs Temperature

Product Folder Links: *AMC1400*

6.13 Typical Characteristics (continued)

at VDD1 = 5 V, VDD2 = 3.3 V, INP = –250 mV to 250 mV, INN = 0 V, and f_{IN} = 10 kHz (unless otherwise noted)

Figure 6-29. Output Bandwidth vs Low-Side Supply Voltage

Figure 6-30. Output Bandwidth vs Temperature
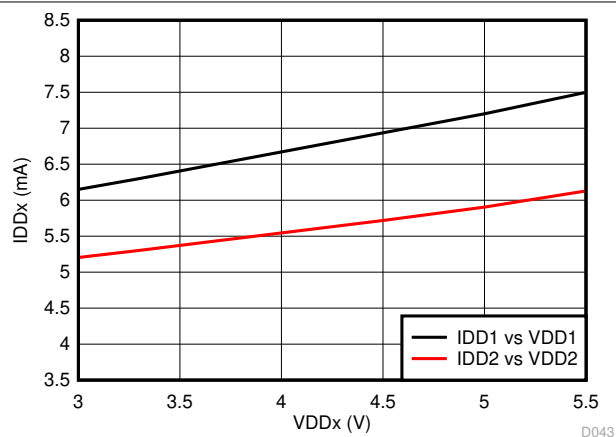
Figure 6-31. Supply Current vs Supply Voltage
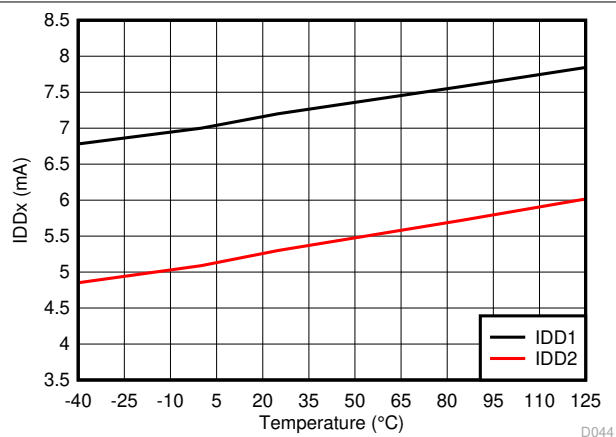
Figure 6-32. Supply Current vs Temperature
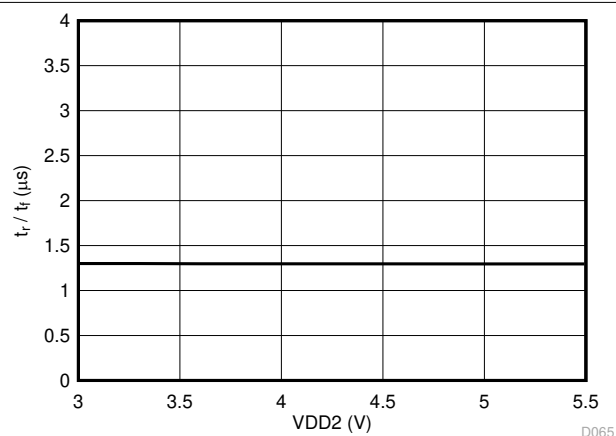
Figure 6-33. Output Rise and Fall Time vs Low-Side Supply
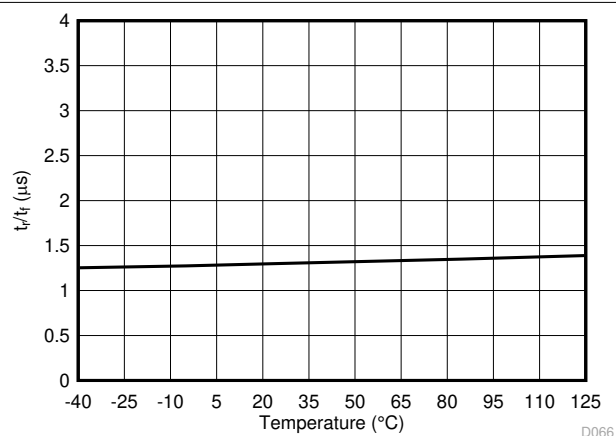
Figure 6-34. Output Rise and Fall Time vs Temperature

6.13 Typical Characteristics (continued)

at VDD1 = 5 V, VDD2 = 3.3 V, INP = –250 mV to 250 mV, INN = 0 V, and f_{IN} = 10 kHz (unless otherwise noted)
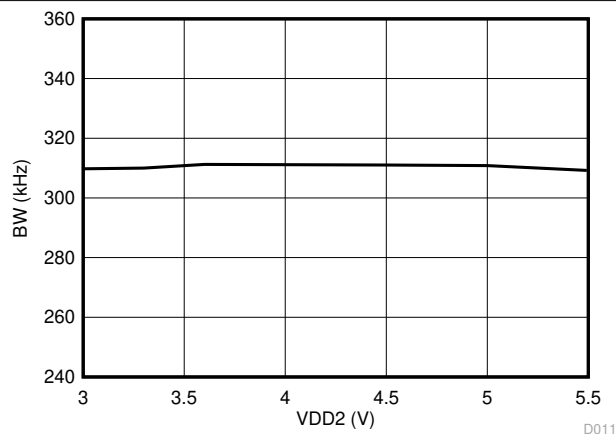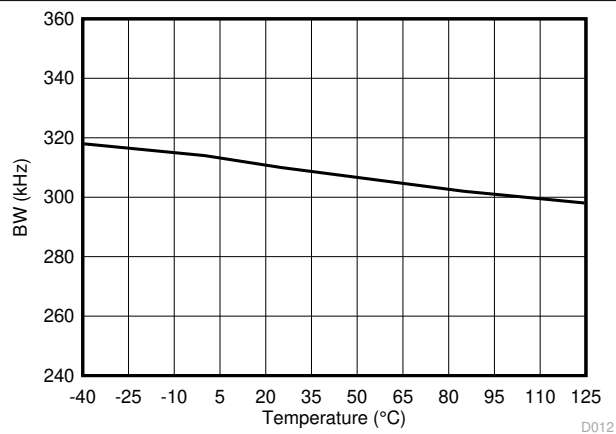

Figure 6-35. V$_{IN}$ to V$_{OUT}$ Signal Delay vs Low-Side Supply Voltage

Figure 6-36. V$_{IN}$ to V$_{OUT}$ Signal Delay vs Temperature

7 Detailed Description

7.1 Overview

The AMC1400 is a fully differential, precision, isolated amplifier. The input stage of the device consists of a fully differential amplifier that drives a second-order, delta-s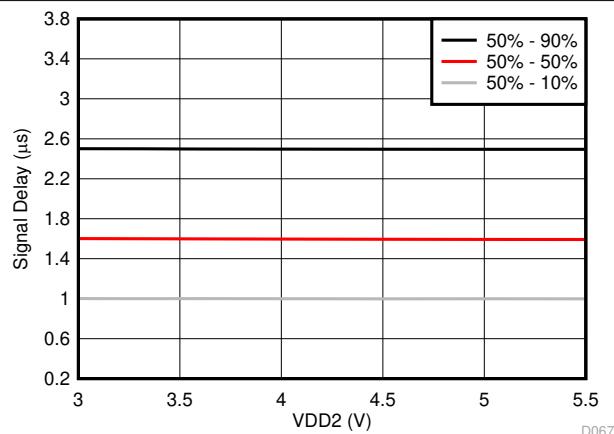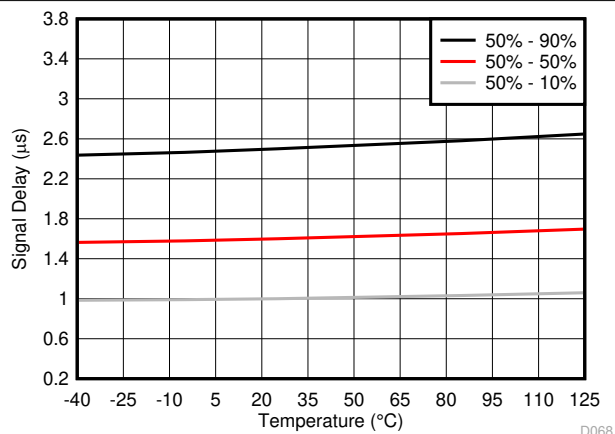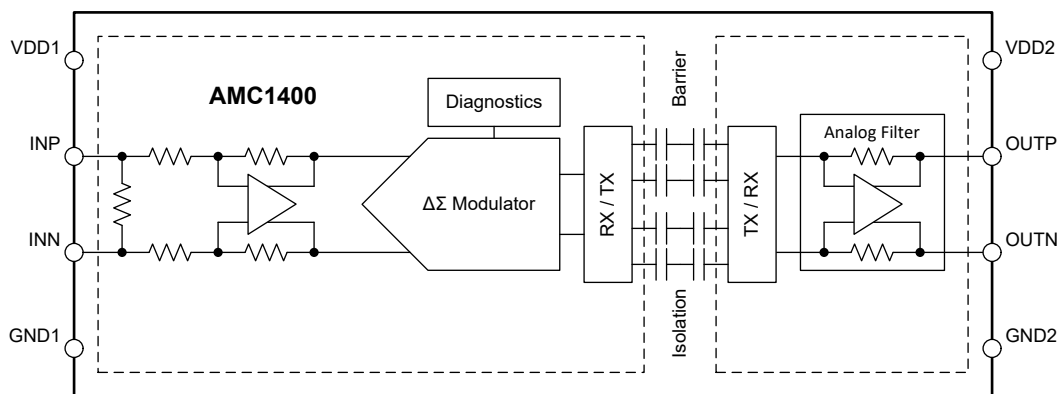igma ($\Delta\Sigma$) modulator. The modulator converts the analog input signal into a digital bitstream that is transferred across the isolation barrier that separates the high-side from the low-side. On the low-side, the received bitstream is processed by a fourth-order analog filter that outputs a differential signal at the OUTP and OUTN pins that is proportional to the input signal.

The SiO_2-based, capacitive isolation barrier supports a high level of magnetic field immunity, as described in the *ISO72x Digital Isolator Magnetic-Field Immunity* application report. The digital modulation used in the AMC1400 to transmit data across the isolation barrier, and the isolation barrier characteristics itself, result in high reliability and common-mode transient immunity.

7.2 Functional Block Diagram

7.3 Feature Description

7.3.1 Analog Input

The differential amplifier input stage of the AMC1400 feeds a second-order, switched-capacitor, feed-forward $\Delta\Sigma$ modulator. The gain of the differential amplifier is set by internal precision resistors with a differential input impedance of R_{IND}. The modulator converts the analog input signal into a bitstream that is transferred across the isolation barrier, as described in the *Isolation Channel Signal Transmission* section.

There are two restrictions on the analog input signals INP and INN. First, if the input voltages V_{INP} or V_{INN} exceed the range specified in the *Absolute Maximum Ratings* table, the input currents must be limited to the absolute maximum value, because the electrostatic discharge (ESD) protection turns on. In addition, the linearity and parametric performance of the device are ensured only when the analog input voltage remains within the linear full-scale range (V_{FSR}) and within the common-mode input voltage range (V_{CM}), as specified in the *Recommended Operating Conditions* table.

7.3.2 Isolation Channel Signal Transmission

The AMC1400 uses an on-off keying (OOK) modulation scheme, as shown in Figure 7-1, to transmit the modulator output bitstream across the SiO$_2$-based isolation barrier. The transmit driver (TX) shown in the *Functional Block Diagram* transmits an internally-generated, high-frequency carrier across the isolation barrier to represent a digital *one* and does not send a signal to represent a digital *zero*. The nominal frequency of the carrier used inside the AMC1400 is 480 MHz.

The receiver (RX) on the other side of the isolation barrier recovers and demodulates the signal and provides the input to the fourth-order analog filter. The AMC1400 transmission channel is optimized to achieve the highest level of common-mode transient immunity (CMTI) and lowest level of radiated emissions caused by the high-frequency carrier and RX/TX buffer switching.
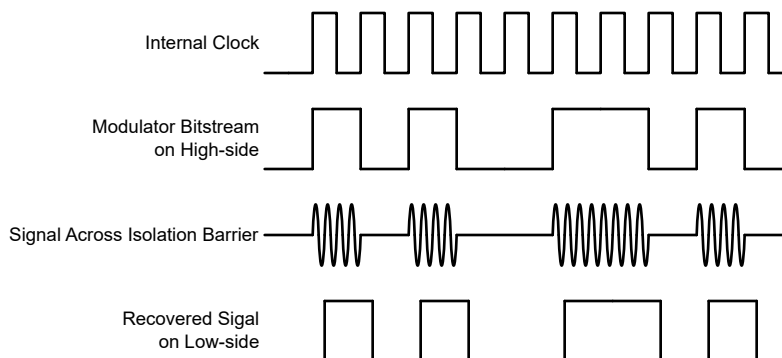

Figure 7-1. OOK-Based Modulation Scheme

7.3.3 Analog Output

The AMC1400 offers a differential analog output comprised of the OUTP and OUTN pins. For differential input voltages ($V_{INP} - V_{INN}$) in the range from –250 mV to +250 mV, the device provides a linear response with a nominal gain of 8.2. For example, for a differential input voltage of 250 mV, the differential output voltage ($V_{OUTP} - V_{OUTN}$) is 2.05 V. At zero input (INP shorted to INN), both pins output the same common-mode output voltage V_{CMout}, as specified in the *Electrical Characteristics* table. For absolute differential input voltages greater than 250 mV but less than 320 mV, the differential output voltage continues to increase in magnitude but with reduced linearity performance. The outputs saturate at a differential output voltage of $V_{CLIPout}$, as shown in Figure 7-2, if the differential input voltage exceeds the $V_{Clipping}$ value.
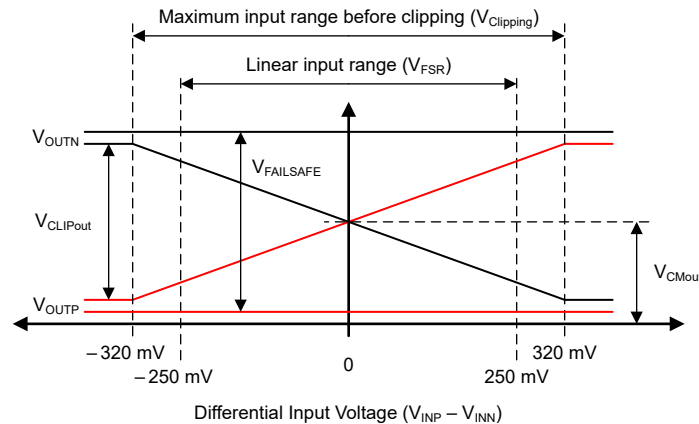
Figure 7-2. Output Behavior of the AMC1400

The AMC1400 offers a fail-safe feature that simplifies diagnostics on a system level. Figure 7-2 shows the fail-safe mode, in which the AMC1400 outputs a negative differential output voltage that does not occur under normal operating conditions. The fail-safe output is active in two cases:

• When the high-side supply is missing or below the VDD1$_{UV}$ threshold
• When the common-mode input voltage, that is $V_{CM} = (V_{INP} + V_{INN}) / 2$, exceeds the common-mode overvoltage detection level V_{CMov}

Use the maximum $V_{FAILSAFE}$ voltage specified in the *Electrical Characteristics* table as a reference value for fail-safe detection on a system level.

7.4 Device Functional Modes

The AMC1400 is operational when the power supplies VDD1 and VDD2 are applied, as specified in the *Recommended Operating Conditions* table.

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

With its stretched SOIC package, the AMC1400 is specifically designed for isolated, high precision, shunt-based current sensing in applications with 800-V and higher working voltages. This device is designed for operating in harsh environments with a high pollution degree or high altitudes.

8.2 Typical Application

Figure 8-1 depicts a simplified block diagram of a solar inverter supporting a 1000-V_{DC} string voltage where the AMC1400 is used to monitor the current on the 1200-V DC link. The output current of the boost converter flows through a shunt resistor (RSHUNT) and produces a voltage drop that is sensed by the AMC1400. The AMC1400 outputs a differential analog voltage that is proportional to the input signal and galvanically isolated from the high-voltage side. The differential output voltage is typically routed to an analog-to-digital converter (ADC) of a microcontroller (MCU) to complete the current-sensing signal chain. The AMC1411 is used in the same application for measuring the DC link voltage. Both devices share a common high-side power supply based on the SN6501 push-pull driver and a transformer that supports the desired isolation voltage ratings.

The stretched SOIC package, differential input, differential output, and the high common-mode transient immunity (CMTI) of the AMC1400 ensure reliable and accurate operation in high-noise environments while meeting IEC standards for reinforced isolation at 1 kV and higher working voltages.
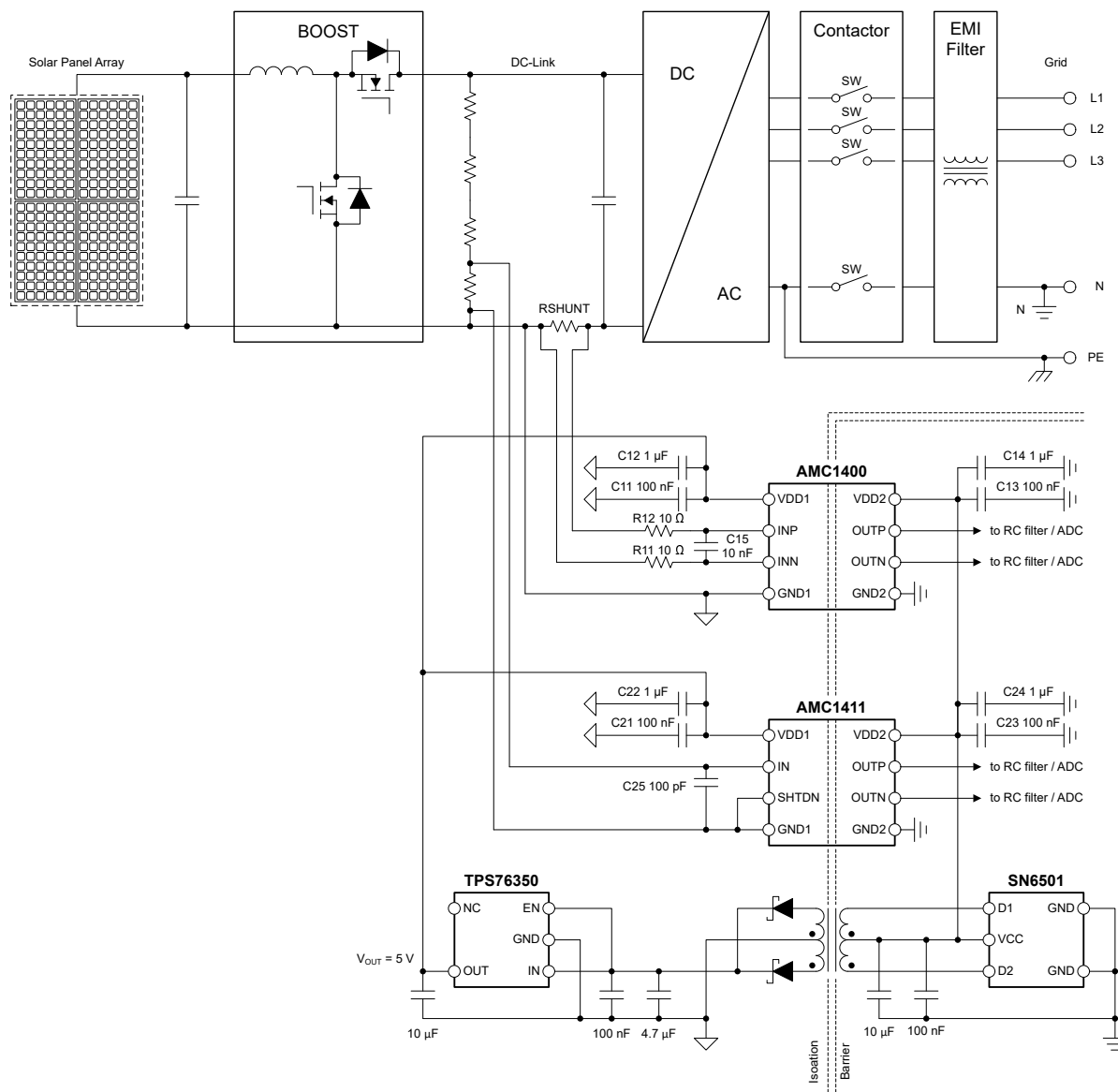
Product Folder Links: *AMC1400*

Figure 8-1. Using the AMC1400 for Current Sensing in a Typical Application

8.2.1 Design Requirements

Table 8-1 lists the parameters for this typical application.

Table 8-1. Design Requirements

PARAMETER	VALUE
DC link voltage	1200 V (maximum)
Overvoltage category	III
Pollution degree	2
Altitude	≤2000 m
High-side supply voltage	3.3 V or 5 V
Low-side supply voltage	3.3 V or 5 V
Transient peak DC link current	10 A
Nominal DC link current	4 A
Voltage drop across RSHUNT for a linear response	±250 mV (maximum)
Maximum voltage drop across RSHUNT before clipping	±320 mV (maximum)

8.2.2 Detailed Design Procedure

The value of the shunt resistor (RSHUNT) is selected such that the transient peak DC link current (10 A) produces a voltage drop across the shunt resistor that matches the linear full-scale input range of the AMC1400 (250 mV). Consider the following two restrictions when selecting the value of the shunt resistor:

- The voltage drop across the shunt caused by the nominal-rated DC link current range must not exceed the recommended differential input voltage range for a linear response: $|V_{SHUNT}| \leq |V_{FSR}|$
- The voltage drop caused by the maximum allowed overcurrent must not exceed the input voltage that causes a clipping output: $|V_{SHUNT}| \leq |V_{Clipping}|$

In this example, a 25-mΩ shunt resistor is selected (RSHUNT = 250 mV / 10 A).

At the nominal-rated current, the power dissipation in the shunt resistor is $R \times I^2 = 25$ mΩ × (4 A)^2 = 0.4 W. For surface-mounted shunts, the heat is mainly dissipated via the device terminals and the printed circuit board (PCB) traces. The power rating of a shunt is typically specified for a 70°C terminal temperature and derated for higher temperatures. This rating ensures that the shunt itself does not exceed its specified maximum operating temperature at the rated power dissipation. Careful PCB design is required not to exceed the terminal temperature at the rated power dissipation. Using wide copper traces to spread the heat over a larger area of the PCB, heat sinks, and air flow can improve the thermal design.

8.2.2.1 Input Filter Design

Place an RC filter in front of the isolated amplifier to improve the signal-to-noise performance of the signal path. Design the input filter such that:

- The cutoff frequency of the filter is at least one order of magnitude lower than the sampling frequency (20 MHz) of the ΔΣ modulator
- The input bias current does not generate a significant voltage drop across the DC impedance of the input filter
- The impedances measured from the analog inputs are equal

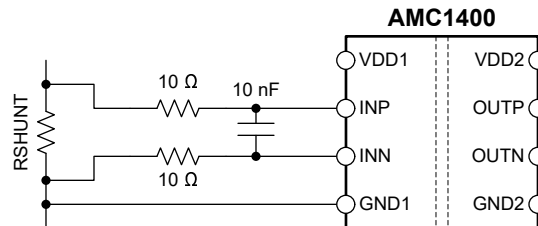For most applications, the structure shown in Figure 8-2 achieves excellent performance.

Figure 8-2. Differential Input Filter

8.2.2.2 Differential to Single-Ended Output Conversion

Figure 8-3 shows an example of a TLV9001-based signal conversion and filter circuit for systems using single-ended input ADCs to convert the analog output voltage into digital. With R1 = R2 = R3 = R4, the output voltage equals $(V_{OUTP} - V_{OUTN}) + V_{REF}$. Tailor the bandwidth of this filter stage to the bandwidth requirement of the system and use NP0-type capacitors for best performance. For most applications, R1 = R2 = R3 = R4 = 3.3 kΩ and C1 = C2 = 330 pF yields good performance.
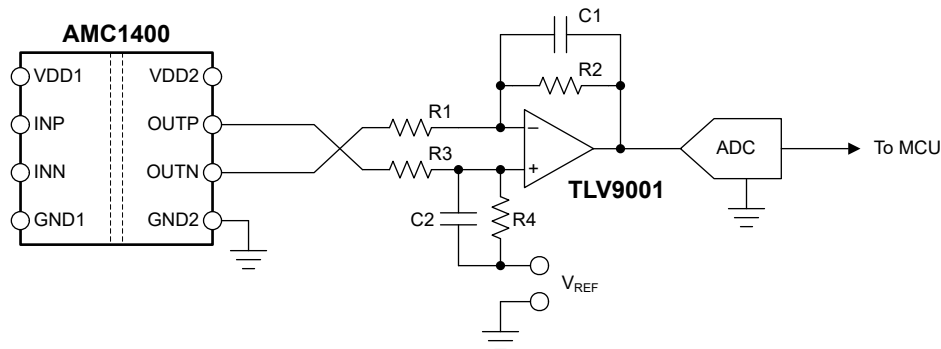
Figure 8-3. Connecting the AMC1400 Output to a Single-Ended Input ADC

For more information on the general procedure to design the filtering and driving stages of SAR ADCs, see the *18-Bit, 1MSPS Data Acquisition Block (DAQ) Optimized for Lowest Distortion and Noise* and *18-Bit Data Acquisition Block (DAQ) Optimized for Lowest Power* reference guides, available for download at www.ti.com.

8.2.3 Application Curve

One important aspect of a power-stage design is the effective detection of an overcurrent condition to protect the switching devices and passive components from damage. To power off the system quickly in the event of an overcurrent condition, a low delay caused by the isolated amplifier is required. Figure 8-4 shows the typical full-scale step response of the AMC1400.
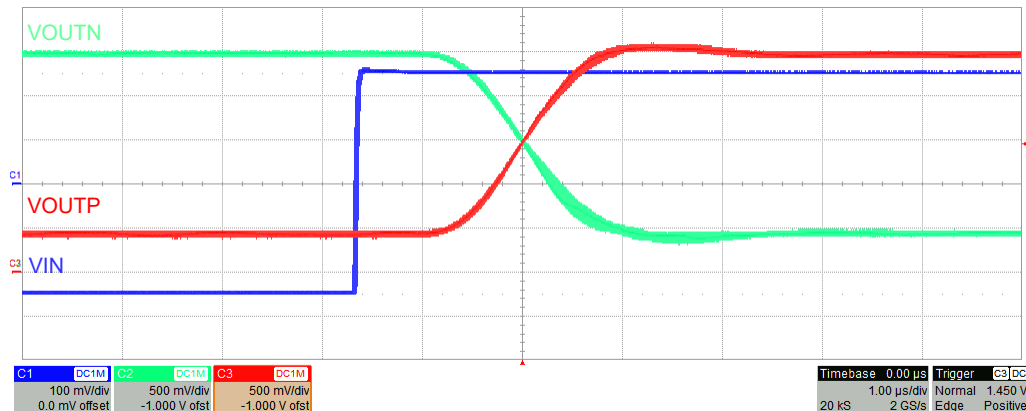

Figure 8-4. Step Response of the AMC1400

8.3 Best Design Practices

Do not leave the inputs of the AMC1400 unconnected (floating) when the device is powered up. If the device inputs are left floating, the input bias current may drive the inputs to a positive value that exceeds the operating common-mode input voltage and the output voltage may not be valid.

Connect the high-side ground (GND1) to INN, either by a hard short or through a resistive path. A DC current path between INN and GND1 is required to define the input common-mode voltage. Take care not to exceed the input common-mode range, as specified in the *Recommended Operating Conditions* table. For best accuracy, route the ground connection as a separate trace that connects directly to the shunt resistor rather than shorting GND1 to INN directly at the input to the device. See the *Layout* section for more details.

8.4 Power Supply Recommendations

The AMC1400 does not require any specific power-up sequencing. The high-side power supply (VDD1) is decoupled with a low-ESR, 100-nF capacitor (C1) parallel to a low-ESR, 1-µF capacitor (C2). The low-side power supply (VDD2) is equally decoupled with a low-ESR, 100-nF capacitor (C3) parallel to a low-ESR, 1-µF capacitor (C4). Place all four capacitors (C1, C2, C3, and C4) as close to the device as possible.

The ground reference for the high-side (GND1) is derived from the end of the shunt resistor, which is connected to the negative input (INN) of the device. For best DC accuracy, use a separate trace (as shown in Figure 8-5) to make this connection instead of shorting GND1 to INN directly at the device input. If a four-terminal shunt is used, the device inputs are connected to the inner leads and GND1 is connected to the outer lead on the INN-side of the shunt.
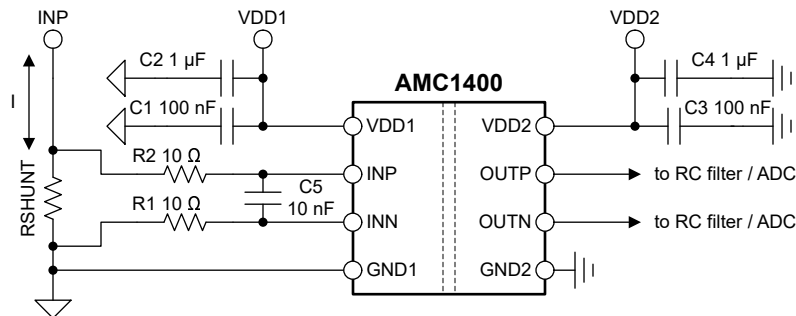

Figure 8-5. Decoupling of the AMC1400

Capacitors must provide adequate effective capacitance under the applicable DC bias conditions they experience in the application. Multilayer ceramic capacitors (MLCCs) typically exhibit only a fraction of their nominal capacitance under real-world conditions and this factor must be taken into consideration when selecting these capacitors. This problem is especially acute in low-profile capacitors, in which the dielectric field strength is higher than in taller components. Reputable capacitor manufacturers provide capacitance versus DC bias curves that greatly simplify component selection.

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Product Folder Links: *AMC1400*

8.5 Layout

8.5.1 Layout Guidelines

Figure 8-6 shows a layout recommendation with the critical placement of the decoupling capacitors (as close as possible to the AMC1400 supply pins) and placement of the other components required by the device. For best performance, place the shunt resistor close to the INP and INN inputs of the AMC1400 and keep the layout of both connections symmetrical.

The ground pin (GND1) of the AMC1400 is connected to the same end of the shunt resistor that is connected to the negative input pin (INN) of the AMC1400. If a four-pin shunt is used, the input pins (INN and INP) of the AMC1400 are connected to the inner leads, and the GND1 pin is connected to the outer lead on the INN-side of the shunt resistor. To minimize offset and improve accuracy, route the ground connection as a separate trace that connects directly to the shunt resistor rather than shorting GND1 to INN directly at the input to the device.
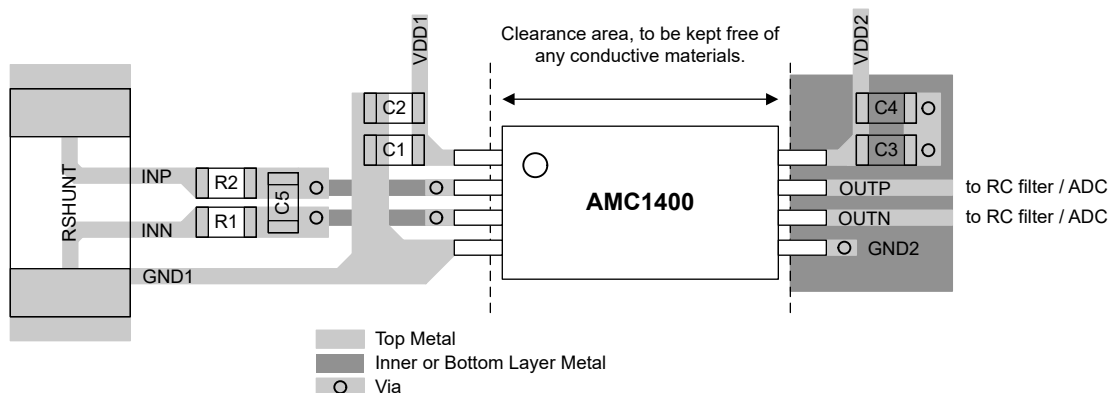
8.5.2 Layout Example

Figure 8-6. Recommended Layout of the AMC1400

9 Device and Documentation Support

9.1 Documentation Support

9.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *Isolation Glossary* application note
- Texas Instruments, *Semiconductor and IC Package Thermal Metrics* application note
- Texas Instruments, *ISO72x Digital Isolator Magnetic-Field Immunity* application note
- Texas Instruments, *TLV900x Low-Power, RRIO, 1-MHz Operational Amplifier for Cost-Sensitive Systems* data sheet
- Texas Instruments, *TPS763 Low-Power, 150-mA, Low-Dropout Linear Regulator* data sheet
- Texas Instrument, *SN6501 Transformer Driver for Isolated Power Supplies* data sheet
- Texas Instruments, *18-Bit, 1-MSPS Data Acquisition Block (DAQ) Optimized for Lowest Distortion and Noise* reference guide
- Texas Instruments, *18-Bit, 1-MSPS Data Acquisition Block (DAQ) Optimized for Lowest Power* reference guide
- Texas Instruments, *Isolated Amplifier Voltage Sensing Excel Calculator* design tool
- Texas Instruments, *Best in Class Radiated Emissions EMI Performance with the AMC1300B-Q1 Isolated Amplifier* technical white paper

9.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

9.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

9.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.6 Glossary

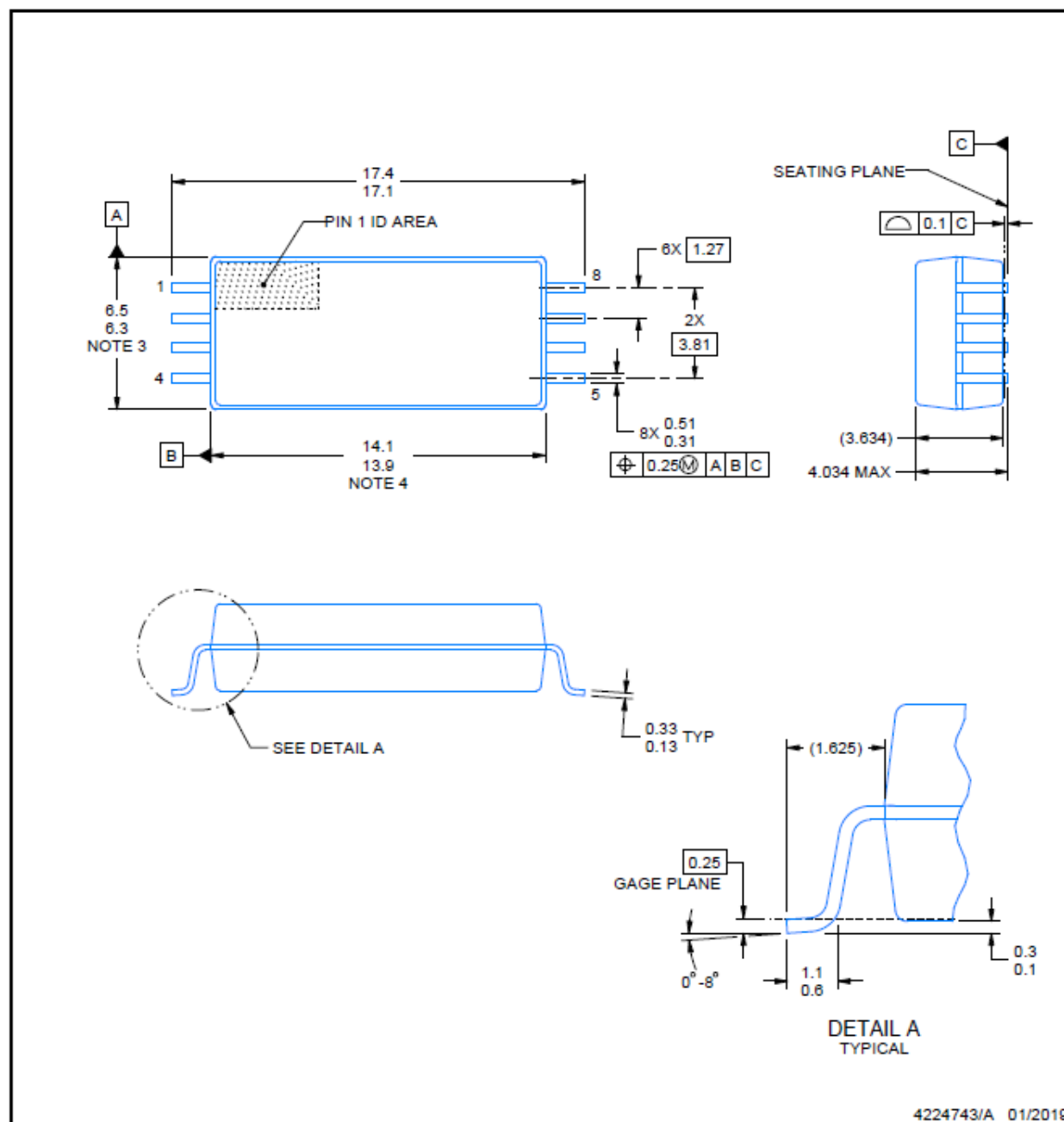TI Glossary   This glossary lists and explains terms, acronyms, and definitions.

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

10.1 Mechanical Data

DWL0008A

PACKAGE OUTLINE

SOIC - 4.034 mm max height

PLASTIC SMALL OUTLINE

PIN 1 ID AREA

17.4
17.1

A

6.5
6.3
NOTE 3

1

4

8X | 0.51
0.31

8

5

6X | 1.27

2X
3.81

⊕ | 0.25 Ⓜ | A | B | C

B

14.1
13.9
NOTE 4

C

SEATING PLANE

△ | 0.1 | C

(3.634)

4.034 MAX

SEE DETAIL A

0.33
0.13 TYP

(1.625)

0.25
GAGE PLANE

0°-8°

1.1
0.6

0.3
0.1

DETAIL A
TYPICAL

4224743/A   01/2019

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 mm per side.
4. This dimension does not include interlead flash.

Product Folder Links: *AMC1400*
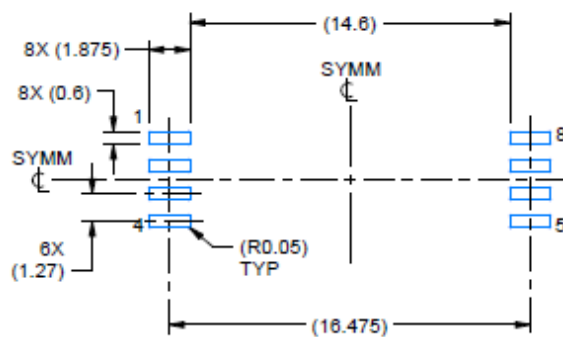
EXAMPLE BOARD LAYOUT
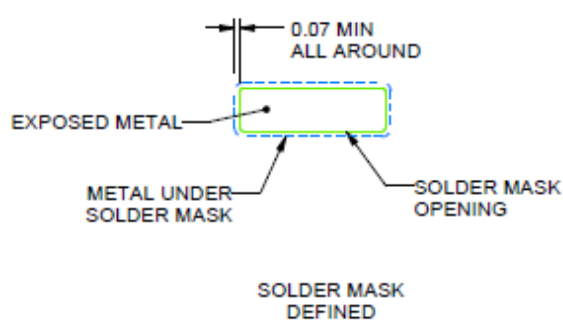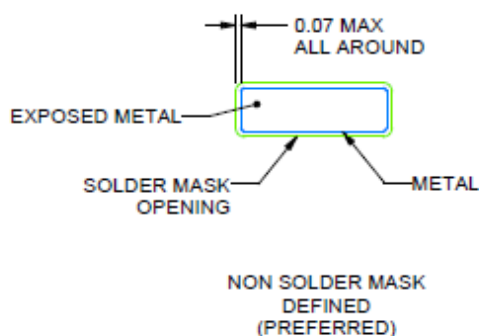
DWL0008A

SOIC - 4.034 mm max height

PLASTIC SMALL OUTLINE
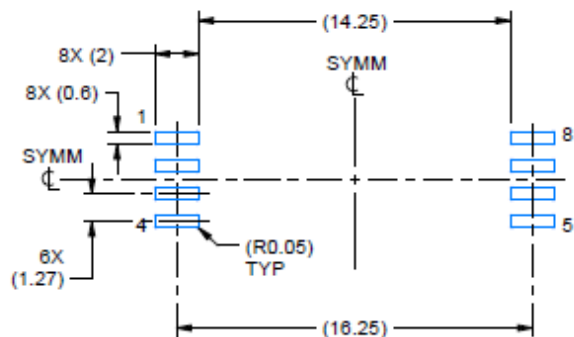
LAND PATTERN EXAMPLE
STANDARD
EXPOSED METAL SHOWN
SCALE:3X

LAND PATTERN EXAMPLE
PCB CLEARANCE & CREEPAGE OPTIMIZED
EXPOSED METAL SHOWN
SCALE:3X

SOLDER MASK DETAILS

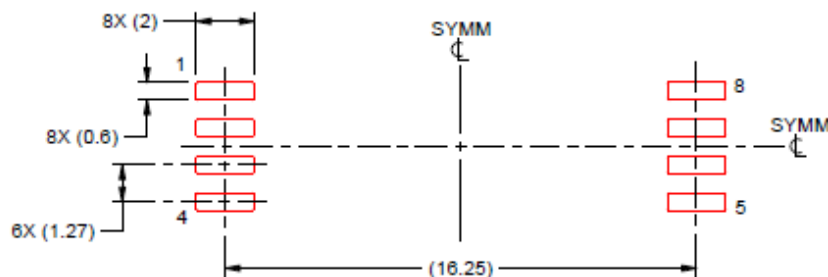4224743/A   01/2019

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DWL0008A

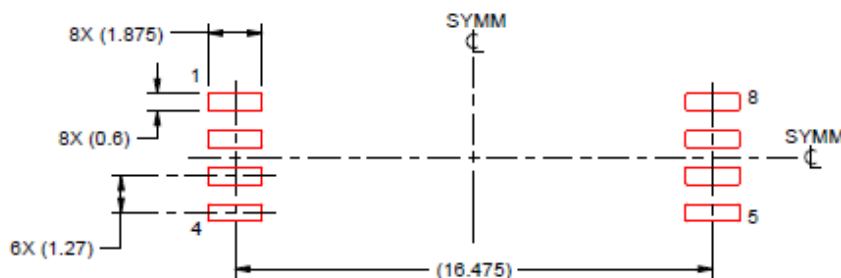### SOIC - 4.034 mm max height

PLASTIC SMALL OUTLINE

8X (2)
1
8X (0.6)
6X (1.27)
4
SYMM
SYMM
8
5
(16.25)

SOLDER PASTE EXAMPLE
STANDARD
BASED ON 0.125 mm THICK STENCIL
SCALE:4X

8X (1.875)
1
8X (0.6)
6X (1.27)
4
SYMM
SYMM
8
5
(16.475)

SOLDER PASTE EXAMPLE
PCB CLEARANCE & CREEPAGE OPTIMIZED
BASED ON 0.125 mm THICK STENCIL
SCALE:4X

4224743/A 01/2019

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

PACKAGE OPTION ADDENDUM

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
AMC1400DWLR	ACTIVE	SOIC	DWL	8	500	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	1400	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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OTHER QUALIFIED VERSIONS OF AMC1400 :

PACKAGE OPTION ADDENDUM

● Automotive : AMC1400-Q1

NOTE: Qualified Version Definitions:

  ● Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

![Texas Instruments logo] **PACKAGE MATERIALS INFORMATION**

TAPE AND REEL INFORMATION

REEL DIMENSIONS

Reel Diameter

Reel Width (W1)

TAPE DIMENSIONS

A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

Sprocket Holes

User Direction of Feed

Pocket Quadrants

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
AMC1400DWLR	SOIC	DWL	8	500	330.0	24.4	18.55	7.2	4.5	24.0	24.0	Q1

PACKAGE MATERIALS INFORMATION

TAPE AND REEL BOX DIMENSIONS

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
AMC1400DWLR	SOIC	DWL	8	500	367.0	367.0	45.0

17.4
17.1

A

PIN 1 ID AREA

1

8

6X 1.27

2X 3.81

6.5
6.3
NOTE 3

4

5

8X 0.51
0.31

B

14.1
13.9
NOTE 4

⊕ 0.25 Ⓜ A B C

C

SEATING PLANE

◯ 0.1 C

(3.634)

4.034 MAX

SEE DETAIL A

0.33
0.13 TYP

(1.625)

0.25

GAGE PLANE

0° -8°

1.1
0.6

0.3
0.1

DETAIL A
TYPICAL

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NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 mm per side.
4. This dimension does not include interlead flash.

LAND PATTERN EXAMPLE
STANDARD
EXPOSED METAL SHOWN
SCALE:3X

(14.25)

8X (2)

8X (0.6)

SYMM

1

4

5

8

SYMM

(R0.05)
TYP

6X
(1.27)

(16.25)

LAND PATTERN EXAMPLE
PCB CLEARANCE & CREEPAGE OPTIMIZED
EXPOSED METAL SHOWN
SCALE:3X

(14.6)

8X (1.875)

8X (0.6)

SYMM

1

4

5

8

SYMM

(R0.05)
TYP

6X
(1.27)

(16.475)

0.07 MAX
ALL AROUND

EXPOSED METAL

SOLDER MASK
OPENING

METAL

NON SOLDER MASK
DEFINED
(PREFERRED)

0.07 MIN
ALL AROUND

EXPOSED METAL

METAL UNDER
SOLDER MASK

SOLDER MASK
OPENING

SOLDER MASK
DEFINED

SOLDER MASK DETAILS

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NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

8X (2)

1

8X (0.6)

6X (1.27)

4

SYMM

8

SYMM

5

(16.25)

SOLDER PASTE EXAMPLE
STANDARD
BASED ON 0.125 mm THICK STENCIL
SCALE:4X

8X (1.875)

1

8X (0.6)

6X (1.27)

4

SYMM

8

SYMM

5

(16.475)

SOLDER PASTE EXAMPLE
PCB CLEARANCE & CREEPAGE OPTIMIZED
BASED ON 0.125 mm THICK STENCIL
SCALE:4X

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NOTES: (continued)

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