HARRIS SEMICONDUCTOR

HC-55536

Continuous Variable Slope Delta-Demodulator (CVSD)

March 1993

Features

- All Digital
- Requires Few External Parts
- Low Power Drain: 1.5mW from Single 3V-6V Supply
- Time Constants Determined by Clock Frequency; No Calibration or Drift Problems; Automatic Offset Adjustment
- Filter Reset by Digital Control
- Automatic Overload Recovery
- Automatic "Quiet" Pattern Generation

Applications

- Voice Decoder for Digital Systems and Speech Syntheses
- Voicemail
- Audio Manipulations; Delay Lines, Echo Generation/ Suppression, Special Effects, etc.
- Pagers/Satellites

Description

The HC-55536 is a CMOS integrated circuit used to convert serial NRZ digital data to an analog (voice) signal. Conversion is by delta demodulation, using the Continuously Variable Slope (CVSD) method of demodulation.

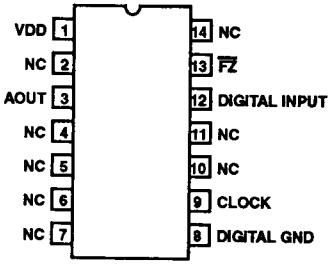
While signals are compatible with other CVSD circuits, the internal design is unique. The analog loop filters have been replaced by digital filters which use very low power and require no external timing components. This digital approach allows inclusion of many desirable features, which otherwise would be difficult to implement. The device is usable from 9Kbits/sec to above 64kbits/sec, and may be easily configured with the HC-55564 CVSD for a complete transmit/receive voice channel.

Ordering Information

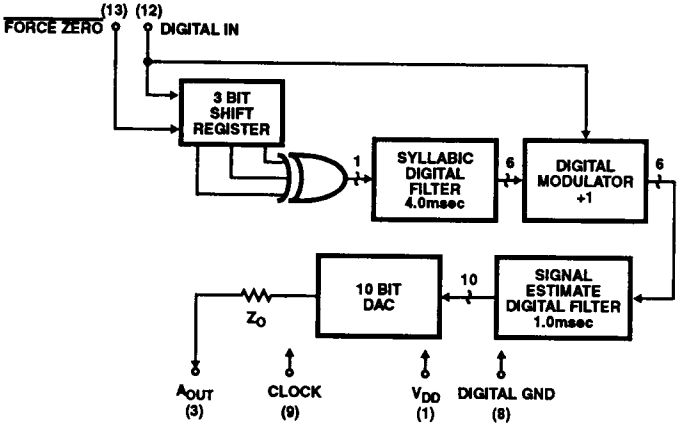
PART NUMBER	TEMPERATURE RANGE	PACKAGE
HC1-55536-5	0°C to +75°C	14 Lead Ceramic DIP
HC1-55536-9	-40°C to +85°C	14 Lead Ceramic DIP
HC3-55536-5	0°C to +75°C	14 Lead Plastic DIP
HC3-55536-9	-40°C to +85°C	14 Lead Plastic DIP

Pinout

HC-55536
(PDIP, CDIP)
TOP VIEW



Functional Diagram



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number **2888.1**

Absolute Maximum Ratings

Voltage at Any Pin ..... GND -0.3V to VDD +0.3V
Maximum V_{DD} Voltage ..... +7.0V
Junction Temperature ..... +175°C
Junction Temperature (Plastic Package) ..... +150°C
Lead Temperature (Soldering 10 Sec.) ..... +300°C

Operating Conditions

Operating Temperature Range
HC-55536-5 ..... 0°C to +75°C
HC-55536-9 ..... -40°C to +85°C
Storage Temperature Range ..... -65°C ≤ T_A ≤ +150°C
Operating V_{DD} Range ..... +3.0V to +6.0V

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Specifications V_{DD} = +5.0V; Bit Rate = 16K Bits/sec; Typical Parameters are at +25°C. Min-Max parameters are over Operating Temperature, Unless Otherwise Specified.

PARAMETERS	SYMBOL	LIMITS			UNITS	NOTES
		MIN	TYP	MAX		
Clock Sampling Rate	CLK	9	16	64	Kbps	1
Clock Duty Cycle	I_{DD}	30		70	%	
Supply Current	V_{OH}		0.3	1.5	mA	
Logic "1" Input	V_{IH}	3.5	4.5		V	2
Logic "0" Input	V_{IL}			1.5	V	2
Audio Output Voltage	A_{OUT}		0.5	1.2	V_{RMS}	3
Audio Output Impedance	Z_{OUT}		150		kΩ	4
Syllabic Filter Time Constant	t_{SF}		4.0		ms	5
Signal Estimate Filter Time Constant	t_{SE}		1.0		ms	5
Step Size Ratio	SSR		24		dB	6
Minimum Step Size	MSS		0.1		$\%V_{DD}$	7
Signal/Noise Ratio	SNR	25			dB	8
Quieting Pattern Amplitude	VQP		10		mV_{P-P}	9
Clamping Threshold	VA_{TH}		0.75		F.S.	10

NOTES:

1. There is one NRZ data bit per clock period. Clock must be phased with digital data such that a positive clock transition occurs in the middle of each received data bit. Clock may be run at greater than 64kbps or less than 9kbps.
2. Logic inputs are CMOS compatible at supply voltage and are diode protected. Digital data input is NRZ at clock rate and changes with negative clock transitions.
3. This output includes a DC bias of $V_{DD}/2$; therefore, an AC coupling capacitor is required unless the output filter also includes this bias.
4. Presents approximately 150kΩ in series with recovered audio voltage. Zero-signal reference is $V_{DD}/2$.
5. Note that filter time constants are inversely proportional to clock rate. Both filters approximate single pole responses.
6. Step size compression ratio of the syllabic filter is defined as the ratio of the filter output, with an equal 1-0 bit density input to the filter, to its minimum output.
7. The minimum audio output voltage that can be produced by the internal DAC.
8. Input signal encoded $1.2V_{RMS}$ 250Hz sinusoid.
9. The "quieting" pattern or idle-channel audio output steps at $^1/_2$ the bit rate, changing state on negative clock transitions.
10. The recovered signal will be clamped, and the computation will be inhibited, when the recovered signal reaches three-quarters of full-scale value, and will unclamp when it falls below this value (positive or negative).

Pin Description

PIN NUMBER	SYMBOL	DESCRIPTION
1	V_{DD}	Positive supply voltage.
2	NC	No internal connection is made to this pin.
3	Audio Out	Recovered audio out. Presents approximately 150kΩ source with DC offset of $V_{DD}/2$. Should be externally AC coupled.
4, 5, 6, 7	NC	No internal connection is made to these pins.
8	Digital GND	Logic Ground.
9	Clock	Sampling rote clock must be synchronized with the digital input data such that the data is valid at the positive clock transition.
10, 11	NC	No internal connection is made to these pins.
12	Digital In	Input for the received serial NRZ digital data.
13	$\overline{FZ}$	Active low logic input. Activating this input resets the internal logic and forces the recovered audio output into the "quieting" condition.
14	NC	No internal connection is made to this pin.

NOTE: No active input should be left in a "floating condition".

Die Characteristic

Transistor Count 1790
Die Dimensions ..... 147 x 82 mils
Substrate Potential ..... $+V_{DD}$
Process ..... BiMOSE

Thermal Constants (°C/W)	θ_{JA}	θ_{JC}
Ceramic DIP	70	20
Plastic DIP	85	-

Figure 1 illustrates the frequency response of the HC-55536 for varying input levels. To prevent slope overload (slew rate limiting) do not exceed the 0dB boundary. The frequency response is directly proportional to the sampling rate. The output levels were measured after filtering.

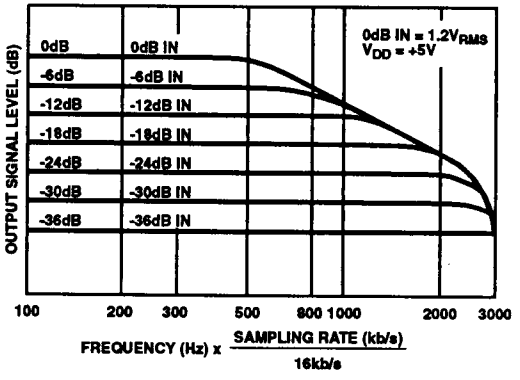
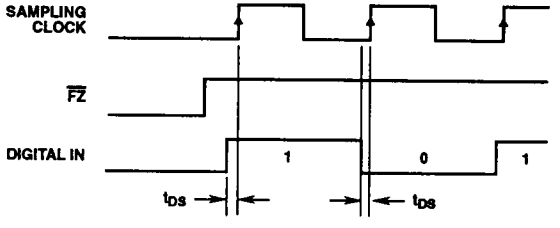


FIGURE 1. TRANSFER FUNCTION FOR CVSD AT 16kbps

Timing Waveforms

CVSD TIMING DIAGRAM



t_{DS}: DATA SET UP TIME 100ns TYPICAL