

MM54C83/MM74C83 4-Bit Binary Full Adder

General Description

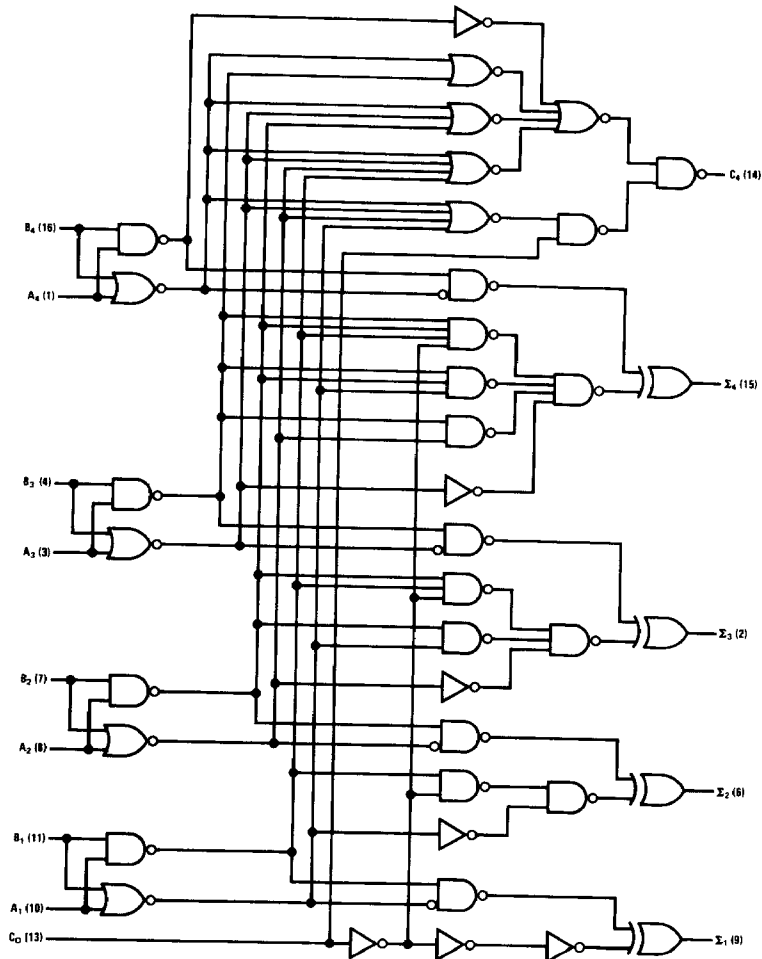
The MM54C83/MM74C83 4-bit binary full adder performs the addition of two 4-bit binary numbers. A carry input (C_0) is included and the sum (Σ) outputs are provided for each bit and the resultant carry (C_4) is obtained from the fourth bit. Since the carry-ripple-time is the limiting delay in the addition of a long word length, carry look-ahead circuitry has been included in the design to minimize this delay. Also, the logic levels of the input and output, including the carry, are in their true form. Thus, the end-around carry is accomplished without the need for level inversion.

Features

- Wide supply voltage range
- Guaranteed noise margin
- High noise immunity
- Low power
- TTL compatibility
- Fast carry ripple (C_0 to C_4)
- Fast summing (Σ_{IN} to Σ_{OUT})

3V to 15V
1V
0.45 V_{CC} (typ.)
fan out of 2
driving 74L
50 ns (typ.) at $V_{CC} = 10V$
and $C_L = 50$ pF
125 ns (typ.) at $V_{CC} = 10V$
and $C_L = 50$ pF

Logic Diagram



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Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Voltage at Any Pin	-0.3V to $V_{CC} + 0.3V$
Operating Temperature Range (T_A)	
MM54C83	-55°C to +125°C
MM74C83	-40°C to +85°C
Storage Temperature Range (T_S)	-65°C to +150°C

Power Dissipation (P_D)	
Dual-In-Line	700 mW
Small Outline	500 mW
Operating V_{CC} Range	3V to 15V
Absolute Maximum V_{CC}	18V
Lead Temperature (T_L)	
(Soldering, 10 seconds)	260°C

DC Electrical Characteristics Min/Max limits apply across temperature range unless otherwise noted

Symbol	Parameter	Conditions	Min	Typ	Max	Units
CMOS TO CMOS						
$V_{IN(1)}$	Logical "1" Input Voltage	$V_{CC} = 5V$ $V_{CC} = 10V$	3.5 8.0			V V
$V_{IN(0)}$	Logical "0" Input Voltage	$V_{CC} = 5V$ $V_{CC} = 10V$			1.5 2.0	V V
$V_{OUT(1)}$	Logical "1" Output Voltage	$V_{CC} = 5V, I_O = -10 \mu A$ $V_{CC} = 10V, I_O = -10 \mu A$	4.5 9.0			V V
$V_{OUT(0)}$	Logical "0" Output Voltage	$V_{CC} = 5V, I_O = 10 \mu A$ $V_{CC} = 10V, I_O = 10 \mu A$			0.5 1.0	V V
$I_{IN(1)}$	Logical "1" Input Current	$V_{CC} = 15V, V_{IN} = 15V$		0.005	1.0	μA
$I_{IN(0)}$	Logic "0" Input Current	$V_{CC} = 15V, V_{IN} = 0V$	-1.0	-0.005		μA
I_{CC}	Supply Current	$V_{CC} = 15V$		0.05	300	μA

CMOS/LPTTL INTERFACE

$V_{IN(1)}$	Logical "1" Input Voltage	54C, $V_{CC} = 4.5V$ 74C, $V_{CC} = 4.75V$	$V_{CC} - 1.5$ $V_{CC} - 1.5$			V V
$V_{IN(0)}$	Logical "0" Input Voltage	54C, $V_{CC} = 4.5V$ 74C, $V_{CC} = 4.75V$			0.8 0.8	V V
$V_{OUT(1)}$	Logical "1" Output Voltage	54C, $V_{CC} = 4.5V, I_O = -360 \mu A$ 74C, $V_{CC} = 4.75V, I_O = -360 \mu A$	2.4 2.4			V V
$V_{OUT(0)}$	Logical "0" Output Voltage	54C, $V_{CC} = 4.5V, I_O = 360 \mu A$ 74C, $V_{CC} = 4.75V, I_O = 360 \mu A$			0.4 0.4	V V

OUTPUT DRIVE (See 54C/74C Family Characteristics Data Sheet) (short circuit current)

I_{SOURCE}	Output Source Current (P-Channel)	$V_{CC} = 5V, V_{OUT} = 0V$ $T_A = 25^\circ C$	-1.75	-3.3		mA
I_{SOURCE}	Output Source Current (P-Channel)	$V_{CC} = 10V, V_{OUT} = 0V$ $T_A = 25^\circ C$	-8.0	-15		mA
I_{SINK}	Output Sink Current (N-Channel)	$V_{CC} = 5V, V_{OUT} = V_{CC}$ $T_A = 25^\circ C$	1.75	3.6		mA
I_{SINK}	Output Sink Current (N-Channel)	$V_{CC} = 10V, V_{OUT} = V_{CC}$ $T_A = 25^\circ C$	8.0	16		mA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

AC Electrical Characteristics* $T_A = 25^\circ\text{C}$, $C_L = 50\text{ pF}$, unless otherwise specified

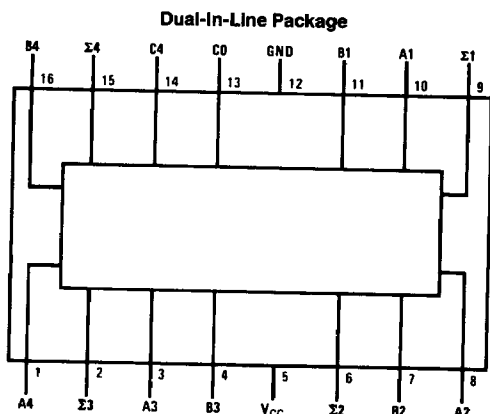
Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{pd1}	Propagation Delay from C_0 to C_4	$V_{CC} = 5\text{V}$ $V_{CC} = 10\text{V}$		120 50	200 80	ns ns
t_{pd1}	Propagation Delay from Sum Inputs to C_4	$V_{CC} = 5\text{V}$ $V_{CC} = 10\text{V}$		250 90	450 150	ns ns
t_{pd1}	Propagation Delay from C_0 to Sum Outputs	$V_{CC} = 5\text{V}$ $V_{CC} = 10\text{V}$		350 125	550 200	ns ns
t_{pd1}	Propagation Delay from Sum Inputs to Sum Outputs	$V_{CC} = 5\text{V}$ $V_{CC} = 10\text{V}$		300 90	550 150	ns ns
C_{IN}	Input Capacitance	Any Input (Note 2)		5		pF
C_{PD}	Power Dissipation Capacitance	Per Package (Note 3)		120		pF

*AC Parameters are guaranteed by DC correlated testing.

Note 2: Capacitance is guaranteed by periodic testing.

Note 3: C_{PD} determines the no load AC power consumption of any CMOS device. For complete explanation see 54C/74C Family Characteristics Application Note—AN-90.

Connection Diagram

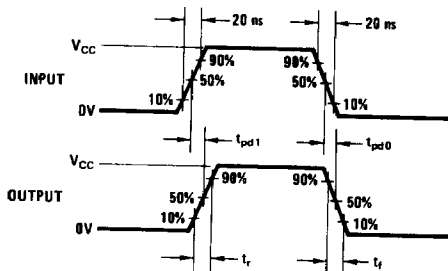


TL/F/6035-2

Order Number MM54C83* or MM74C83*

*Please look into Section 8, Appendix D for availability of various package types.

Switching Time Waveforms



TL/F/6035-3

Inputs must be tied to appropriate logic level.

