National Semiconductor

October 2002

LM4820-6 Boomer® Audio Power Amplifier Series
Fixed Gain 1 Watt Audio Power Amplifier

General Description

The LM4820-6 is an audio power amplifier primarily designed for demanding applications in mobile phones and other portable communication device applications. It is capable of delivering 1 watt of continuous average power to an 8Ω BTL load with less than 1% distortion (THD+N) at 6dB of BTL gain from a $5V_{DC}$ power supply.

Boomer audio power amplifiers were designed specifically to provide high quality output power with a minimal amount of external components. The LM4820-6 does not require input and gain resistors, output coupling capacitors or bootstrap capacitors, and therefore is ideally suited for mobile phone and other low voltage applications where minimal parts count and low power consumption is a primary requirement.

The LM4820-6 features a low-power consumption shutdown mode, which is achieved by driving the shutdown pin with logic low. Additionally, the LM4820-6 features an internal thermal shutdown protection mechanism.

The LM4820-6 contains advanced pop & click circuitry which eliminates noises which would otherwise occur during turn-on and turn-off transitions.

Key Specifications

■ Improved PSRR at 217Hz	62dB
■ Power Output at 5.0V & 1% THD	1.0W(typ.)
■ Power Output at 3.3V & 1% THD	400mW(typ.)
■ Shutdown Current	0.1μA(typ.)

Features

- Fixed 6dB BTL voltage gain
- Available in space-saving packages micro SMD, MSOP and SOIC
- Ultra low current shutdown mode
- Can drive capacitive loads up to 500 pF
- Improved pop & click circuitry eliminates noises during turn-on and turn-off transitions
- 2.0 - 5.5V operation
- No output coupling capacitors, snubber networks or bootstrap capacitors required
- External gain configuration still possible

Applications

- Mobile Phones
- PDAs
- Portable electronic devices

Typical Application

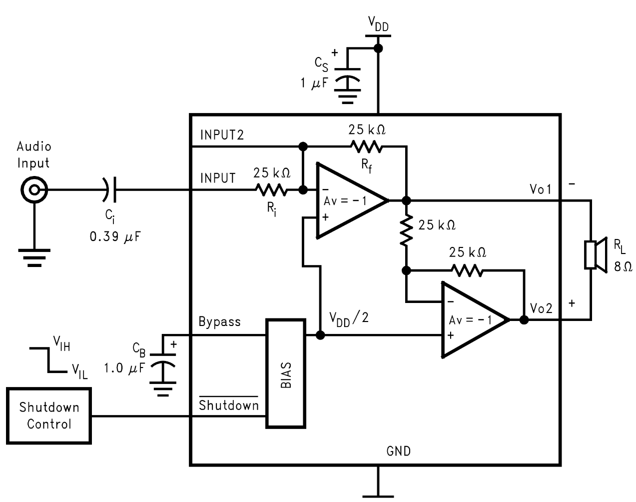

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FIGURE 1. Typical Audio Amplifier Application Circuit

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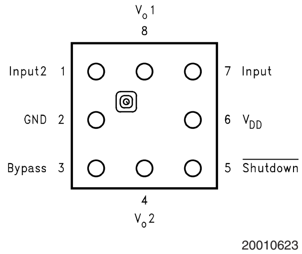
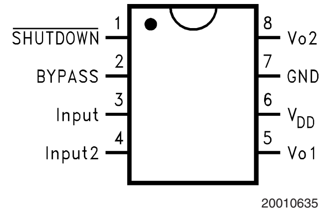
Connection Diagrams

8 Bump micro SMD



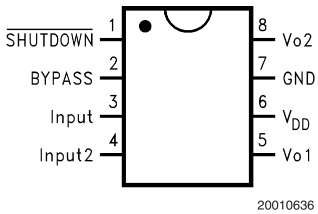
Top View
Order Number LM4820IBP-6, LM4820IBPX-6
See NS Package Number BPA08DDB

Small Outline (SO) Package



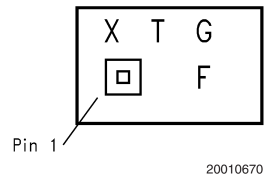
Top View
Order Number LM4820M-6
See NS Package Number M08A

Mini Small Outline (MSOP) Package



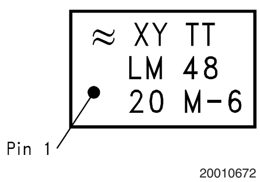
Top View
Order Number LM4820MM-6
See NS Package Number MUA08A

micro SMD Marking



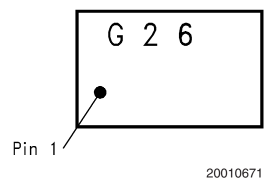
Top View
X - Date Code
T - Die Traceability
G - Boomer Family
F - LM4820IBP-6

SO Marking



Top View
XY - Date Code
TT - Die Traceability
Bottom 2 lines - Part Number (LM4820M-6)

MSOP Marking



Top View
G- Boomer Family
26 - LM4820MM-6

Absolute Maximum Ratings (Note 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage	6.0V
Storage Temperature	−65˚C to +150˚C
Input Voltage	−0.3V to V_{DD} +0.3V
Power Dissipation (Note 3)	Internally Limited
ESD Susceptibility (Note 4)	2500V
ESD Susceptibility (Note 5)	250V
Junction Temperature	150˚C
Thermal Resistance	
θ_{JC} (SO)	35˚C/W
θ_{JA} (SO)	150˚C/W
θ_{JA} (micro SMD)	220˚C/W
θ_{JC} (MSOP)	56˚C/W
θ_{JA} (MSOP)	190˚C/W

Soldering Information

See AN-1112 "microSMD Wafers Level Chip Scale Package".

Operating Ratings

Temperature Range	
$T_{MIN} \leq T_A \leq T_{MAX}$	$-40˚C \leq T_A \leq 85˚C$
Supply Voltage	$2.0V \leq V_{DD} \leq 5.5V$

Electrical Characteristics V_{DD} = 5V (Notes 1, 2, 8)

The following specifications apply for V_{DD} = 5V, A_V = 1, and 8Ω load unless otherwise specified. Limits apply for T_A = 25˚C.

Symbol	Parameter	Conditions	LM4820-6		Units
			Typical	Limit	
			(Note 6)	(Note 7)	
I_{DD}	Quiescent Power Supply Current	V_{IN} = 0V, I_o = 0A	4	10	mA (max)
I_{SD}	Shutdown Current	$V_{\overline{shutdown}}$ = GND	0.1		µA (max)
P_o	Output Power	THD = 2% (max); f = 1 kHz	1		W
THD+N	Total Harmonic Distortion+Noise	P_o = 0.4 Wrms; f = 1kHz	0.1		%
PSRR	Power Supply Rejection Ratio	V_{ripple} = 200mV sine p-p	62 (f = 217Hz) 66 (f = 1kHz)		dB
A_V	Fixed Voltage Gain	1.41V_{in} rms, R_L = 8Ω	6.0	6.5 5.5	dB Max dB Min

Electrical Characteristics V_{DD} = 3.3V (Notes 1, 2, 8)

The following specifications apply for V_{DD} = 3.3V, A_V = 1, and 8Ω load unless otherwise specified. Limits apply for T_A = 25˚C.

Symbol	Parameter	Conditions	LM4820-6		Units
			Typical	Limit	
			(Note 6)	(Note 7)	
I_{DD}	Quiescent Power Supply Current	V_{IN} = 0V, I_o = 0A	3.5		mA (max)
I_{SD}	Shutdown Current	$V_{\overline{shutdown}}$ = GND	0.1		µA (max)
P_o	Output Power	THD = 1% (max); f = 1kHz	0.4		W
THD+N	Total Harmonic Distortion+Noise	P_o = 0.15Wrms; f = 1kHz	0.1		%
PSRR	Power Supply Rejection Ratio	V_{ripple} = 200mV sine p-p	60 (f = 217Hz) 62 (f = 1kHz)		dB
A_V	Fixed Voltage Gain	.7V_{in} rms, R_L = 8Ω	6.0		dB

Electrical Characteristics V_{DD} = 2.6V (Notes 1, 2, 8)

The following specifications apply for V_{DD} = 2.6V and 8Ω Load unless otherwise specified. Limits apply for T_A = 25˚C.

Symbol	Parameter	Conditions	LM4820-6		Units
			Typical	Limit	
			(Note 6)	(Note 7)	
I_{DD}	Quiescent Power Supply Current	V_{IN} = 0V, I_o = 0A	2.6		mA (max)
I_{SD}	Shutdown Current	$V_{\overline{shutdown}}$ = GND	0.1		µA (max)

Electrical Characteristics V_{DD} = 2.6V (Notes 1, 2, 8)

The following specifications apply for V_{DD} = 2.6V and 8Ω Load unless otherwise specified. Limits apply for T_A = 25˚C. (Continued)

Symbol	Parameter	Conditions	LM4820-6		Units
			Typical	Limit	
			(Note 6)	(Note 7)	
P_o	Output Power (8Ω) Output Power (4Ω)	THD = 1% (max); f = 1 kHz THD = 1% (max); f = 1 kHz	0.2 0.4		W W
THD+N	Total Harmonic Distortion+Noise	P_o = 0.1Wrms; f = 1kHz	0.08		%
PSRR	Power Supply Rejection Ratio	V_{ripple} = 200mV sine p-p	44 (f = 217Hz) 44 (f = 1kHz)		dB
A_V	Fixed Voltage Gain	.5V_{in} rms, R_L = 8Ω	6.0		dB

Note 1: All voltages are measured with respect to the ground pin, unless otherwise specified.

Note 2: *Absolute Maximum Ratings* indicate limits beyond which damage to the device may occur. *Operating Ratings* indicate conditions for which the device is functional, but do not guarantee specific performance limits. *Electrical Characteristics* state DC and AC electrical specifications under particular test conditions which guarantee specific performance limits. This assumes that the device is within the Operating Ratings. Specifications are not guaranteed for parameters where no limit is given, however, the typical value is a good indication of device performance.

Note 3: The maximum power dissipation must be derated at elevated temperatures and is dictated by T_{JMAX}, θ_{JA}, and the ambient temperature T_A. The maximum allowable power dissipation is $P_{DMAX} = (T_{JMAX}-T_A)/\theta_{JA}$ or the number given in Absolute Maximum Ratings, whichever is lower. For the LM4820-6, see power derating curves for additional information.

Note 4: Human body model, 100 pF discharged through a 1.5 kΩ resistor.

Note 5: Machine Model, 220 pF–240 pF discharged through all pins.

Note 6: Typicals are measured at 25˚C and represent the parametric norm.

Note 7: Limits are guaranteed to National's AOQL (Average Outgoing Quality Level).

Note 8: For micro SMD only, shutdown current is measured in a Normal Room Environment. Exposure to direct sunlight will increase I_{SD} by a maximum of 2μA.

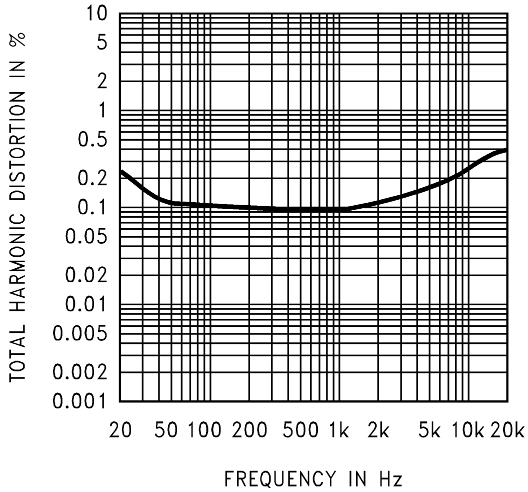
External Components Description

(*Figure 1*)

Components		Functional Description
2.	C_i	Input coupling capacitor which blocks the DC voltage at the amplifiers input terminals. Also creates a highpass filter with R_i at $f_c = 1/(2\pi R_iC_i)$. Refer to the section, **Proper Selection of External Components**, for an explanation of how to determine the value of C_i.
4.	C_S	Supply bypass capacitor which provides power supply filtering. Refer to the **Power Supply Bypassing** section for information concerning proper placement and selection of the supply bypass capacitor.
5.	C_B	Bypass pin capacitor which provides half-supply filtering. Refer to the section, **Proper Selection of External Components**, for information concerning proper placement and selection of C_B.

Typical Performance Characteristics

THD+N vs Frequency
at V_{DD} = 5V, 8Ω R_L, and PWR = 250mW



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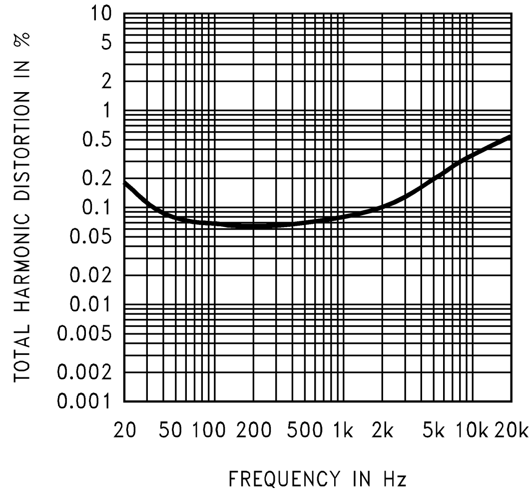
THD+N vs Frequency
at V_{DD} = 3.3V, 8Ω R_L, and PWR = 150mW



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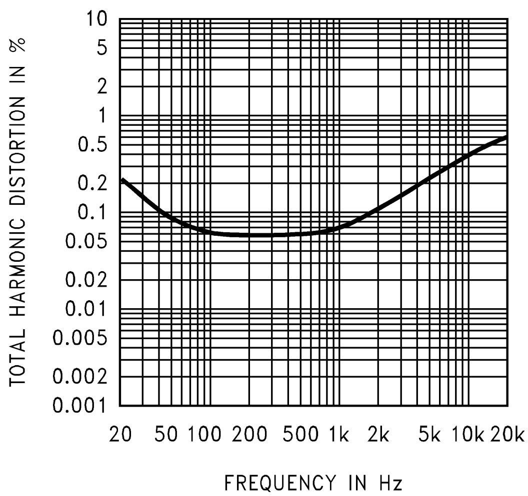
THD+N vs Frequency
at V_{DD} = 2.6V, 8Ω R_L, and PWR = 100mW



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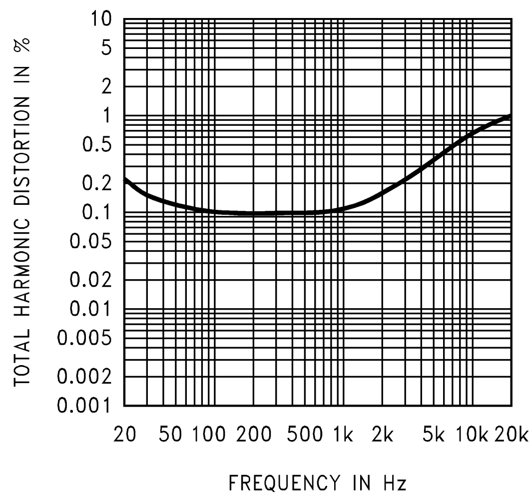
THD+N vs Frequency
at V_{DD} = 2.6V, 4Ω R_L, and PWR = 100mW



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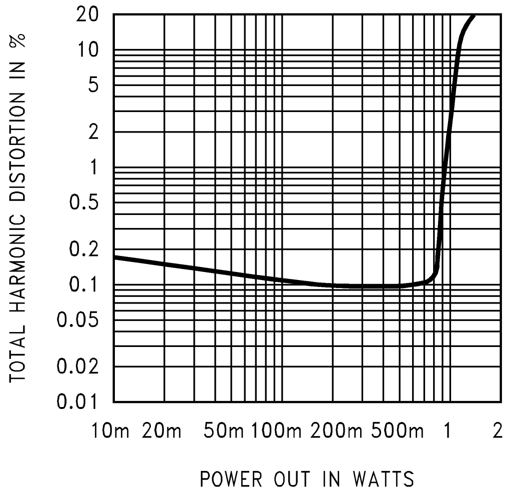
Typical Performance Characteristics (Continued)

THD+N vs Power Out
@ V_{DD} = 5V, 8Ω R_L, 1kHz



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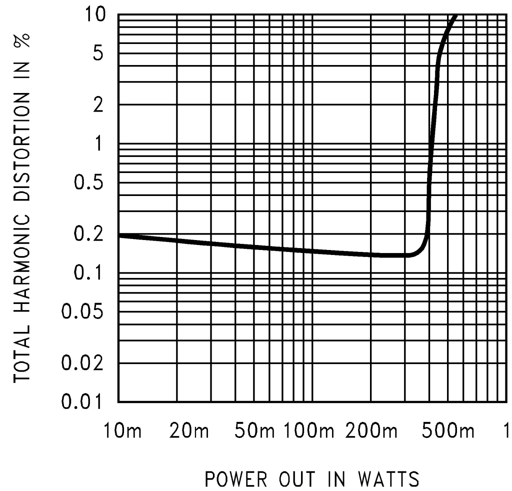
THD+N vs Power Out
@ V_{DD} = 3.3V, 8Ω R_L, 1kHz



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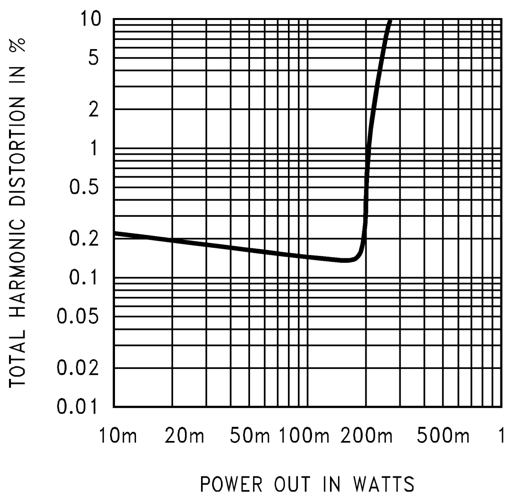
THD+N vs Power Out
@ V_{DD} = 2.6V, 8Ω R_L, 1kHz



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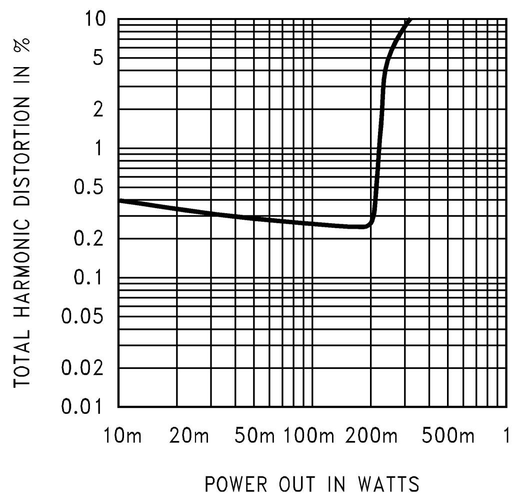
THD+N vs Power Out
@ V_{DD} = 2.6V, 4Ω R_L, 1kHz



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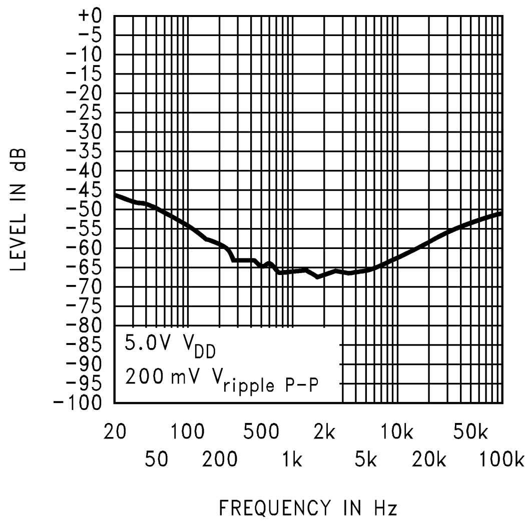
Typical Performance Characteristics (Continued)

Power Supply Rejection Ratio (PSRR) @ V_{DD} = 5V



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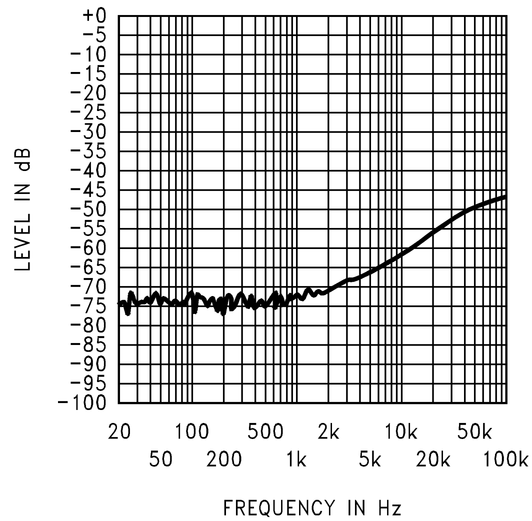
Input terminated with 10Ω R

Power Supply Rejection Ratio (PSRR) @ V_{DD} = 5V



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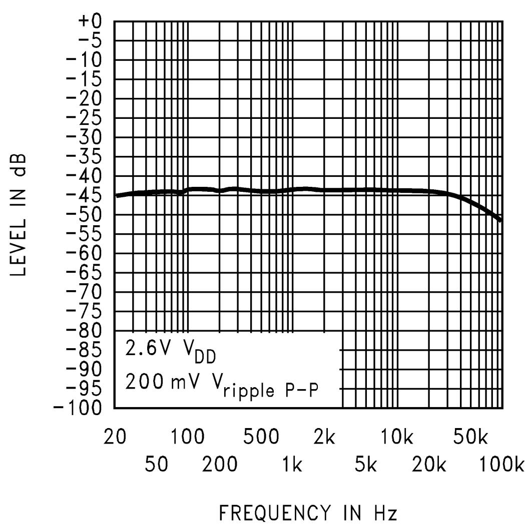
Input Floating

Power Supply Rejection Ratio (PSRR) @ V_{DD} = 2.6V



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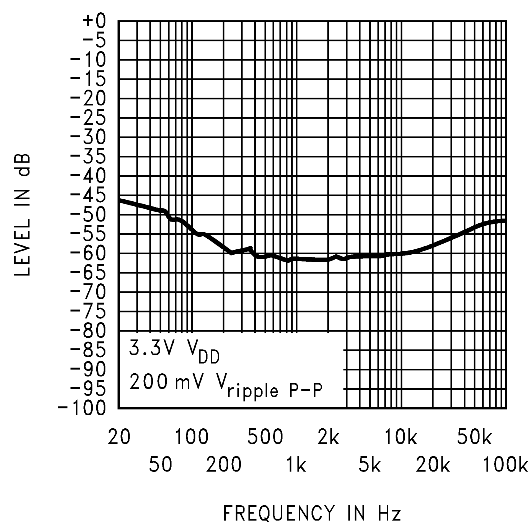
Input terminated with 10Ω R

Power Supply Rejection Ratio (PSRR) @ V_{DD} = 3.3V



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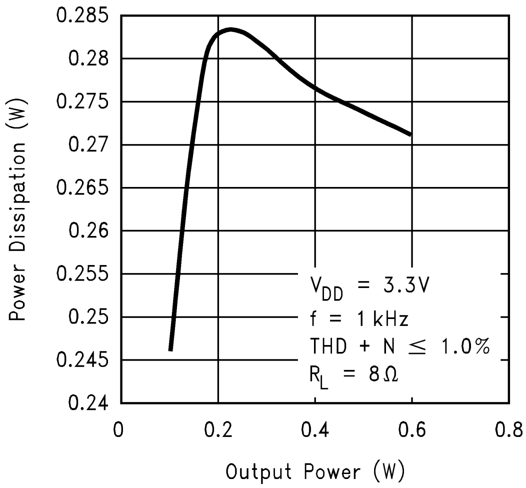
Input terminated with 10Ω R

Typical Performance Characteristics (Continued)

Power Dissipation vs Output Power V_{DD} = 3.3V



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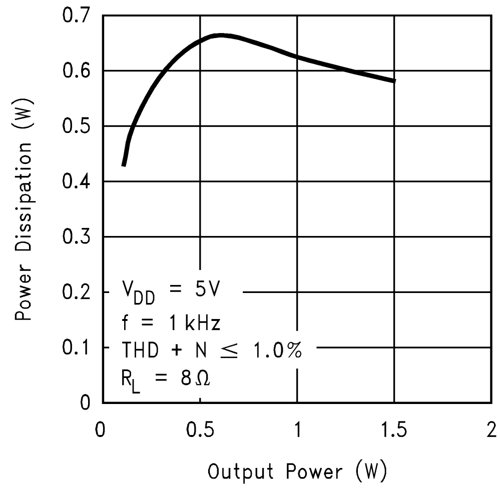
Power Dissipation vs Output Power @ V_{DD} = 5V



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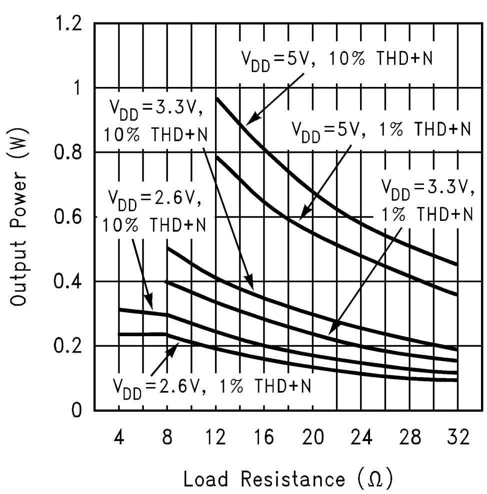
Output Power vs Load Resistance



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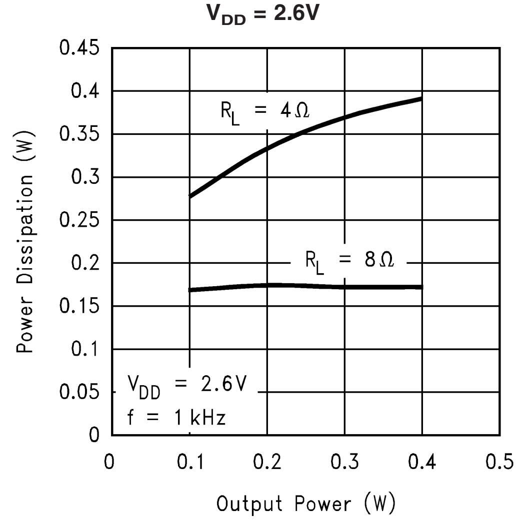
Power Dissipation vs Output Power V_{DD} = 2.6V



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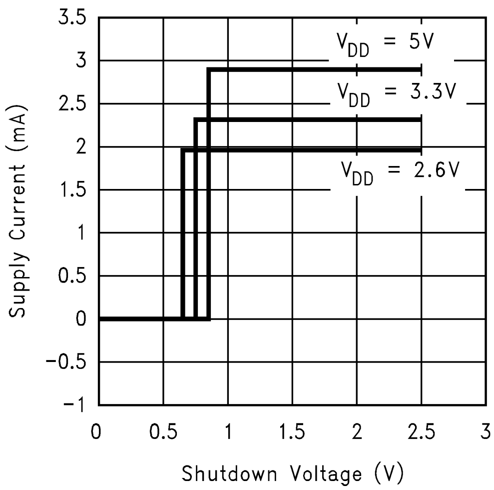
Typical Performance Characteristics (Continued)

Supply Current vs Shutdown Voltage



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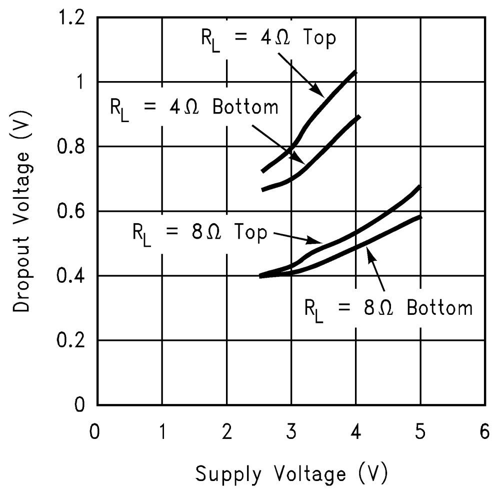
Clipping (Dropout) Voltage vs Supply Voltage



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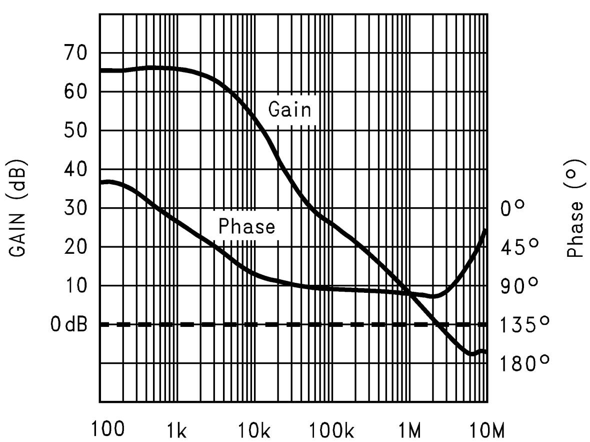
Open Loop Frequency Response



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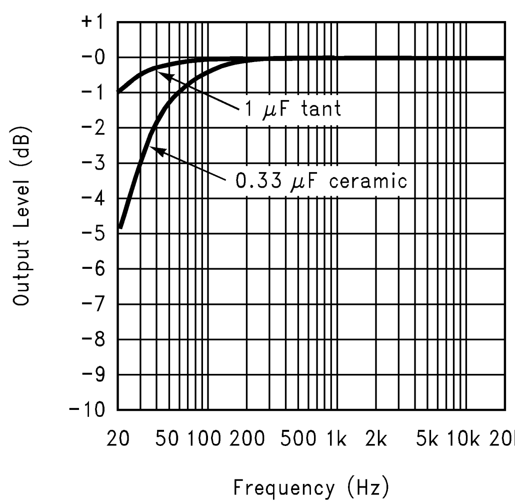
Frequency Response vs Input Capacitor Size



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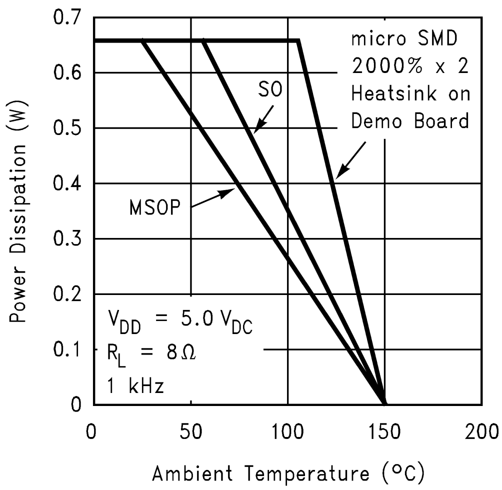
Typical Performance Characteristics (Continued)

Power Derating Curves



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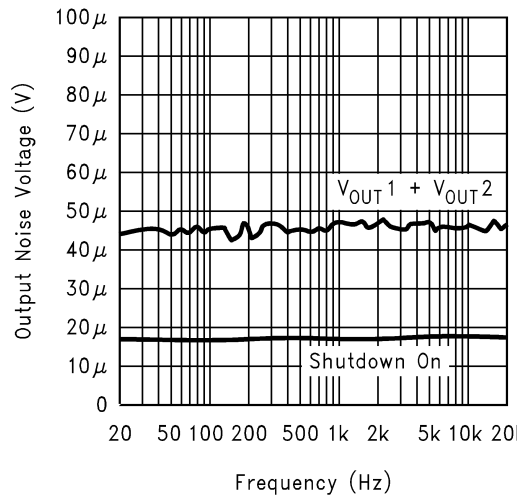
Noise Floor



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Application Information

BRIDGE CONFIGURATION EXPLANATION

As shown in *Figure 1*, the LM4820-6 has two operational amplifiers internally. *Figure 1* shows that the output of amplifier one serves as the input to amplifier two which results in both amplifiers producing signals identical in magnitude, but out of phase by 180˚. Consequently, the differential gain for the IC is

$$A_{VD} = 2 * (R_f/R_i) \quad (1)$$

By driving the load differentially through outputs Vo1 and Vo2, an amplifier configuration commonly referred to as “bridged mode” is established. Bridged mode operation is different from the classical single-ended amplifier configuration where one side of the load is connected to ground.

A bridge amplifier design has a few distinct advantages over the single-ended configuration, as it provides differential drive to the load, thus doubling output swing for a specified supply voltage. Four times the output power is possible as compared to a single-ended amplifier under the same conditions. This increase in attainable output power assumes that the amplifier is not current limited or clipped. In order to choose an amplifier’s closed-loop gain without causing excessive clipping, please refer to the **Audio Power Amplifier Design** section.

A bridge configuration, such as the one used in LM4820-6, also creates a second advantage over single-ended amplifiers. Since the differential outputs, Vo1 and Vo2, are biased at half-supply, no net DC voltage exists across the load. This eliminates the need for an output coupling capacitor which is required in a single supply, single-ended amplifier configuration. Without an output coupling capacitor, the half-supply bias across the load would result in both increased internal IC power dissipation and also possible loudspeaker damage.

POWER DISSIPATION

Power dissipation is a major concern when designing a successful amplifier, whether the amplifier is bridged or single-ended. A direct consequence of the increased power delivered to the load by a bridge amplifier is an increase in internal power dissipation. Since the LM4820-6 has two operational amplifiers in one package, the maximum internal power dissipation is 4 times that of a single-ended amplifier. The maximum power dissipation for a given application can be derived from the power dissipation graphs or from Equation 2.

$$P_{DMAX} = 4*(V_{DD})^2/(2\pi^2 R_L) \quad (2)$$

It is critical that the maximum junction temperature T_{JMAX} of 150˚C is not exceeded. T_{JMAX} can be determined from the power derating curves by using P_{DMAX} and the PC board foil area. By adding additional copper foil, the thermal resistance of the application can be reduced from a free air value of 150˚C/W, resulting in higher P_{DMAX}. Additional copper foil can be added to any of the leads, bumps or vias connected to the LM4820-6. It is especially effective when connected to V_{DD}, G_{ND}, and the output pins. Refer to the application information on the LM4820-6 reference design board for an example of good heat sinking. If T_{JMAX} still exceeds 150˚C, then additional changes must be made. These changes can include reduced supply voltage, higher load impedance, or reduced ambient temperature. Internal power dissipation is a function of output power. Refer to the **Typical Performance Characteristics** curves for power dissipation information for different output powers and output loading.

POWER SUPPLY BYPASSING

As with any amplifier, proper supply bypassing is critical for low noise performance and high power supply rejection. The capacitor location on both the bypass and power supply pins should be as close to the device as possible. Typical applications employ a 5V regulator with 10 µF tantalum or electrolytic capacitor and a ceramic bypass capacitor which aid in supply stability. This does not eliminate the need for bypassing the supply nodes of the LM4820-6. The selection of a bypass capacitor, especially C_B, is dependent upon PSRR requirements, click and pop performance (as explained in the section, **Proper Selection of External Components**), system cost, and size constraints.

SHUTDOWN FUNCTION

In order to reduce power consumption while not in use, the LM4820-6 contains a shutdown pin to externally turn off the amplifier’s bias circuitry. This shutdown feature turns the amplifier off when a logic low is placed on the shutdown pin. By switching the shutdown pin to ground, the LM4820-6 supply current draw will be minimized in idle mode. While the device will be disabled with shutdown pin voltages less than $0.5V_{DC}$, the idle current may be greater than the typical value of 0.1µA. (Idle current is measured with the shutdown pin grounded).

In many applications, a microcontroller or microprocessor output is used to control the shutdown circuitry to provide a quick, smooth transition into shutdown. Another solution is to use a single-pole, single-throw switch in conjunction with an external pull-up resistor. When the switch is closed, the shutdown pin is connected to ground and disables the amplifier. If the switch is open, then the external pull-up resistor will enable the LM4820-6. This scheme guarantees that the shutdown pin will not float thus preventing unwanted state changes.

PROPER SELECTION OF EXTERNAL COMPONENTS

Proper selection of external components in applications using integrated power amplifiers is critical to optimize device and system performance. While the LM4820-6 is tolerant of external component combinations, consideration to component values must be used to maximize overall system quality.

The LM4820-6 is unity-gain stable which gives the designer maximum system flexibility. The LM4820-6 at 6dB of fixed gain is a low gain configuration which minimizes THD+N values, and maximizes the signal to noise ratio. Low gain configurations require large input signals to obtain a given output power. Input signals equal to or greater than 1 Vrms are available from sources such as audio codecs. Please refer to the section, **Audio Power Amplifier Design**, for a more complete explanation of proper gain selection.

Besides gain, one of the major considerations is the closed-loop bandwidth of the amplifier. To a large extent, the bandwidth is dictated by the choice of external components shown in *Figure 1*. The input coupling capacitor, C_i, forms a first order high pass filter which limits low frequency response. This value should be chosen based on needed frequency response for a few distinct reasons.

Selection Of Input Capacitor Size

Large input capacitors are both expensive and space hungry for portable designs. Clearly, a certain sized capacitor is needed to couple in low frequencies without severe attenuation. But in many cases the speakers used in portable systems, whether internal or external, have little ability to

Application Information (Continued)

reproduce signals below 100 Hz to 150 Hz. Thus, using a large input capacitor may not increase actual system performance.

In addition to system cost and size, click and pop performance is effected by the size of the input coupling capacitor, C_i. A larger input coupling capacitor requires more charge to reach its quiescent DC voltage (nominally 1/2 V_{DD}). This charge comes from the output via the feedback and is apt to create pops upon device enable. Thus, by minimizing the capacitor size based on necessary low frequency response, turn-on pops can be minimized.

Besides minimizing the input capacitor size, careful consideration should be paid to the bypass capacitor value. Bypass capacitor, C_B, is the most critical component to minimize turn-on pops since it determines how fast the LM4820-6 turns on. The slower the LM4820-6's outputs ramp to their quiescent DC voltage (nominally 1/2 V_{DD}), the smaller the turn-on pop. Choosing C_B equal to 1.0 µF along with a small value of C_i (in the range of 0.1 µF to 0.39 µF), should produce a virtually clickless and popless shutdown function. While the device will function properly, (no oscillations or motorboating), with C_B equal to 0.1 µF, the device will be much more susceptible to turn-on clicks and pops. Thus, a value of C_B equal to 1.0 µF is recommended in all but the most cost sensitive designs.

AUDIO POWER AMPLIFIER DESIGN

A 1W/8Ω Audio Amplifier

Given:

Power Output	1 Wrms
Load Impedance	8Ω
Input Level	1 Vrms
Input Impedance	25 kΩ
Bandwidth	100 Hz–20 kHz ± 0.25 dB

A designer must first determine the minimum supply rail to obtain the specified output power. By extrapolating from the Output Power vs Supply Voltage graphs in the **Typical Performance Characteristics** section, the supply rail can be easily found. A second way to determine the minimum supply rail is to calculate the required V_{opeak} using Equation 3. Using this method, the minimum supply voltage would be (V_{opeak} + ($V_{OD_{TOP}}$ + $V_{OD_{BOT}}$)), where $V_{OD_{BOT}}$ and $V_{OD_{TOP}}$ are extrapolated from the Dropout Voltage vs Supply Voltage curve in the **Typical Performance Characteristics** section.

$$V_{opeak} = \sqrt{(2R_LP_O)} \tag{3}$$

2.7V_{DD} to 5V_{DD} is a standard supply voltage range for most applications. Extra supply voltage creates headroom that allows the LM4820-6 to reproduce peaks in excess of 1W without producing audible distortion. At this time, the designer must make sure that the power supply choice along with the output impedance does not violate the conditions explained in the **Power Dissipation** section.

Once the power dissipation equations have been addressed, the differential gain is determined from Equations 4 or 5.

$$A_{VD} \geq \sqrt{(P_OR_L)}/(V_{IN}) = V_{orms}/V_{inrms} \tag{4}$$

or

$$A_{VD} = 2\ (R_f/R_i) \tag{5}$$

$$R_f = R_i = 25k\Omega$$

$$A_{VD} = 2\ (25k\Omega/25k\Omega)$$

$$A_{VD} = 2$$

The last step in this design example is setting the amplifier's -3dB frequency bandwidth. To achieve the desired ±0.25dB pass band magnitude variation limit, the low frequency response must extend to at least one-fifth the lower bandwidth limit. The high frequency response must extend to at least five times the upper bandwidth limit. The gain variation for both response limits is 0.17dB, well within the ±0.25dB desired limit. The results are

f_L = 100Hz/5 = 20Hz

and

f_H = 20kHz x 5 = 100kHz

As mentioned in the **Selecting Proper External Components** section, R_i and C_i create a highpass filter that sets the amplifier's lower bandpass frequency limit. To find the coupling capacitor's value, use Equation 6

$$C_i \geq 1/(2\pi R_i f_L) \tag{6}$$

The result is

1/(2π*25kΩ*20kHz) = .318µf

Use a 0.33µf capacitor, the closest standard value.

The product of the desired high frequency cutoff (100kHz in this example) and the differential gain A_{VD}, determines the upper passband response limit. With A_{VD} = 2 and f_H = 100kHz, the closed-loop gain bandwidth product (GBWP) is 200kHz. This is less than the LM4820-6's 25MHz GBWP. With this margin, the amplifier can be used in designs that require more differential gain while avoiding performance, restricting bandwidth limitations.

Application Information (Continued)

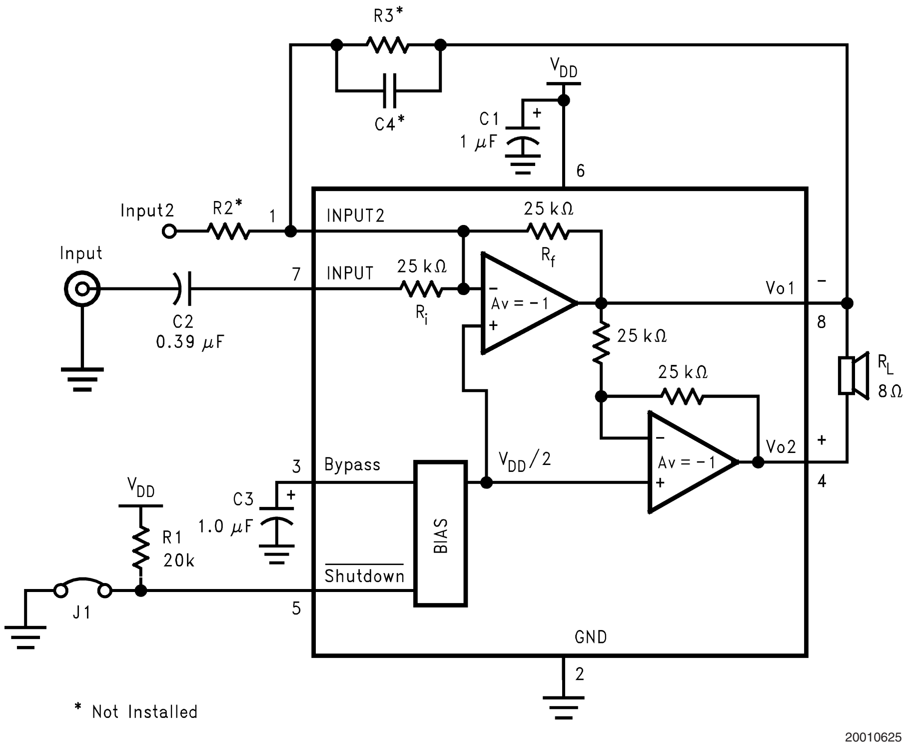
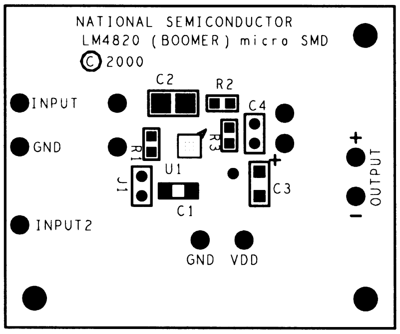


FIGURE 2. Reference Design Board and Layout - micro SMD

Application Information (Continued)

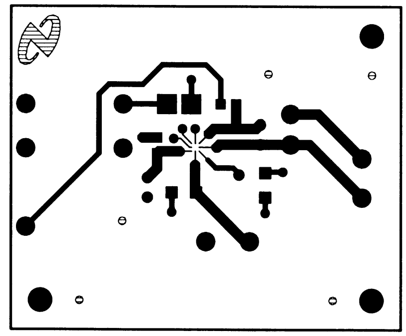
LM4820-6 micro SMD BOARD ARTWORK

Silk Screen



20010657

Top Layer



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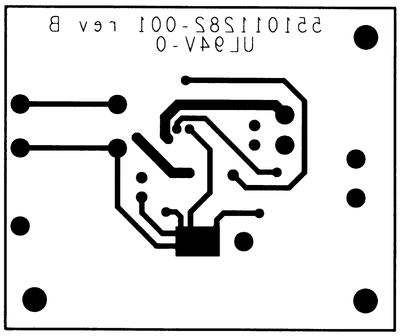
Bottom Layer



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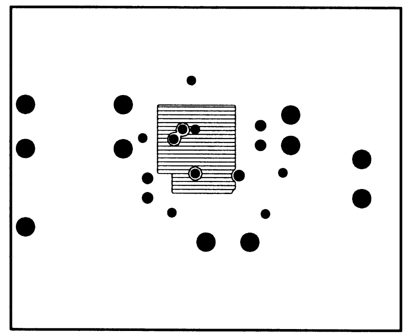
Inner Layer Ground



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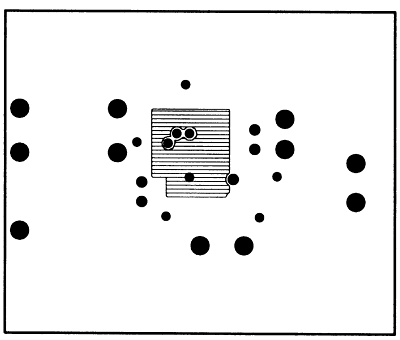
Inner Layer V_{DD}



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Application Information (Continued)

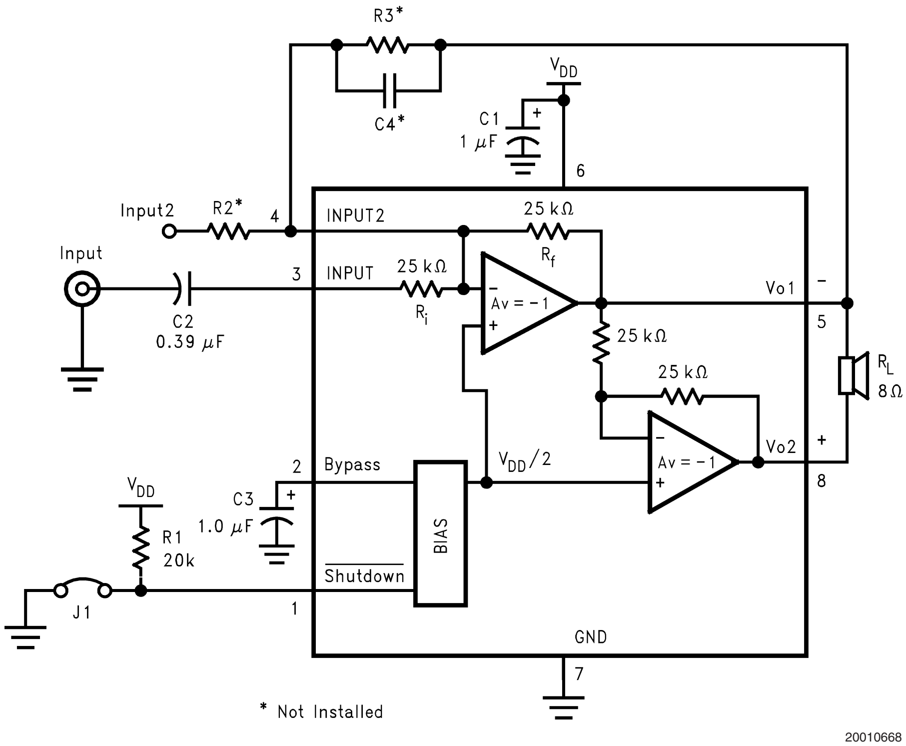

FIGURE 3. Reference Design Board and PCB Layout Guidelines - MSOP & SO Boards

Application Information (Continued)

LM4820-6 SO DEMO BOARD ARTWORK

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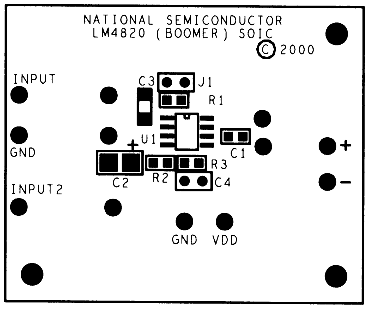

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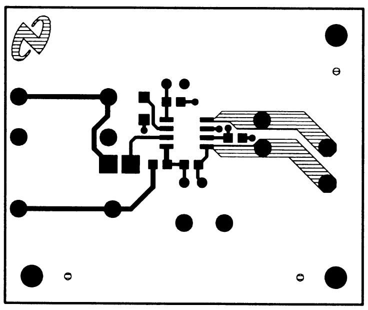

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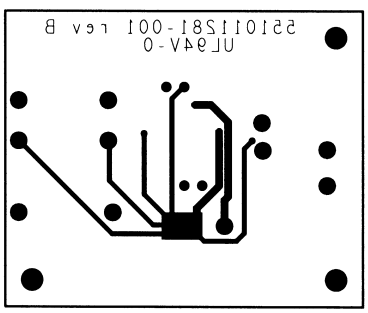
Bottom Layer



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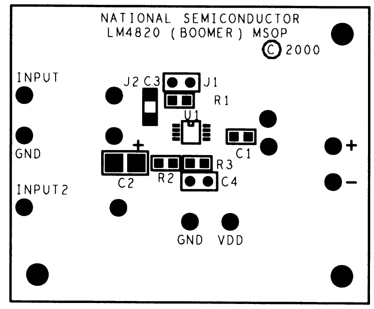
LM4820-6 MSOP DEMO BOARD ARTWORK

Silk Screen



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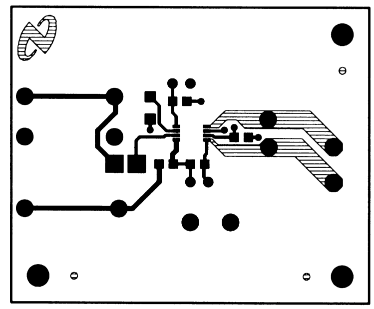
Top Layer



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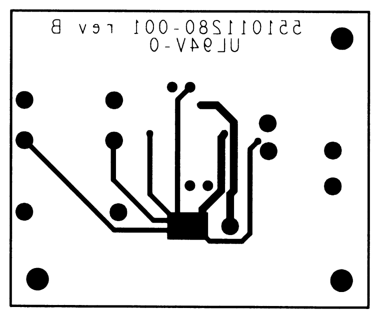
Bottom Layer



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Application Information (Continued)

Mono LM4820-6 Reference Design Boards
Bill of Material for all 3 Demo Boards

Item	Part Number	Part Description	Qty	Ref Designator
1	551011208-001	LM4820-6 Mono Reference Design Board	1	
10	482911183-001	LM4820-6 Audio AMP	1	U1
20	151911207-001	Tant Cap 1uF 16V 10	1	C1
21	151911207-002	Cer Cap 0.39uF 50V Z5U 20% 1210	1	C2
25	152911207-001	Tant Cap 1uF 16V 10	1	C3
30	472911207-001	Res 20K Ohm 1/10W 5	3	R1
35	210007039-002	Jumper Header Vertical Mount 2X1 0.100	2	J1

PCB LAYOUT GUIDELINES

This section provides practical guidelines for mixed signal PCB layout that involves various digital/analog power and ground traces. Designers should note that these are only "rule-of-thumb" recommendations and the actual results will depend heavily on the final layout.

General Mixed Signal Layout Recommendation

Power and Ground Circuits

For 2 layer mixed signal design, it is important to isolate the digital power and ground trace paths from the analog power and ground trace paths. Star trace routing techniques (bringing individual traces back to a central point rather than daisy chaining traces together in a serial manner) can have a major impact on low level signal performance. Star trace routing refers to using individual traces to feed power and ground to each circuit or even device. This technique will take require a greater amount of design time but will not increase the final price of the board. The only extra parts required will be some jumpers.

Single-Point Power / Ground Connections

The analog power traces should be connected to the digital traces through a single point (link). A "Pi-filter" can be helpful in minimizing High Frequency noise coupling between the analog and digital sections. It is further recommended to put digital and analog power traces over the corresponding digital and analog ground traces to minimize noise coupling.

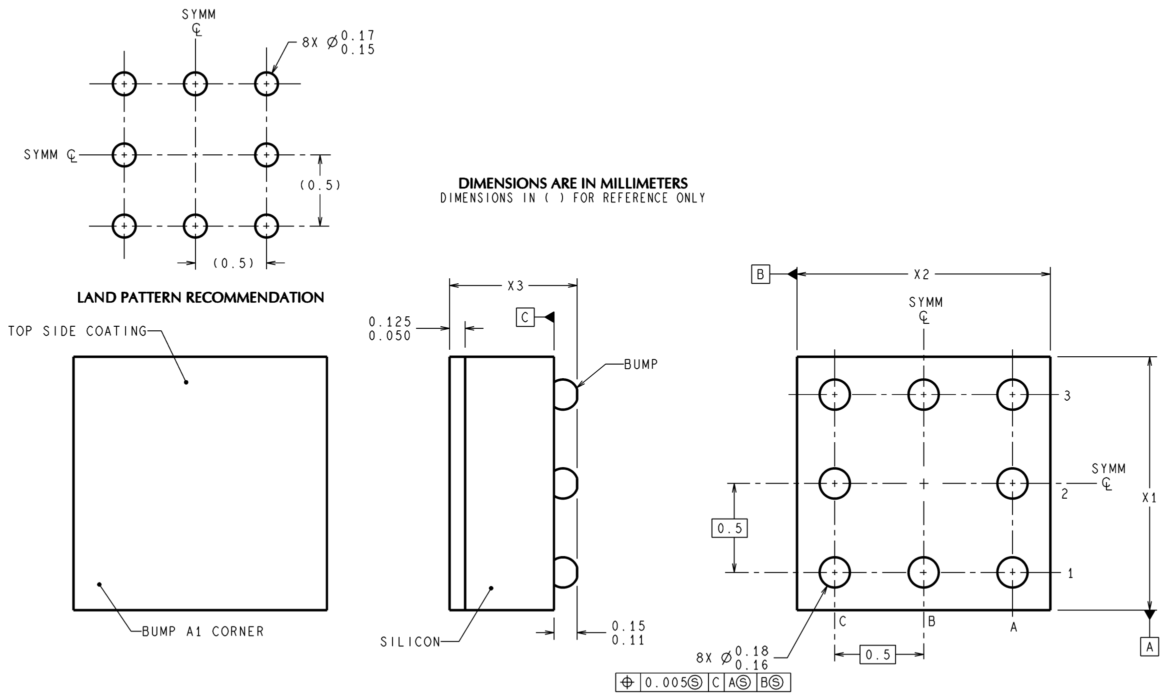
Placement of Digital and Analog Components

All digital components and high-speed digital signals traces should be located as far away as possible from analog components and circuit traces.

Avoiding Typical Design / Layout Problems

Avoid ground loops or running digital and analog traces parallel to each other (side-by-side) on the same PCB layer. When traces must cross over each other do it at 90 degrees. Running digital and analog traces at 90 degrees to each other from the top to the bottom side as much as possible will minimize capacitive noise coupling and cross talk.

Physical Dimensions inches (millimeters) unless otherwise noted



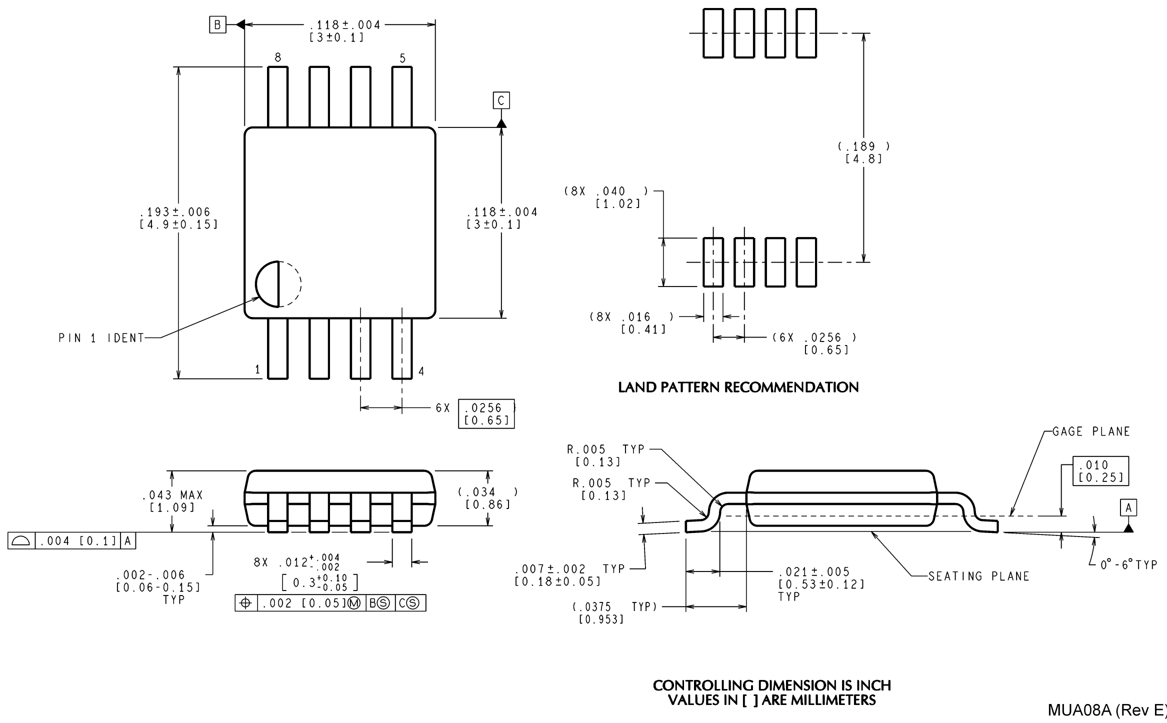
BPA08XXX (Rev D)

Note: Unless otherwise specified.

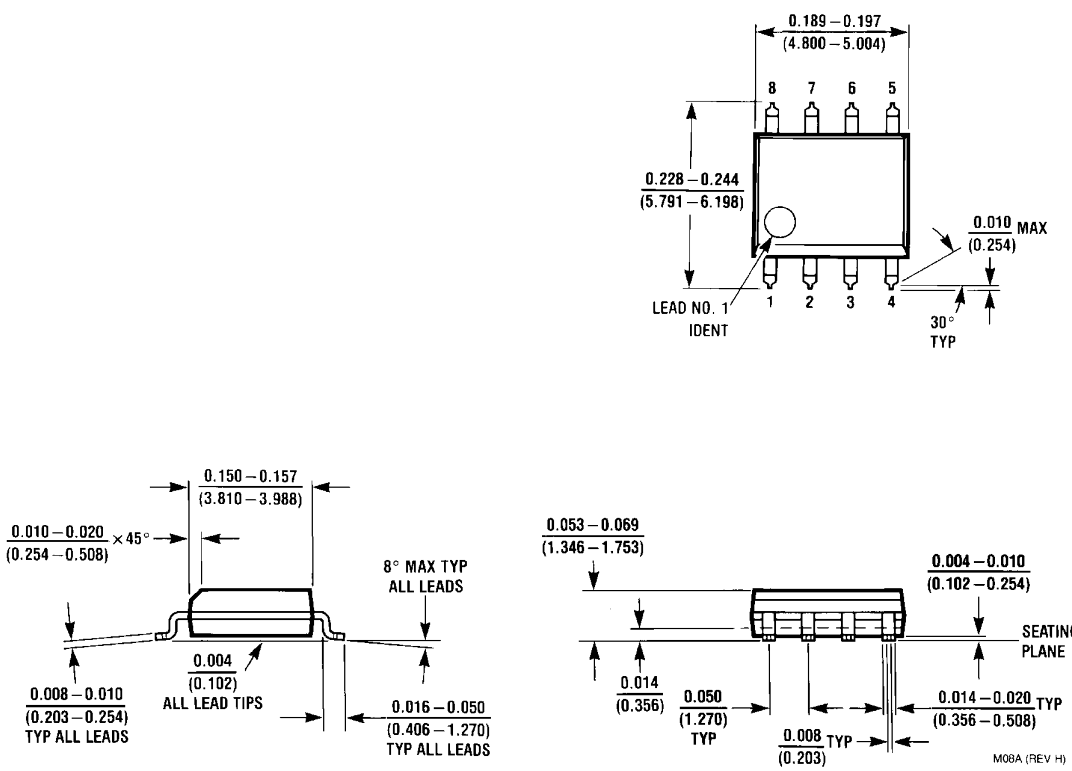
1. Epoxy coating.
2. 63Sn/37Pb eutectic bump.
3. Recommend non-solder mask defined landing pad.
4. Pin 1 is established by lower left corner with respect to text orientation pins are numbered counterclockwise.
5. Reference JEDEC registration MO-211, variation BC.

8-Bump micro SMD
Order Number LM4820IBP-6, LM4820IBPX-6
NS Package Number BPA08DDB
X1 = 1.361±0.03 X2 = 1.361±0.03 X3 = 0.850±0.10

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



MSOP
Order Number LM4820MM-6
NS Package Number MUA08A



SO
Order Number LM4820M-6
NS Package Number M08A

Notes

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