

## Automotive door actuator driver with embedded LIN

Datasheet - production data



### Features

- AEC-Q100 qualified 
- 1 half bridge for 7.5 A load ( $R_{ON} = 100 \text{ m}\Omega$ )
- 1 half bridge for 7.5 A load ( $R_{ON} = 150 \text{ m}\Omega$ )
- 2 half bridges for 3 A load ( $R_{ON} = 300 \text{ m}\Omega$ )
- 1 configurable high-side driver for up to 1.5 A ( $R_{ON} = 500 \text{ m}\Omega$ ) or 0.35 A ( $R_{ON} = 1600 \text{ m}\Omega$ ) load
- 1 configurable high-side driver for 0.8 A ( $R_{ON} = 800 \text{ m}\Omega$ ) or 0.35 A ( $R_{ON} = 1600 \text{ m}\Omega$ ) load
- 3 configurable high-side drivers for 0.15 A/0.35 A ( $R_{ON} = 2 \text{ }\Omega$ )
- 1 configurable high-side driver for 0.25 A/0.5 A ( $R_{ON} = 2 \text{ }\Omega$ )
- 4 configurable high-side drivers for 0.15 A/0.25 A ( $R_{ON} = 5 \text{ }\Omega$ )
- Internal 10bit PWM timer for each stand-alone high-side driver
- Buffered supply for voltage regulators and 2 high-side drivers (OUT15 & OUT\_HS / both P-channel) to supply e.g. external contacts
- Programmable soft-start function to drive loads with higher inrush currents as current limitation value (for OUT1-6, OUT7, OUT8 and OUT\_HS) with thermal expiration feature
- All the embedded outputs come with protection and supervision features:
  - Current Monitor (high-side only)
  - Open-load

- Overcurrent
- Thermal warning
- Thermal shutdown
- Fully protected driver for external MOSFETs in H-bridge configuration
- Two 5 V voltage regulators for microcontroller and peripheral supply
- Programmable reset generator for power-on and undervoltage
- Configurable window watchdog
- LIN 2.2a compliant (SAEJ2602 compatible) transceiver
- Separated (Isolated) fail-safe block with 2 LS ( $R_{ON} = 1 \text{ }\Omega$ ) to pull down the gates of the external HS MOSFETs
- Thermal clusters
- A/D conversion of supply voltages and internal temperature sensors
- Embedded and programmable VS duty cycle adjustment for LED driver outputs

### Applications

Door zone applications.

**Table 1. Device summary**

| Package      | Order codes |               |
|--------------|-------------|---------------|
|              | Tray        | Tape and reel |
| LQFP-64 epad | L99DZ120    | L99DZ120TR    |



# Contents

|          |                                                               |           |
|----------|---------------------------------------------------------------|-----------|
| <b>1</b> | <b>Description .....</b>                                      | <b>12</b> |
| <b>2</b> | <b>Block diagram and pin descriptions .....</b>               | <b>13</b> |
| <b>3</b> | <b>Electrical specifications .....</b>                        | <b>18</b> |
| 3.1      | Absolute maximum ratings .....                                | 18        |
| 3.2      | ESD protection .....                                          | 20        |
| 3.3      | Thermal data .....                                            | 20        |
| 3.3.1    | LQFP64 thermal data .....                                     | 21        |
| 3.4      | Electrical characteristics .....                              | 25        |
| 3.4.1    | Supply and supply monitoring .....                            | 25        |
| 3.4.2    | Oscillator .....                                              | 26        |
| 3.4.3    | Power-on reset (VSREG) .....                                  | 26        |
| 3.4.4    | Voltage regulator V1 .....                                    | 27        |
| 3.4.5    | Voltage regulator V2 .....                                    | 29        |
| 3.4.6    | Reset output .....                                            | 29        |
| 3.4.7    | Watchdog timing .....                                         | 31        |
| 3.4.8    | Current monitor output (CM) .....                             | 33        |
| 3.4.9    | Charge pump .....                                             | 34        |
| 3.4.10   | Outputs OUT1 - OUT15, OUT_HS .....                            | 35        |
| 3.4.11   | Power outputs switching times .....                           | 37        |
| 3.4.12   | Over Current Recovery settings .....                          | 38        |
| 3.4.13   | Current monitoring .....                                      | 39        |
| 3.4.14   | H-bridge driver .....                                         | 41        |
| 3.4.15   | Gate drivers for the external Power-MOS switching times ..... | 42        |
| 3.4.16   | Drain source monitoring external H-bridge .....               | 45        |
| 3.4.17   | Open-load monitoring external H-bridge .....                  | 45        |
| 3.4.18   | Fail safe low-side switch .....                               | 46        |
| 3.4.19   | Wake up input WU .....                                        | 47        |
| 3.4.20   | LIN transceiver .....                                         | 47        |
| 3.4.21   | SPI .....                                                     | 50        |
| 3.4.22   | Input LIN_FLASH for Flash mode .....                          | 52        |
| 3.4.23   | Inputs DIR, DIRH, PWMH .....                                  | 53        |
| 3.4.24   | Debug input .....                                             | 53        |

|          |                                                     |           |
|----------|-----------------------------------------------------|-----------|
| 3.4.25   | ADC characteristics                                 | 53        |
| 3.4.26   | Temperature diode characteristics                   | 54        |
| 3.4.27   | Interrupt outputs                                   | 54        |
| 3.4.28   | Timer1 and Timer2                                   | 55        |
| 3.4.29   | SGND loss comparator                                | 58        |
| <b>4</b> | <b>Application information</b>                      | <b>59</b> |
| 4.1      | Supply $V_S$ , $V_{SREG}$                           | 59        |
| 4.2      | Voltage regulators                                  | 59        |
| 4.2.1    | Voltage regulator: V1                               | 59        |
| 4.2.2    | Voltage regulator: V2                               | 59        |
| 4.2.3    | Voltage regulator failure                           | 60        |
| 4.2.4    | Short to ground detection                           | 60        |
| 4.2.5    | Voltage regulator behavior                          | 61        |
| 4.3      | Operating modes                                     | 61        |
| 4.3.1    | Active mode                                         | 61        |
| 4.3.2    | Flash mode                                          | 62        |
| 4.3.3    | SW-debug mode                                       | 62        |
| 4.3.4    | V1_standby mode                                     | 62        |
| 4.3.5    | Interrupt                                           | 63        |
| 4.3.6    | VBAT_standby mode                                   | 63        |
| 4.4      | Wake-up from Standby modes                          | 63        |
| 4.4.1    | Wake up input                                       | 64        |
| 4.5      | Functional overview (truth table)                   | 64        |
| 4.6      | Configurable window watchdog                        | 66        |
| 4.6.1    | Change watchdog timing                              | 69        |
| 4.7      | Fail-safe mode                                      | 69        |
| 4.7.1    | Temporary failures                                  | 69        |
| 4.7.2    | Non-recoverable failures – forced Vbat_standby mode | 70        |
| 4.8      | Reset output (NReset)                               | 71        |
| 4.9      | LIN Bus Interface                                   | 71        |
| 4.9.1    | Features                                            | 72        |
| 4.9.2    | Error handling                                      | 72        |
| 4.9.3    | Wake up from Standby modes                          | 73        |
| 4.9.4    | Receive-only mode                                   | 73        |
| 4.10     | Serial Peripheral Interface (ST SPI Standard)       | 74        |

|          |                                                                                      |           |
|----------|--------------------------------------------------------------------------------------|-----------|
| 4.11     | Power supply failure . . . . .                                                       | 75        |
| 4.11.1   | $V_S$ supply failure . . . . .                                                       | 75        |
| 4.11.2   | $V_{SREG}$ supply failure . . . . .                                                  | 76        |
| 4.12     | Temperature warning and thermal shutdown . . . . .                                   | 77        |
| 4.13     | Power outputs OUT1..15 and OUT_HS . . . . .                                          | 78        |
| 4.14     | Auto-recovery alert and thermal expiration . . . . .                                 | 79        |
| 4.15     | Charge pump . . . . .                                                                | 81        |
| 4.16     | Inductive loads . . . . .                                                            | 81        |
| 4.17     | Open-load detection . . . . .                                                        | 82        |
| 4.18     | Overcurrent detection . . . . .                                                      | 82        |
| 4.19     | Current monitor . . . . .                                                            | 82        |
| 4.20     | PWM mode of the power outputs . . . . .                                              | 82        |
| 4.21     | Cross-current protection . . . . .                                                   | 82        |
| 4.22     | Programmable soft-start function to drive loads with higher inrush current . . . . . | 83        |
| 4.23     | H-bridge control . . . . .                                                           | 85        |
| 4.24     | H-bridge driver slew-rate control . . . . .                                          | 86        |
| 4.25     | Resistive low . . . . .                                                              | 87        |
| 4.26     | Short circuit detection / drain source monitoring . . . . .                          | 87        |
| 4.27     | H-bridge monitoring in off-mode . . . . .                                            | 88        |
| 4.28     | Programmable cross current protection . . . . .                                      | 91        |
| 4.29     | Power window H-bridge safety switch off block . . . . .                              | 91        |
| 4.30     | Temperature warning and shutdown . . . . .                                           | 93        |
| 4.31     | Thermal clusters . . . . .                                                           | 93        |
| 4.32     | $V_S$ compensation (duty cycle adjustment) module . . . . .                          | 95        |
| 4.33     | Analog digital converter . . . . .                                                   | 96        |
| <b>5</b> | <b>Serial Peripheral Interface (SPI) . . . . .</b>                                   | <b>97</b> |
| 5.1      | ST SPI 4.0 . . . . .                                                                 | 97        |
| 5.1.1    | Physical layer . . . . .                                                             | 98        |
| 5.2      | Signal description . . . . .                                                         | 98        |
| 5.2.1    | Clock and Data Characteristics . . . . .                                             | 99        |
| 5.2.2    | Communication protocol . . . . .                                                     | 100       |
| 5.2.3    | Address definition . . . . .                                                         | 103       |

|          |        |                                             |            |
|----------|--------|---------------------------------------------|------------|
|          | 5.2.4  | Protocol failure detection                  | 109        |
| <b>6</b> |        | <b>Application</b>                          | <b>111</b> |
| <b>7</b> |        | <b>SPI Registers</b>                        | <b>112</b> |
|          | 7.1    | Global Status Byte GSB                      | 112        |
|          | 7.2    | Control register overview                   | 115        |
|          | 7.3    | Status register overview                    | 119        |
|          | 7.4    | Control registers                           | 121        |
|          | 7.4.1  | Control Register CR1 (0x01)                 | 121        |
|          | 7.4.2  | Control Register CR2 (0x02)                 | 123        |
|          | 7.4.3  | Control Register CR3 (0x03)                 | 126        |
|          | 7.4.4  | Control Register CR4 (0x04)                 | 128        |
|          | 7.4.5  | Control Register CR5 (0x05)                 | 129        |
|          | 7.4.6  | Control Register CR6 (0x06)                 | 131        |
|          | 7.4.7  | Control Register CR7 (0x07)                 | 132        |
|          | 7.4.8  | Control Register CR8 (0x08)                 | 134        |
|          | 7.4.9  | Control Register CR9 (0x09)                 | 135        |
|          | 7.4.10 | Control Register CR10 (0x0A)                | 136        |
|          | 7.4.11 | Control Register CR11 (0x0B)                | 137        |
|          | 7.4.12 | Control Register CR12 (0x0C)                | 137        |
|          | 7.4.13 | Control Register CR13 (0x0D) to CR17 (0x11) | 139        |
|          | 7.4.14 | Control Register CR18 (0x12) to CR22 (0x16) | 140        |
|          | 7.4.15 | Control Register CR34 (0x22)                | 142        |
|          | 7.4.16 | Configuration Register (0x3F)               | 142        |
|          | 7.5    | Status Registers                            | 145        |
|          | 7.5.1  | Status Register SR1 (0x31)                  | 145        |
|          | 7.5.2  | Status Register SR2 (0x32)                  | 147        |
|          | 7.5.3  | Status Register SR3 (0x33)                  | 149        |
|          | 7.5.4  | Status Register SR4 (0x34)                  | 150        |
|          | 7.5.5  | Status Register SR5 (0x35)                  | 151        |
|          | 7.5.6  | Status Register SR6 (0x36)                  | 152        |
|          | 7.5.7  | Status Register SR7 (0x37) to SR9 (0x39)    | 153        |
|          | 7.5.8  | Status Register SR10 (0x3A)                 | 154        |
|          | 7.5.9  | Status Register SR11 (0x3B)                 | 155        |
| <b>8</b> |        | <b>Package information</b>                  | <b>157</b> |

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|          |                                   |            |
|----------|-----------------------------------|------------|
| 8.1      | LQFP-64 package information ..... | 157        |
| 8.2      | LQFP-64 marking information ..... | 159        |
| <b>9</b> | <b>Revision history .....</b>     | <b>160</b> |

## List of tables

|           |                                                                          |    |
|-----------|--------------------------------------------------------------------------|----|
| Table 1.  | Device summary . . . . .                                                 | 1  |
| Table 2.  | Pin definitions and functions . . . . .                                  | 13 |
| Table 3.  | Absolute maximum ratings . . . . .                                       | 18 |
| Table 4.  | ESD protection . . . . .                                                 | 20 |
| Table 5.  | Operating junction temperature . . . . .                                 | 20 |
| Table 6.  | Temperature warning and thermal shutdown . . . . .                       | 21 |
| Table 7.  | Supply and supply monitoring . . . . .                                   | 25 |
| Table 8.  | Oscillator . . . . .                                                     | 26 |
| Table 9.  | Power-on reset ( $V_{SREG}$ ) . . . . .                                  | 27 |
| Table 10. | Voltage regulator V1 . . . . .                                           | 27 |
| Table 11. | Voltage regulator V2 . . . . .                                           | 29 |
| Table 12. | Reset output . . . . .                                                   | 29 |
| Table 13. | Watchdog timing . . . . .                                                | 31 |
| Table 14. | Current monitor output (CM) . . . . .                                    | 33 |
| Table 15. | Charge pump electrical characteristics . . . . .                         | 34 |
| Table 16. | Outputs OUT1 - OUT15, OUT_HS . . . . .                                   | 35 |
| Table 17. | Power outputs switching times . . . . .                                  | 37 |
| Table 18. | Half bridges (OUT1, OUT4, OUT5 and OUT6) OCR timing parameters . . . . . | 38 |
| Table 19. | High-side (OUT7, OUT8 and OUT_HS) OCR timing parameters . . . . .        | 38 |
| Table 20. | Current monitoring . . . . .                                             | 40 |
| Table 21. | H-bridge driver . . . . .                                                | 41 |
| Table 22. | Gate drivers for the external Power-MOS switching times . . . . .        | 42 |
| Table 23. | Drain source monitoring external H-bridge . . . . .                      | 45 |
| Table 24. | Open-load monitoring external H-bridge . . . . .                         | 46 |
| Table 25. | Fail safe low-side switch . . . . .                                      | 46 |
| Table 26. | Wake-up inputs . . . . .                                                 | 47 |
| Table 27. | LIN transmit data input: pin TxD . . . . .                               | 47 |
| Table 28. | LIN receive data output: pin RxD . . . . .                               | 47 |
| Table 29. | LIN transmitter and receiver: pin LIN . . . . .                          | 48 |
| Table 30. | LIN transceiver timing . . . . .                                         | 49 |
| Table 31. | Input: CSN . . . . .                                                     | 50 |
| Table 32. | Inputs: CLK, DI . . . . .                                                | 50 |
| Table 33. | DI, CLK and CSN timing . . . . .                                         | 51 |
| Table 34. | Output: DO . . . . .                                                     | 51 |
| Table 35. | DO timing . . . . .                                                      | 52 |
| Table 36. | CSN timing . . . . .                                                     | 52 |
| Table 37. | Inputs LIN_FLASH for Flash mode . . . . .                                | 52 |
| Table 38. | Inputs DIR, DIRH, PWMH . . . . .                                         | 53 |
| Table 39. | Debug input . . . . .                                                    | 53 |
| Table 40. | ADC characteristics . . . . .                                            | 53 |
| Table 41. | Temperature diode characteristics . . . . .                              | 54 |
| Table 42. | Interrupt outputs . . . . .                                              | 54 |
| Table 43. | Timer1 and Timer2 . . . . .                                              | 55 |
| Table 44. | SGND loss comparator . . . . .                                           | 58 |
| Table 45. | Wake-up events description . . . . .                                     | 64 |
| Table 46. | Status of different functions/features vs operating modes . . . . .      | 64 |
| Table 47. | Temporary failures description . . . . .                                 | 70 |
| Table 48. | Non-recoverable failure . . . . .                                        | 70 |

|            |                                               |     |
|------------|-----------------------------------------------|-----|
| Table 49.  | Power output settings . . . . .               | 79  |
| Table 50.  | H-bridge control truth table . . . . .        | 86  |
| Table 51.  | H-bridge monitoring in off-mode . . . . .     | 90  |
| Table 52.  | Thermal cluster definition . . . . .          | 95  |
| Table 53.  | Operation codes . . . . .                     | 100 |
| Table 54.  | Global Status Byte . . . . .                  | 102 |
| Table 55.  | Device application access . . . . .           | 103 |
| Table 56.  | Device information read access . . . . .      | 103 |
| Table 57.  | RAM address range . . . . .                   | 103 |
| Table 58.  | ROM address range . . . . .                   | 104 |
| Table 59.  | Information Registers Map . . . . .           | 105 |
| Table 60.  | SPI Mode Register . . . . .                   | 106 |
| Table 61.  | Burst Read Bit. . . . .                       | 106 |
| Table 62.  | SPI Data Length . . . . .                     | 106 |
| Table 63.  | Data Consistency Check . . . . .              | 107 |
| Table 64.  | WD Type/Timing . . . . .                      | 107 |
| Table 65.  | WD bit position . . . . .                     | 108 |
| Table 66.  | Global Status Byte (GSB) . . . . .            | 112 |
| Table 67.  | GSB signals description . . . . .             | 112 |
| Table 68.  | Control register overview . . . . .           | 115 |
| Table 69.  | Status register overview . . . . .            | 119 |
| Table 70.  | Control Register CR1 . . . . .                | 121 |
| Table 71.  | CR1 signals description . . . . .             | 121 |
| Table 72.  | Wake-up input1 filter configuration . . . . . | 122 |
| Table 73.  | Voltage regulator V2 configuration . . . . .  | 122 |
| Table 74.  | Standby transition configuration . . . . .    | 123 |
| Table 75.  | Control Register CR2 . . . . .                | 123 |
| Table 76.  | CR2 signals description . . . . .             | 123 |
| Table 77.  | Configuration of Timer x on-time . . . . .    | 125 |
| Table 78.  | Control Register CR3 . . . . .                | 126 |
| Table 79.  | CR3 signals description . . . . .             | 127 |
| Table 80.  | Control Register CR4 . . . . .                | 128 |
| Table 81.  | CR4 signals description . . . . .             | 128 |
| Table 82.  | Control Register CR5 . . . . .                | 129 |
| Table 83.  | CR5 signals description . . . . .             | 130 |
| Table 84.  | OUTx Configuration bits . . . . .             | 130 |
| Table 85.  | Control Register CR6 . . . . .                | 131 |
| Table 86.  | CR6 signals description . . . . .             | 131 |
| Table 87.  | Control Register CR7 . . . . .                | 132 |
| Table 88.  | CR7 signals description . . . . .             | 132 |
| Table 89.  | Control Register CR8 . . . . .                | 134 |
| Table 90.  | CR8 signals description . . . . .             | 134 |
| Table 91.  | Control Register CR9 . . . . .                | 135 |
| Table 92.  | CR9 signals description . . . . .             | 135 |
| Table 93.  | Control Register CR10 . . . . .               | 136 |
| Table 94.  | CR10 signals description . . . . .            | 136 |
| Table 95.  | Control Register CR11 . . . . .               | 137 |
| Table 96.  | CR11 signals description . . . . .            | 137 |
| Table 97.  | Control Register CR12 . . . . .               | 137 |
| Table 98.  | CR12 signals description . . . . .            | 138 |
| Table 99.  | Control Register CR13 to CR17 . . . . .       | 139 |
| Table 100. | CR13 to CR17 signals description . . . . .    | 139 |

|            |                                          |     |
|------------|------------------------------------------|-----|
| Table 101. | Control Register CR18                    | 140 |
| Table 102. | CR18 to CR22 signals description         | 141 |
| Table 103. | Control Register CR34                    | 142 |
| Table 104. | CR34 signals description                 | 142 |
| Table 105. | Configuration Register                   | 142 |
| Table 106. | CR signals description                   | 143 |
| Table 107. | Status Register SR1 (0x31)               | 145 |
| Table 108. | SR1 signals description                  | 145 |
| Table 109. | Status Register SR2 (0x32)               | 147 |
| Table 110. | SR2 signals description                  | 147 |
| Table 111. | Status Register SR3 (0x33)               | 149 |
| Table 112. | SR3 signals description                  | 149 |
| Table 113. | Status Register SR4 (0x34)               | 150 |
| Table 114. | SR4 signals description                  | 151 |
| Table 115. | Status Register SR5 (0x35)               | 151 |
| Table 116. | SR5 signals description                  | 151 |
| Table 117. | Status Register SR6 (0x36)               | 152 |
| Table 118. | SR6 signals description                  | 152 |
| Table 119. | Status Register SR7 (0x37) to SR9 (0x39) | 153 |
| Table 120. | SR7 to SR9 signals description           | 153 |
| Table 121. | Status Register SR10 (0x3A)              | 154 |
| Table 122. | SR10 signals description                 | 154 |
| Table 123. | Status Register SR11 (0x3B)              | 155 |
| Table 124. | SR11 signals description                 | 155 |
| Table 125. | LQFP-64 mechanical data                  | 157 |
| Table 126. | Document revision history                | 160 |

## List of figures

|            |                                                                                                                                                             |    |
|------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------|----|
| Figure 1.  | Block diagram . . . . .                                                                                                                                     | 13 |
| Figure 2.  | Pin connection (top view) . . . . .                                                                                                                         | 17 |
| Figure 3.  | Activation profile 1 . . . . .                                                                                                                              | 22 |
| Figure 4.  | Activation profile 1 (first cycle) . . . . .                                                                                                                | 22 |
| Figure 5.  | Activation profile 2 . . . . .                                                                                                                              | 23 |
| Figure 6.  | Activation profile 2 (first cycle) . . . . .                                                                                                                | 24 |
| Figure 7.  | LQFP64 package and PCB thermal configuration . . . . .                                                                                                      | 24 |
| Figure 8.  | Voltage regulator V1 characteristics (quiescent current and accuracy) . . . . .                                                                             | 28 |
| Figure 9.  | Watchdog timing . . . . .                                                                                                                                   | 32 |
| Figure 10. | Watchdog early, late and safe windows . . . . .                                                                                                             | 33 |
| Figure 11. | Hard Short case, the OC threshold is reached before end of blanking time. . . . .                                                                           | 39 |
| Figure 12. | Overload case, the OC threshold is reached after end of blanking time. . . . .                                                                              | 39 |
| Figure 13. | H-driver delay times . . . . .                                                                                                                              | 44 |
| Figure 14. | IGHxr ranges . . . . .                                                                                                                                      | 44 |
| Figure 15. | IGHxf ranges. . . . .                                                                                                                                       | 45 |
| Figure 16. | LIN transmit, receive timing . . . . .                                                                                                                      | 50 |
| Figure 17. | SPI – transfer timing diagram . . . . .                                                                                                                     | 55 |
| Figure 18. | SPI input timing. . . . .                                                                                                                                   | 56 |
| Figure 19. | SPI output timing . . . . .                                                                                                                                 | 57 |
| Figure 20. | SPI CSN - output timing . . . . .                                                                                                                           | 58 |
| Figure 21. | SPI – CSN high to low transition and global status bit access . . . . .                                                                                     | 58 |
| Figure 22. | Voltage regulator behaviour and diagnosis during supply voltage . . . . .                                                                                   | 61 |
| Figure 23. | NINT pins . . . . .                                                                                                                                         | 63 |
| Figure 24. | Main operating modes . . . . .                                                                                                                              | 66 |
| Figure 25. | Watchdog in normal operating mode (no errors) . . . . .                                                                                                     | 67 |
| Figure 26. | Watchdog with error conditions . . . . .                                                                                                                    | 68 |
| Figure 27. | Watchdog in Flash mode . . . . .                                                                                                                            | 68 |
| Figure 28. | NReset pin . . . . .                                                                                                                                        | 71 |
| Figure 29. | RxDL pin . . . . .                                                                                                                                          | 71 |
| Figure 30. | Wake-up behavior according to LIN 2.2a . . . . .                                                                                                            | 73 |
| Figure 31. | Thermal shutdown protection and diagnosis . . . . .                                                                                                         | 77 |
| Figure 32. | Example of long auto-recovery on OUT7. Temperature acquisition starts after $t_{AR}$ , thermal expiration occurs after a $\Delta T = 30^\circ$ . . . . .    | 80 |
| Figure 33. | Block diagram of physical realization of AR alert and thermal expiration . . . . .                                                                          | 81 |
| Figure 34. | Charge pump low filtering and start up implementation . . . . .                                                                                             | 81 |
| Figure 35. | Software strategy for half bridges before applying auto-recovery mode. . . . .                                                                              | 84 |
| Figure 36. | Overcurrent recovery mode . . . . .                                                                                                                         | 85 |
| Figure 37. | H-bridge GSHx slope . . . . .                                                                                                                               | 87 |
| Figure 38. | H-bridge diagnosis . . . . .                                                                                                                                | 88 |
| Figure 39. | H-bridge open-load-detection (no open-load detected) . . . . .                                                                                              | 89 |
| Figure 40. | H-bridge open-load-detection (open-load detected) . . . . .                                                                                                 | 89 |
| Figure 41. | H-bridge open-load-detection (short to ground detected). . . . .                                                                                            | 90 |
| Figure 42. | H-bridge open-load detection (short to $V_S$ detected) . . . . .                                                                                            | 90 |
| Figure 43. | PWMH cross current protection time implementation. . . . .                                                                                                  | 91 |
| Figure 44. | LSx_FSO: low-side driver “passively” turned on, taking supply from output pin (if main supply fails), can guarantee $V_{LSx\_FSO} < V_{OUT\_max}$ . . . . . | 92 |
| Figure 45. | Safety concept . . . . .                                                                                                                                    | 93 |
| Figure 46. | Thermal clusters identification . . . . .                                                                                                                   | 94 |

|            |                                                                       |     |
|------------|-----------------------------------------------------------------------|-----|
| Figure 47. | Block diagram $V_S$ compensation (duty cycle adjustment) module       | 95  |
| Figure 48. | Sequential ADC Read Out for $V_{SREG}$ , $V_S$ , WU and THCL1 ..THCL6 | 96  |
| Figure 49. | SPI pin description                                                   | 98  |
| Figure 50. | SDO pin                                                               | 99  |
| Figure 51. | SPI signal description                                                | 99  |
| Figure 52. | SDI Frame                                                             | 100 |
| Figure 53. | SDO frame                                                             | 102 |
| Figure 54. | Window watchdog operation                                             | 108 |
| Figure 55. | Typical application diagram                                           | 111 |
| Figure 56. | Timer_x controlled by DIR1                                            | 126 |
| Figure 57. | LQFP-64 package dimension                                             | 157 |
| Figure 58. | LQFP-64 footprint                                                     | 159 |
| Figure 59. | LQFP-64 marking information                                           | 159 |

# 1 Description

The L99DZ120 is a door zone systems IC providing electronic control modules with enhanced power management power supply functionality, including various standby modes, as well as LIN physical communication layers.

The two low-drop voltage regulators of the devices supply the system microcontroller and external peripheral loads such as sensors and provide enhanced system standby functionality with programmable local and remote wake-up capability. In addition 8 high-side drivers to supply LEDs, 2 high-side drivers to supply bulbs increase the system integration level.

Up to 3 DC motors and 4 external MOS transistors in H-bridge configuration can be driven. All outputs are SC protected and implement an open-load diagnosis.

The ST standard SPI interface (4.0) allows control and diagnosis of the device and enables generic software development.

## 2 Block diagram and pin descriptions

Figure 1. Block diagram

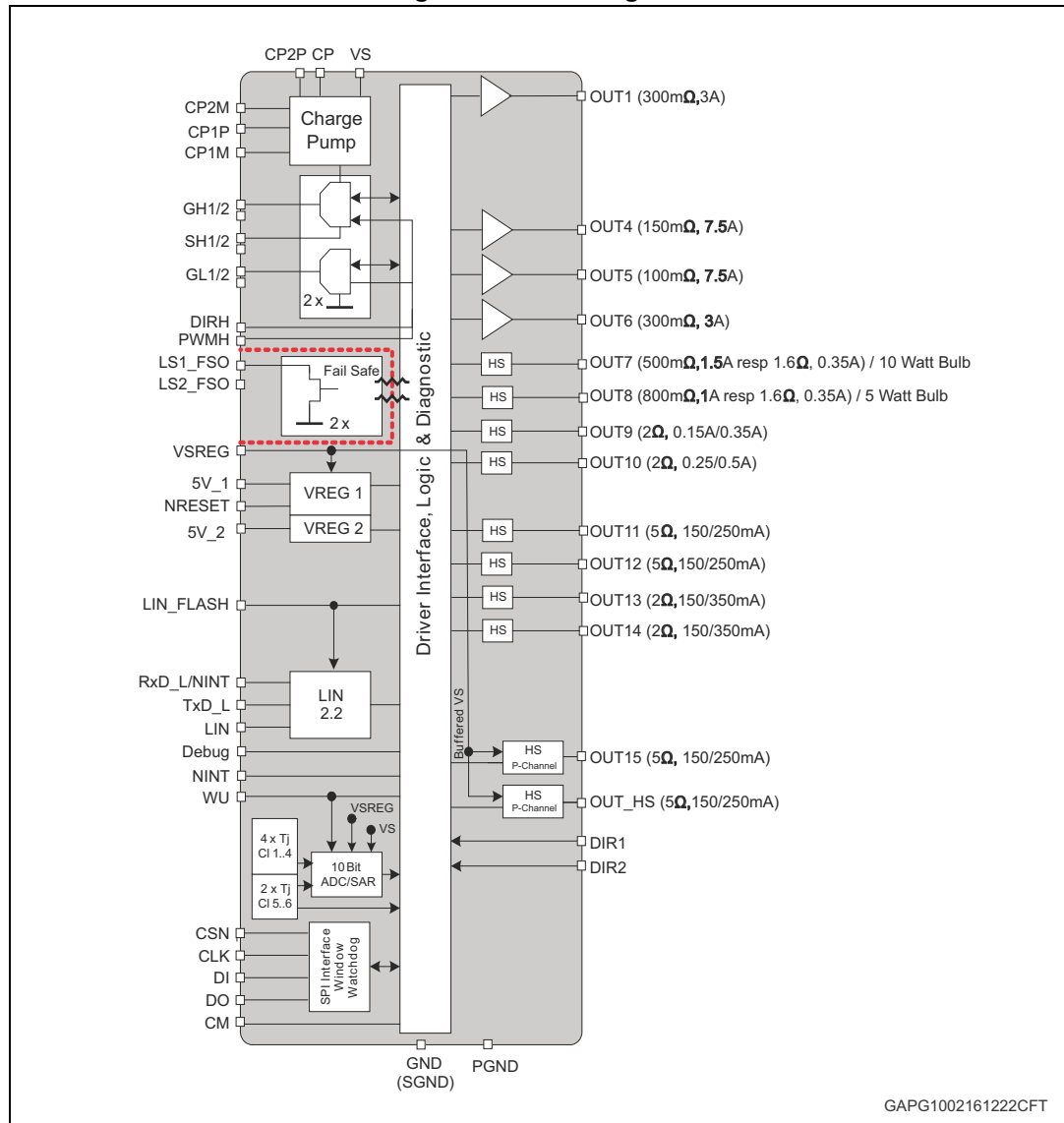


Table 2. Pin definitions and functions

| Pin | Symbol | Function                                                                      |
|-----|--------|-------------------------------------------------------------------------------|
| 1   | WU     | Wake-up Input: Input pin for static or cyclic monitoring of external contacts |
| 2   | CP2M   | Charge pump pin for capacitor 2, negative side                                |
| 3   | CP2P   | Charge pump pin for capacitor 2, positive side                                |
| 4   | CP     | Charge pump output                                                            |
| 5   | CP1P   | Charge pump pin for capacitor 1, positive side                                |
| 6   | CP1M   | Charge pump pin for capacitor 1, negative side                                |

Table 2. Pin definitions and functions (continued)

| Pin | Symbol        | Function                                                                                                                                                                                                                                                                                                                       |
|-----|---------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7   | NC            | Not connected                                                                                                                                                                                                                                                                                                                  |
| 8   | NC            | Not connected                                                                                                                                                                                                                                                                                                                  |
| 9   | OUT14         | High-side-driver output to drive LEDs                                                                                                                                                                                                                                                                                          |
| 10  | OUT13         | High-side-driver output to drive LEDs                                                                                                                                                                                                                                                                                          |
| 11  | OUT12         | High-side-driver output to drive LEDs                                                                                                                                                                                                                                                                                          |
| 12  | OUT9          | High-side-driver output to drive LEDs                                                                                                                                                                                                                                                                                          |
| 13  | OUT10         | High-side-driver-output                                                                                                                                                                                                                                                                                                        |
| 14  | OUT11         | High-side-driver output to drive LEDs                                                                                                                                                                                                                                                                                          |
| 15  | LS1_FSO       | Fail Safe low-side switch (Active low)                                                                                                                                                                                                                                                                                         |
| 16  | LS2_FSO       | Fail Safe low-side switch (Active low)                                                                                                                                                                                                                                                                                         |
| 17  | VS            | Power supply voltage for power stage outputs (external reverse battery protection required), for this input a ceramic capacitor as close as possible to GND is recommended. Important: For the capability of driving, the full current at the outputs all pins of VS must be connected externally!                             |
| 18  | VS; 2nd pin   | Current capability (pin description see above)                                                                                                                                                                                                                                                                                 |
| 19  | OUT7          | High-side-driver output to drive LEDs or a 10 Watt bulb (programmable $R_{dson}$ )                                                                                                                                                                                                                                             |
| 20  | OUT6          | Half-bridge outputs: the output is built by a high-side and a low-side switch which are internally connected. The output stage of both switches is a power DMOS transistor. Each driver has an internal parasitic reverse diode (bulk-drain-diode: high-side driver from output to VS, low-side driver from GND to output)     |
| 21  | OUT1          | Half-bridge outputs: the output is built by a high-side and a low-side switch which are internally connected. The output stage of both switches is a power DMOS transistor. Each driver has an internal parasitic reverse diode (bulk-drain-diode: high-side driver from output to VS, low-side driver from GND to output)     |
| 22  | NC            | Not connected                                                                                                                                                                                                                                                                                                                  |
| 23  | OUT5          | Half-bridge outputs: the output is built by a high-side and a low-side switch which are internally connected. The output stage of both switches is a power DMOS transistor. Each driver has an internal parasitic reverse diode (bulk-drain-diode: high-side driver from output to $V_S$ , low-side driver from GND to output) |
| 24  | OUT5; 2nd pin | Current capability (pin description see above)                                                                                                                                                                                                                                                                                 |
| 25  | $V_{SREG}$    | Power supply voltage to supply the internal voltage regulators, OUT15 and the OUT_HS (external reverse battery protection required / Diode) for this input a ceramic capacitor as close as possible to GND and an electrolytic back up capacitor is recommended.                                                               |
| 26  | OUT_HS        | High-side-driver output to drive LEDs or to supply contacts                                                                                                                                                                                                                                                                    |

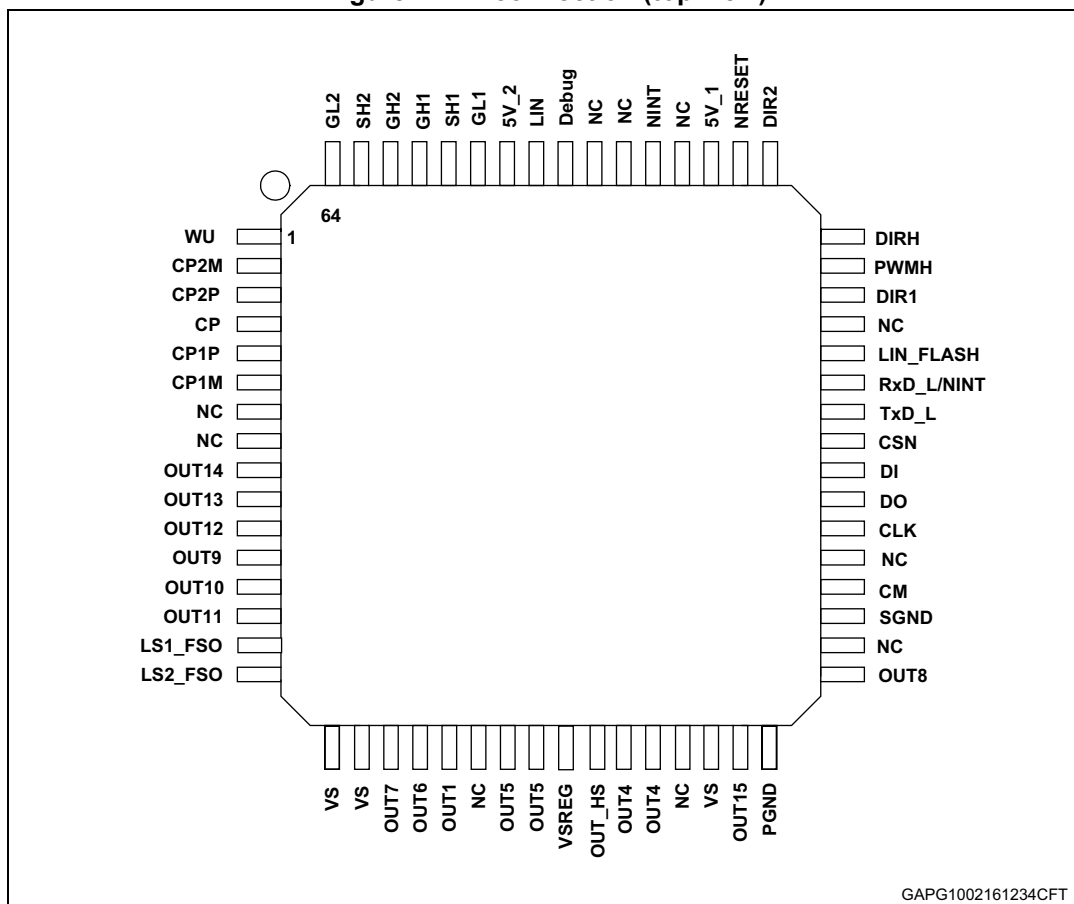
Table 2. Pin definitions and functions (continued)

| Pin | Symbol                    | Function                                                                                                                                                                                                                                                                                                                       |
|-----|---------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 27  | OUT4                      | Half-bridge outputs: the output is built by a high-side and a low-side switch which are internally connected. The output stage of both switches is a power DMOS transistor. Each driver has an internal parasitic reverse diode (bulk-drain-diode: high-side driver from output to $V_S$ , low-side driver from GND to output) |
| 28  | OUT4; 2 <sup>nd</sup> pin | Current capability (pin description see above)                                                                                                                                                                                                                                                                                 |
| 29  | NC                        | Not connected                                                                                                                                                                                                                                                                                                                  |
| 30  | VS; 3rd pin               | Current capability (for the pin description see above)                                                                                                                                                                                                                                                                         |
| 31  | OUT15                     | High-side-driver output to drive LEDs                                                                                                                                                                                                                                                                                          |
| 32  | PGND                      | Power GND                                                                                                                                                                                                                                                                                                                      |
| 33  | OUT8                      | High-side-driver output to drive LEDs or a 5 Watt bulb (programmable $R_{dson}$ )                                                                                                                                                                                                                                              |
| 34  | NC                        | Not connected                                                                                                                                                                                                                                                                                                                  |
| 35  | SGND                      | Signal Ground                                                                                                                                                                                                                                                                                                                  |
| 36  | CM                        | Current monitor output: depending on the selected multiplexer bits $CM\_SEL\_x$ (CR 7) of the; Control Register this output sources an image of the instant current; through the corresponding high-side driver with a fixed ratio                                                                                             |
| 37  | NC                        | Not connected                                                                                                                                                                                                                                                                                                                  |
| 38  | CLK                       | SPI: serial clock input                                                                                                                                                                                                                                                                                                        |
| 39  | DO                        | SPI: serial data output (push pull output stage)                                                                                                                                                                                                                                                                               |
| 40  | DI                        | SPI: serial data input                                                                                                                                                                                                                                                                                                         |
| 41  | CSN                       | SPI: chip select not input                                                                                                                                                                                                                                                                                                     |
| 42  | TxD_L                     | LIN Transmit data input                                                                                                                                                                                                                                                                                                        |
| 43  | RxD_L/NINT                | RxDL -> LIN receive data output; NINT -> indicates local/remote wake-up events (push pull output stage)                                                                                                                                                                                                                        |
| 44  | LIN_FLASH                 | LIN Flash Mode enable (former TxD_C pin, to guarantee family compatibility)                                                                                                                                                                                                                                                    |
| 45  | NC                        | Not connected                                                                                                                                                                                                                                                                                                                  |
| 46  | DIR1                      | Direct Drive Input 1                                                                                                                                                                                                                                                                                                           |
| 47  | PWMH                      | PWMH input: this input signal can be used to control the H-bridge Gate Drivers.                                                                                                                                                                                                                                                |
| 48  | DIRH                      | Direction Input: this input controls the H-bridge Drivers for the external MOSFETs                                                                                                                                                                                                                                             |
| 49  | DIR2                      | Direct Drive Input 2                                                                                                                                                                                                                                                                                                           |
| 50  | NRESET                    | NReset output to micro controller; (reset state = LOW) (low-side switch with drain connected to the output pin and internal pull up resistance to 5V_1)                                                                                                                                                                        |
| 51  | 5V_1                      | Voltage regulator 1 output: 5 V supply e.g. micro controller                                                                                                                                                                                                                                                                   |
| 52  | NC                        | Not connected                                                                                                                                                                                                                                                                                                                  |

Table 2. Pin definitions and functions (continued)

| Pin | Symbol | Function                                                                                                                                                |
|-----|--------|---------------------------------------------------------------------------------------------------------------------------------------------------------|
| 53  | NINT   | Interrupt output (low active; push-pull output stage) to indicate $V_{SREG}$ early warning (Active mode); indicates wake-up events from V1_standby mode |
| 54  | NC     | Not connected                                                                                                                                           |
| 55  | NC     | Not connected                                                                                                                                           |
| 56  | Debug  | Debug input to deactivate the window watchdog (high active)                                                                                             |
| 57  | LIN    | LIN bus line                                                                                                                                            |
| 58  | 5V_2   | Voltage regulator 2 output: 5 V supply for external loads (potentiometer, sensors). V2 is protected against reverse supply                              |
| 59  | GL1    | Gate driver for PowerMOS low-side switch in half-bridge 1                                                                                               |
| 60  | SH1    | Source of high-side switch in half-bridge 1                                                                                                             |
| 61  | GH1    | Gate driver for PowerMOS high-side switch in half-bridge 1                                                                                              |
| 62  | GH2    | Gate driver for PowerMOS high-side switch in half-bridge 2                                                                                              |
| 63  | SH2    | Source of high-side switch in half-bridge 2                                                                                                             |
| 64  | GL2    | Gate driver for PowerMOS low-side switch in half-bridge 2                                                                                               |

Figure 2. Pin connection (top view)



### 3 Electrical specifications

#### 3.1 Absolute maximum ratings

Stressing the device above the rating listed in [Table 3](#) may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability

**Table 3. Absolute maximum ratings**

| Symbol                                                                                                                | Parameter / test condition                                    | Value [DC voltage]                                                | Unit |
|-----------------------------------------------------------------------------------------------------------------------|---------------------------------------------------------------|-------------------------------------------------------------------|------|
| $V_S, V_{SREG}$                                                                                                       | DC supply voltage / "jump start"                              | -0.3 to +28                                                       | V    |
|                                                                                                                       | Load dump                                                     | -0.3 to +40                                                       | V    |
| 5V_1                                                                                                                  | Stabilized supply voltage, logic supply                       | -0.3 to 6.5<br>$V_1 < V_{SREG}$                                   | V    |
| 5V_2 <sup>(1)</sup>                                                                                                   | Stabilized supply voltage                                     | -0.3 to +28 <sup>(2)</sup>                                        | V    |
| $V_{DI}, V_{CLK}, V_{CSN}, V_{DO}, V_{RXDL/NINT}, V_{NRESET}, V_{CM}, V_{DIR}, V_{DIR2}, V_{PWMH}, V_{DIRH}, V_{INT}$ | Logic input / output voltage range                            | -0.3 to $V_1+0.3$                                                 | V    |
| $V_{LIN\_FLASH}, V_{TXDL}$                                                                                            | Multi Level Inputs                                            | -0.3 to 40                                                        | V    |
| $V_{Debug}$                                                                                                           | Debug input pin voltage range                                 | -0.3 to 40                                                        | V    |
| $V_{LS1\_FSO}, V_{LS2\_FSO}$                                                                                          | Output voltage range of Fail-Safe low-side Switches           | -0.3 to 35                                                        | V    |
| $V_{WU}$                                                                                                              | DC Wake up input voltage / "jump start"                       | -0.3 to +28                                                       | V    |
|                                                                                                                       | Load dump                                                     | -0.3 to +40                                                       | V    |
| $V_{LIN}$                                                                                                             | LIN bus I/O voltage range                                     | -20 to +40                                                        | V    |
| $I_{Input}^{(3)}$                                                                                                     | Current injection into $V_S$ related input pins               | 20                                                                | mA   |
| $I_{OUT\_INJ}^{(3)}$                                                                                                  | Current injection into $V_S$ related outputs                  | 20                                                                | mA   |
| $V_{OUTn}, V_{out\_HS}$                                                                                               | Output voltage (n = 1 to 15)                                  | -0.3 to $V_S+0.3$                                                 | V    |
| $V_{GH1}, V_{GH2} (V_{Gxy})$                                                                                          | High Voltage Signal Pins                                      | $V_{Sxy}-0.3$ to $V_{Sxy}+13; V_{CP}+0.3$                         | V    |
| $V_{GL1}, V_{GL2} (V_{Gxy})$                                                                                          | High Voltage Signal Pins                                      | $V_{Sxy}-0.3$ to $V_{Sxy}+13; V_{CP}-0.3V$ to +12V; $V_{cp}+0.3V$ | V    |
| $V_{SH1}, V_{SH2} (V_{Sxy})$                                                                                          | High Voltage Signal Pins                                      | -1 to 40                                                          | V    |
|                                                                                                                       | High Voltage Signal Pins; single pulse with $t_{max} = 200ns$ | -5 to 40                                                          | V    |
| $V_{CP1P}$                                                                                                            | High Voltage Signal Pins                                      | $V_S-0.3$ to $V_S+14$                                             | V    |
| $V_{CP2P}$                                                                                                            | High Voltage Signal Pins                                      | $V_S-0.6$ to $V_S+14$                                             | V    |

Table 3. Absolute maximum ratings (continued)

| Symbol                                                                                    | Parameter / test condition                                                                 | Value [DC voltage]    | Unit |
|-------------------------------------------------------------------------------------------|--------------------------------------------------------------------------------------------|-----------------------|------|
| $V_{CP1M}, V_{CP2M}$                                                                      | High Voltage Signal Pins                                                                   | -0.3 to $V_S+0.3$     | V    |
| $V_{CP}$                                                                                  | High Voltage Signal Pin $V_S \leq 26$ V                                                    | $V_S-0.3$ to $V_S+14$ | V    |
|                                                                                           | High Voltage Signal Pin $V_S > 26$ V                                                       | $V_S-0.3$ to +40      | V    |
| $I_{OUT9}, I_{OUT10}, I_{OUT11}, I_{OUT12}, I_{OUT13}, I_{OUT14}, I_{OUT15}, I_{OUT\_HS}$ | Output current <sup>(2)</sup>                                                              | $\pm 1.25$            | A    |
| $I_{OUT8}$                                                                                |                                                                                            | $\pm 2.5$             | A    |
| $I_{OUT7}$                                                                                |                                                                                            | $\pm 5$               | A    |
| $I_{OUT1,6}$                                                                              |                                                                                            | $\pm 5$               | A    |
| $I_{OUT4,5}$                                                                              |                                                                                            | $\pm 10$              | A    |
| $I_{VScum}$                                                                               | Maximum cumulated current at $V_S$ drawn by OUT1 <sup>(2)</sup>                            | $\pm 7.5$             | A    |
|                                                                                           | Maximum cumulated current at $V_S$ drawn by OUT8 & OUT10 <sup>(2)</sup>                    | $\pm 2.5$             | A    |
|                                                                                           | Maximum cumulated current at $V_S$ drawn by OUT4 <sup>(2)</sup>                            | $\pm 10$              | A    |
|                                                                                           | Maximum cumulated current at $V_S$ drawn by OUT5 <sup>(2)</sup>                            | $\pm 10$              | A    |
|                                                                                           | Maximum cumulated current at $V_S$ drawn by OUT6 & OUT7 <sup>(2)</sup>                     | $\pm 7.5$             | A    |
|                                                                                           | Maximum cumulated current at $V_S$ drawn by OUT9, OUT11, OUT12, OUT13, OUT14, OUT15 and CP | $\pm 2.5$             | A    |
| $I_{VSREG}$                                                                               | Maximum current at $V_{SREG}$ pin <sup>(2)</sup> (5V_1, 5V_2 and OUT_HS)                   | $\pm 2.5$             | A    |
| $I_{PGNDcum}$                                                                             | Maximum cumulated current at PGND drawn by OUT1 & OUT6 <sup>(2)</sup>                      | $\pm 7.5$             | A    |
|                                                                                           | Maximum cumulated current at PGND drawn by OUT5 <sup>(2)</sup>                             | $\pm 12.5$            | A    |
|                                                                                           | Maximum cumulated current at PGND drawn by OUT4 <sup>(2)</sup>                             | $\pm 12.5$            | A    |
| $I_{SGND}$                                                                                | Maximum current at SGND <sup>(2)</sup>                                                     | $\pm 1.25$            | A    |
| GND pins                                                                                  | PGND versus SGND                                                                           | -0.3 to 0.3           | V    |

- 5V\_2 is robust against SC to 28 V only in case  $V_{SREG}$  is supplied.
- Values for the absolute maximum DC current through the bond wires. This value does not consider maximum power dissipation or other limits.
- Guaranteed by design.

**Note:** All maximum ratings are absolute ratings. Leaving the limitation of any of these values may cause an irreversible damage of the integrated circuit!

**Note:** *Loss of ground or ground shift with externally grounded loads: ESD structures are configured for nominal currents only. If external loads are connected to different grounds, the current load must be limited to this nominal current.*

## 3.2 ESD protection

**Table 4. ESD protection**

| Parameter                                                   | Value                                                              | Unit |
|-------------------------------------------------------------|--------------------------------------------------------------------|------|
| All pins <sup>(1)</sup>                                     | +/-2                                                               | kV   |
| All power output pins <sup>(2)</sup> : OUT1 – OUT15, OUT_HS | +/-4                                                               | kV   |
| LIN                                                         | +/-8 <sup>(2)</sup><br>+/-10 <sup>(3)</sup><br>+/-6 <sup>(4)</sup> | kV   |
| All pins <sup>(5)</sup>                                     | +/-500                                                             | V    |
| Corner pins <sup>(5)</sup>                                  | +/-750 <sup>(6)</sup>                                              | V    |
| All pins <sup>(7)</sup>                                     | +/- 200                                                            | V    |

1. HBM (human body model, 100 pF, 1.5 kΩ) according to MIL 883C, Method 3015.7 or EIA/JESD22A114-A.
2. HBM with all none zapped pins grounded.
3. Indirect ESD Test according to IEC 61000-4-2 (150 pF, 330 Ω) and 'Hardware Requirements for LIN, CAN and Flexray Interfaces in Automotive Applications' (version 1.3, 2012-05-04).
4. Direct ESD Test according to IEC 61000-4-2 (150 pF, 330 Ω) and 'Hardware Requirements for LIN, CAN and Flexray Interfaces in Automotive Applications' (version 1.3, 2012-05-04).
5. Charged device model.
6. For WU, these limits are referred to one-zap stress; in case of three-zap stress, the limits are +750V/-400V.
7. Machine model; C = 220 pF, R = 0 Ω.

## 3.3 Thermal data

**Table 5. Operating junction temperature**

| Symbol         | Parameter                      | Value      | Unit |
|----------------|--------------------------------|------------|------|
| T <sub>j</sub> | Operating junction temperature | -40 to 175 | °C   |

All parameters are guaranteed in the junction temperature range -40 to 150°C (unless otherwise specified); the device is still operative and functional at higher temperatures (up to 175°C).

**Note:** *Parameters limits at higher junction temperatures than 150°C may change respect to what is specified as per the standard temperature range.*

**Note:** *Device functionality at high junction temperature is guaranteed by characterization.*

Table 6. Temperature warning and thermal shutdown

| Symbol        | Parameter                                 |                                           | Min.       | Typ.       | Max.       | Unit |
|---------------|-------------------------------------------|-------------------------------------------|------------|------------|------------|------|
| $T_W$         | Thermal overtemperature warning threshold | $T_j^{(1)}$                               | 140        | 150        | 160        | °C   |
| $T_{SD1}$     | Thermal shutdown junction temperature 1   | $T_j^{(1)}$<br>Cluster 1-4<br>Cluster 5-6 | 165<br>165 | 175<br>175 | 185<br>190 | °C   |
| $T_{SD2}$     | Thermal shutdown junction temperature 2   | $T_j^{(1)}$                               | 175        | 185        | 195        | °C   |
| $T_{SD12hys}$ |                                           | Hysteresis                                |            | 5          |            | °C   |
| $T_{jft}$     | Thermal warning / shutdown filter time    |                                           |            | 32         |            | µs   |

1. Non-overlapping.

### 3.3.1 LQFP64 thermal data

Devices belonging to L99DZxxx family embed a multitude of junctions (i.e. Outputs based on a PowerMOSFET stage) housed in a relatively small piece of silicon. The most complex device contains, among all the described features, 6 half-bridges (12 N-Channel PowerMOS), 10 high-sides and two voltage regulators; all the other derivatives, even if smaller than the family super set device, still contain a significant number of junctions.

For this reason, using the Thermal Impedance of a single junction (i.e. voltage regulator or major power dissipation contributor) does not allow to predict thermal behavior of the whole device and therefore it is not possible to assess if a device is thermally suitable for a given activation profile and loads characteristics.

Thermal information is provided as temperature reading by different clusters placed close to the most dissipative junctions.

Some representative and realistic worst-case thermal profiles are described in the below paragraph.

Following measurement methods can be easily implemented, by final user, for a specific activation profile.

#### L99DZ120 thermal profiles

##### Profile 1

Battery Voltage: 16V, Ambient temperature start: 85°C

DC activation

- V1 charged with 70 mA (DC activation)
- V2 charged with 30 mA (DC activation)
- OUT7: 1 x10W bulb (DC activation)
- OUT8: 1 x 5W bulb (DC activation)
- OUT11: 300 Ω resistor (DC activation)
- OUT12: 300 Ω resistor (DC activation)
- OUT13: 300 Ω resistor (DC activation)
- OUT14: 300 Ω resistor (DC activation)

## Cyclic activation

- OUT4 – OUT5: 3,3  $\Omega$  resistor placed across those outputs
  - 10 activations of Lock/Un-lock (250 ms ON Lock; 500 ms wait; 250 ms ON Un-lock unlock; 500 ms wait)
- OUT5 – OUT6: 10  $\Omega$  resistor placed across those outputs
  - (250 ms ON Safe Lock; 500 ms wait; 250 ms ON Safe unlock; 500 ms wait)

## Test execution:

Once thermal equilibrium is reached with all DC load active, the “Cyclic Activation” sequence is applied.

Temperature reading is logged just at the end of the whole sequence.

Figure 3. Activation profile 1

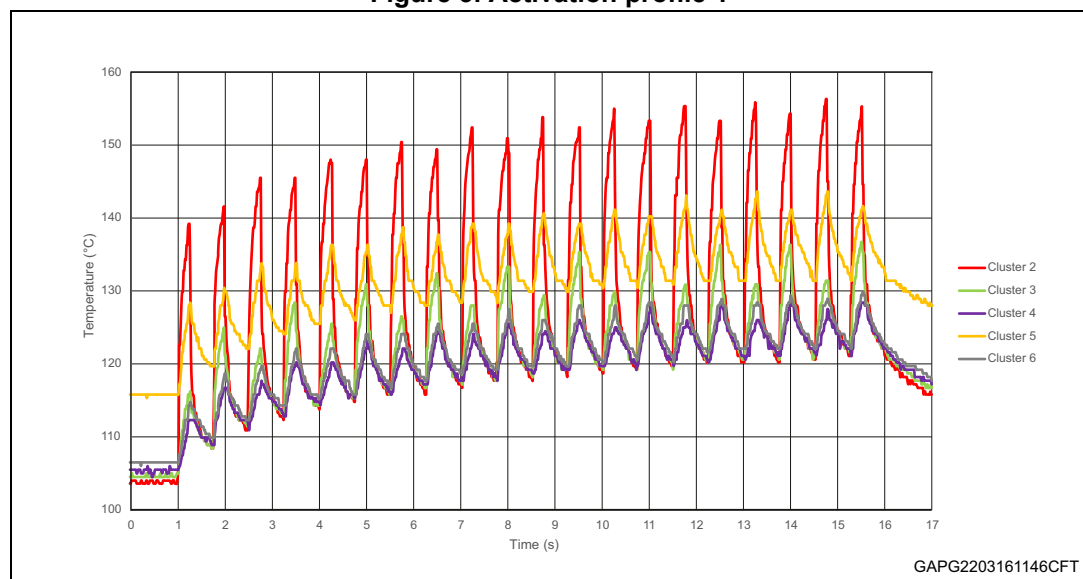
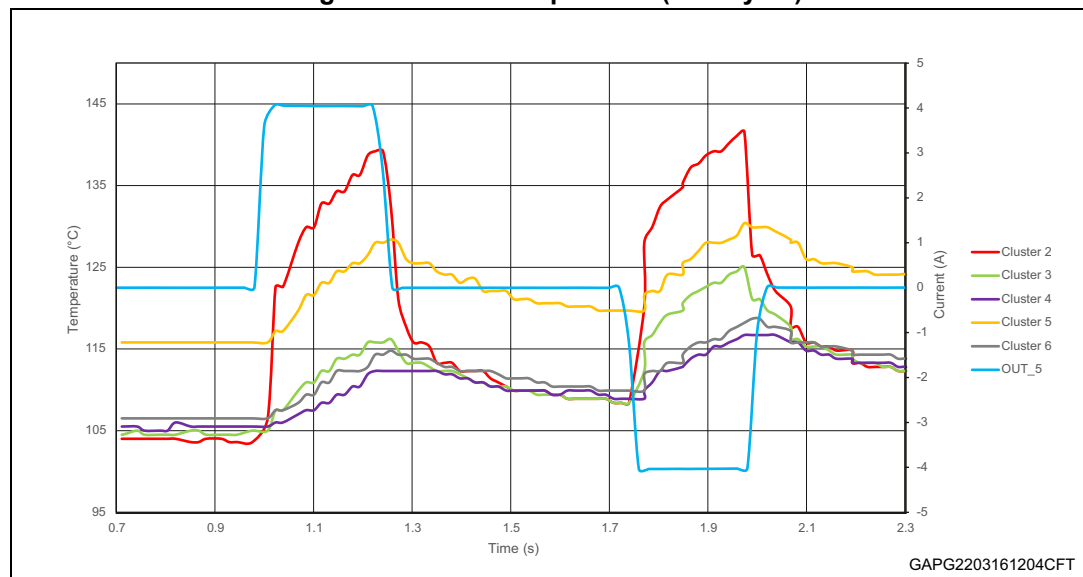


Figure 4. Activation profile 1 (first cycle)



Note: All curves are plotted interpolating measured samples with 15 ms of period.

### Profile 2

Battery Voltage: 16V, Ambient temperature start: 85°C

DC activation

- V1 charged with 70 mA (DC activation)
- V2 charged with 30 mA (DC activation)
- OUT7: 1 x10W bulb (DC activation)
- OUT8: 1 x 5W bulb (DC activation)
- OUT11: 300  $\Omega$  resistor (DC activation)
- OUT12: 300  $\Omega$  resistor (DC activation)
- OUT13: 300  $\Omega$  resistor (DC activation)
- OUT14: 300  $\Omega$  resistor (DC activation)

Cyclic activation

- OUT1 – OUT6: 6,8  $\Omega$  resistor placed across those outputs
  - 2 activations (3s ON; 1s OFF; 2x)

Test execution:

Once thermal equilibrium is reached with all DC load active, the “Cyclic Activation” sequence is applied.

Figure 5. Activation profile 2

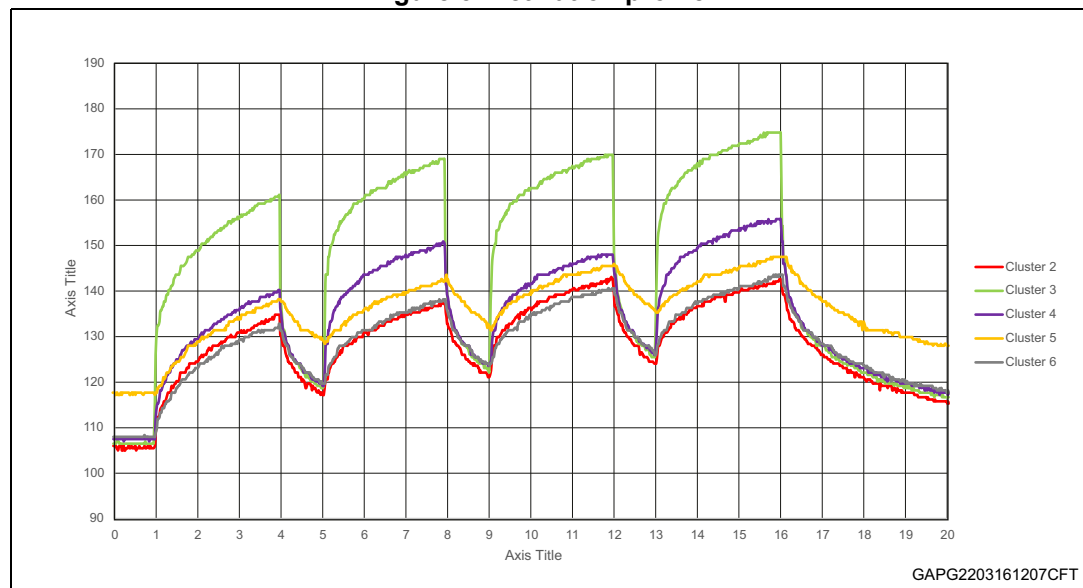
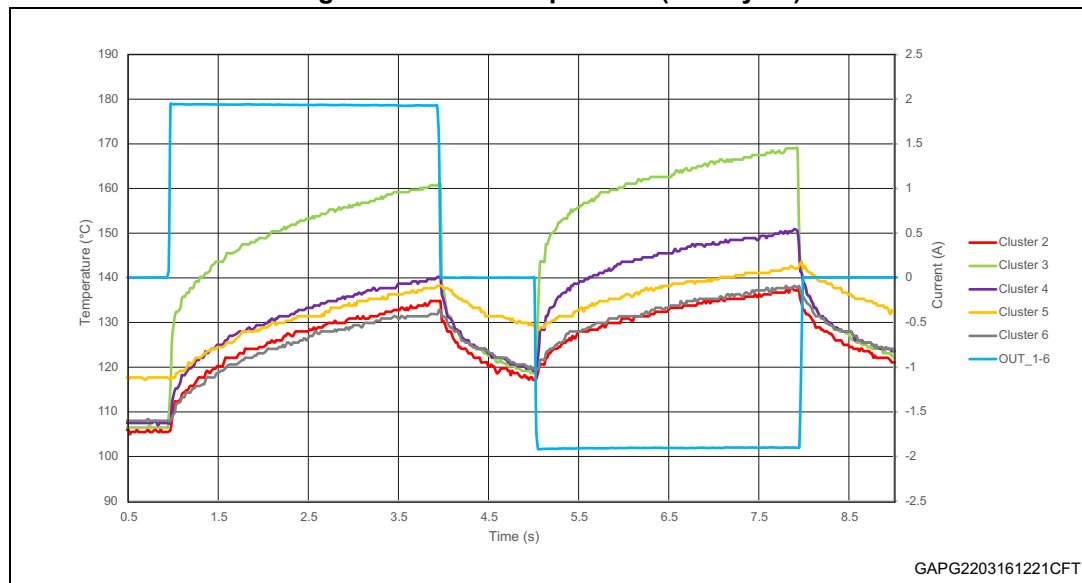
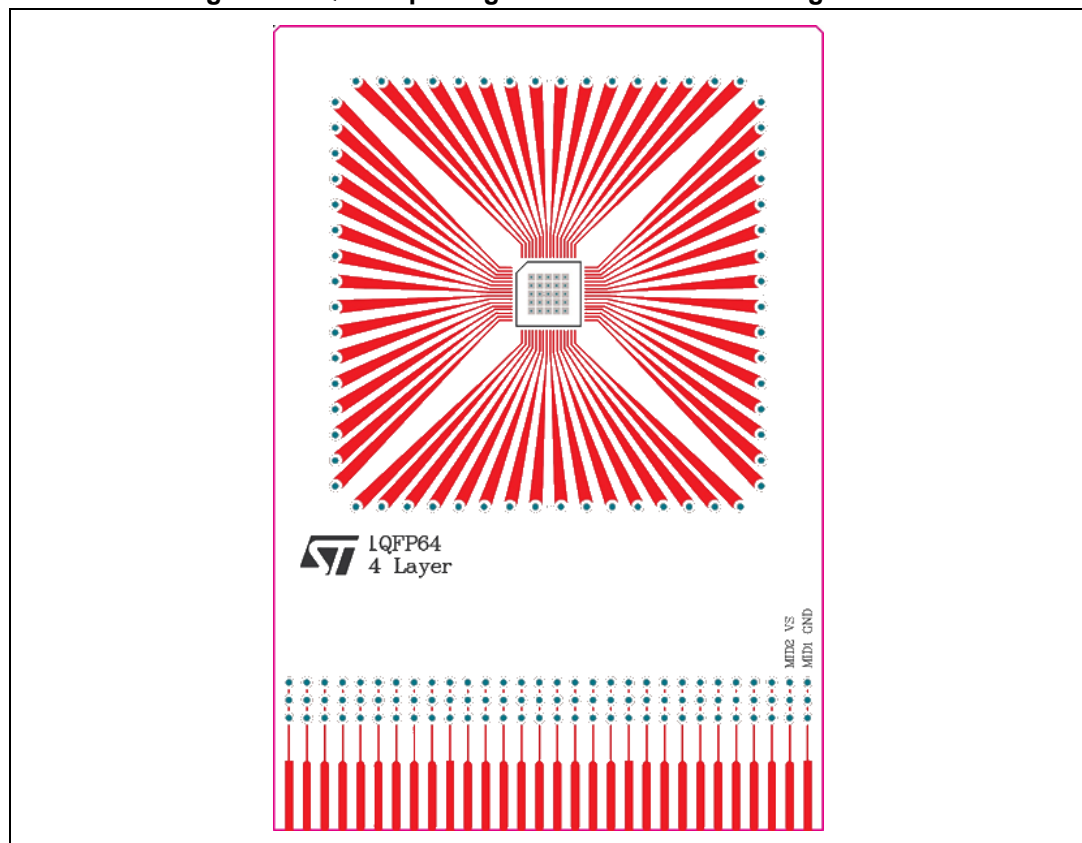


Figure 6. Activation profile 2 (first cycle)



Note: All curves are plotted interpolating measured samples with 15 ms of period.

Figure 7. LQFP64 package and PCB thermal configuration



Note: Layout condition for Thermal Characterization (board finishing thickness 1.5 mm +/- 10%, board four layers, board dimension 77 mm x 114 mm, board material FR4, Cu thickness 0,070 mm for outer layers, 0.0035 mm for inner layers, thermal vias separation 1.2 mm).

## 3.4 Electrical characteristics

### 3.4.1 Supply and supply monitoring

All SPI communication, logic and oscillator parameters are working down to  $V_{SREG} = 3.5\text{ V}$  and parameters are as specified in the following chapters (guaranteed by design).

- SPI thresholds
- Oscillator frequency (delay times correctly elapsed)
- Internal register status correctly kept (reset at default values for  $V_{SREG} < V_{POR}$ )
- Reset threshold correctly detected

The voltages are referred to ground and currents are assumed positive, when the current flows into the pin.  $6\text{ V} \leq V_S \leq 28\text{ V}$ ;  $6\text{ V} \leq V_{SREG} \leq 28\text{ V}$ ;  $T_j = -40\text{ }^\circ\text{C}$  to  $150\text{ }^\circ\text{C}$ , unless otherwise specified.

**Table 7. Supply and supply monitoring**

| Symbol           | Parameter                                                                               | Test condition                                                                                                       | Min. | Typ. | Max. | Unit          |
|------------------|-----------------------------------------------------------------------------------------|----------------------------------------------------------------------------------------------------------------------|------|------|------|---------------|
| $V_{SUV}$        | $V_S$ undervoltage threshold                                                            | $V_S$ increasing / decreasing                                                                                        | 4.7  |      | 5.4  | V             |
| $V_{hyst\_UV}$   | $V_S$ undervoltage hysteresis                                                           |                                                                                                                      | 0.04 | 0.1  | 0.2  | V             |
| $V_{SOV}$        | $V_S$ overvoltage threshold                                                             | $V_S$ increasing                                                                                                     | 20   |      | 22.5 | V             |
|                  |                                                                                         | $V_S$ decreasing                                                                                                     | 18.5 |      | 22.5 |               |
| $V_{hyst\_OV}$   | $V_S$ overvoltage hysteresis                                                            |                                                                                                                      | 0.5  | 1    | 1.5  | V             |
| $V_{SREG\_UV}$   | $V_{SREG}$ undervoltage threshold                                                       | $V_{SREG}$ increasing / decreasing                                                                                   | 4.2  |      | 4.9  | V             |
| $V_{hyst\_UV}$   | $V_{SREG}$ undervoltage hysteresis                                                      |                                                                                                                      | 0.04 | 0.1  | 0.2  | V             |
| $V_{SREG\_OV}$   | $V_{SREG}$ overvoltage threshold                                                        | $V_{SREG}$ increasing                                                                                                | 20   |      | 22.5 | V             |
|                  |                                                                                         | $V_{SREG}$ decreasing                                                                                                | 18.5 |      | 22.5 |               |
| $V_{hyst\_OV}$   | $V_{SREG}$ overvoltage hysteresis                                                       |                                                                                                                      | 0.5  | 1    | 1.5  | V             |
| $t_{ovuv\_filt}$ | $V_S/V_{SREG}$ over/undervoltage filter time                                            |                                                                                                                      |      | 64   |      | $\mu\text{s}$ |
| $I_{V(act)}$     | Current consumption in Active mode                                                      | $V_S = V_{SREG} = 12\text{ V}$ ;<br>TxD LIN = high; V1 = ON;<br>V2 = ON; HS/LS Driver OFF;<br>CP = ON                |      | 11   | 14   | mA            |
| $I_{V(BAT)}$     | Current consumption in $V_{bat\_standby}$ mode <sup>(1)</sup>                           | $V_S = 12\text{ V}$ ; Both voltage regulators deactivated; HS/LS Driver OFF                                          | 8    | 16   | 30   | $\mu\text{A}$ |
| $I_{V(BAT)CS}$   | Current consumption in $V_{bat\_standby}$ mode with cyclic sense enabled <sup>(1)</sup> | $V_S = 12\text{ V}$ ; Both voltage regulators deactivated;<br>$T = 50\text{ ms}$ , $t_{ON} = 100\text{ }\mu\text{s}$ | 30   | 80   | 130  | $\mu\text{A}$ |
| $I_{V(BAT)CW}$   | Current consumption in $V_{bat\_standby}$ mode with cyclic wake enabled <sup>(1)</sup>  | $V_S = 12\text{ V}$ ; Both voltage regulators deactivated during standby phase                                       | 30   | 80   | 130  | $\mu\text{A}$ |

Table 7. Supply and supply monitoring (continued)

| Symbol           | Parameter                                                                                                      | Test condition                                                                               | Min. | Typ. | Max. | Unit          |
|------------------|----------------------------------------------------------------------------------------------------------------|----------------------------------------------------------------------------------------------|------|------|------|---------------|
| $I_{V(V1stby)}$  | Current consumption in $V_{1\_standby}$ mode <sup>(1)</sup>                                                    | $V_S = 12\text{ V}$ ; Voltage regulator V1 active; ( $I_{V1} = 0$ ); HS/LS Driver OFF        | 16   | 50   | 70   | $\mu\text{A}$ |
|                  | Current consumption in $V_{1\_standby}$ mode <sup>(1) (2)</sup>                                                | $V_S = 12\text{ V}$ ; Voltage regulator V1 active; ( $I_{V1} = I_{CMP}$ ); HS/LS Driver OFF  |      |      | 196  | $\mu\text{A}$ |
|                  | Current consumption in $V_{1\_standby}$ mode <sup>(1)</sup>                                                    | $V_S = 12\text{ V}$ ; Voltage regulator V1 active; ( $I_{V1} = I_{PEAK}$ ); HS/LS Driver OFF |      |      | 436  | $\mu\text{A}$ |
| $I_{qLIN}$       | Quiescent current adder for LIN wake up activated                                                              | Guaranteed by design                                                                         |      | 0    |      | $\mu\text{A}$ |
| $I_{OUT\_HS}$    | Additional bias quiescent current for switched on OUT_HS or OUT15 by DIR or Timer; value for 1 output          | Guaranteed by design                                                                         |      | 620  | 1100 | $\mu\text{A}$ |
| $I_{OUTHS\_DIR}$ | Quiescent current adder if OUT_HS and/or OUT15 are configured for Direct Drive; value during output off        | Guaranteed by design                                                                         |      | 0    | 5    | $\mu\text{A}$ |
| $I_{timer}$      | Quiescent current adder if timer1 and/or timer 2 are active to provide interrupt on NINT upon timer expiration | Guaranteed by design                                                                         |      | 65   | 110  | $\mu\text{A}$ |

1. Conditions for specified current consumption:

- $V_{LIN} > (V_S - 1.5\text{ V})$
- $V_{WU} < 1\text{ V}$  or  $V_{WU} > (V_S - 1.5\text{ V})$

2.  $I_q = I_{q0} + 2\% \cdot I_{LOAD}$  (see also [Figure 8: Voltage regulator V1 characteristics \(quiescent current and accuracy\)](#))

### 3.4.2 Oscillator

The voltages are referred to ground and currents are assumed positive, when the current flows into the pin.  $6\text{ V} \leq V_S \leq 28\text{ V}$ ;  $6\text{ V} \leq V_{SREG} \leq 28\text{ V}$ ;  $T_j = -40\text{ }^\circ\text{C}$  to  $150\text{ }^\circ\text{C}$ , unless otherwise specified.

Table 8. Oscillator

| Symbol           | Parameter                  | Test condition | Min. | Typ. | Max. | Unit |
|------------------|----------------------------|----------------|------|------|------|------|
| $f_{CLK1}^{(1)}$ | Oscillation frequency OSC1 |                | 1.66 | 2.0  | 2.34 | MHz  |
| $f_{CLK2}^{(1)}$ | Oscillation frequency OSC2 |                | 30.4 | 32.0 | 33.6 | MHz  |

1. OSC1: charge pump, SPI, output drivers, watchdog  
OSC2: ADC

### 3.4.3 Power-on reset ( $V_{SREG}$ )

All outputs open;  $T_j = -40\text{ }^\circ\text{C}$  to  $150\text{ }^\circ\text{C}$ , unless otherwise specified.

Table 9. Power-on reset ( $V_{SREG}$ )

| Symbol       | Parameter           | Test condition                    | Min. | Typ. | Max. | Unit |
|--------------|---------------------|-----------------------------------|------|------|------|------|
| $V_{POR\_R}$ | $V_{POR}$ threshold | $V_{SREG}$ rising                 |      | 3.45 | 4.5  | V    |
| $V_{POR\_F}$ | $V_{POR}$ threshold | $V_{SREG}$ falling <sup>(1)</sup> | 2.45 |      | 3.5  | V    |

1. This threshold is valid if  $V_{SREG}$  had already reached  $V_{POR\_R(max)}$  previously.

### 3.4.4 Voltage regulator V1

The voltages are referred to ground and currents are assumed positive, when the current flows into the pin.  $4.5\text{ V} \leq V_S \leq 28\text{ V}$ ;  $4.5\text{ V} \leq V_{SREG} \leq 28\text{ V}$ ;  $T_j = -40\text{ }^\circ\text{C}$  to  $150\text{ }^\circ\text{C}$ , unless otherwise specified.

Table 10. Voltage regulator V1

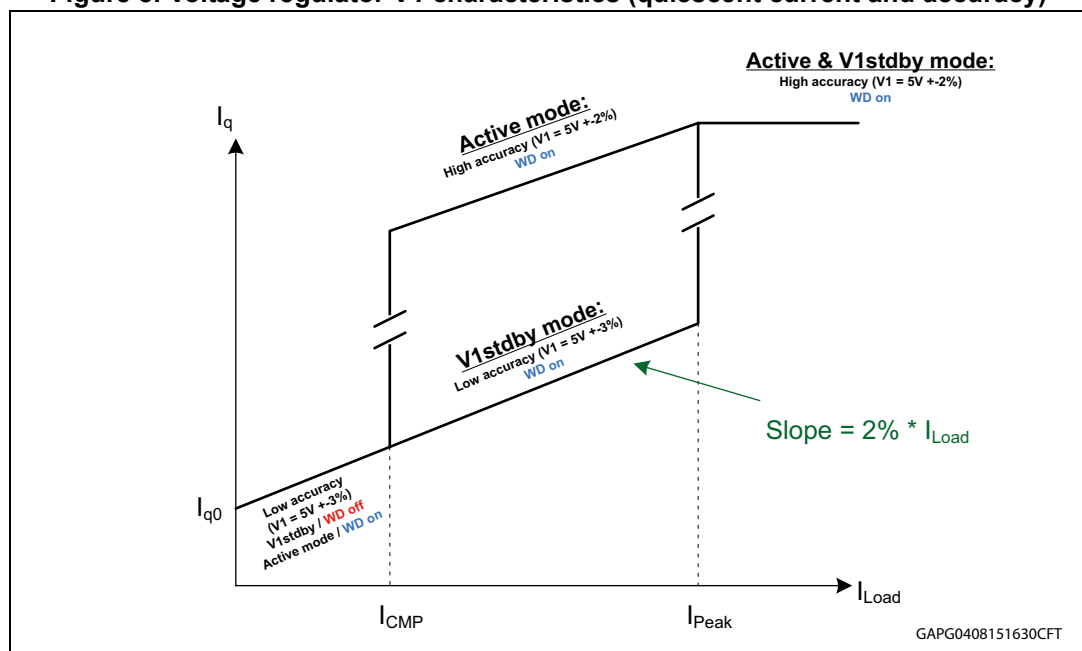
| Symbol             | Parameter                                                       | Test condition                                                                                                                                | Min.                | Typ. | Max. | Unit          |
|--------------------|-----------------------------------------------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------|---------------------|------|------|---------------|
| V1                 | Output voltage                                                  | $V_{SREG} = 13.5\text{ V}$                                                                                                                    |                     | 5.0  |      | V             |
| $V_{SREG\_absmin}$ | $V_{SREG}$ absolute minimum value for controlling NRESET output | $V_{SREG}$ rising/falling                                                                                                                     |                     |      | 2    | V             |
| $V1\_low\_acc$     | Output voltage tolerance low accuracy mode                      | $I_{LOAD} = 0\text{ mA}$ to $I_{CMP}$ ; (Active mode) or $I_{LOAD} = 0\text{ mA}$ to $I_{PEAK}$ ( $V1stdby$ ); $V_{SREG} = 13.5\text{ V}$     | -3                  |      | 3    | %             |
| $V1\_hi\_acc$      | Output voltage tolerance high accuracy mode                     | $I_{LOAD} = I_{CMP}$ to $100\text{ mA}$ ; (Active mode) or $I_{LOAD} = I_{PEAK}$ to $100\text{ mA}$ ( $V1stdby$ ); $V_{SREG} = 13.5\text{ V}$ | -2                  |      | 2    | %             |
| $V1_{250mA}$       | Output voltage tolerance (100 to 250mA)                         | $I_{LOAD} = 250\text{ mA}$ ; $V_{SREG} = 13.5\text{ V}$                                                                                       | -3                  |      | 3    | %             |
| $V_{DP1}$          | Drop-out Voltage                                                | $I_{LOAD} = 50\text{ mA}$ ; $V_{SREG} = 5\text{ V}$                                                                                           |                     | 0.2  | 0.4  | V             |
|                    |                                                                 | $I_{LOAD} = 100\text{ mA}$ ; $V_{SREG} = 5\text{ V}$                                                                                          |                     | 0.3  | 0.5  | V             |
|                    |                                                                 | $I_{LOAD} = 150\text{ mA}$ ; $V_{SREG} = 5\text{ V}$                                                                                          |                     | 0.45 | 0.6  | V             |
| $I_{CC1}$          | Output current in Active mode                                   | Max. continuous load current                                                                                                                  |                     |      | 250  | mA            |
| $I_{CCmax1}$       | Short circuit output current                                    | Current limitation                                                                                                                            | 340                 | 600  | 900  | mA            |
| $C_{load1}$        | Load capacitor1                                                 | Ceramic (+/- 20%)                                                                                                                             | 0.22 <sup>(1)</sup> |      |      | $\mu\text{F}$ |
| $t_{TSD}$          | V1 deactivation time after thermal shut-down                    |                                                                                                                                               |                     | 1    |      | sec           |
| $I_{CMP\_ris}$     | Current comp. rising thresh                                     | Rising current                                                                                                                                | 2                   | 4    | 6    | mA            |
| $I_{CMP\_fal}$     | Current comp. falling threshold                                 | Falling current                                                                                                                               | 1.4                 | 2.8  | 4.2  | mA            |

Table 10. Voltage regulator V1 (continued)

| Symbol                       | Parameter                                            | Test condition  | Min. | Typ. | Max. | Unit          |
|------------------------------|------------------------------------------------------|-----------------|------|------|------|---------------|
| $I_{\text{CMP\_hys}}$        | Current comp. Hysteresis                             |                 |      | 1.2  |      | mA            |
| $I_{\text{Peak\_ris}}^{(2)}$ | Current comp. rising thresh.                         | Rising current  | 6    | 12   | 18   | mA            |
| $I_{\text{Peak\_fal}}^{(2)}$ | Current comp. falling threshold                      | Falling current | 5    | 10   | 15   | mA            |
| $I_{\text{Peak\_hys}}^{(2)}$ | Current comp. Hysteresis                             |                 |      | 2    |      | mA            |
| $V1_{\text{fail}}$           | V1 fail threshold                                    | V1 forced       |      | 2    |      | V             |
| $t_{V1\text{fail}}$          | V1 fail filter time                                  |                 |      | 2    |      | $\mu\text{s}$ |
| $t_{V1\text{short}}$         | V1 short filter time                                 |                 |      | 4    |      | ms            |
| $t_{V1\text{FS}}$            | V1 Fail-Safe Filter Time                             |                 |      | 2    |      | ms            |
| $t_{V1\text{off}}$           | V1 deactivation time after 8 consecutive WD failures | Tested by scan  | 150  | 200  | 250  | ms            |

1. Nominal capacitor value required for stability of the regulator. Tested with 220 nF ceramic (+/- 20%). Capacitor must be located close to the regulator output pin. A 2.2  $\mu\text{F}$  capacitor is recommended to minimize the DPI stress in the application.
2. In Active mode, V1 regulator is switched to high accuracy mode, dropping below the  $I_{\text{CMP}}$  threshold regulator switches to low accuracy mode.

Figure 8. Voltage regulator V1 characteristics (quiescent current and accuracy)



### 3.4.5 Voltage regulator V2

The voltages are referred to ground and currents are assumed positive, when the current flows into the pin.  $4.5\text{ V} \leq V_S \leq 28\text{ V}$ ;  $4.5\text{ V} \leq V_{SREG} \leq 28\text{ V}$ ;  $T_j = -40\text{ }^{\circ}\text{C}$  to  $150\text{ }^{\circ}\text{C}$ , unless otherwise specified.

**Table 11. Voltage regulator V2**

| Symbol               | Parameter                               | Test condition                                          | Min.                | Typ. | Max. | Unit |
|----------------------|-----------------------------------------|---------------------------------------------------------|---------------------|------|------|------|
| V2                   | Output voltage                          | $V_{SREG} = 13.5\text{ V}$                              |                     | 5.0  |      | V    |
| V2_1mA               | Output voltage tolerance (0 to 1 mA)    | $I_{LOAD} = 1\text{ mA}$ ; $V_{SREG} = 13.5\text{ V}$   | -6.5                |      | 6.5  | %    |
| V2_25mA              | Output voltage tolerance (1 to 25 mA)   | $I_{LOAD} = 25\text{ mA}$ ; $V_{SREG} = 13.5\text{ V}$  | -3                  |      | 3    | %    |
| V2_50mA              | Output voltage tolerance (25 to 50 mA)  | $I_{LOAD} = 50\text{ mA}$ ; $V_{SREG} = 13.5\text{ V}$  | -4                  |      | 4    | %    |
| V2_100mA             | Output voltage tolerance (50 to 100 mA) | $I_{LOAD} = 100\text{ mA}$ ; $V_{SREG} = 13.5\text{ V}$ | -4                  |      | 4    | %    |
| V <sub>DP2</sub>     | Drop-out voltage                        | $I_{LOAD} = 25\text{ mA}$ ; $V_{SREG} = 5.25\text{ V}$  |                     | 0.3  | 0.4  | V    |
|                      |                                         | $I_{LOAD} = 50\text{ mA}$ ; $V_{SREG} = 5.25\text{ V}$  |                     | 0.4  | 0.8  | V    |
|                      |                                         | $I_{LOAD} = 100\text{ mA}$ ; $V_{SREG} = 13.5\text{ V}$ |                     | 1    | 1.6  | V    |
| I <sub>CC2</sub>     | Output current in Active mode           | Max. continuous load current                            |                     |      | 50   | mA   |
| I <sub>CCmax2</sub>  | Short circuit output current            | Current limitation                                      | 100                 | 150  | 250  | mA   |
| C <sub>load</sub>    | Load capacitor                          | Ceramic (+/- 20%)                                       | 0.22 <sup>(1)</sup> |      |      | μF   |
| V2 <sub>fail</sub>   | V2 fail threshold                       | V2 forced                                               |                     | 2    |      | V    |
| t <sub>V2fail</sub>  | V2 fail filter time                     |                                                         |                     | 2    |      | μs   |
| t <sub>V2short</sub> | V2 short filter time                    |                                                         |                     | 4    |      | ms   |

1. Nominal capacitor value required for stability of the regulator. Tested with 220 nF ceramic (+/- 20%). Capacitor must be located close to the regulator output pin. A 2.2 μF capacitor is recommended to minimize the DPI stress in the application.

### 3.4.6 Reset output

The voltages are referred to ground and currents are assumed positive, when the current flows into the pin.  $4\text{ V} \leq V_{SREG} \leq 28\text{ V}$ ;  $T_j = -40\text{ }^{\circ}\text{C}$  to  $150\text{ }^{\circ}\text{C}$ , unless otherwise specified.

**Table 12. Reset output**

| Symbol                  | Parameter                | Test condition             | Min. | Typ. | Max. | Unit |
|-------------------------|--------------------------|----------------------------|------|------|------|------|
| V <sub>RT1falling</sub> | Reset threshold voltage1 | V <sub>V1</sub> decreasing | 3.25 | 3.5  | 3.7  | V    |
| V <sub>RT2falling</sub> | Reset threshold voltage2 | V <sub>V1</sub> decreasing | 3.55 | 3.8  | 4    | V    |
| V <sub>RT3falling</sub> | Reset threshold voltage3 | V <sub>V1</sub> decreasing | 3.75 | 4.0  | 4.2  | V    |

Table 12. Reset output (continued)

| Symbol           | Parameter                                                    | Test condition                                | Min. | Typ. | Max. | Unit          |
|------------------|--------------------------------------------------------------|-----------------------------------------------|------|------|------|---------------|
| $V_{RT4falling}$ | Reset threshold voltage4                                     | $V_{V1}$ decreasing                           | 4.1  | 4.3  | 4.5  | V             |
| $V_{RTrising}$   | Reset threshold voltage4                                     | $V_{V1}$ increasing                           | 4.67 | 4.8  | 4.87 | V             |
| $V_{RESET}$      | Reset Pin low output voltage                                 | $V1 > 1\text{ V}$ ; $I_{RESET} = 5\text{ mA}$ |      | 0.2  | 0.4  | V             |
| $R_{RESET}$      | Reset pull up int. resistor                                  |                                               | 10   | 20   | 30   | $k\Omega$     |
| $t_{RR}$         | Reset reaction time                                          | $I_{LOAD} = 1\text{ mA}$                      | 6    |      | 40   | $\mu\text{s}$ |
| $t_{UV1}$        | V1 undervoltage filter time                                  |                                               |      | 16   |      | $\mu\text{s}$ |
| $t_{V1R}$        | Reset pulse duration (V1 undervoltage and V1 power on reset) |                                               | 1.5  | 2.0  | 2.5  | ms            |
| $t_{WDR}$        | Reset pulse duration (watchdog failure)                      |                                               | 3    | 4    | 5    | ms            |

### 3.4.7 Watchdog timing

$4.5\text{ V} \leq V_{\text{SREG}} \leq 28\text{ V}$ ;  $T_j = -40\text{ }^{\circ}\text{C}$  to  $150\text{ }^{\circ}\text{C}$ , unless otherwise specified.

**Table 13. Watchdog timing**

| Symbol            | Parameter              | Test condition | Min. | Typ. | Max. | Unit |
|-------------------|------------------------|----------------|------|------|------|------|
| $t_{\text{LW}}$   | Long open window       |                | 160  | 200  | 240  | ms   |
| $T_{\text{EFW1}}$ | Early Failure Window 1 |                |      |      | 4.5  | ms   |
| $T_{\text{LFW1}}$ | Late Failure Window 1  |                | 20   |      |      | ms   |
| $T_{\text{SW1}}$  | Safe Window 1          |                | 7.5  |      | 12   | ms   |
| $T_{\text{EFW2}}$ | Early Failure Window 2 |                |      |      | 22.3 | ms   |
| $T_{\text{LFW2}}$ | Late Failure Window 2  |                | 100  |      |      | ms   |
| $T_{\text{SW2}}$  | Safe Window 2          |                | 37.5 |      | 60   | ms   |
| $T_{\text{EFW3}}$ | Early Failure Window 3 |                |      |      | 45   | ms   |
| $T_{\text{LFW3}}$ | Late Failure Window 3  |                | 200  |      |      | ms   |
| $T_{\text{SW3}}$  | Safe Window 3          |                | 75   |      | 120  | ms   |
| $T_{\text{EFW4}}$ | Early Failure Window 4 |                |      |      | 90   | ms   |
| $T_{\text{LFW4}}$ | Late Failure Window 4  |                | 400  |      |      | ms   |
| $T_{\text{SW4}}$  | Safe Window 4          |                | 150  |      | 240  | ms   |

Figure 9. Watchdog timing

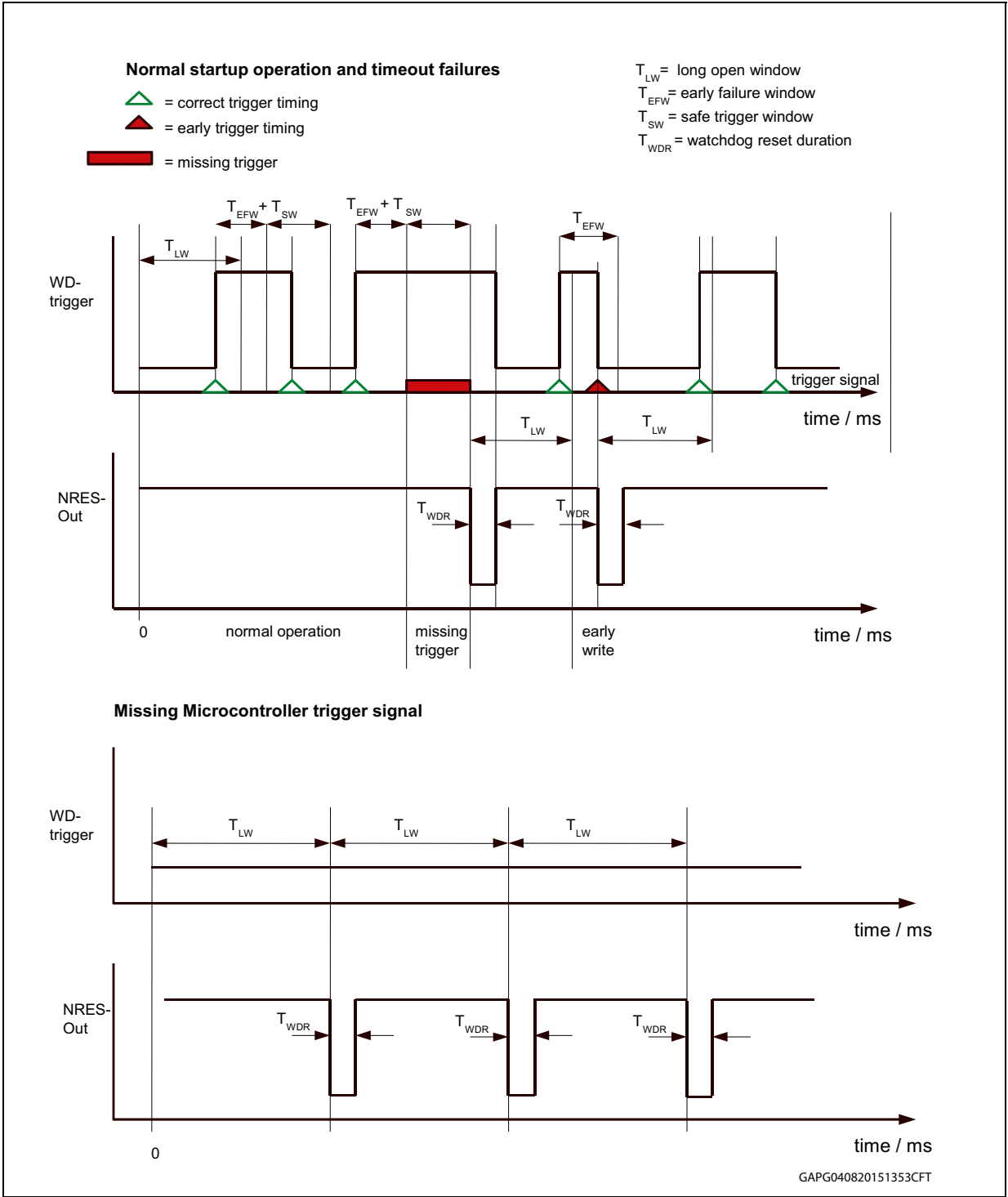
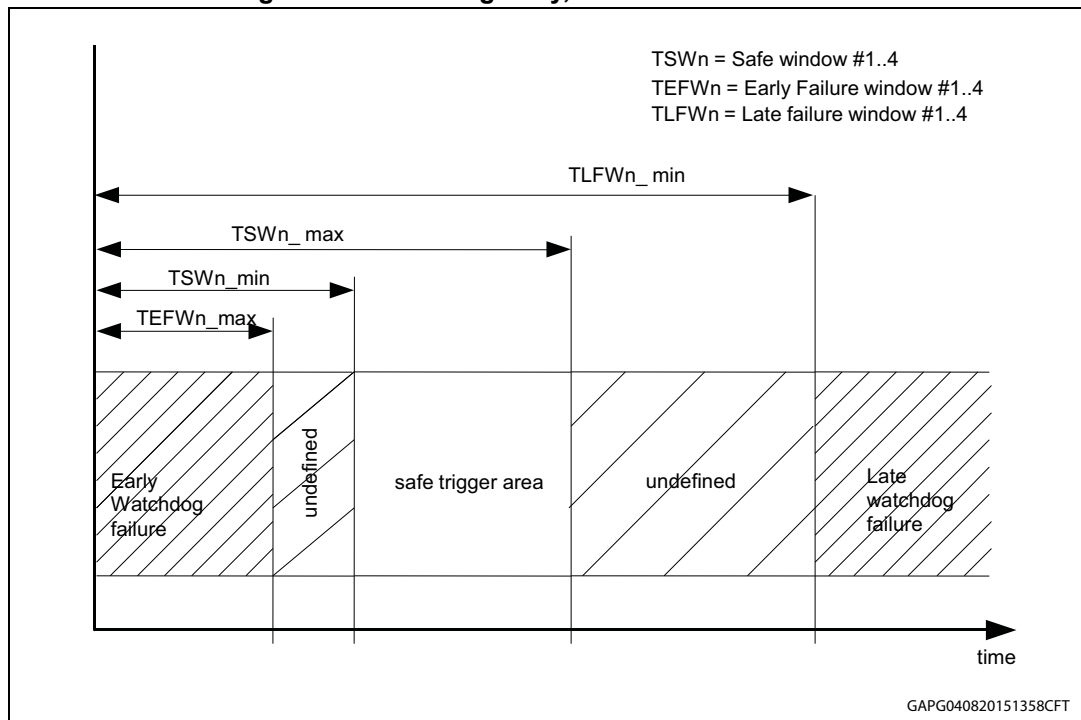


Figure 10. Watchdog early, late and safe windows



### 3.4.8 Current monitor output (CM)

The voltages are referred to ground and currents are assumed positive, when the current flows into the pin.  $6\text{ V} \leq V_S \leq 28\text{ V}$ ;  $6\text{ V} \leq V_{SREG} \leq 28\text{ V}$ ;  $T_j = -40\text{ }^\circ\text{C}$  to  $150\text{ }^\circ\text{C}$ , unless otherwise specified

Table 14. Current monitor output (CM)

| Symbol    | Parameter                                                                          | Test condition                                   | Min. | Typ.    | Max.               | Unit |
|-----------|------------------------------------------------------------------------------------|--------------------------------------------------|------|---------|--------------------|------|
| $V_{CM}$  | Functional voltage range                                                           |                                                  | 0    |         | $V_1 - 1\text{ V}$ | V    |
| $I_{CMr}$ | Current monitor output ratio:<br>$I_{CM}/I_{OUT1,4,5,6}$ and 7 (low on-resistance) | $0\text{ V} \leq V_{CM} \leq (V_1 - 1\text{ V})$ |      | 1/10000 |                    |      |
|           | $I_{CM}/I_{OUT8}$ (low on-resistance)                                              |                                                  |      | 1/6500  |                    |      |
|           | $I_{CM}/I_{OUT7,8}$ (high on-resistance)                                           |                                                  |      | 1/2000  |                    |      |
|           | $I_{CM}/I_{OUT9,10,11,12,13,14,15}$ and HS                                         |                                                  |      | 1/1000  |                    |      |

Table 14. Current monitor output (CM) (continued)

| Symbol             | Parameter                                                                                                  | Test condition                                                                                                                                                              | Min. | Typ.                         | Max.                         | Unit    |
|--------------------|------------------------------------------------------------------------------------------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------|------------------------------|------------------------------|---------|
| $I_{CM\ acc}$      | Current monitor accuracy<br>$accI_{CMOUT1,4,5,6\ and\ 7}$ (low on-resistance)                              | $0\ V \leq V_{CM} \leq (V_1 - 1\ V)$ ;<br>$I_{OUTmin} = 500\ mA$ ;<br>$I_{OUT4,5max} = 7.4\ A$ ;<br>$I_{OUT1,6max} = 2.9\ A$ ;<br>$I_{OUT7max} = 1.4\ A$                    |      |                              |                              |         |
|                    | Current monitor accuracy<br>$accI_{CMOUT\ 8}$ (low on-resistance)                                          | $0\ V \leq V_{CM} \leq (V_1 - 1\ V)$ ;<br>$I_{OUTmin} = 100\ mA$ ;<br>$I_{OUT8max} = 0.9\ A$                                                                                |      | 4% + 1%<br>FS <sup>(1)</sup> | 8% + 2%<br>FS <sup>(1)</sup> |         |
|                    | Current monitor accuracy<br>$accI_{CMOUT9,10,11,12,13,14,15\ ,HS}$<br>and $OUT_{7,8}$ (high on-resistance) | $0\ V \leq V_{CM} \leq (V_1 - 1\ V)$ ;<br>$I_{OUT.min} = 100\ mA$ ; $I_{OUT11,12,15\ HS} = 0.2\ A$ ; $I_{OUT7,8\ max} = 0.3\ A$                                             |      |                              |                              |         |
| $I_{CM\ acc\_2ol}$ | Current monitor accuracy<br>$accI_{CMOUT1,4,5,6\ and\ 7}$ (low on-resistance)                              | $0\ V \leq V_{CM} \leq (V_1 - 1\ V)$ ;<br>$I_{OUTmin} = 2 * I_{OLD}$ ;<br>$I_{OUT4,5max} = 7.4\ A$ ;<br>$I_{OUT1,6max} = 2.9\ A$ ;<br>$I_{OUT7max} = 1.4\ A$                |      | 4% + 1%<br>FS <sup>(1)</sup> | 8% + 2%<br>FS <sup>(1)</sup> |         |
|                    | Current monitor accuracy<br>$accI_{CMOUT\ 8}$ (low on-resistance)                                          | $0\ V \leq V_{CM} \leq (V_1 - 1\ V)$ ;<br>$I_{OUTmin} = 2 * I_{OLD}$ ;<br>$I_{OUT8max} = 0.9\ A$                                                                            |      |                              |                              |         |
|                    | Current monitor accuracy<br>$accI_{CMOUT9,11,12,13,14,15, HS}$ and<br>$OUT_{7,8}$ (high on-resistance)     | $0\ V \leq V_{CM} \leq (V_1 - 1\ V)$ ;<br>$I_{OUT.min} = 2 * I_{OLD}$ ;<br>$I_{OUT9,13,14max} = 0.3\ A$ ;<br>$I_{OUT11,12,15\ HS} = 0.2\ A$ ;<br>$I_{OUT7,8\ max} = 0.3\ A$ |      |                              |                              |         |
|                    | Current monitor accuracy<br>$accI_{CMOUT10}$                                                               | $0\ V \leq V_{CM} \leq (V_1 - 1\ V)$ ;<br>$I_{OUT.min} = 2 * I_{OLD}$ ;<br>$I_{OUT10max} = 0.4\ A$                                                                          |      | 4% + 1%<br>FS <sup>(1)</sup> | 8% + 4%<br>FS <sup>(1)</sup> |         |
| $t_{cmb}$          | Current monitor blanking time                                                                              |                                                                                                                                                                             |      | 32                           |                              | $\mu s$ |

1. FS (full scale) =  $I_{OUTmax} * I_{CMr}$

### 3.4.9 Charge pump

The voltages are referred to ground and currents are assumed positive, when the current flows into the pin.  $6\ V \leq V_S \leq 28\ V$ ;  $T_j = -40\ ^\circ C$  to  $150\ ^\circ C$ , unless otherwise specified.

Table 15. Charge pump electrical characteristics

| Symbol   | Parameter                                 | Test condition                                                                  | Min.       | Typ.       | Max.         | Unit |
|----------|-------------------------------------------|---------------------------------------------------------------------------------|------------|------------|--------------|------|
| $V_{CP}$ | Charge pump output voltage                | $V_S = 6\ V$ , $I_{CP} = -15\ mA$                                               | $V_S + 6$  | $V_S + 7$  |              | V    |
|          |                                           | $V_S \geq 10\ V$ , $I_{CP} = -15\ mA$                                           | $V_S + 11$ | $V_S + 12$ | $V_S + 13.5$ | V    |
| $I_{CP}$ | Charge pump output current <sup>(1)</sup> | $V_{CP} = V_S + 10\ V$ ;<br>$V_S = 13.5\ V$ ;<br>$C_1 = C_2 = C_{CP} = 100\ nF$ | 22.5       |            |              | mA   |

Table 15. Charge pump electrical characteristics (continued)

| Symbol        | Parameter                                            | Test condition                                                                      | Min.        | Typ.      | Max.        | Unit          |
|---------------|------------------------------------------------------|-------------------------------------------------------------------------------------|-------------|-----------|-------------|---------------|
| $I_{CPlim}$   | Charge pump output current limitation <sup>(2)</sup> | $V_{CP} = V_S$ ;<br>$V_S = 13.5\text{ V}$ ;<br>$C_1 = C_2 = C_{CP} = 100\text{ nF}$ |             |           | 70          | mA            |
| $V_{CP\_low}$ | Charge pump low threshold voltage                    |                                                                                     | $V_S + 4.5$ | $V_S + 5$ | $V_S + 5.5$ | V             |
| $T_{CP}$      | Charge pump low filter time                          |                                                                                     |             | 64        |             | $\mu\text{s}$ |
| $f_{CP}$      | Charge Pump frequency                                |                                                                                     |             | 400       |             | kHz           |

1.  $I_{CP}$  is the minimum current the device can provide to an external circuit without  $V_{CP}$  going below  $V_S + 10\text{ V}$ .

2.  $I_{CPlim}$  is the maximum current, which flows out of the device in case of a short to  $V_S$ .

### 3.4.10 Outputs OUT1 - OUT15, OUT\_HS

The voltages are referred to power ground and currents are assumed positive, when the current flows into the pin.  $6\text{ V} \leq V_S \leq 28\text{ V}$ ;  $6\text{ V} \leq V_{SREG} \leq 28\text{ V}$ , all outputs open;  
 $T_j = -40\text{ }^\circ\text{C}$  to  $150\text{ }^\circ\text{C}$ , unless otherwise specified.

Table 16. Outputs OUT1 - OUT15, OUT\_HS

| Symbol           | Parameter                                       | Test condition                                                                                 | Min. | Typ. | Max. | Unit             |
|------------------|-------------------------------------------------|------------------------------------------------------------------------------------------------|------|------|------|------------------|
| $r_{ON\ OUT1,6}$ | On-resistance to supply or GND                  | $V_S = 13.5\text{ V}$ ; $T_j = 25\text{ }^\circ\text{C}$ ;<br>$I_{OUT1,6} = \pm 1.5\text{ A}$  |      | 300  |      | $\text{m}\Omega$ |
|                  |                                                 | $V_S = 13.5\text{ V}$ ; $T_j = 130\text{ }^\circ\text{C}$ ;<br>$I_{OUT1,6} = \pm 1.5\text{ A}$ |      |      | 600  | $\text{m}\Omega$ |
| $r_{ON\ OUT4}$   | On-resistance to supply or GND                  | $V_S = 13.5\text{ V}$ ; $T_j = 25\text{ }^\circ\text{C}$ ;<br>$I_{OUT4} = \pm 3\text{ A}$      |      | 150  |      | $\text{m}\Omega$ |
|                  |                                                 | $V_S = 13.5\text{ V}$ ; $T_j = 130\text{ }^\circ\text{C}$ ;<br>$I_{OUT4} = \pm 3\text{ A}$     |      |      | 300  | $\text{m}\Omega$ |
| $r_{ON\ OUT5}$   | On-resistance to supply or GND                  | $V_S = 13.5\text{ V}$ ; $T_j = 25\text{ }^\circ\text{C}$ ;<br>$I_{OUT5} = \pm 3\text{ A}$      |      | 100  |      | $\text{m}\Omega$ |
|                  |                                                 | $V_S = 13.5\text{ V}$ ; $T_j = 130\text{ }^\circ\text{C}$ ;<br>$I_{OUT5} = 3\text{ A}$         |      |      | 200  | $\text{m}\Omega$ |
| $r_{ON\ OUT7}$   | On-resistance to supply in low resistance mode  | $V_S = 13.5\text{ V}$ ; $T_j = 25\text{ }^\circ\text{C}$ ;<br>$I_{OUT7} = -0.8\text{ A}$       |      | 500  |      | $\text{m}\Omega$ |
|                  |                                                 | $V_S = 13.5\text{ V}$ ; $T_j = 130\text{ }^\circ\text{C}$ ;<br>$I_{OUT7} = -0.8\text{ A}$      |      |      | 1000 | $\text{m}\Omega$ |
|                  | On-resistance to supply in high resistance mode | $V_S = 13.5\text{ V}$ ; $T_j = 25\text{ }^\circ\text{C}$ ;<br>$I_{OUT7} = -0.2\text{ A}$       |      | 1600 |      | $\text{m}\Omega$ |
|                  |                                                 | $V_S = 13.5\text{ V}$ ; $T_j = 130\text{ }^\circ\text{C}$ ;<br>$I_{OUT7} = -0.2\text{ A}$      |      |      | 3200 | $\text{m}\Omega$ |

Table 16. Outputs OUT1 - OUT15, OUT\_HS (continued)

| Symbol                    | Parameter                                                        | Test condition                                                                              | Min. | Typ. | Max. | Unit          |
|---------------------------|------------------------------------------------------------------|---------------------------------------------------------------------------------------------|------|------|------|---------------|
| $r_{ON\ OUT8}$            | On-resistance to supply in low resistance mode                   | $V_S = 13.5\text{ V}; T_j = 25\text{ }^\circ\text{C}; I_{OUT8} = -0.4\text{ A}$             |      | 800  |      | m $\Omega$    |
|                           |                                                                  | $V_S = 13.5\text{ V}; T_j = 130\text{ }^\circ\text{C}; I_{OUT8} = -0.4\text{ A}$            |      |      | 1600 | m $\Omega$    |
|                           | On-resistance to supply in high resistance mode                  | $V_S = 13.5\text{ V}; T_j = 25\text{ }^\circ\text{C}; I_{OUT8} = -0.2\text{ A}$             |      | 1600 |      | m $\Omega$    |
|                           |                                                                  | $V_S = 13.5\text{ V}; T_j = 130\text{ }^\circ\text{C}; I_{OUT8} = -0.2\text{ A}$            |      |      | 3200 | m $\Omega$    |
| $r_{ON\ OUT9,10,13,14}$   | On-resistance to supply                                          | $V_S = 13.5\text{ V}; T_j = 25\text{ }^\circ\text{C}; I_{OUT9,10,13,14} = -75\text{ mA}$    |      | 2000 |      | m $\Omega$    |
|                           |                                                                  | $V_S = 13.5\text{ V}; T_j = 130\text{ }^\circ\text{C}; I_{OUT9,10,13,14} = -75\text{ mA}$   |      |      | 4000 | m $\Omega$    |
| $r_{ON\ OUT11,12,15, HS}$ | On-resistance to supply                                          | $V_S = 13.5\text{ V}; T_j = 25\text{ }^\circ\text{C}; I_{OUT11,12,15, HS} = -75\text{ mA}$  |      | 5    |      | $\Omega$      |
|                           |                                                                  | $V_S = 13.5\text{ V}; T_j = 130\text{ }^\circ\text{C}; I_{OUT11,12,15, HS} = -75\text{ mA}$ |      |      | 10   | $\Omega$      |
| $I_{QLH}$                 | Switched-off output current high-side drivers of OUT7-15, OUT_HS | $V_{OUT} = 0\text{ V}; \text{standby mode}$                                                 | -5   |      |      | $\mu\text{A}$ |
|                           |                                                                  | $V_{OUT} = 0\text{ V}; \text{active mode}$                                                  | -10  |      |      | $\mu\text{A}$ |
| $I_{QLH}$                 | Switched-off output current high-side drivers of OUT1-6          | $V_{OUT} = 0\text{ V}; \text{standby mode}$                                                 | -5   |      |      | $\mu\text{A}$ |
|                           |                                                                  | $V_{OUT} = 0\text{ V}; \text{Active mode}$                                                  | -100 |      |      | $\mu\text{A}$ |
| $I_{QLL}$                 | Switched-off output current low-side drivers of OUT1-6           | $V_{OUT} = V_S; \text{standby mode}$                                                        |      |      | 165  | $\mu\text{A}$ |
|                           |                                                                  | $V_{OUT} = V_S - 0.5\text{ V}; \text{active mode}$                                          | -100 |      |      | $\mu\text{A}$ |

### 3.4.11 Power outputs switching times

The voltages are referred to power ground and currents are assumed positive, when the current flows into the pin.  $6\text{ V} \leq V_S \leq 28\text{ V}$ ;  $6\text{ V} \leq V_{SREG} \leq 28\text{ V}$ ;  $T_j = -40\text{ }^\circ\text{C}$  to  $150\text{ }^\circ\text{C}$ , unless otherwise specified.

**Table 17. Power outputs switching times**

| Symbol               | Parameter                                                                                                | Test condition                                                                                                                                                         | Min. | Typ. | Max. | Unit                   |
|----------------------|----------------------------------------------------------------------------------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------|------|------|------------------------|
| $t_{d\text{ ON H}}$  | Output delay time high-side driver on (OUT <sub>1,4,5,6</sub> )                                          | $V_S = 13.5\text{ V}$ ; $V_1 = 5\text{ V}$ ; corresponding low-side driver is not active <sup>(1)(2)(3)</sup>                                                          | 15   | 40   | 80   | $\mu\text{s}$          |
|                      | Output delay time high-side driver on (OUT <sub>7,8</sub> )                                              | (from CSN 50% to OUT 50%) see <a href="#">Figure 20</a>                                                                                                                | 20   | 40   | 90   | $\mu\text{s}$          |
| $t_{d\text{ OFF H}}$ | Output delay time high-side driver off (OUT <sub>1,4,5,6</sub> )                                         | $V_S = 13.5\text{ V}$ ; $V_1 = 5\text{ V}$ <sup>(1)(2)(3)</sup> (from CSN 50% to                                                                                       | 50   | 150  | 300  | $\mu\text{s}$          |
|                      | Output delay time high-side driver off (OUT <sub>7,8</sub> )                                             | OUT 50%) see <a href="#">Figure 20</a>                                                                                                                                 | 20   | 70   | 130  | $\mu\text{s}$          |
| $t_{d\text{ ON H}}$  | Output delay time high-side driver on (OUT9 ...OUT15, OUT_HS)                                            | $V_S/V_{SREG} = 13.5\text{ V}$ ; $V_1 = 5\text{ V}$ ; (from CSN 80% to OUT 80%)                                                                                        |      |      | 30   | $\mu\text{s}$          |
| $t_{d\text{ OFF H}}$ | Output switch off delay time high-side driver on (OUT9 ...OUT15, OUT_HS)                                 | $V_S/V_{SREG} = 13.5\text{ V}$ ; $V_1 = 5\text{ V}$ ; (from CSN 80% to OUT 20%)                                                                                        |      |      | 35   | $\mu\text{s}$          |
| $t_{d\text{ ON L}}$  | Output delay time low-side driver (OUT <sub>1-6</sub> ) on                                               | $V_S = 13.5\text{ V}$ ; $V_1 = 5\text{ V}$ ; corresponding high-side driver is not active <sup>(1)(2)(3)</sup> (from CSN 50% to OUT 50%) see <a href="#">Figure 20</a> | 15   | 30   | 70   | $\mu\text{s}$          |
| $t_{d\text{ OFF L}}$ | Output delay time low-side driver (OUT <sub>1-6</sub> ) off                                              | $V_S = 13.5\text{ V}$ ; $V_1 = 5\text{ V}$ <sup>(1)(2)(3)</sup> (from CSN 50% to OUT 50%) see <a href="#">Figure 20</a>                                                | 40   | 150  | 300  | $\mu\text{s}$          |
| $t_{d\text{ HL}}$    | Cross current protection time (OUT <sub>1-6</sub> )                                                      | $t_{cc\text{ ONLS\_OFFHS}} - t_{d\text{ OFF H}}$ <sup>(4)</sup>                                                                                                        | 50   | 200  | 400  | $\mu\text{s}$          |
| $t_{d\text{ LH}}$    |                                                                                                          | $t_{cc\text{ ONHS\_OFFLS}} - t_{d\text{ OFF L}}$ <sup>(4)</sup>                                                                                                        |      |      |      |                        |
| $dV_{OUT}/dt$        | Slew rate of OUT <sub>1</sub> -OUT <sub>8</sub>                                                          | $V_S = 13.5\text{ V}$ ; $V_1 = 5\text{ V}$ <sup>(1)(2)(3)</sup>                                                                                                        | 0.1  | 0.2  | 0.6  | $\text{V}/\mu\text{s}$ |
| $dV_{max}/dt$        | Maximum external applied slew rate on OUT1-OUT6 without switching on the LS and HS (only in Active mode) | Guaranteed by design                                                                                                                                                   | 20   |      |      | $\text{V}/\mu\text{s}$ |
| $dV_{OUT}/dt$        | Slew rate of OUT9-OUT15, OUT_HS                                                                          | $V_S/V_{SREG} = 13.5\text{ V}$ ; $V_1 = 5\text{ V}$ <sup>(1)(2)(3)</sup>                                                                                               |      | 2    |      | $\text{V}/\mu\text{s}$ |
| $f_{PWMx(00)}$       | PWM switching frequency                                                                                  | $V_S/V_{SREG} = 13.5\text{ V}$ ; $V_1 = 5\text{ V}$                                                                                                                    |      | 100  |      | Hz                     |
| $f_{PWMx(01)}$       | PWM switching frequency                                                                                  | $V_S/V_{SREG} = 13.5\text{ V}$ ; $V_1 = 5\text{ V}$                                                                                                                    |      | 200  |      | Hz                     |

Table 17. Power outputs switching times (continued)

| Symbol         | Parameter               | Test condition                                        | Min. | Typ. | Max. | Unit |
|----------------|-------------------------|-------------------------------------------------------|------|------|------|------|
| $f_{PWMx(10)}$ | PWM switching frequency | $V_S/V_{SREG} = 13.5\text{ V};$<br>$V_1 = 5\text{ V}$ |      | 330  |      | Hz   |
| $f_{PWMx(11)}$ | PWM switching frequency | $V_S/V_{SREG} = 13.5\text{ V};$<br>$V_1 = 5\text{ V}$ |      | 500  |      | Hz   |

1.  $R_{LOAD} = 16\ \Omega$  at  $OUT_{1,6}$  and  $OUT_{7,8}$  in low on-resistance mode
2.  $R_{LOAD} = 4\ \Omega$  at  $OUT_{4,5}$
3.  $R_{LOAD} = 128\ \Omega$  at  $OUT_{4,9,10,11,12,13,15,15,HS}$  and  $OUT_{7,8}$  in high on-resistance mode
4.  $t_{CC}$  is the switch-on delay time if complement in half bridge has to switch off

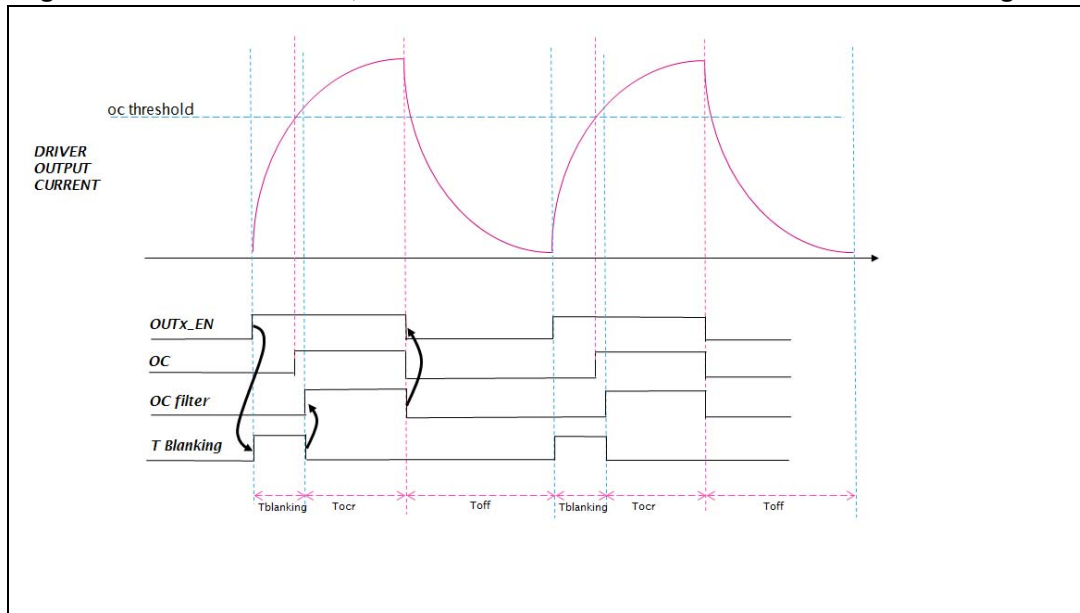
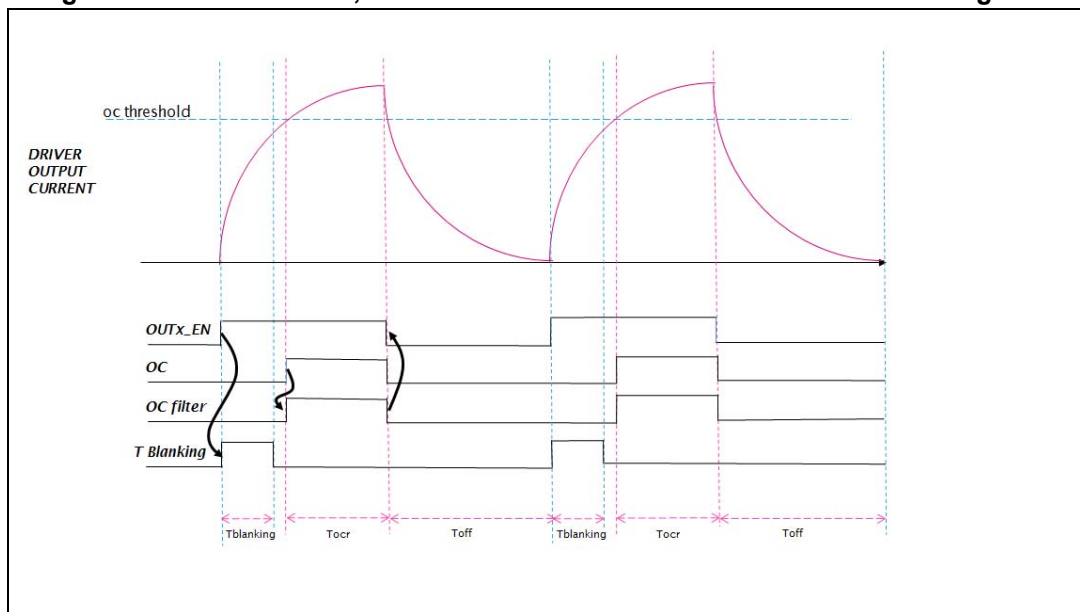
### 3.4.12 Over Current Recovery settings

Table 18. Half bridges (OUT1, OUT4, OUT5 and OUT6) OCR timing parameters

| Symbol    | Parameter                                 | Test condition       | Min. | Typ. | Max. | Unit          |
|-----------|-------------------------------------------|----------------------|------|------|------|---------------|
| Tblanking |                                           | Guaranteed by Design | 33   | 40   | 47   | $\mu\text{s}$ |
| Tocr_hb   | Over current filter time for half bridges | Guaranteed by Design | 26   | 32   | 38   | $\mu\text{s}$ |
| Toff_hb   | OFF Time for half bridges OCR_FREQ=0      | Guaranteed by Design | 218  | 264  | 310  | $\mu\text{s}$ |
|           | OFF Time for half bridges OCR_FREQ=1      |                      | 106  | 128  | 150  | $\mu\text{s}$ |

Table 19. High-side (OUT7, OUT8 and OUT\_HS) OCR timing parameters

| Symbol    | Parameter                              | Test condition       | Min. | Typ. | Max. | Unit          |
|-----------|----------------------------------------|----------------------|------|------|------|---------------|
| Tblanking |                                        | Guaranteed by Design | 33   | 40   | 47   | $\mu\text{s}$ |
| Tocr_hs   | Over current filter time for high-side | Guaranteed by Design | 53   | 64   | 75   | $\mu\text{s}$ |
| Toff_hs   | OFF Time for high-side OCR_FREQ=0      | Guaranteed by Design | 398  | 480  | 562  | $\mu\text{s}$ |
|           | OFF Time for high-side OCR_FREQ=1      |                      | 192  | 232  | 272  | $\mu\text{s}$ |

**Figure 11. Hard Short case, the OC threshold is reached before end of blanking time****Figure 12. Overload case, the OC threshold is reached after end of blanking time**

### 3.4.13 Current monitoring

The voltages are referred to power ground and currents are assumed positive, when the current flows into the pin.  $6\text{ V} \leq V_S \leq 28\text{ V}$ ;  $6\text{ V} \leq V_{SREG} \leq 28\text{ V}$ ;  $T_j = -40\text{ }^\circ\text{C}$  to  $150\text{ }^\circ\text{C}$ , unless otherwise specified.

Table 20. Current monitoring

| Symbol                                                       | Parameter                                           | Test condition                                                                                                                    | Min. | Typ. | Max. | Unit |
|--------------------------------------------------------------|-----------------------------------------------------|-----------------------------------------------------------------------------------------------------------------------------------|------|------|------|------|
| $I_{OC1}$ ,<br>$I_{OC6}$                                     | Overcurrent threshold HS & LS                       | $V_S = 13.5\text{ V}$ ; $V_1 = 5\text{ V}$ ; sink and source                                                                      | 3    |      | 5    | A    |
| $I_{OC4}$                                                    |                                                     | $V_S = 13.5\text{ V}$ ; $V_1 = 5\text{ V}$ ; sink and source; $T_j = -40\text{ }^{\circ}\text{C}$ to $70\text{ }^{\circ}\text{C}$ | 7.5  |      | 10   | A    |
|                                                              |                                                     | $V_S = 13.5\text{ V}$ ; $V_1 = 5\text{ V}$ ; sink and source; $T_j = 130\text{ }^{\circ}\text{C}$                                 | 6    |      | 10   | A    |
| $I_{OC5\_1}$                                                 |                                                     | $V_S = 13.5\text{ V}$ ; $V_1 = 5\text{ V}$ ; sink and source                                                                      | 3    | 4    | 5    | A    |
| $I_{OC5\_2}$                                                 |                                                     |                                                                                                                                   | 4.5  | 6    | 7.5  | A    |
| $I_{OC5\_3}$                                                 |                                                     |                                                                                                                                   | 7.5  |      | 10   | A    |
| $I_{OC7}$                                                    | Overcurrent threshold HS in low on-resistance mode  | $V_S/V_{SREG} = 13.5\text{ V}$ ;<br>$V_1 = 5\text{ V}$ ; source                                                                   | 1.5  |      | 2.5  | A    |
|                                                              | Overcurrent threshold HS in high on-resistance mode |                                                                                                                                   | 0.35 |      | 0.65 | A    |
| $I_{OC8}$                                                    | Overcurrent threshold HS in low on-resistance mode  |                                                                                                                                   | 0.7  |      | 1.3  | A    |
|                                                              | Overcurrent threshold HS in high on-resistance mode |                                                                                                                                   | 0.35 |      | 0.65 | A    |
| $I_{OC9}$ ,<br>$I_{OC13}$ ,<br>$I_{OC14}$                    | Overcurrent threshold HS in high current mode       |                                                                                                                                   | 0.35 |      | 0.7  | A    |
|                                                              | Overcurrent threshold to HS in low current mode     |                                                                                                                                   | 0.15 |      | 0.3  | A    |
| $I_{OC10}$                                                   | Overcurrent threshold HS in high current mode       |                                                                                                                                   | 0.5  |      | 1    | A    |
|                                                              | Overcurrent threshold HS in low current mode        |                                                                                                                                   | 0.25 |      | 0.5  | A    |
| $I_{OC11}$ ,<br>$I_{OC12}$ ,<br>$I_{OC15}$ ,<br>$I_{OC\_HS}$ | Overcurrent threshold HS in high current mode       |                                                                                                                                   | 0.25 |      | 0.5  | A    |
|                                                              | Overcurrent threshold HS in low current mode        |                                                                                                                                   | 0.15 |      | 0.3  | A    |
| $t_{AR}$                                                     | Auto recovery time limit                            | OUT1 to OUT6                                                                                                                      |      | 100  |      | ms   |
|                                                              |                                                     | OUT7, OUT8, OUT_HS                                                                                                                |      | 120  |      | ms   |
| $I_{OLD1}$ ,<br>$I_{OLD6}$                                   | Under-current threshold HS & LS                     | $V_S = 13.5\text{ V}$ ; $V_1 = 5\text{ V}$ ; sink and source                                                                      | 10   | 30   | 80   | mA   |
| $I_{OLD4}$ ,<br>$I_{OLD5}$                                   |                                                     |                                                                                                                                   | 60   | 150  | 300  | mA   |

Table 20. Current monitoring (continued)

| Symbol                                                                                            | Parameter                                             | Test condition                                                              | Min. | Typ. | Max. | Unit |
|---------------------------------------------------------------------------------------------------|-------------------------------------------------------|-----------------------------------------------------------------------------|------|------|------|------|
| I <sub>OLD7</sub>                                                                                 | Under-current threshold HS in low on-resistance mode  | V <sub>S</sub> /V <sub>SREG</sub> = 13.5 V;<br>V <sub>1</sub> = 5 V; source | 15   | 40   | 60   | mA   |
|                                                                                                   | Under-current threshold HS in high on-resistance mode |                                                                             | 5    | 10   | 15   | mA   |
| I <sub>OLD8</sub>                                                                                 | Under-current threshold HS in low on-resistance mode  |                                                                             | 10   | 30   | 45   | mA   |
|                                                                                                   | Under-current threshold HS in high on-resistance mode |                                                                             | 5    | 10   | 15   | mA   |
| I <sub>OLD9</sub>  ,<br> I <sub>OLD13</sub>  ,<br> I <sub>OLD14</sub>                             | Under-current threshold HS in high current mode       |                                                                             | 6    |      | 12   | mA   |
|                                                                                                   | Under-current threshold HS in low current mode        |                                                                             | 0.5  |      | 4    | mA   |
| I <sub>OLD10</sub>                                                                                | Under -current threshold HS in high current mode      |                                                                             | 10   |      | 30   | mA   |
|                                                                                                   | Under -current threshold HS in low current mode       |                                                                             | 0.3  |      | 4    | mA   |
| I <sub>OLD11</sub>  ,<br> I <sub>OLD12</sub>  ,<br> I <sub>OLD15</sub>  ,<br> I <sub>OLD_HS</sub> | Under -current threshold HS in high current mode      |                                                                             | 6    |      | 12   | mA   |
|                                                                                                   | Under -current threshold HS in low current mode       |                                                                             | 0.85 |      | 4    | mA   |
| t <sub>OL_out</sub>                                                                               | Filter time of open-load signal                       | Duration of open-load condition to set the status bit                       | 150  | 200  | 250  | μs   |

### 3.4.14 H-bridge driver

The voltages are referred to power ground and currents are assumed positive, when the current flows into the pin.  $6\text{ V} \leq V_S \leq 28\text{ V}$ ;  $6\text{ V} \leq V_{SREG} \leq 28\text{ V}$ ;  $T_j = -40^\circ\text{C}$  to  $150^\circ\text{C}$ , unless otherwise specified.

Table 21. H-bridge driver

| Symbol                                  | Parameter                             | Test condition                                                               | Min.                 | Typ.                  | Max.                    | Unit |
|-----------------------------------------|---------------------------------------|------------------------------------------------------------------------------|----------------------|-----------------------|-------------------------|------|
| Drivers for external high-side PowerMOS |                                       |                                                                              |                      |                       |                         |      |
| I <sub>GHx(Ch)</sub>                    | Average charge current (charge stage) | T <sub>j</sub> = 25 °C                                                       |                      | 0.3                   |                         | A    |
| R <sub>GHx</sub>                        | On-resistance (discharge-stage)       | V <sub>SHx</sub> = 0 V; I <sub>GHx</sub> = 50 mA;<br>T <sub>j</sub> = 25 °C  | 6                    | 10                    | 14                      | Ω    |
|                                         |                                       | V <sub>SHx</sub> = 0 V; I <sub>GHx</sub> = 50 mA;<br>T <sub>j</sub> = 130 °C |                      | 14                    | 20                      | Ω    |
| V <sub>GHHx</sub>                       | Gate-on voltage                       | V <sub>S</sub> = SH = 6 V; I <sub>CP</sub> = 15 mA                           | V <sub>SHx</sub> + 6 |                       |                         | V    |
|                                         |                                       | V <sub>S</sub> = SH = 12 V; I <sub>CP</sub> = 15 mA                          | V <sub>SHx</sub> + 8 | V <sub>SHx</sub> + 10 | V <sub>SHx</sub> + 11.5 | V    |

Table 21. H-bridge driver (continued)

| Symbol                                  | Parameter                             | Test condition                                                                     | Min.          | Typ.           | Max.             | Unit      |
|-----------------------------------------|---------------------------------------|------------------------------------------------------------------------------------|---------------|----------------|------------------|-----------|
| $R_{GSHx}$                              | Passive gate-clamp resistance         | $V_{GHx} = 0.5 \text{ V}$                                                          |               | 15             |                  | $k\Omega$ |
| Drivers for external low-side Power-MOS |                                       |                                                                                    |               |                |                  |           |
| $I_{GLx(Ch)}$                           | Average charge-current (charge stage) | $T_j = 25 \text{ }^\circ\text{C}$                                                  |               | 0.3            |                  | A         |
| $R_{GLx}$                               | On-resistance (discharge-stage)       | $V_{SLx} = 0 \text{ V}; I_{GHx} = 50 \text{ mA}; T_j = 25 \text{ }^\circ\text{C}$  | 6             | 10             | 14               | $\Omega$  |
|                                         |                                       | $V_{SLx} = 0 \text{ V}; I_{GHx} = 50 \text{ mA}; T_j = 130 \text{ }^\circ\text{C}$ |               | 14             | 20               | $\Omega$  |
| $V_{GHLx}$                              | Gate-on voltage                       | $V_S = 6 \text{ V}; I_{CP} = 15 \text{ mA}$                                        | $V_{SLx} + 6$ |                |                  | V         |
|                                         |                                       | $V_S = 12 \text{ V}; I_{CP} = 15 \text{ mA}$                                       | $V_{SLx} + 8$ | $V_{SLx} + 10$ | $V_{SLx} + 11.5$ | V         |
| $R_{GSLx}$                              | Passive gate-clamp resistance         |                                                                                    |               | 15             |                  | $k\Omega$ |

### 3.4.15 Gate drivers for the external Power-MOS switching times

The voltages are referred to power ground and currents are assumed positive, when the current flows into the pin.  $6 \text{ V} \leq V_S \leq 28 \text{ V}$ ;  $6 \text{ V} \leq V_{SREG} \leq 28 \text{ V}$ ;  $T_j = -40 \text{ }^\circ\text{C}$  to  $150 \text{ }^\circ\text{C}$ , unless otherwise specified.

Table 22. Gate drivers for the external Power-MOS switching times

| Symbol         | Parameter                                                                           | Test condition                                                                                  | Min.                                        | Typ. | Max. | Unit          |
|----------------|-------------------------------------------------------------------------------------|-------------------------------------------------------------------------------------------------|---------------------------------------------|------|------|---------------|
| $T_{G(HL)xHL}$ | Propagation delay time high to low (switch mode) <sup>(1)</sup>                     | $V_S = 13.5 \text{ V}; V_{SHx} = 0;$<br>$R_G = 0 \Omega; C_G = 2.7 \text{ nF}$                  |                                             | 1.5  |      | $\mu\text{s}$ |
| $T_{G(HL)xLH}$ | Propagation delay time low to high (switch mode) <sup>(1)</sup>                     | $V_S = 13.5 \text{ V}; V_{SLx} = 0;$<br>$R_G = 0 \Omega; C_G = 2.7 \text{ nF}$                  |                                             | 1.5  |      | $\mu\text{s}$ |
| $I_{GHxmax}$   | Maximum source current (current mode)                                               | $V_S = 13.5 \text{ V}; V_{SHx} = 0;$<br>$V_{GHx} = 1 \text{ V};$<br>$SLEW<4:0> = 1 \text{ F}_H$ |                                             | 32   |      | mA            |
| $I_{GHxfmax}$  | Maximum sink current (current mode)                                                 | $V_S = 13.5 \text{ V}; V_{SHx} = 0;$<br>$V_{GHx} = 2 \text{ V};$<br>$SLEW<4:0> = 1 \text{ F}_H$ |                                             | 32   |      | mA            |
| $dI_{GHxr}$    | Source current accuracy                                                             | $V_S = 13.5 \text{ V}; V_{SHx} = 0;$<br>$V_{GHx} = 1 \text{ V}$                                 | See <a href="#">Figure 14: IGHxr ranges</a> |      |      |               |
| $dI_{GHxf}$    | Sink current accuracy                                                               | $V_S = 13.5 \text{ V}; V_{SHx} = 0;$<br>$V_{GHx} = 2 \text{ V}$                                 | See <a href="#">Figure 15: IGHxf ranges</a> |      |      |               |
| $V_{DSHxrSW}$  | Switching voltage ( $V_S - V_{SH}$ ) between current mode and switch mode (rising)  | $V_S = 13.5 \text{ V}$                                                                          |                                             | 2.8  |      | V             |
| $V_{DSHxfSW}$  | Switching voltage ( $V_S - V_{SH}$ ) between switch mode and current mode (falling) | $V_S = 13.5 \text{ V}$                                                                          |                                             | 2.8  |      | V             |

Table 22. Gate drivers for the external Power-MOS switching times (continued)

| Symbol        | Parameter                                  | Test condition                                                                                                                        | Min. | Typ. | Max. | Unit |
|---------------|--------------------------------------------|---------------------------------------------------------------------------------------------------------------------------------------|------|------|------|------|
| $t_{0GHxr}$   | Rise time (switch mode)                    | $V_S = 13.5\text{ V}; V_{SHx} = 0;$<br>$R_G = 0\ \Omega; C_G = 2.7\text{ nF}$                                                         |      | 45   |      | ns   |
| $t_{0GHxf}$   | Fall time (switch mode)                    | $V_S = 13.5\text{ V}; V_{SHx} = 0;$<br>$R_G = 0\ \Omega; C_G = 2.7\text{ nF}$                                                         |      | 85   |      | ns   |
| $t_{0GLxr}$   | Rise time                                  | $V_S = 13.5\text{ V}; V_{SLx} = 0;$<br>$R_G = 0\ \Omega; C_G = 2.7\text{ nF}$                                                         |      | 45   |      | ns   |
| $t_{0GLxf}$   | Fall time                                  | $V_S = 13.5\text{ V}; V_{SLx} = 0;$<br>$R_G = 0\ \Omega; C_G = 2.7\text{ nF}$                                                         |      | 85   |      | ns   |
| $tccp_{0001}$ | Programmable cross-current protection time |                                                                                                                                       |      | 500  |      | ns   |
| $tccp_{0010}$ | Programmable cross-current protection time |                                                                                                                                       |      | 750  |      | ns   |
| $tccp_{0011}$ | Programmable cross-current protection time |                                                                                                                                       |      | 1000 |      | ns   |
| $tccp_{0100}$ | Programmable cross-current protection time |                                                                                                                                       |      | 1250 |      | ns   |
| $tccp_{0101}$ | Programmable cross-current protection time |                                                                                                                                       |      | 1500 |      | ns   |
| $tccp_{0110}$ | Programmable cross-current protection time |                                                                                                                                       |      | 1750 |      | ns   |
| $tccp_{0111}$ | Programmable cross-current protection time |                                                                                                                                       |      | 2000 |      | ns   |
| $tccp_{1000}$ | Programmable cross-current protection time |                                                                                                                                       |      | 2250 |      | ns   |
| $tccp_{1001}$ | Programmable cross-current protection time |                                                                                                                                       |      | 2500 |      | ns   |
| $tccp_{1010}$ | Programmable cross-current protection time |                                                                                                                                       |      | 2750 |      | ns   |
| $tccp_{1011}$ | Programmable cross-current protection time |                                                                                                                                       |      | 3000 |      | ns   |
| $tccp_{1100}$ | Programmable cross-current protection time |                                                                                                                                       |      | 3250 |      | ns   |
| $tccp_{1101}$ | Programmable cross-current protection time |                                                                                                                                       |      | 3500 |      | ns   |
| $tccp_{1110}$ | Programmable cross-current protection time |                                                                                                                                       |      | 3750 |      | ns   |
| $tccp_{1111}$ | Programmable cross-current protection time |                                                                                                                                       |      | 4000 |      | ns   |
| $f_{PWMH}$    | PWMH switching frequency                   | $V_S = 13.5\text{ V}; V_{SLx} = 0;$<br>$R_G = 0\ \Omega; C_G = 2.7\text{ nF};$<br>PWMH-Duty-Cycle = 50%;<br>$tccp$ configured as 0001 |      |      | 50   | kHz  |

Figure 13. H-driver delay times

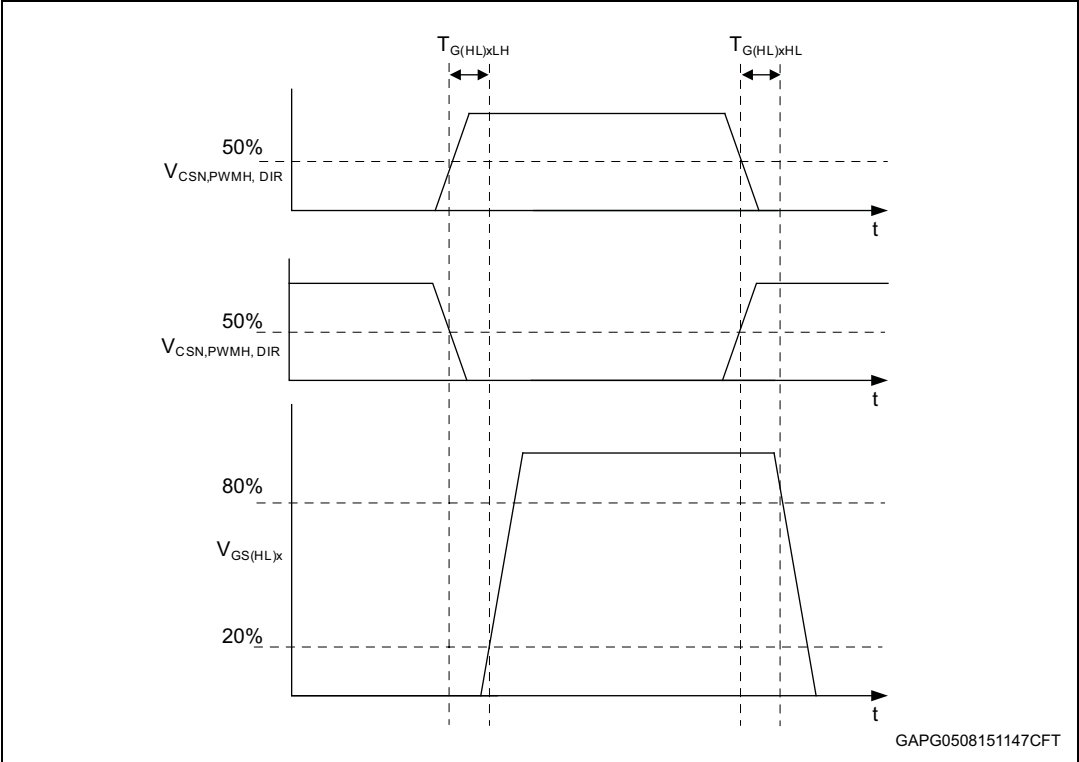


Figure 14. IGHxr ranges

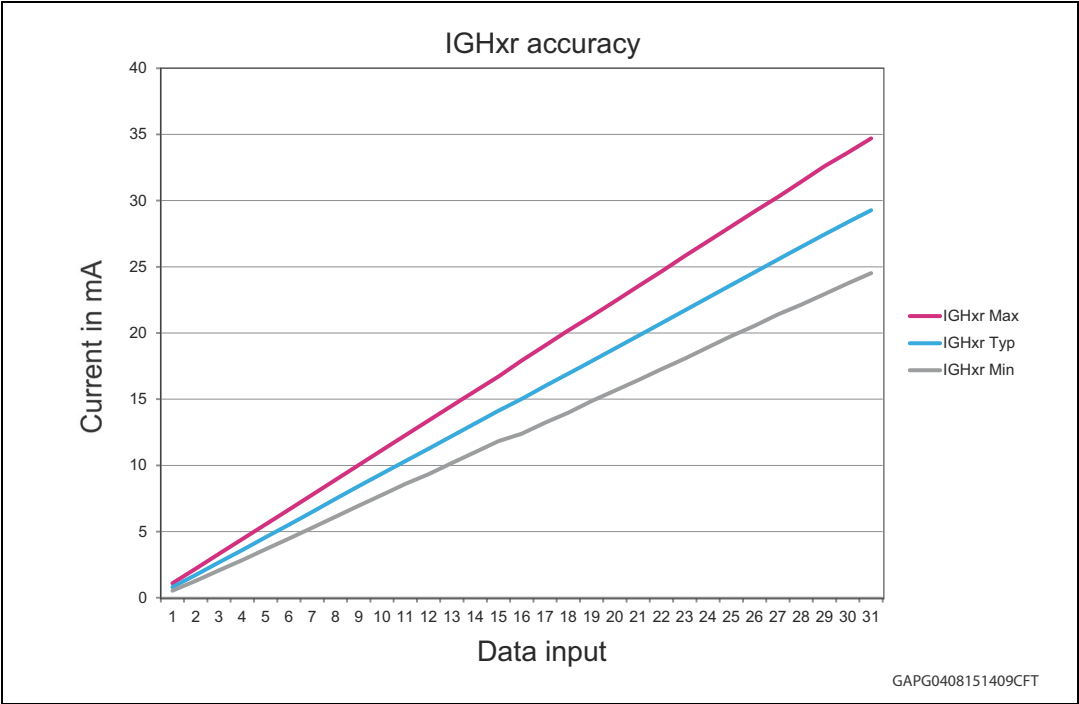
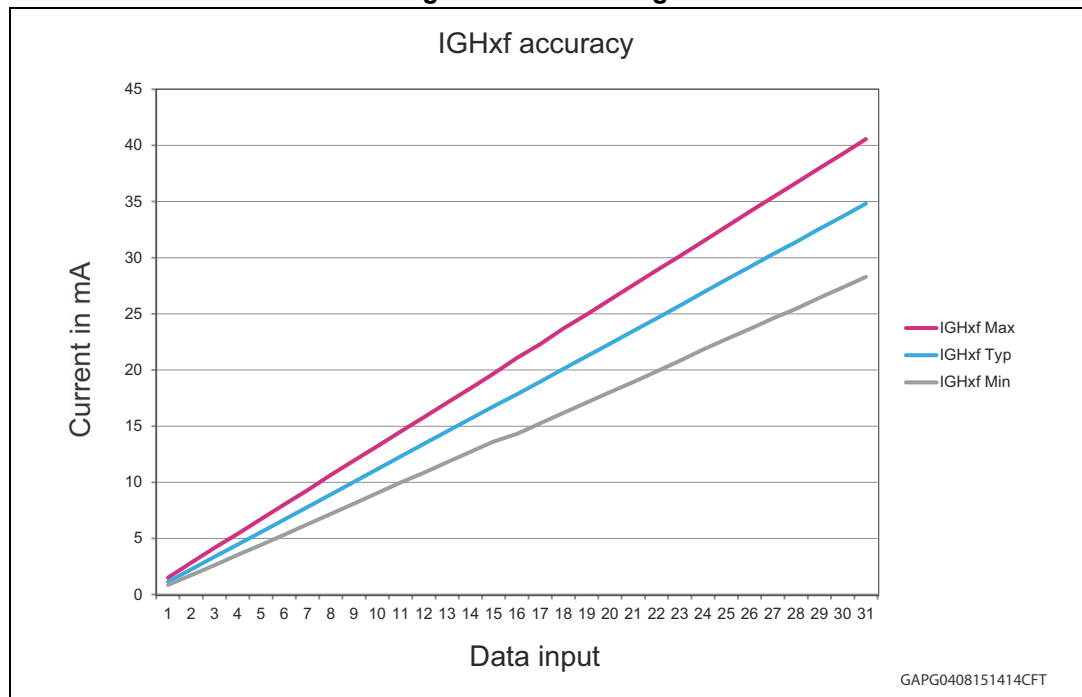


Figure 15. IGHxf ranges



### 3.4.16 Drain source monitoring external H-bridge

The voltages are referred to power ground and currents are assumed positive, when the current flows into the pin.  $6\text{ V} \leq V_S \leq 28\text{ V}$ ;  $6\text{ V} \leq V_{SREG} \leq 28\text{ V}$ ;  $T_j = -40^\circ\text{C}$  to  $150^\circ\text{C}$ , unless otherwise specified.

Table 23. Drain source monitoring external H-bridge

| Symbol         | Parameter                             | Test condition                                                     | Min.  | Typ. | Max.  | Unit          |
|----------------|---------------------------------------|--------------------------------------------------------------------|-------|------|-------|---------------|
| $V_{SCd1\_HB}$ | Drain-source threshold voltage        |                                                                    | 0.375 | 0,5  | 0.625 | V             |
| $V_{SCd2\_HB}$ | Drain-source threshold voltage        |                                                                    | 0.6   | 0,75 | 0.9   | V             |
| $V_{SCd3\_HB}$ | Drain-source threshold voltage        |                                                                    | 0,85  | 1    | 1,15  | V             |
| $V_{SCd4\_HB}$ | Drain-source threshold voltage        |                                                                    | 1,06  | 1,25 | 1,43  | V             |
| $V_{SCd5\_HB}$ | Drain-source threshold voltage        |                                                                    | 1,27  | 1,5  | 1,73  | V             |
| $V_{SCd6\_HB}$ | Drain-source threshold voltage        |                                                                    | 1,49  | 1,75 | 2,01  | V             |
| $V_{SCd7\_HB}$ | Drain-source threshold voltage        |                                                                    | 1,7   | 2    | 2,3   | V             |
| $t_{SCd\_HB}$  | Drain-source monitor filter time      |                                                                    |       | 6    |       | $\mu\text{s}$ |
| $t_{scs\_HB}$  | Drain-source comparator settling time | $V_S = 13.5\text{ V}$ ;<br>$V_{SH} = \text{jump from GND to } V_S$ |       |      | 5     | $\mu\text{s}$ |

### 3.4.17 Open-load monitoring external H-bridge

The voltages are referred to power ground and currents are assumed positive, when the current flows into the pin.  $6\text{ V} \leq V_S \leq 28\text{ V}$ ;  $6\text{ V} \leq V_{SREG} \leq 28\text{ V}$ ;  $T_j = -40^\circ\text{C}$  to  $150^\circ\text{C}$ , unless otherwise specified.

Table 24. Open-load monitoring external H-bridge

| Symbol       | Parameter                                                          | Test condition                                                      | Min. | Typ.       | Max. | Unit       |
|--------------|--------------------------------------------------------------------|---------------------------------------------------------------------|------|------------|------|------------|
| $V_{ODSL}$   | Low-side drain-source monitor low off-threshold voltage            | $V_{SLx} = 0\text{ V}; V_S = 13.5\text{ V}$                         |      | $0.15 V_S$ |      | V          |
| $V_{ODSH}$   | Low-side drain-source monitor high off-threshold voltage           | $V_{SLx} = 0\text{ V}; V_S = 13.5\text{ V}$                         |      | $0.85 V_S$ |      | V          |
| $V_{OLSHx}$  | Output voltage of selected SHx in open-load test mode              | $V_{SLx} = 0\text{ V}; V_S = 13.5\text{ V}$                         |      | $0.5 V_S$  |      | V          |
| $R_{pdOL}$   | Pull-down resistance of the non-selected SHx pin in open-load mode | $V_{SLx} = 0\text{ V}; V_S = 13.5\text{ V}; V_{SHx} = 4.5\text{ V}$ |      | 20         |      | k $\Omega$ |
| $t_{OL\_HB}$ | Open-load filter time                                              |                                                                     |      | 2          |      | ms         |

### 3.4.18 Fail safe low-side switch

The voltages are referred to power ground and currents are assumed positive, when the current flows into the pin.  $6\text{ V} \leq V_S \leq 18\text{ V}$ ;  $T_j = 40\text{ }^{\circ}\text{C}$  to  $150\text{ }^{\circ}\text{C}$ , unless otherwise specified.

Table 25. Fail safe low-side switch

| Symbol         | Parameter                                                                         | Test condition                                                | Min. | Typ. | Max. | Unit             |
|----------------|-----------------------------------------------------------------------------------|---------------------------------------------------------------|------|------|------|------------------|
| $V_{OUT\_max}$ | Max output voltage in case of missing supply                                      | $I_{OUT} = 1\text{ mA}; V_S = V_{SREG} = 0\text{ V}$          |      | 2    | 2.5  | V                |
| $R_{DSON}$     | DC output resistance                                                              | $I_{LOAD} = 250\text{ mA}; T_j = 25\text{ }^{\circ}\text{C}$  |      | 1.4  |      | $\Omega$         |
|                |                                                                                   | $I_{LOAD} = 250\text{ mA}; T_j = 130\text{ }^{\circ}\text{C}$ |      |      | 2.2  | $\Omega$         |
| $I_{OLimit}$   | Overcurrent limitation                                                            | $8\text{ V} < V_S < 16\text{ V}$                              | 500  |      | 1500 | mA               |
| $t_{ONHL}$     | Turn on delay time to 10% $V_{OUT}$                                               |                                                               |      |      | 100  | $\mu\text{s}$    |
| $t_{OFFLH}$    | Turn off delay time to 90% $V_{OUT}$                                              |                                                               |      |      | 100  | $\mu\text{s}$    |
| $t_{SCF}$      | Short circuit filter time                                                         |                                                               |      | 64   |      | $\mu\text{s}$    |
| $dV_{max}/dt$  | Maximum external applied slew rate on LS1_FSO and LS2_FSO without switching on LS | Guaranteed by design                                          | 60   |      |      | V/ $\mu\text{s}$ |

### 3.4.19 Wake up input WU

The voltages are referred to ground and currents are assumed positive, when the current flows into the pin.  $6\text{ V} \leq V_{\text{SREG}} \leq 28\text{ V}$ ;  $T_j = 40\text{ }^\circ\text{C}$  to  $150\text{ }^\circ\text{C}$ , unless otherwise specified.

**Table 26. Wake-up inputs**

| Symbol                 | Parameter                                                                             | Test condition                                                                        | Min.                      | Typ.                      | Max.                      | Unit          |
|------------------------|---------------------------------------------------------------------------------------|---------------------------------------------------------------------------------------|---------------------------|---------------------------|---------------------------|---------------|
| $V_{\text{WUthn}}$     | Wake-up negative edge threshold voltage                                               |                                                                                       | 0.4<br>$V_{\text{SREG}}$  | 0.45<br>$V_{\text{SREG}}$ | 0.5<br>$V_{\text{SREG}}$  | V             |
| $V_{\text{WUthp}}$     | Wake-up positive edge threshold voltage                                               |                                                                                       | 0.5<br>$V_{\text{SREG}}$  | 0.55<br>$V_{\text{SREG}}$ | 0.6<br>$V_{\text{SREG}}$  | V             |
| $V_{\text{HYST}}$      | Hysteresis                                                                            |                                                                                       | 0.05<br>$V_{\text{SREG}}$ | 0.1<br>$V_{\text{SREG}}$  | 0.15<br>$V_{\text{SREG}}$ | V             |
| $t_{\text{WU\_stat}}$  | Static wake filter time                                                               |                                                                                       |                           | 64                        |                           | $\mu\text{s}$ |
| $I_{\text{WU\_stdby}}$ | Input current in standby mode                                                         | $V_{\text{WU}} < 1\text{ V}$ or<br>$V_{\text{WU}} > (V_{\text{SREG}} - 1.5\text{ V})$ | 5                         | 30                        | 60                        | $\mu\text{A}$ |
| $R_{\text{WU\_act}}$   | Input resistor to GND in Active mode and in Standby mode during Wake-up input sensing |                                                                                       | 80                        | 160                       | 300                       | k $\Omega$    |
| $t_{\text{WU\_cyc}}$   | Cyclic wake filter time                                                               |                                                                                       |                           | 16                        |                           | $\mu\text{s}$ |

### 3.4.20 LIN transceiver

LIN 2.2 compliant for bit-rates up to 20 kBit/s SAE J2602 compatible.

The voltages are referred to ground and currents are assumed positive, when the current flows into the pin.  $6\text{ V} \leq V_{\text{SREG}} \leq 18\text{ V}$ ;  $T_{\text{junction}} = -40\text{ }^\circ\text{C}$  to  $150\text{ }^\circ\text{C}$  unless otherwise specified.

**Table 27. LIN transmit data input: pin TxD**

| Symbol               | Parameter                                | Test condition | Min. | Typ. | Max. | Unit       |
|----------------------|------------------------------------------|----------------|------|------|------|------------|
| $V_{\text{TXDLOW}}$  | Input voltage dominant level             | Active mode    | 1.0  |      |      | V          |
| $V_{\text{TXDHIGH}}$ | Input voltage recessive level            | Active mode    |      |      | 2.3  | V          |
| $V_{\text{TXDHYS}}$  | $V_{\text{TXDHIGH}} - V_{\text{TXDLOW}}$ | Active mode    | 0.2  |      |      | V          |
| $R_{\text{TXDPU}}$   | TXD pull up resistor                     | Active mode    | 13   | 29   | 46   | k $\Omega$ |

**Table 28. LIN receive data output: pin RxD**

| Symbol               | Parameter                      | Test condition | Min.        | Typ.        | Max. | Unit |
|----------------------|--------------------------------|----------------|-------------|-------------|------|------|
| $V_{\text{RXDLOW}}$  | Output voltage dominant level  | Active mode    |             | 0.2         | 0.5  | V    |
| $V_{\text{RXDHIGH}}$ | Output voltage recessive level | Active mode    | $V_1 - 0.5$ | $V_1 - 0.2$ |      | V    |

Table 29. LIN transmitter and receiver: pin LIN

| Symbol              | Parameter                                                    | Test condition                                                                                                                    | Min.                | Typ.               | Max.                | Unit       |
|---------------------|--------------------------------------------------------------|-----------------------------------------------------------------------------------------------------------------------------------|---------------------|--------------------|---------------------|------------|
| $V_{THdom}$         | Receiver threshold voltage recessive to dominant state       |                                                                                                                                   | 0.4<br>$V_{SREG}$   | 0.45<br>$V_{SREG}$ | 0.5<br>$V_{SREG}$   | V          |
| $V_{Busdom}$        | Receiver dominant state                                      |                                                                                                                                   |                     |                    | $0.4V_{SREG}$       | V          |
| $V_{THrec}$         | Receiver threshold voltage dominant to recessive state       |                                                                                                                                   | 0.5<br>$V_{SREG}$   | 0.55<br>$V_{SREG}$ | 0.6<br>$V_{SREG}$   | V          |
| $V_{Busrec}$        | Receiver recessive state                                     |                                                                                                                                   | 0.6<br>$V_{SREG}$   |                    |                     | V          |
| $V_{THhys}$         | Receiver threshold hysteresis: $V_{THrec} - V_{THdom}$       |                                                                                                                                   | 0.07<br>$V_{SREG}$  | 0.1<br>$V_{SREG}$  | 0.175<br>$V_{SREG}$ | V          |
| $V_{THcnt}$         | Receiver tolerance center value: $(V_{THrec} + V_{THdom})/2$ |                                                                                                                                   | 0.475<br>$V_{SREG}$ | 0.5<br>$V_{SREG}$  | 0.525<br>$V_{SREG}$ | V          |
| $V_{THwkup}$        | Activation threshold for wake-up comparator                  |                                                                                                                                   | 1.0                 | 1.5                | 2                   | V          |
| $V_{THwkdown}$      | Activation threshold for wake-up comparator                  |                                                                                                                                   | $V_{SREG} - 3.5$    | $V_{SREG} - 2.5$   | $V_{SREG} - 1.5$    | V          |
| $t_{LINBUS}$        | LIN Bus Wake-up Dominant Filter time                         | Sleep mode; edge: rec-dom                                                                                                         |                     | 64                 |                     | $\mu s$    |
| $t_{dom\_LIN}$      | LIN Bus Wake-up Dominant Filter time                         | Sleep mode; edge: rec-dom-rec                                                                                                     | 28                  |                    |                     | $\mu s$    |
| $I_{LINDomSC}$      | Transmitter input current limit in dominant state            | $V_{TXD} = V_{TXDLOW}$ ;<br>$V_{LIN} = V_{BATMAX} = 18\text{ V}$                                                                  | 40                  | 100                | 180                 | mA         |
| $I_{bus\_PAS\_dom}$ | Input leakage current at the receiver incl. pull-up resistor | $V_{TXD} = V_{TXDHIGH}$ ; $V_{LIN} = 0\text{ V}$ ;<br>$V_{BAT} = 12\text{ V}$ ; Slave mode                                        | -1                  |                    |                     | mA         |
| $I_{bus\_PAS\_rec}$ | Transmitter input current in recessive state                 | In standby modes;<br>$V_{TXD} = V_{TXDHIGH}$ ; $V_{LIN} > 8\text{ V}$ ;<br>$V_{BAT} < 18\text{ V}$ ; $V_{LIN} \geq V_{BAT}$       |                     |                    | 20                  | $\mu A$    |
| $I_{bus\_NO\_GND}$  | Input current if loss of GND at device                       | $GND = V_{SREG}$ ;<br>$0\text{ V} < V_{LIN} < 18\text{ V}$ ;<br>$V_{BAT} = 12\text{ V}$                                           | -1                  |                    | 1                   | mA         |
| $I_{bus}$           | Input current if loss of $V_{BAT}$ at device                 | $GND = V_S$ ; $0\text{ V} < V_{LIN} < 18\text{ V}$<br>$T_j = -40\text{ }^{\circ}\text{C} \dots 105\text{ }^{\circ}\text{C}^{(1)}$ |                     |                    | 30                  | $\mu A$    |
|                     |                                                              | $GND = V_S$ ; $0\text{ V} < V_{LIN} < 18\text{ V}$<br>$T_j = 130\text{ }^{\circ}\text{C}^{(2)}$                                   |                     |                    | 35                  | $\mu A$    |
| $V_{LINdom}$        | LIN voltage level in dominant state                          | Active mode;<br>$V_{TXD} = V_{TXDLOW}$ ;<br>$R_{bus} = 500\text{ }\Omega$                                                         |                     |                    | 1.2                 | V          |
| $V_{LINrec}$        | LIN voltage level in recessive state                         | Active mode;<br>$V_{TXD} = V_{TXDHIGH}$ ;<br>$I_{LIN} = 10\text{ }\mu A$                                                          | $0.8 \cdot V_S$     |                    |                     | V          |
| $R_{LINup}$         | LIN output pull up resistor                                  | $V_{LIN} = 0\text{ V}$                                                                                                            | 20                  | 40                 | 60                  | k $\Omega$ |
| $C_{LIN}$           | LIN input capacitance                                        | Guaranteed by design                                                                                                              |                     |                    | 100                 | pF         |

1. 105°C is the maximum junction temperature of an unpowered device according to this test condition within the specified ambient temperature range
2. Used for device test only

The voltages are referred to ground and currents are assumed positive, when the current flows into the pin.  $6V \leq V_S \leq 28V$ ;  $T_j = -40\text{ }^{\circ}\text{C}$  to  $150\text{ }^{\circ}\text{C}$ , unless otherwise specified.

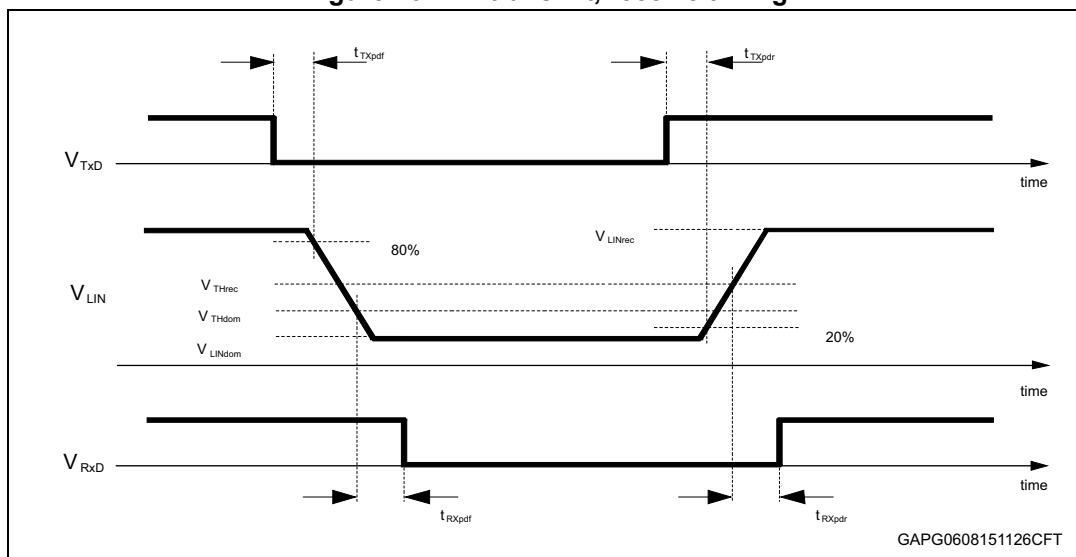
**Table 30. LIN transceiver timing**

| Symbol          | Parameter                                                             | Test condition                                                                                                                                                                                                                                                                                                                                                                                       | Min.  | Typ. | Max.  | Unit          |
|-----------------|-----------------------------------------------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------|------|-------|---------------|
| $t_{RXpd}$      | Receiver propagation delay time                                       | $t_{RXpd} = \max(t_{RXpdr}, t_{RXpdf})$ ;<br>$t_{RXpdf} = t(0.5 V_{RXD}) - t(0.45 V_{LIN})$ ;<br>$t_{RXpdr} = t(0.5 V_{RXD}) - t(0.55 V_{LIN})$ ;<br>$V_{SREG} = 12\text{ V}$ ; $C_{RXD} = 20\text{ pF}$ ;<br>$R_{bus} = 1\text{ k}\Omega$ , $C_{bus} = 1\text{ nF}$ ; $R_{bus} = 660\text{ }\Omega$ ,<br>$C_{bus} = 6.8\text{ nF}$ ; $R_{bus} = 500\text{ }\Omega$ ,<br>$C_{bus} = 10\text{ nF}$    |       |      | 6     | $\mu\text{s}$ |
| $t_{RXpd\_sym}$ | Symmetry of receiver propagation delay time (rising vs. falling edge) | $t_{RXpd\_sym} = t_{RXpdr} - t_{RXpdf}$ ; $V_{SRE} = 12\text{ V}$ ;<br>$R_{bus} = 1\text{ k}\Omega$ ; $C_{bus} = 1\text{ nF}$ ; $C_{RXD} = 20\text{ pF}$                                                                                                                                                                                                                                             | -2    |      | 2     | $\mu\text{s}$ |
| D1              | Duty Cycle 1                                                          | $TH_{Rec}(\max) = 0.744 * V_{SREG}$ ;<br>$TH_{Dom}(\max) = 0.581 * V_{SREG}$ ;<br>$V_{SREG} = 7\text{ to }18\text{ V}$ , $t_{bit} = 50\text{ }\mu\text{s}$ ;<br>$D1 = t_{bus\_rec}(\min) / (2 * t_{bit})$ ;<br>$R_{bus} = 1\text{ k}\Omega$ , $C_{bus} = 1\text{ nF}$ ; $R_{bus} = 660\text{ }\Omega$ ,<br>$C_{bus} = 6.8\text{ nF}$ ; $R_{bus} = 500\text{ }\Omega$ ,<br>$C_{bus} = 10\text{ nF}$   | 0.396 |      |       |               |
| D2              | Duty Cycle 2                                                          | $TH_{Rec}(\min) = 0.422 * V_{SREG}$ ;<br>$TH_{Dom}(\min) = 0.284 * V_{SREG}$ ;<br>$V_{SREG} = 7.6\text{ to }18\text{ V}$ , $t_{bit} = 50\text{ }\mu\text{s}$ ;<br>$D2 = t_{bus\_rec}(\max) / (2 * t_{bit})$ ;<br>$R_{bus} = 1\text{ k}\Omega$ , $C_{bus} = 1\text{ nF}$ ; $R_{bus} = 660\text{ }\Omega$ ,<br>$C_{bus} = 6.8\text{ nF}$ ; $R_{bus} = 500\text{ }\Omega$ ,<br>$C_{bus} = 10\text{ nF}$ |       |      | 0.581 |               |
| D3              | Duty Cycle 3                                                          | $TH_{Rec}(\max) = 0.778 * V_{SREG}$ ;<br>$TH_{Dom}(\max) = 0.616 * V_{SREG}$ ; $V_{SREG} = 7$<br>to $18\text{ V}$ , $t_{bit} = 96\text{ }\mu\text{s}$ ;<br>$D3 = t_{bus\_rec}(\min) / (2 * t_{bit})$ ;<br>$R_{bus} = 1\text{ k}\Omega$ , $C_{bus} = 1\text{ nF}$ ; $R_{bus} = 660\text{ }\Omega$ ,<br>$C_{bus} = 6.8\text{ nF}$ ; $R_{bus} = 500\text{ }\Omega$ ,<br>$C_{bus} = 10\text{ nF}$        | 0.417 |      |       |               |
| D4              | Duty Cycle 4                                                          | $TH_{Rec}(\min) = 0.389 * V_{SREG}$ ;<br>$TH_{Dom}(\min) = 0.251 * V_{SREG}$ ;<br>$V_{SREG} = 7.6\text{ to }18\text{ V}$ , $t_{bit} = 96\text{ }\mu\text{s}$ ;<br>$D4 = t_{bus\_rec}(\max) / (2 * t_{bit})$ ;<br>$R_{bus} = 1\text{ k}\Omega$ , $C_{bus} = 1\text{ nF}$ ; $R_{bus} = 660\text{ }\Omega$ ,<br>$C_{bus} = 6.8\text{ nF}$ ; $R_{bus} = 500\text{ }\Omega$ ,<br>$C_{bus} = 10\text{ nF}$ |       |      | 0.590 |               |
| $t_{dom}(TXDL)$ | TXDL dominant time-out                                                |                                                                                                                                                                                                                                                                                                                                                                                                      |       | 12   |       | ms            |

Table 30. LIN transceiver timing (continued)

| Symbol         | Parameter                           | Test condition | Min. | Typ. | Max. | Unit    |
|----------------|-------------------------------------|----------------|------|------|------|---------|
| $t_{LIN}$      | LIN permanent recessive time-out    |                |      | 40   |      | $\mu s$ |
| $t_{dom(bus)}$ | LIN Bus permanent dominant time-out |                |      | 12   |      | ms      |

Figure 16. LIN transmit, receive timing



### 3.4.21 SPI

The voltages are referred to ground and currents are assumed positive, when the current flows into the pin.  $6\text{ V} < V_{SREG} < 18\text{ V}$ ;  $V_1 = 5\text{ V}$ ; all outputs open;  $T_j = -40\text{ }^{\circ}\text{C}$  to  $150\text{ }^{\circ}\text{C}$ , unless otherwise specified.

Table 31. Input: CSN

| Symbol        | Parameter                  | Test condition | Min. | Typ. | Max. | Unit       |
|---------------|----------------------------|----------------|------|------|------|------------|
| $V_{CSNLOW}$  | Input voltage low level    | Normal mode    | 1.0  |      |      | V          |
| $V_{CSNHIGH}$ | Input voltage high level   | Normal mode    |      |      | 2.3  | V          |
| $V_{CSNHYS}$  | $V_{CSNHIGH} - V_{CSNLOW}$ | Normal mode    | 0.2  |      |      | V          |
| $I_{CSNPU}$   | CSN Pull up resistor       | Normal mode    | 13   | 29   | 46   | k $\Omega$ |

Table 32. Inputs: CLK, DI

| Symbol        | Parameter                              | Test condition                                                    | Min. | Typ. | Max. | Unit    |
|---------------|----------------------------------------|-------------------------------------------------------------------|------|------|------|---------|
| $t_{set}$     | Delay time from standby to Active mode | Time until SPI, ADC and OUT15/OUT_HS are operative                |      | 10   |      | $\mu s$ |
| $t_{set\_CP}$ | Delay time from standby to Active mode | Time until power stages that are supplied by the CP are operative | 560  | 750  | 960  | $\mu s$ |

Table 32. Inputs: CLK, DI (continued)

| Symbol         | Parameter                                                      | Test condition          | Min. | Typ. | Max. | Unit          |
|----------------|----------------------------------------------------------------|-------------------------|------|------|------|---------------|
| $V_{in\_L}$    | Input low level                                                |                         | 1.0  |      |      | V             |
| $V_{in\_H}$    | Input high level                                               |                         |      |      | 2.3  | V             |
| $V_{in\_Hyst}$ | Input hysteresis                                               |                         | 0.2  |      |      | V             |
| $I_{pdin}$     | Pull down current at input                                     | $V_{in} = 1.5\text{ V}$ | 5    | 30   | 60   | $\mu\text{A}$ |
| $C_{in}^{(1)}$ | Input capacitance at input CSN, CLK, DI and PWM <sub>1,2</sub> | Guaranteed by design    |      |      | 15   | pF            |
| $f_{CLK}$      | SPI input frequency at CLK                                     |                         |      |      | 4    | MHz           |

1. Value of input capacity is not measured in production test. Parameter guaranteed by design.

Table 33. DI, CLK and CSN timing

| Symbol         | Parameter                                          | Test condition | Min. | Typ. | Max. | Unit |
|----------------|----------------------------------------------------|----------------|------|------|------|------|
| $t_{CLK}$      | Clock period                                       |                | 250  |      |      | ns   |
| $t_{CLKH}$     | Clock high time                                    |                | 100  |      |      | ns   |
| $t_{CLKL}$     | Clock low time                                     |                | 100  |      |      | ns   |
| $t_{set\_CSN}$ | CSN setup time, CSN low before rising edge of CLK  |                | 150  |      |      | ns   |
| $t_{set\_CLK}$ | CLK setup time, CLK high before rising edge of CSN |                | 150  |      |      | ns   |
| $t_{set\_DI}$  | DI setup time                                      |                | 25   |      |      | ns   |
| $t_{hold\_DI}$ | DI hold time                                       |                | 25   |      |      | ns   |
| $t_{r\_in}$    | Rise time of input signal DI, CLK, CSN             |                |      |      | 25   | ns   |
| $t_{f\_in}$    | Fall time of input signal DI, CLK, CSN             |                |      |      | 25   | ns   |

Note: See [Figure 18: SPI input timing](#).

Table 34. Output: DO

| Symbol     | Parameter                 | Test condition                             | Min.        | Typ. | Max. | Unit          |
|------------|---------------------------|--------------------------------------------|-------------|------|------|---------------|
| $V_{DOL}$  | Output low level          | $I_{DO} = -4\text{ mA}$                    |             |      | 0.5  | V             |
| $V_{DOH}$  | Output high level         | $I_{DO} = 4\text{ mA}$                     | $V_1 - 0.5$ |      |      | V             |
| $I_{DOLK}$ | 3-state leakage current   | $V_{CSN} = V_1, 0\text{ V} < V_{DO} < V_1$ | -10         |      | 10   | $\mu\text{A}$ |
| $C_{DO}$   | 3-state input capacitance | Guaranteed by design                       |             | 10   | 15   | pF            |

Table 35. DO timing

| Symbol                | Parameter                                  | Test condition                                                                | Min. | Typ. | Max. | Unit |
|-----------------------|--------------------------------------------|-------------------------------------------------------------------------------|------|------|------|------|
| $t_{r\ DO}$           | DO rise time                               | $C_L = 50\text{ pF}$ ; $I_{LOAD} = -1\text{ mA}$                              |      |      | 25   | ns   |
| $t_{f\ DO}$           | DO fall time                               | $C_L = 50\text{ pF}$ ; $I_{LOAD} = -1\text{ mA}$                              |      |      | 25   | ns   |
| $t_{en\ DO\ tri\ L}$  | DO enable time from 3-state to low level   | $C_L = 50\text{ pF}$ ; $I_{LOAD} = -1\text{ mA}$ ; pull-up load to V1         |      | 50   | 100  | ns   |
| $t_{dis\ DO\ L\ tri}$ | DO disable time from low level to 3-state  | $C_L = 50\text{ pF}$ ; $I_{LOAD} = -1\text{ mA}$ ; pull-up load to V1         |      | 50   | 100  | ns   |
| $t_{en\ DO\ tri\ H}$  | DO enable time from 3-state to high level  | $C_L = 50\text{ pF}$ ; $I_{LOAD} = -1\text{ mA}$ ; pull-down load to GND      |      | 50   | 100  | ns   |
| $t_{dis\ DO\ H\ tri}$ | DO disable time from high level to 3-state | $C_L = 50\text{ pF}$ ; $I_{LOAD} = -1\text{ mA}$ ; pull-down load to GND      |      | 50   | 100  | ns   |
| $t_d\ DO$             | DO delay time                              | $V_{DO} < 0.3\text{ V1}$ ;<br>$V_{DO} > 0.7\text{ V1}$ ; $C_L = 50\text{ pF}$ |      | 30   | 60   | ns   |

Note: See [Figure 19: SPI output timing](#).

Table 36. CSN timing

| Symbol            | Parameter                          | Test condition                            | Min. | Typ. | Max. | Unit          |
|-------------------|------------------------------------|-------------------------------------------|------|------|------|---------------|
| $t_{CSN\_HI,min}$ | Minimum CSN high time, active mode | Transfer of SPI-command to Input Register | 6    |      |      | $\mu\text{s}$ |
| $t_{CSNfail}$     | CSN low timeout                    |                                           | 20   | 35   | 50   | ms            |

Note: See [Figure 20: SPI CSN - output timing](#).

### 3.4.22 Input LIN\_FLASH for Flash mode

The voltages are referred to ground and currents are assumed positive, when the current flows into the pin.  $6\text{V} \leq V_{SREG} \leq 18$ ;  $V1 = 5\text{ V}$ ;  $T_j = -40\text{ }^\circ\text{C}$  to  $150\text{ }^\circ\text{C}$ .

Table 37. Inputs LIN\_FLASH for Flash mode

| Symbol         | Parameter                                                           | Test condition | Min. | Typ. | Max. | Unit |
|----------------|---------------------------------------------------------------------|----------------|------|------|------|------|
| $V_{flashL}$   | Input low level ( $V_{LIN\_FLASH}$ for exit from Flash mode)        |                | 6.1  | 7.25 | 8.4  | V    |
| $V_{flashH}$   | Input high level ( $V_{LIN\_FLASH}$ for transition into Flash mode) |                | 7.4  | 8.4  | 9.4  | V    |
| $V_{flashHYS}$ | Input voltage hysteresis                                            |                | 0.6  | 0.8  | 1.0  | V    |

### 3.4.23 Inputs DIR, DIRH, PWMH

The voltages are referred to ground and currents are assumed positive, when the current flows into the pin.  $6\text{ V} \leq V_{\text{SREG}} \leq 18\text{ V}$ ;  $T_j = -40\text{ }^{\circ}\text{C}$  to  $150\text{ }^{\circ}\text{C}$ .

**Table 38. Inputs DIR, DIRH, PWMH**

| Symbol            | Parameter                | Test condition                    | Min. | Typ. | Max. | Unit          |
|-------------------|--------------------------|-----------------------------------|------|------|------|---------------|
| $V_{\text{IL}}$   | Input voltage low level  | $V_{\text{SREG}} = 13.5\text{ V}$ | 1    |      |      | V             |
| $V_{\text{IH}}$   | Input voltage high level | $V_{\text{SREG}} = 13.5\text{ V}$ |      |      | 2.3  | V             |
| $V_{\text{IHYS}}$ | Input hysteresis         | $V_{\text{SREG}} = 13.5\text{ V}$ | 0.2  |      |      | V             |
| $I_{\text{in}}$   | Input pull-down current  | $V_{\text{SREG}} = 13.5\text{ V}$ | 5    | 30   | 60   | $\mu\text{A}$ |

### 3.4.24 Debug input

The voltages are referred to ground and currents are assumed positive, when the current flows into the pin.  $6\text{ V} \leq V_{\text{SREG}} \leq 18\text{ V}$ ;  $T_j = -40\text{ }^{\circ}\text{C}$  to  $150\text{ }^{\circ}\text{C}$ .

**Table 39. Debug input**

| Symbol             | Parameter                | Test condition                               | Min. | Typ. | Max. | Unit             |
|--------------------|--------------------------|----------------------------------------------|------|------|------|------------------|
| $V_{\text{dIL}}$   | Input voltage low level  | $V_{\text{SREG}} = 13.5\text{ V}$            | 1    |      |      | V                |
| $V_{\text{dIH}}$   | Input voltage high level | $V_{\text{SREG}} = 13.5\text{ V}$            |      |      | 2.3  | V                |
| $V_{\text{dIHYS}}$ | Input hysteresis         | $V_{\text{SREG}} = 13.5\text{ V}$            | 0.2  |      |      | V                |
| $R_{\text{din}}$   | Pull-down resistor       | $V_{\text{DEBUG}} = 6\text{ to }18\text{ V}$ | 2.5  | 5    | 7.5  | $\text{k}\Omega$ |

### 3.4.25 ADC characteristics

The voltages are referred to ground and currents are assumed positive, when the current flows into the pin.  $6\text{ V} \leq V_{\text{SREG}} \leq 18\text{ V}$ ,  $T_j = -40\text{ }^{\circ}\text{C}$  to  $150\text{ }^{\circ}\text{C}$ .

**Table 40. ADC characteristics**

| Symbol           | Parameter                                | Test condition                                     | Min. | Typ. | Max. | Unit          |
|------------------|------------------------------------------|----------------------------------------------------|------|------|------|---------------|
| $t_{\text{con}}$ | Conversion time                          |                                                    |      | 2.5  |      | $\mu\text{s}$ |
| $f_{\text{ADC}}$ | Clock frequency (see $f_{\text{clk}2}$ ) |                                                    |      | 8    |      | MHz           |
| Acc              | Accuracy                                 | Voltage divider + reference <sup>(1)</sup>         | -2   |      | 2    | %             |
|                  |                                          | Overall accuracy for WU input: $WU = 22\text{ V}$  | -3   |      | 3    |               |
|                  |                                          | Overall accuracy for WU input: $WU = 18\text{ V}$  | -3.5 |      | 3.5  |               |
|                  |                                          | Overall accuracy for WU input: $WU = 6\text{ V}$   | -4   |      | 4    |               |
|                  |                                          | Overall accuracy for WU input: $WU = 4.5\text{ V}$ | -4.6 |      | 4.6  |               |

Table 40. ADC characteristics (continued)

| Symbol        | Parameter                                              | Test condition | Min. | Typ. | Max. | Unit |
|---------------|--------------------------------------------------------|----------------|------|------|------|------|
| $IE_I$        | Integral linearity error                               |                |      |      | 4    | LSB  |
| $IE_D$        | Differential linearity error                           |                |      |      | 2    | LSB  |
| $V_{AINVS}$   | Conversion voltage range ( $V_S$ , $V_{SREG}$ & $WU$ ) |                | 1    |      | 22   | V    |
| $V_{AINTemp}$ | Conversion voltage range ( $T_{CL1} \dots T_{CL6}$ )   |                | 0    |      | 2    | V    |

1. Guaranteed by design.

### 3.4.26 Temperature diode characteristics

The voltages are referred to ground and currents are assumed positive, when the current flows into the pin.  $6\text{ V} \leq V_{SREG} \leq 18\text{ V}$ ,  $T_j = -40\text{ }^\circ\text{C}$  to  $150\text{ }^\circ\text{C}$

Table 41. Temperature diode characteristics

| Symbol           | Parameter                                                | Test condition                                                                                        | Min. | Typ. | Max. | Unit |
|------------------|----------------------------------------------------------|-------------------------------------------------------------------------------------------------------|------|------|------|------|
| $V_{TROOM\ 1-6}$ | $T_{SENSE}$ output voltage at $25\text{ }^\circ\text{C}$ | $V_S = 12\text{ V}$ ; $T = 25\text{ }^\circ\text{C}$                                                  | —    | 1.4  |      | V    |
| $V_{TSENSE1-6}$  | $T_{SENSE}$ output voltage 1 - 8                         | $T = 25\text{ }^\circ\text{C}$ ; $T = 130\text{ }^\circ\text{C}$ ;<br>$T = -40\text{ }^\circ\text{C}$ | —    | -4   |      | mV/K |

### 3.4.27 Interrupt outputs

The voltages are referred to ground and currents are assumed positive, when the current flows into the pin.  $6\text{ V} \leq V_{SREG} \leq 18\text{ V}$ ,  $T_j = -40\text{ }^\circ\text{C}$  to  $150\text{ }^\circ\text{C}$

Table 42. Interrupt outputs

| Symbol           | Parameter                                       | Test condition              | Min.       | Typ. | Max. | Unit          |
|------------------|-------------------------------------------------|-----------------------------|------------|------|------|---------------|
| $V_{INTL}$       | Output low level                                | $I_{INT} = -4\text{ mA}$    |            |      | 0.5  | V             |
| $V_{INTH}$       | Output high level                               | $I_{INT} = 4\text{ mA}$     | $V1 - 0.5$ |      |      | V             |
| $I_{INTLK}$      | 3-state leakage current                         | $0\text{ V} < V_{INT} < V1$ | -10        |      | 10   | $\mu\text{A}$ |
| $t_{Interrupt}$  | Interrupt pulse duration (NINT, $RxD\_L/NINT$ ) |                             |            | 56   |      | $\mu\text{s}$ |
| $t_{Int\_react}$ | Interrupt reaction time                         | Tested by scan chain        | 6          |      | 40   | $\mu\text{s}$ |

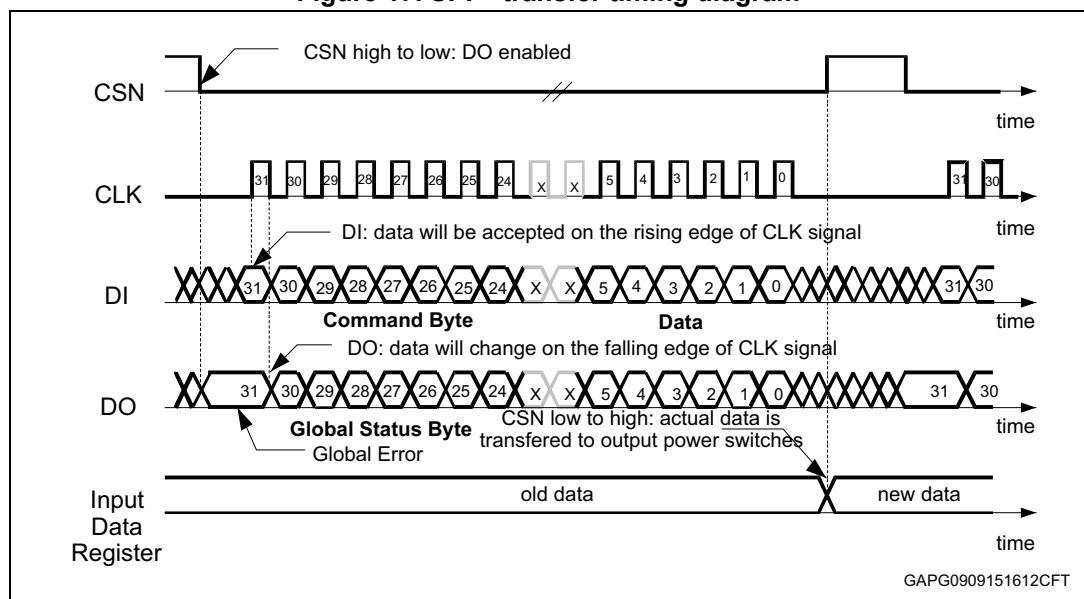
### 3.4.28 Timer1 and Timer2

$6\text{ V} \leq V_{\text{SREG}} \leq 18\text{ V}$ ;  $T_j = -40\text{ }^{\circ}\text{C}$  to  $150\text{ }^{\circ}\text{C}$

**Table 43. Timer1 and Timer2**

| Symbol | Parameter     | Test condition | Min. | Typ. | Max. | Unit |
|--------|---------------|----------------|------|------|------|------|
| ton 1  | Timer on time |                |      | 0.1  |      | ms   |
| ton 2  | Timer on time |                |      | 0.3  |      | ms   |
| ton 3  | Timer on time |                |      | 1    |      | ms   |
| ton 4  | Timer on time |                |      | 10   |      | ms   |
| ton 5  | Timer on time |                |      | 20   |      | ms   |
| T1     | Timer period  |                |      | 10   |      | ms   |
| T2     | Timer period  |                |      | 20   |      | ms   |
| T3     | Timer period  |                |      | 50   |      | ms   |
| T4     | Timer period  |                |      | 100  |      | ms   |
| T5     | Timer period  |                |      | 200  |      | ms   |
| T6     | Timer period  |                |      | 500  |      | ms   |
| T7     | Timer period  |                |      | 1000 |      | ms   |
| T8     | Timer period  |                |      | 2000 |      | ms   |

**Figure 17. SPI – transfer timing diagram**



The SPI can be driven by a micro controller with its SPI peripheral running in the following mode:

CPOL = 0 and CPHA = 0.

For this mode input data is sampled by the low to high transition of the clock CLK, and output data is changed from the high to low transition of CLK.

Figure 18. SPI input timing

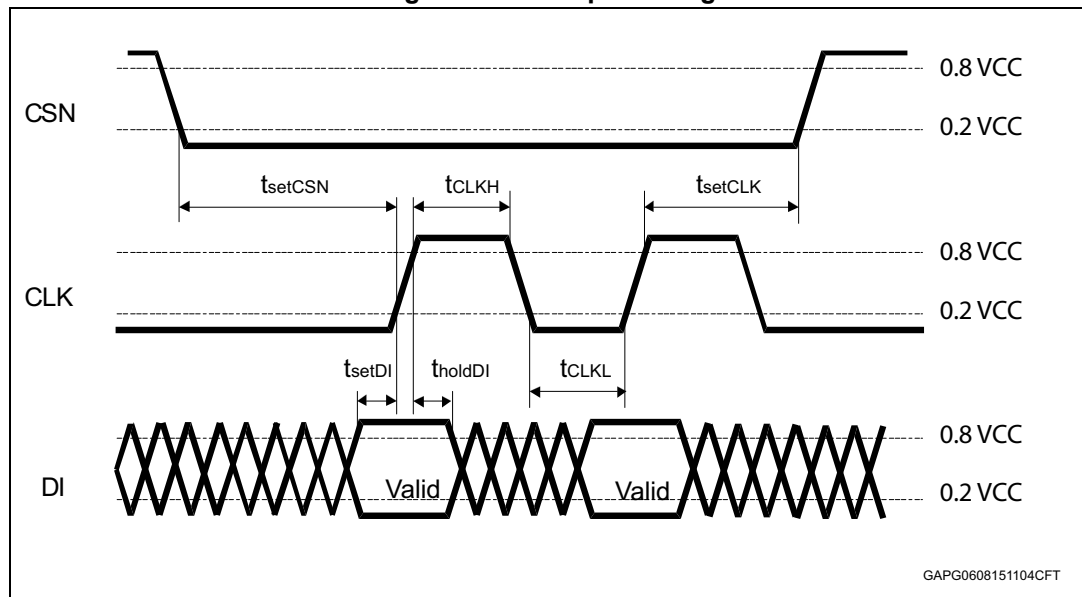


Figure 19. SPI output timing

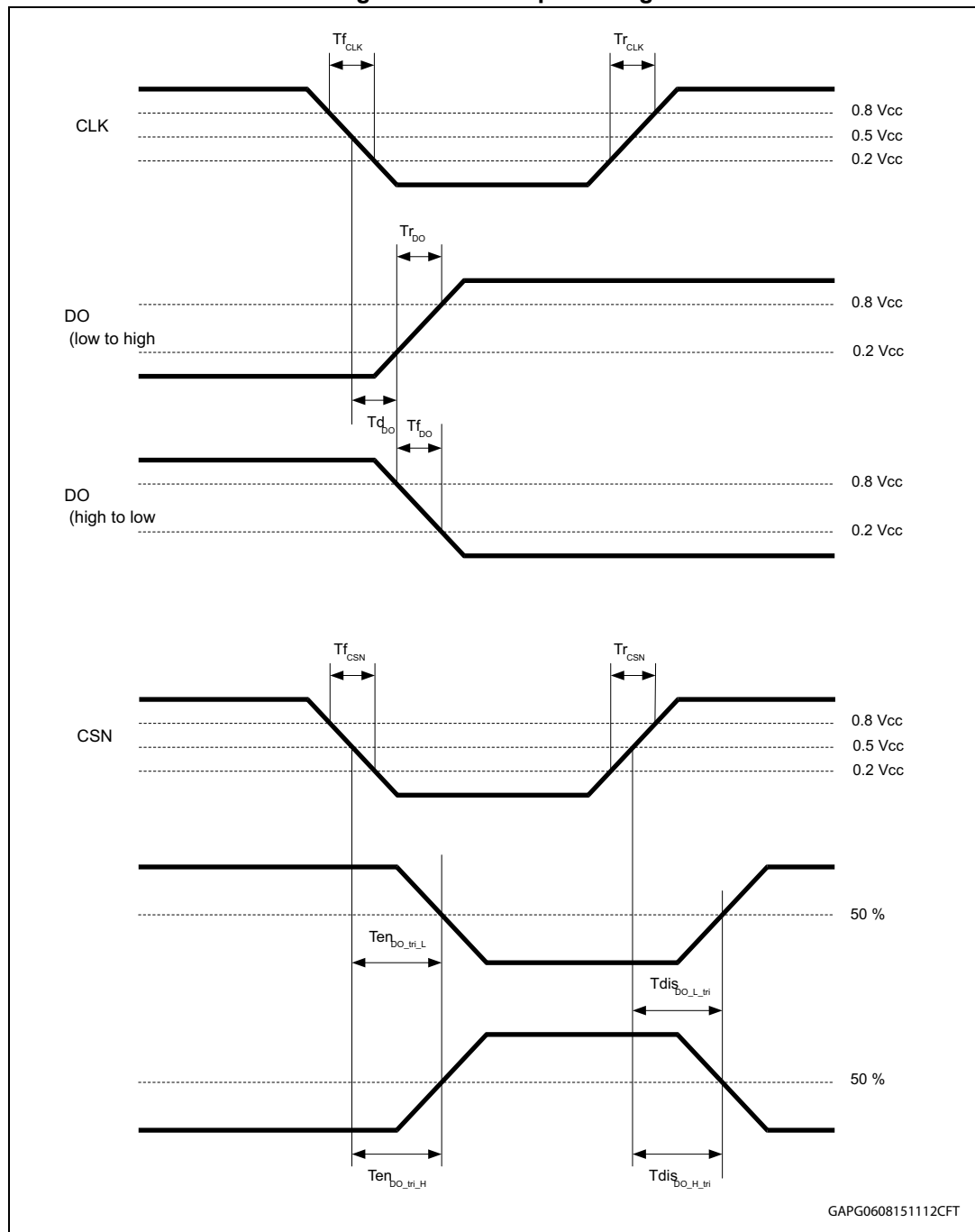


Figure 20. SPI CSN - output timing

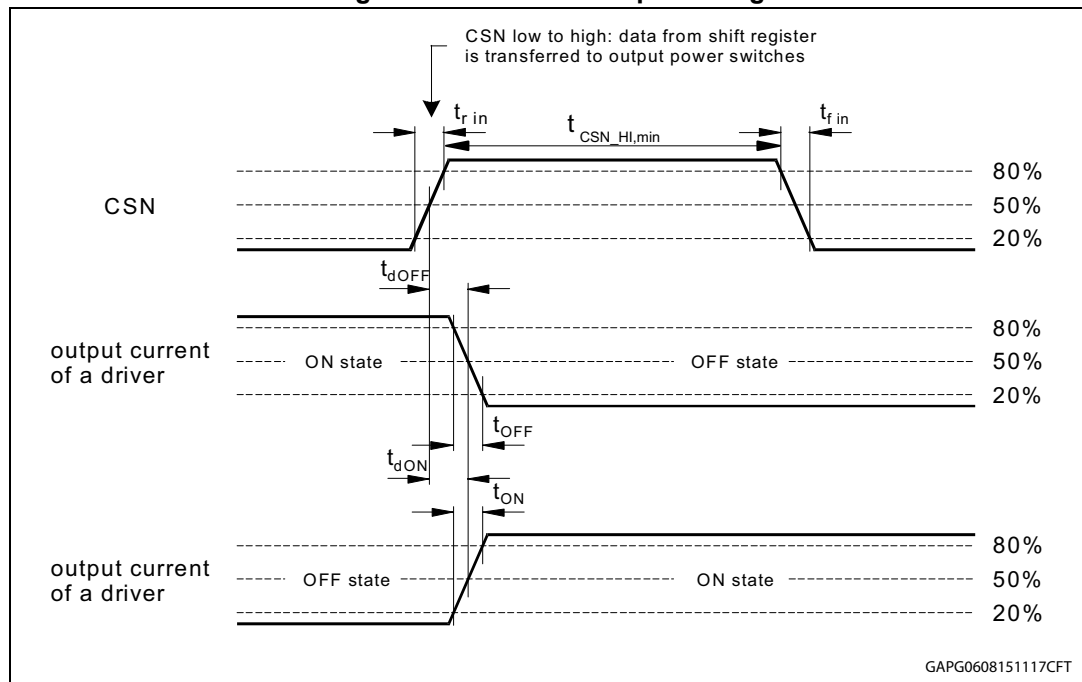
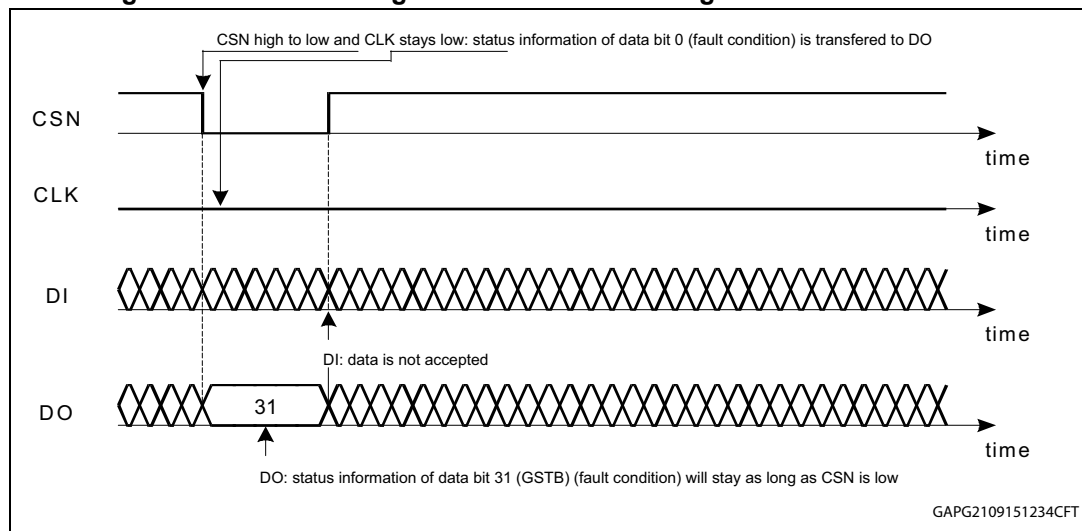


Figure 21. SPI – CSN high to low transition and global status bit access



### 3.4.29 SGND loss comparator

$T_j = -40\text{ }^{\circ}\text{C}$  to  $150\text{ }^{\circ}\text{C}$ , unless otherwise specified.

Table 44. SGND loss comparator

| Symbol         | Parameter                   | Test condition          | Min. | Typ. | Max. | Unit          |
|----------------|-----------------------------|-------------------------|------|------|------|---------------|
| $V_{SGNDloss}$ | $V_{SGND}$ loss threshold   | $(V_{SGND} - V_{PGND})$ | 100  | 270  | 500  | mV            |
| $t_{SGNDloss}$ | $V_{SGND}$ loss filter time |                         | 5    | 7    | 9    | $\mu\text{s}$ |

## 4 Application information

### 4.1 Supply $V_S$ , $V_{SREG}$

$V_{SREG}$  supplies voltage regulators V1 and V2, all internal regulated voltages for analog and digital functionality, LIN and both P-channel high-side switches OUT15 and OUT\_HS.

All other high-sides, Fail Safe block and the charge pump are supplied by  $V_S$ .

In case the  $V_{SREG}$  pin is disconnected, all power outputs connected to  $V_S$  are automatically switched off.

### 4.2 Voltage regulators

The device contains two independent and fully protected low drop voltage regulators designed for very fast transient response and do not require electrolytic output capacitors for stability.

The output voltage is stable with ceramic load capacitors >220 nF.

#### 4.2.1 Voltage regulator: V1

The V1 voltage regulator provides 5 V supply voltage and up to 250 mA continuous load current to supply the system microcontroller. The V1 regulator is embedded in the power management and fail-safe functionality of the device and operates according to the selected operating mode. The V1 voltage regulator is supplied by pin  $V_{SREG}$ .

In addition, the V1 regulator supplies the devices internal loads. The voltage regulator is protected against overload and overtemperature. An external reverse current protection has to be provided by the application circuitry to prevent the input capacitor from being discharged by negative transients or low input voltage. Current limitation of the regulator ensures fast charge of external bypass capacitors. The output voltage is stable for ceramic load capacitors >220 nF.

In case the device temperature exceeds the TSD1 threshold (either cluster or grouped mode) the V1 regulator remains on. The micro controller has the possibility for interaction or error logging. If the chip temperature exceeds the TSD2 threshold ( $TSD2 > TSD1$ ), V1 will be deactivated and all wakeup sources (LIN, WU and Timer) are disabled. After  $t_{TSD}$ , the voltage regulator will restart automatically. If the restart fails 7 times within one minute the devices enter the Forced Vbat\_standby mode. The status bit FORCED\_SLEEP\_TSD2/V1SC (SR1) is set.

#### 4.2.2 Voltage regulator: V2

The voltage regulator V2 is supplied by pin  $V_{SREG}$  and can supply additional 5 V loads such as sensors or potentiometers. The maximum continuous load current is 50 mA. The regulator is protected against:

- Overload
- Overtemperature
- Short-circuit (short to ground and battery supply voltage)
- Reverse biasing

### 4.2.3 Voltage regulator failure

The V1, and V2 regulator output voltages are monitored.

In case of a drop below the failure thresholds ( $V1 < V1_{fail}$  for  $t > t_{V1fail}$ ,  $V2 < V2_{fail}$  for  $t > t_{V2fail}$ ), the failure bits V1FAIL, V2FAIL (SR 2) are latched.

### 4.2.4 Short to ground detection

At turn-on of the V1 and V2 regulators, a short-to-GND condition is detected by monitoring the regulator output voltage.

If V1 or V2 is below the  $V1_{fail}$  (or  $V2_{fail}$ ) threshold for  $t > t_{V1short}$  ( $t > t_{V2short}$ ) after turn-on, the devices will identify a short circuit condition at the related regulator will be switched off.

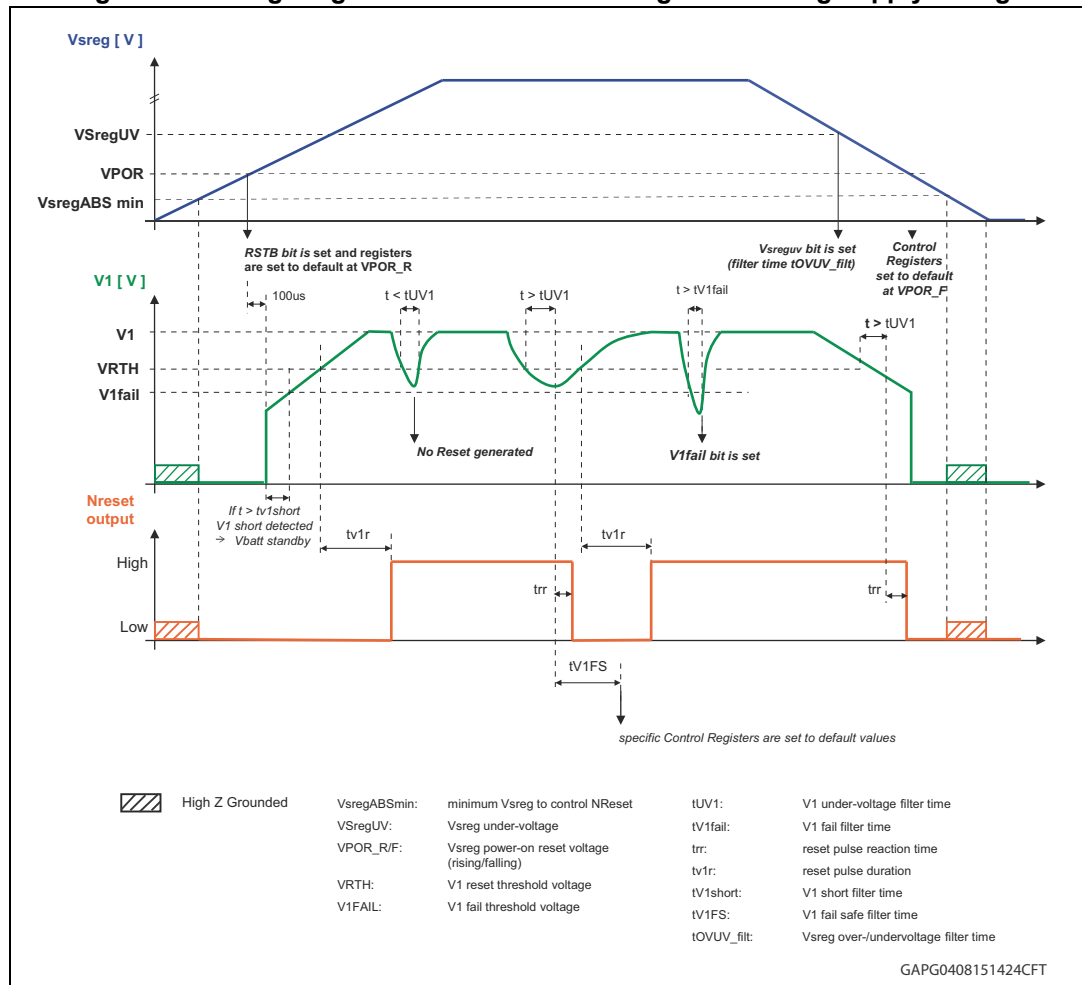
In case of V1 short-to-GND the device enters Forced Vbat\_standby mode automatically. Bits FORCED\_SLEEP\_TSD2/V1SC and (SR 1) V1FAIL (SR 2) are set.

In case of a V2 short-to-GND failure the V2SC (SR 2) and V2FAIL (SR 2) bits are set.

Once the output voltage of the corresponding regulator exceeded the  $V1_{fail}$  ( $V2_{fail}$ ) threshold the short-to-ground detection is disabled. In case of a short-to-ground condition, the regulator is switched off due to thermal shutdown. V1 is switched off at TSD2, V2 is switched off at TSD1.

## 4.2.5 Voltage regulator behavior

Figure 22. Voltage regulator behaviour and diagnosis during supply voltage



## 4.3 Operating modes

The devices can be operated in the following operating modes:

- Active
- LIN Flash
- $V_1\_standby$
- $VBAT\_standby$
- Debug

### 4.3.1 Active mode

All functions are available and the device is controlled by SPI.

### 4.3.2 Flash mode

To program the system microcontroller via LIN bus signals, the devices can be operated in LIN Flash mode. The watchdog is disabled in this mode.

The Flash mode is entered by applying an external voltage at the pin:

- $V_{\text{LIN\_FLASH}} \geq V_{\text{FlashH}}$  (LIN Flash mode)

In LIN Flash mode the maximum bitrate is increased to 100 kbit/s automatically (LIN\_HS\_EN = 1).

A transition from Flash mode to V1\_standby or Vbat\_standby mode is not possible.

At exit from Flash modes ( $V_{\text{LIN\_FLASH}} < V_{\text{FlashL}}$ ) no NReset pulse is generated. The watchdog starts with a Long Open Window ( $t_{\text{LW}}$ ).

### 4.3.3 SW-debug mode

To allow software debugging, the watchdog can be deactivated by applying an external voltage to the DEBUG input pin ( $V_{\text{debug}} > V_{\text{diH}}$ ).

In Debug mode, all device functionality and Operating modes are available. The watchdog is deactivated. At Exit from Debug mode ( $V_{\text{debug}} < V_{\text{diL}}$ ) the watchdog starts with a Long Open Window.

*Note: The device includes a test mode. This mode is activated by a dedicated sequence which includes a high voltage at the Debug Pin. The Debug Pin must be kept at nominal voltage levels in order to avoid accidental activation of the test mode.*

### 4.3.4 V1\_standby mode

The transition from Active mode to V1\_standby mode is controlled by SPI.

To supply the micro controller in a low power mode, the V1 voltage regulator remains active.

After the V1\_standby command (CSN low to high transition), the device enters V1\_standby mode immediately and the watchdog starts a Long Open Window ( $t_{\text{LW}}$ ). The watchdog is deactivated as soon as the V1 load current drops below the  $I_{\text{CMP}}$  threshold ( $I_{\text{V1}} < I_{\text{cmp\_fal}}$ ).

The V1 load current monitoring can be deactivated by setting ICMP = 1. In this configuration the watchdog will be deactivated upon transition into V1\_standby mode without monitoring the V1 load current.

Writing ICMP (CR 34) = 1 is only possible with the first SPI command after setting ICMP\_CONFIG\_EN (Config Reg) = 1.

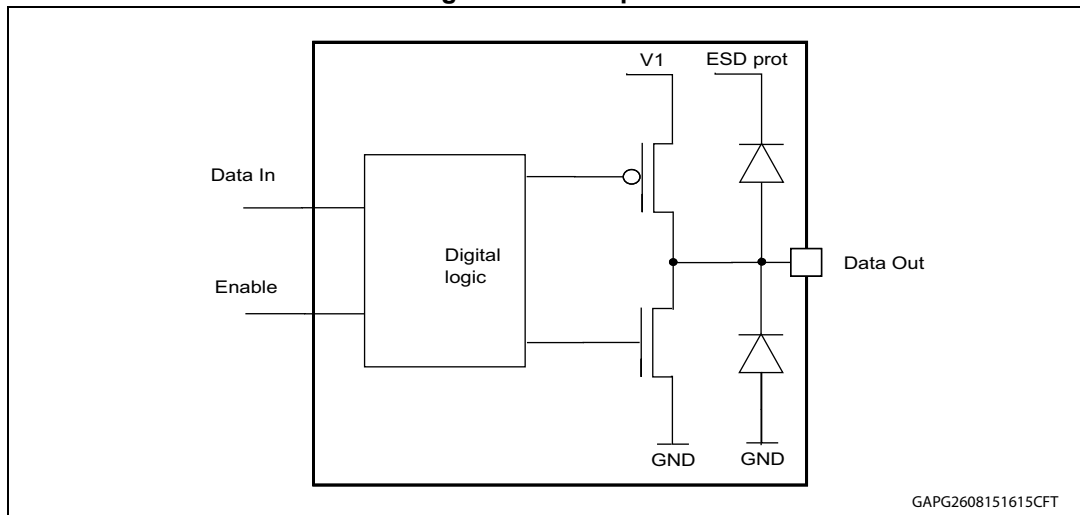
The ICMP\_CONFIG\_EN bit is reset to 0 automatically with the next SPI command.

Power outputs (except OUT\_HS & OUT15) are switched off in V1\_standby mode. OUT\_HS & OUT15 remain in the configuration programmed prior to the standby command in order to enable (cyclic) supply of external contacts. The timer signal (Timer1 or Timer2) can be mirrored to the NINT output pin during V1\_standby mode.

LIN transmitter (TxDL) is off.

### 4.3.5 Interrupt

Figure 23. NINT pins



RxDL/NINT indicates:

- a wake-up event from V1\_standby mode and the programmable timer interrupt  
RxDL/NINT pin is pulled low for  $t = t_{\text{interrupt}}$ .

NINT indicates:

- In Active mode:  
V<sub>SREG</sub> dropped below the programmed early warning threshold in Control Register 3 (V<sub>SREG</sub> < VSREG\_EW\_TH); feature is deactivated if VSREG\_EW\_TH is set to 0 V.  
In V1\_standby mode
  - Programmable timer interrupt; An NINT pulse is generated at the beginning of the timer on-time (Timer 1 or Timer2)
  - Wake-up from V1\_standby mode by any wake-up source
 NINT is pulled low for  $t = t_{\text{interrupt}}$

In case of increasing V1 load current during V1\_standby mode ( $I_{V1} > I_{\text{cmp\_ris}}$ ), the device remains in standby mode and the watchdog starts with a Long Open Window. No Interrupt signal is generated.

### 4.3.6 VBAT\_standby mode

The transition from Active mode to Vbat\_standby mode is initiated by an SPI command. In Vbat\_standby mode, the voltage regulators V1 and V2 (depending on configuration in CR 1), the power outputs (except OUT15 and OUT\_HS) as well as LIN transmitter are switched off.

An NReset pulse is generated upon wake-up from Vbat\_standby mode.

## 4.4 Wake-up from Standby modes

A wake-up from standby mode will switch the device to Active mode. This can be initiated by one or more of the following events:

Table 45. Wake-up events description

| Wake up source                                | Description                                                                                                                                                                                                                                                                                              |
|-----------------------------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| LIN bus activity                              | Always enabled                                                                                                                                                                                                                                                                                           |
| Level change of WU                            | Can be configured or disabled by SPI                                                                                                                                                                                                                                                                     |
| $I_{V1} > I_{cmp\_ris}$                       | Device remains in <i>V1_standby mode</i> but watchdog is enabled (If $I_{CMP} = 0$ ). No interrupt is generated.                                                                                                                                                                                         |
| Timer Interrupt / Wake up of $\mu C$ by TIMER | Programmable by SPI:<br>– <i>V1_standby mode</i> : device wakes up after programmable timer expiration. NINT and RxDL/NINT interrupt signals are generated<br>– <i>Vbat_standby mode</i> : device wakes up after programmable timer expiration, V1 regulator is turned on and NReset signal is generated |
| SPI Access                                    | Always active (except in <i>VBAT_STANDBY mode</i> )<br>Wake up event: CSN is low and first rising edge on CLK                                                                                                                                                                                            |

#### 4.4.1 Wake up input

The WU input can be configured as wake-up source. The wake-up input is sensitive to any level transition (positive and negative edge) and can be configured for static or cyclic monitoring of the input voltage level.

For static contact monitoring, a filter time of  $t_{WU\_STAT}$  is implemented. The filter is started when the input voltage passes the specified threshold  $V_{WU\_THP}$  or  $V_{WU\_THN}$ .

Cyclic contact monitoring allows periodical activation of the wake-up input to read the status of the external contact. The periodical activation can be configured to Timer 1 or Timer 2. The input signal is filtered with a filter time of  $t_{WU\_CYC}$  after a delay (80% of the configured Timer on-time). A Wake-up will be processed if the status has changed versus the previous cycle. The buffered output OUT\_HS can be used to supply the external contacts with the timer setting according to the cyclic monitoring of the wake-up input.

In standby modes, the input WU is configurable with an internal pull-up or pull-down current source according to the setup of the external contact. In Active mode the inputs have an internal pull down resistor ( $R_{WU\_act}$ ) and the input status can be read by SPI. Static sense should be configured before the read operation is started in order to reflect the actual input level.

## 4.5 Functional overview (truth table)

Table 46. Status of different functions/features vs operating modes

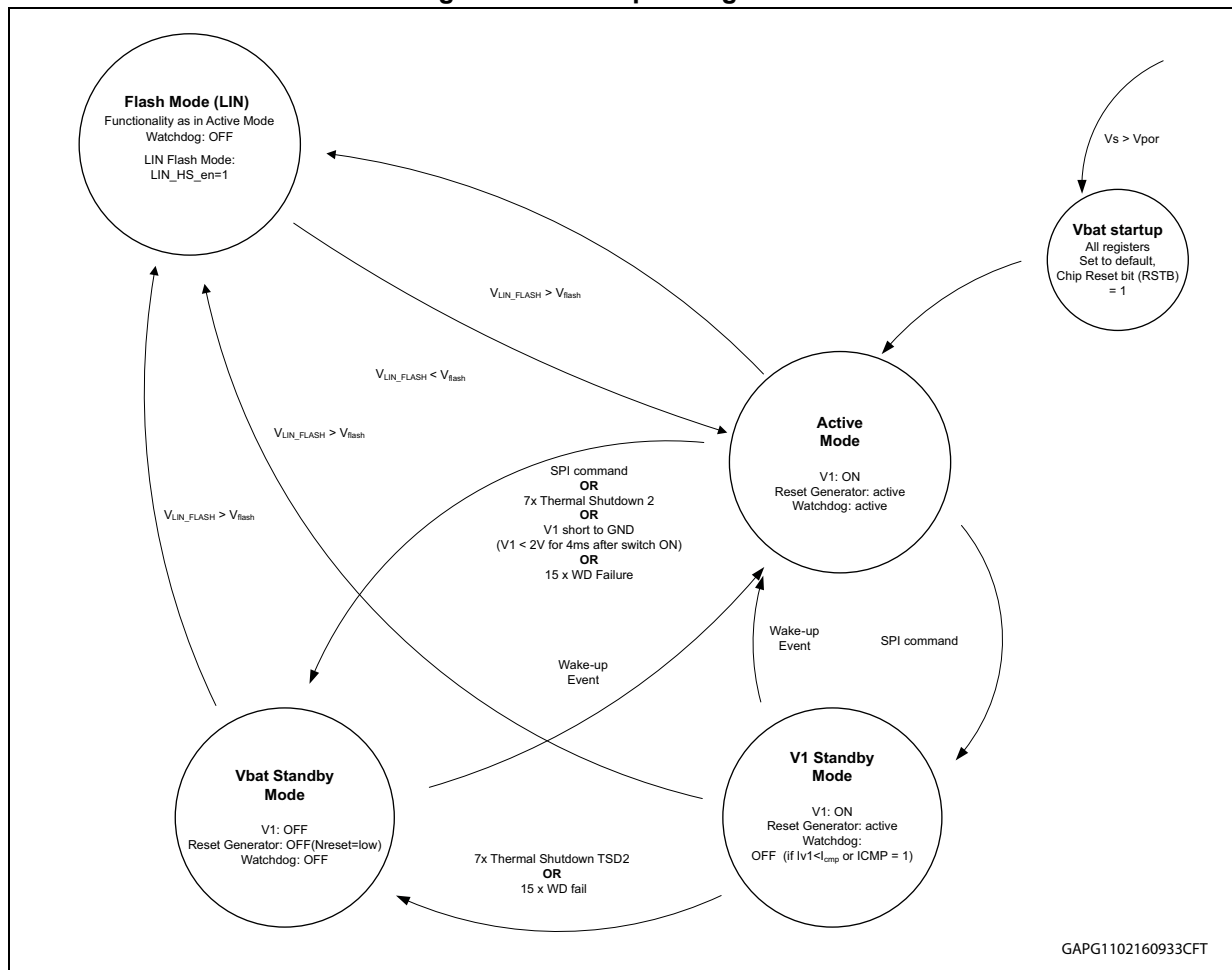
| Function             | Comments               | Operating modes        |                                                    |                                                      |
|----------------------|------------------------|------------------------|----------------------------------------------------|------------------------------------------------------|
|                      |                        | Active mode            | V <sub>1</sub> -standby static mode (cyclic sense) | V <sub>bat</sub> -standby static mode (cyclic sense) |
| Voltage regulator V1 | $V_{OUT} = 5\text{ V}$ | On                     | On <sup>(1)</sup>                                  | Off                                                  |
| Voltage regulator V2 | $V_{OUT} = 5\text{ V}$ | On/ Off <sup>(2)</sup> | On <sup>(2)</sup> / Off                            | On <sup>(2)</sup> / Off                              |
| Reset generator      |                        | On                     | On                                                 | Off                                                  |

Table 46. Status of different functions/features vs operating modes (continued)

| Function                                                                                                       | Comments               | Operating modes        |                                                    |                                                      |
|----------------------------------------------------------------------------------------------------------------|------------------------|------------------------|----------------------------------------------------|------------------------------------------------------|
|                                                                                                                |                        | Active mode            | V <sub>1</sub> -standby static mode (cyclic sense) | V <sub>bat</sub> -standby static mode (cyclic sense) |
| Window watchdog                                                                                                | V <sub>1</sub> monitor | On                     | Off (on if $I_{V1} > I_{CMP}$ and $I_{CMP} = 0$ )  | Off                                                  |
| Wake up                                                                                                        |                        | Off                    | Active <sup>(3)</sup>                              | Active <sup>(3)</sup>                                |
| HS-cyclic supply                                                                                               | Oscillator time base   | On / Off               | On <sup>(2)</sup> / Off                            | On <sup>(2)</sup> / Off                              |
| LIN                                                                                                            | LIN 2.2a               | On                     | Off <sup>(4)</sup>                                 | Off <sup>(4)</sup>                                   |
| Oscillator OSC1                                                                                                | 2 MHz                  | On                     | On/Off <sup>(5)</sup>                              | On/Off <sup>(5)</sup>                                |
| Oscillator OSC2                                                                                                | 32 MHz                 | ON                     | Off                                                | Off                                                  |
| V <sub>SREG</sub> -Monitor                                                                                     |                        | On                     | (6)                                                | (6)                                                  |
| V <sub>S</sub> -Monitor                                                                                        |                        | On                     | Off                                                | Off                                                  |
| H-bridge Gate Driver, bridge drivers, all high-side drivers (except OUT_HS & OUT15) supplied by V <sub>S</sub> |                        | On/ Off <sup>(2)</sup> | Off                                                | Off                                                  |
| Fail-safe low-side switches                                                                                    |                        | On/ Off <sup>(7)</sup> | On                                                 | On                                                   |
| Short circuit protection for fail-safe low-side switches (in case LS is switched on)                           |                        | On                     | On                                                 | On                                                   |
| OUT_HS & OUT15 (P-channel HS) supplied by V <sub>SREG</sub>                                                    |                        | On/ Off <sup>(2)</sup> | On/ Off <sup>(2)</sup>                             | On/ Off <sup>(2)</sup>                               |
| Charge pump                                                                                                    |                        | On                     | Off                                                | Off                                                  |
| ADC (SPI read out and V <sub>SREG</sub> early warning interrupt)                                               |                        | On                     | Off                                                | Off                                                  |
| Thermal shutdown TSD2                                                                                          |                        | On                     | On                                                 | Off                                                  |
| Thermal shutdown TSD1x for OUT_HS and OUT15 (P-channel HS)                                                     |                        | On                     | On/ Off <sup>(2)</sup>                             | On/ Off <sup>(2)</sup>                               |

1. Supply the processor in low current mode.
2. According to SPI setting and DIR.
3. Unless disabled by SPI.
4. The bus state is internally stored when going to standby mode. A change of bus state will lead to a wake-up after exceeding of internal filter time.
5. ON, if cyclic sense is enabled or during wake-up request.
6. Cyclic activation = pulsed ON during cyclic sense.
7. ON in Fail-Safe mode; if standby mode is entered with active Fail-safe mode the output remains ON in standby mode.

Figure 24. Main operating modes



## 4.6 Configurable window watchdog

During normal operation, the watchdog monitors the micro controller within a programmable trigger cycle.

After power-on or standby mode, the watchdog is started with a timeout (Long Open Window  $t_{LW}$ ). The timeout allows the micro controller to run its own setup and then to start the window watchdog by setting TRIG (CR1,ConfigReg) = 1

Subsequently, the micro controller has to serve the watchdog by alternating the watchdog trigger bit TRIG (CR1,Config Reg) within the safe trigger area  $T_{SWX}$ .

The trigger time is configurable by SPI. A correct watchdog trigger signal will immediately start the next cycle. After 8 watchdog failures in sequence, the V1 regulator is switched off for  $t_{V1OFF}$ . After 7 additional watchdog failures the V1 regulator is turned off permanently and the device goes into Forced Vbat\_standby mode. The status bit FORCED\_SLEEP\_WD (SR 1) is set. A wake-up is possible by LIN.

After wake-up from Forced Vbat\_standby mode and the watchdog trigger still fails, the device enters Forced Vbat\_standby mode again after one Long Open Window.

This actually produces an additional watchdog failure but the watchdog fail counter will remain at maximum value of 15 failures.

This sequence is repeated until a valid watchdog trigger event is performed by writing  $TRIG = 1$ .

In case of a Watchdog failure, the power outputs and V2 are switched off and the status bit WDFAIL (SR 1) is set to 1. A reset pulse is generated at NReset output and the device enters Fail-safe mode. Control registers are set to their Fail Safe values and the Fail-safe low-side switches are turned on. Please refer to chapter [Section 4.7: Fail-safe mode](#) for more details.

The following diagrams illustrate the Watchdog behavior of the devices. The diagrams are split into 3 parts. The first diagram shows the functional behavior of the watchdog without any error. The second diagram covers the behavior covering all the error conditions, which can affect the watchdog behavior. [Figure 27: Watchdog in Flash mode](#) shows the transition in and out of Flash modes. [Figure 25](#), [Figure 26](#) and [Figure 27](#) can be overlapped to get all the possible state transitions under all circumstances. For a better readability, they were split in normal operating, operating with errors and Flash mode.

**Figure 25. Watchdog in normal operating mode (no errors)**

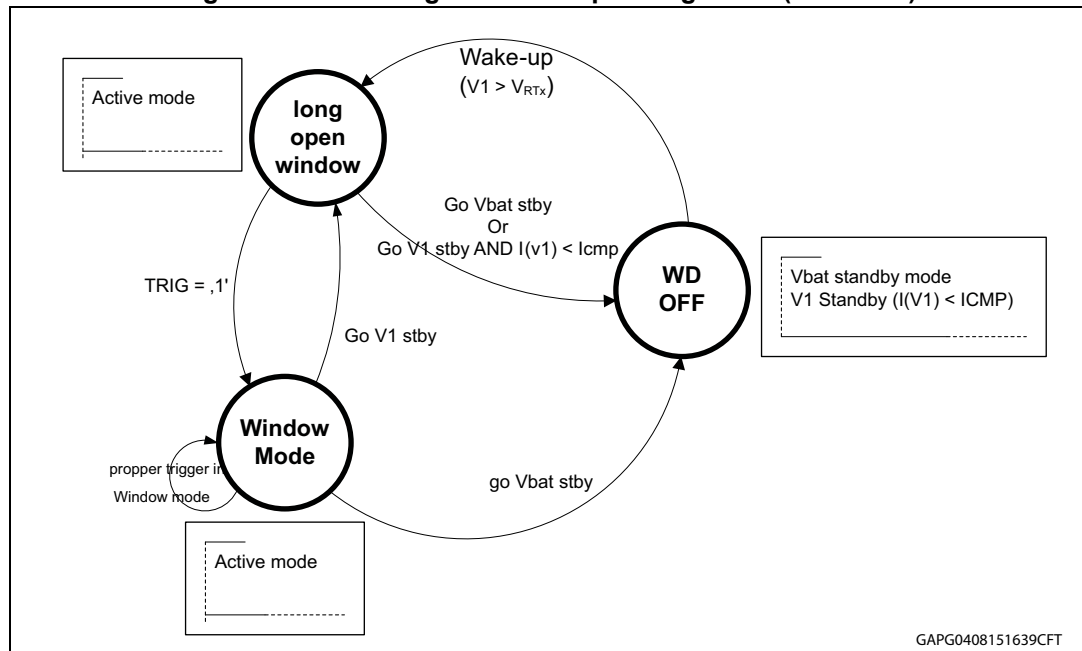


Figure 26. Watchdog with error conditions

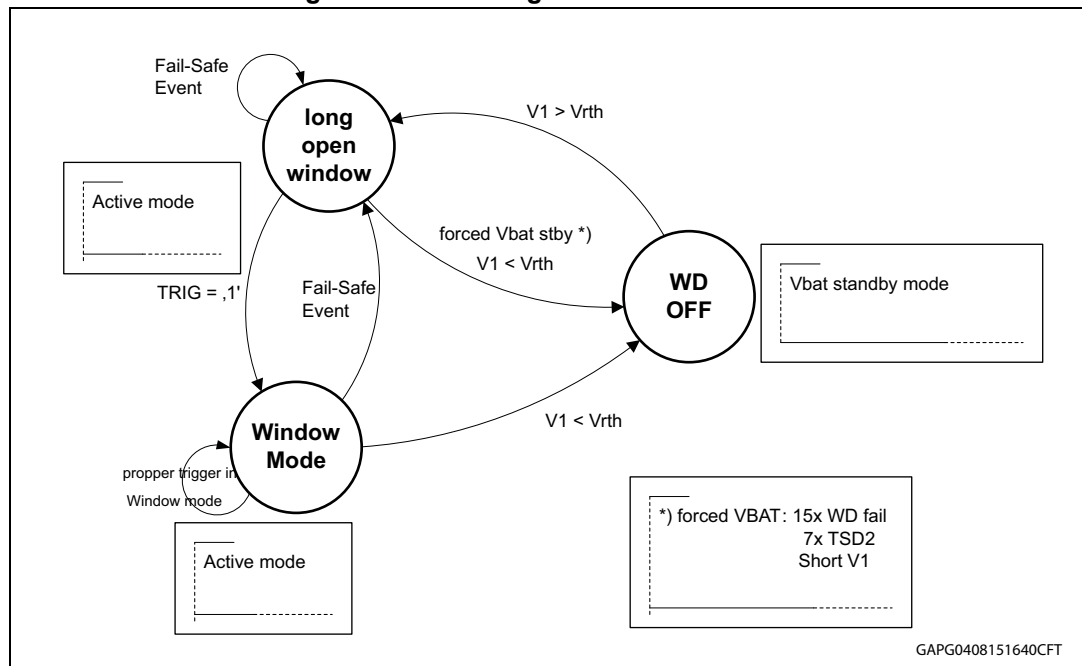
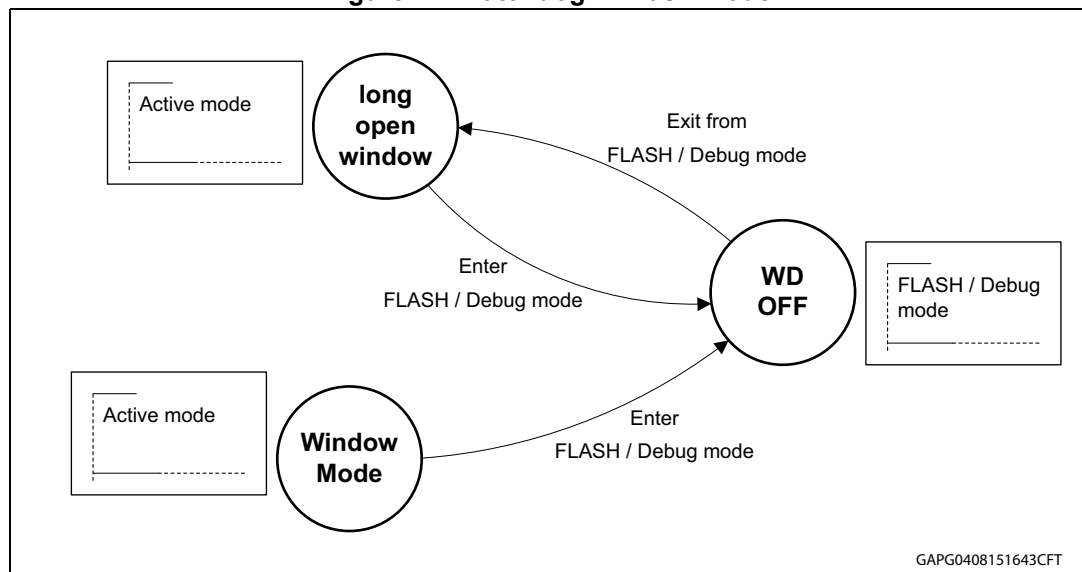


Figure 27. Watchdog in Flash mode



**Note:** Whenever the device is operated without servicing the mandatory watchdog trigger events, a sequence of 15 consecutive reset events is performed and the device enters the Forced\_Vbat\_Stby mode with bit FORCED\_SLEEP\_WD in SR1 set.

If the device is woken up after such a forced VBAT\_Standby condition and the watchdog is still not serviced, the device, after one long open watchdog window will re-enter the same Forced\_Vbat\_Stby mode until the next wake up event. In this case, an additional watchdog failure is generated, but the fail counter is not cleared, keeping the maximum number of 15 failures. This sequence is repeated until a valid watchdog trigger event is performed by writing  $TRIG = 1$ .

### 4.6.1 Change watchdog timing

The watchdog trigger time is configured by setting WD\_TIME\_x (CR 2). Writing to these bits is possible only using the first SPI command after setting WD\_CONFIG\_EN = 1 (Config Reg). The WD\_CONFIG\_EN bit is reset to 0 automatically with the next SPI command.

## 4.7 Fail-safe mode

### 4.7.1 Temporary failures

The devices enter Fail-safe mode in case of:

- Watchdog failure
- V1 turn on failure
  - V1 short ( $V1 < V1_{fail}$  for  $t > t_{V1short}$ )
- V1 failure ( $V1 < V_{RTxfalling}$  for  $t > t_{V1FS}$ )
- Thermal Shutdown TSD2

The Fail Safe functionality is also available in V1\_Standby mode. During V1\_Standby mode the Fail Safe mode is entered in the following cases:

- V1 failure ( $V1 < V_{RTxfalling}$  for  $t > t_{V1FS}$ )
- Watchdog failure (if watchdog still running due to  $I_{V1} > I_{cmp\_fal}$ )
- Thermal Shutdown TSD2

In Fail Safe mode the devices return to a fail safe state. The Fail Safe condition is indicated to the system in the Global Status Byte. The conditions during Fail Safe mode are:

- All outputs beside LS1\_FSO and LS2\_FSO are turned off
- All Control Registers are set to fail safe default values
- Write operations to Control Registers are blocked until the Fail Safe condition is cleared. The following bits are not WRITE protected:
  - TRIG (CR1<bit 0>, Config Register <bit 0>): watchdog trigger bit
  - V2\_x (CR1<bit 4:5>): Voltage Regulator V2 control
  - CR2 (bit <8:23>): Timer1 and Timer2 settings
  - OUT\_HS\_x (CR5 <bit 0:3>): OUT\_HS configuration
  - OUT15\_x (CR6<bit 0:3>): OUT15 configuration
  - PWMx\_freq\_y (CR12): PWM frequency configuration
  - PWMx\_DC\_y (CR13 – CR17): PWM duty cycle configuration
- LIN transmitter and SPI remain on (transmitters are deactivated in case of thermal shutdown TSD1 (TSD1 cluster 5 or 6 in cluster mode))
- Corresponding Failure Bits in Status Registers are set
- FS Bit (Global Status Byte) is set
- LS1\_FSO and LS2\_FSO will be turned on
- Charge pump is switched off

If the Fail Safe mode was entered it keeps active until the Fail safe condition is removed and the Fail Safe was read by SPI. Depending on the root cause of the Fail Safe operation, the actions to exit Fail safe mode are as shown in the following table.

Table 47. Temporary failures description

| Failure source               | Failure condition                              | Diagnosis                                                                        | Exit from Fail-safe mode                               |
|------------------------------|------------------------------------------------|----------------------------------------------------------------------------------|--------------------------------------------------------|
| Microcontroller (oscillator) | Watchdog early write failure or expired window | FS (Global Status Byte) =1;<br>WDFAIL (SR 1) =1;<br>WDFAIL_CNT_x (SR 1) = n+1    | TRIG (CR 1) = 1 during long open window Read&Clear SR1 |
| V1                           | Short at turn-on                               | FS (Global Status Byte) =1;<br>FORCED_SLEEP_TSD2/V1SC (SR 1) =1                  | Wake-up;<br>Read&Clear SR1                             |
|                              | Undervoltage                                   | FS (Global Status Byte) = 1; V1UV (SR 1) = 1; V1fail (SR 2) = 1 <sup>(1)</sup>   | V1 > V <sub>RTrising</sub> ;<br>Read&Clear SR1         |
| Temperature                  | T <sub>j</sub> > T <sub>SD2</sub>              | FS (Global Status Byte) = 1; TW (SR 2) = 1;<br>TSD1 (SR 1) =1;<br>TSD2 (SR 1) =1 | T <sub>j</sub> < T <sub>SD2</sub> ;<br>Read&Clear SR1  |

1. If V1 < V1<sub>fail</sub> (for t > t<sub>V1fail</sub>). The Fail-safe Bit is located in the Global Status Register.

#### 4.7.2 Non-recoverable failures – forced Vbat\_standby mode

If the Fail-safe condition persists and all attempts to return to normal system operation fail, the devices enter the *Forced Vbat\_standby* mode in order to prevent damage to the system. The Forced Vbat\_standby mode can be terminated by any wake-up source. The root cause of the Forced Vbat\_standby mode is indicated in the SPI Status Registers.

In Forced Vbat\_standby mode, all Control Registers are set to power-on default values except:

- CP\_DITH\_DIS (Config. Reg <bit 5>)

The Forced Vbat\_standby mode is entered in case of:

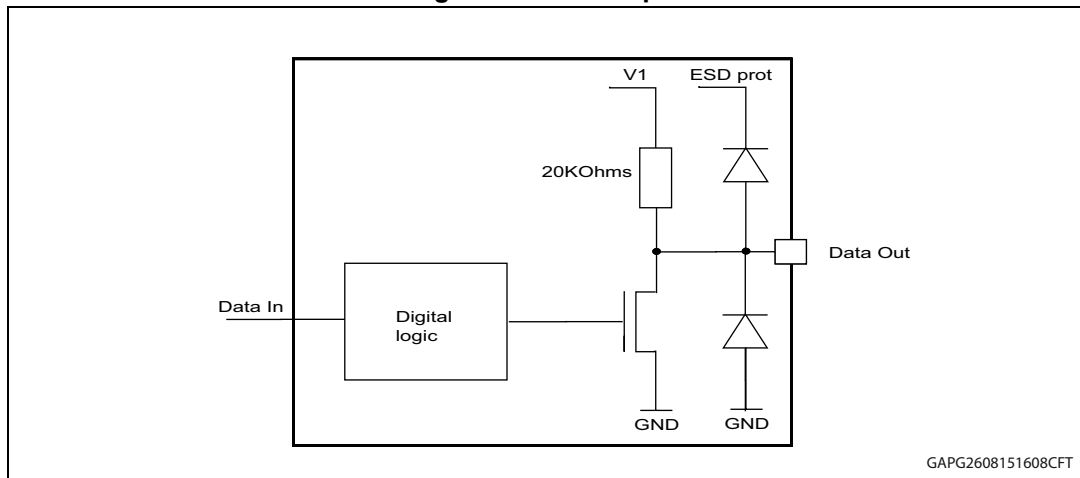
- Multiple watchdog failures: FORCED\_SLEEP\_WD (SR 1) = 1 (15 x watchdog failure)
- Multiple thermal shutdown 2: FORCED\_SLEEP\_TSD2/V1SC (SR 1) = 1 (7 x TSD2)
- V1 short at turn-on (V1 < V1<sub>fail</sub> for t > t<sub>V1short</sub>):  
FORCED\_SLEEP\_TSD2/V1SC (SR 1) = 1

Table 48. Non-recoverable failure

| Failure source               | Failure condition                | Diagnosis                                                                                                            | Exit from Fail-safe mode                                            |
|------------------------------|----------------------------------|----------------------------------------------------------------------------------------------------------------------|---------------------------------------------------------------------|
| Microcontroller (Oscillator) | 15 consecutive Watchdog Failures | FS (Global Status Byte) = 1; WDFAIL (SR 1) = 1; FORCED_SLEEP_WD (SR 1) = 1                                           | Wake-up;<br>TRIG (CR 1) = 1 during long open window; Read&Clear SR1 |
| V1                           | Short at turn-on                 | FS (Global Status Byte) = 1;<br>FORCED_SLEEP_TSD2/V1SC (SR 1) = 1                                                    | Wake-up;<br>Read&Clear SR1                                          |
| Temperature                  | 7 times TSD2                     | FS (Global Status Byte) =1; TW (SR 2) = 1;<br>TSD1 (SR 1) = 1; TSD2 (SR 1) = 1;<br>FORCED_SLEEP_TSD2/V1SC (SR 1) = 1 | Wake-up;<br>Read&Clear SR1                                          |

## 4.8 Reset output (NReset)

Figure 28. NReset pin



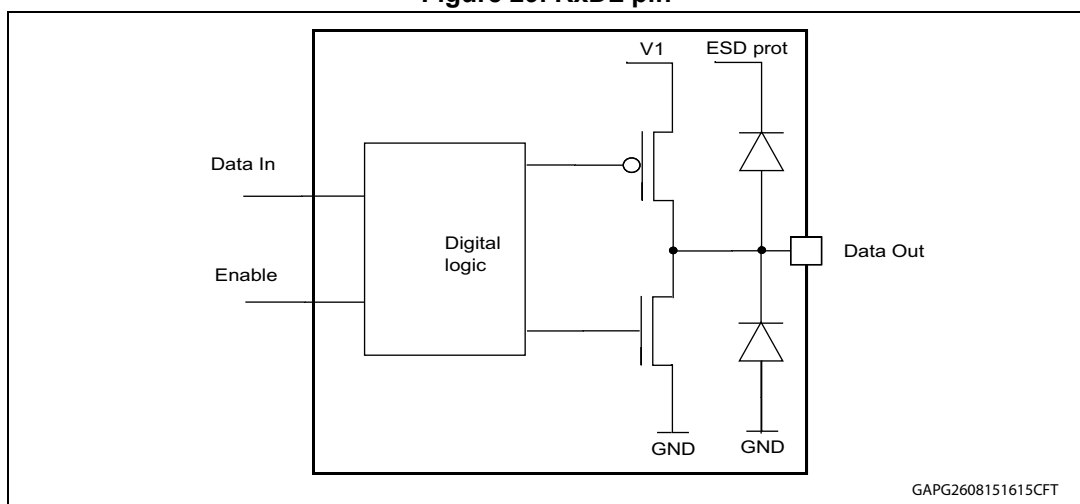
If V1 is turned on and the voltage exceeds the V1 reset threshold, the reset output *NReset* is pulled up to V1 by an internal pull-up resistor after a reset delay time ( $t_{V1R}$ ). This is necessary for a defined start of the micro controller when the application is switched on. Since the *NReset* output is realized as an open drain output it is also possible to connect an external *NReset* open drain *NReset* source to the output. As soon as the *NReset* is released by the devices the watchdog starts with a long open window.

A reset pulse is generated in case of:

- V1 drops below  $V_{RTxfalling}$  (configurable by SPI) for  $t > t_{UV1}$
- Watchdog failure
- Turn-on of the V1 regulator ( $V_{SREG}$  Power-on or wake-up from Vbat\_standby mode)

## 4.9 LIN Bus Interface

Figure 29. RxDL pin



### 4.9.1 Features

- LIN 2.2a compliant (SAEJ2602 compatible) transceiver
- LIN Cell has been designed according to “Hardware requirements for transceivers (version 1.3)”
- Bitrate up to 20 kbit/s
- Dedicated LIN Flash mode with bitrate up to 100 kbit/s
- GND disconnection fail safe at module level
- Off mode: does not disturb network
- GND shift operation at system level
- Micro controller Interface with CMOS-compatible I/O pins
- Internal pull-up resistor
- Receive-only mode
- ESD and transient immunity according to ISO7637 and EN / IEC61000-4-2
- Matched output slopes and propagation delay
- Wake-up behaviour according to LIN2.2a and Hardware Requirements for LIN, CAN and Flexray Interfaces (version 1.3)

At  $V_{SREG} > V_{POR}$  (i.e.  $V_{SREG}$  power-on reset threshold), the LIN transceiver is enabled. The LIN transmitter is disabled in case of the following errors:

- Dominant TxDL time out
- LIN permanent recessive
- Thermal shutdown 1
- $V_{SREG}$  overvoltage/ undervoltage

The LIN receiver is not disabled in case of any failure condition.

The default bitrate of the transceiver allows communication up to 20 kbit/s. To enable fast flashing via the LIN bus, the transceiver can be operated in high speed mode by setting bit LIN\_HS\_EN (Config Reg) = 1. This feature is enabled automatically in LIN Flash mode.

### 4.9.2 Error handling

The devices LIN transceiver provides the following 3 error handling features.

#### Dominant TxDL time out

If TXD\_L is in dominant state (low) for  $t > t_{dom(TXDL)}$  the transmitter will be disabled, the status bit LIN\_TXD\_DOM (SR 2) will be set.

The transmitter remains disabled until the status bit is cleared.

The TxD dominant timeout detection can be disabled via SPI (LIN\_TXD\_TOUT\_EN = 0).

#### Permanent recessive

If TXD\_L changes to dominant (low) state but RXD\_L signal does not follow within  $t < t_{LIN}$  the transmitter will be disabled, the status bit LIN\_PERM\_REC (SR 2) will be set.

The transmitter remains disabled until the status bit is cleared.

### Permanent dominant

If the bus state is dominant (low) for  $t > t_{\text{dom}}(\text{bus})$  a bus permanent dominant failure will be detected. The status bit LIN\_PERM\_DOM (SR 2) will be set.

The transmitter will not be disabled.

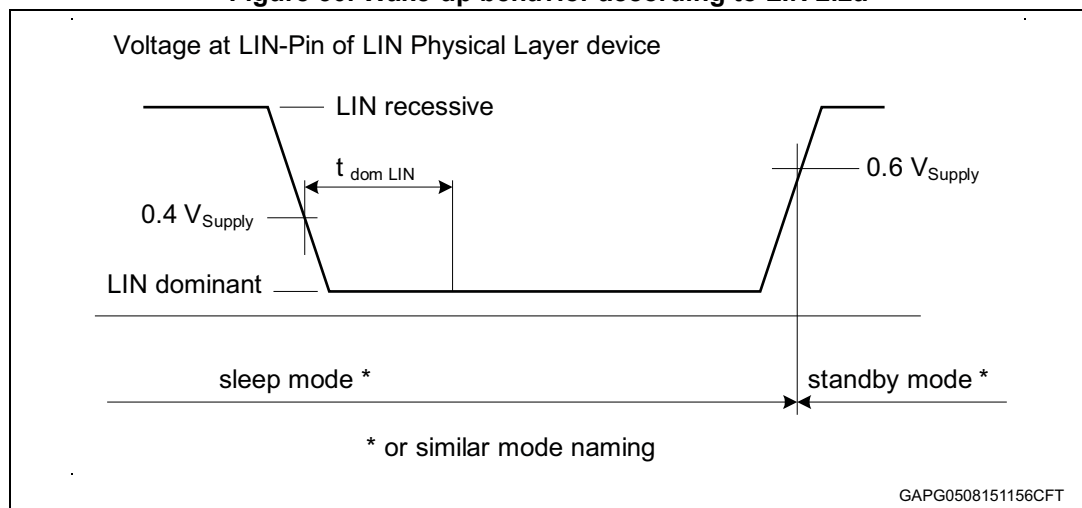
### 4.9.3 Wake up from Standby modes

In low power modes (V1\_standby mode and Vbat\_standby mode) the devices can receive two types of wake up signals from the LIN bus (configurable by SPI bit LIN\_WU\_CONFIG (Config Reg)):

- Recessive-Dominant-recessive pattern with  $t > t_{\text{dom\_LIN}}$  (default, according to LIN 2.2a)
- State Change recessive-to-dominant or dominant-to-recessive (according to LIN 2.1)

#### Pattern Wake-up (default)

Figure 30. Wake-up behavior according to LIN 2.2a



#### Status change wake-up - Recessive-to-dominant

Normal wake-up can occur when the LIN transceiver was set in standby mode while LIN was in recessive (high) state. A dominant level at LIN for  $t > t_{\text{LINBUS}}$ , will switch the devices to Active mode.

#### Status change wake-up - Dominant-to-recessive

If the LIN transceiver was set in standby mode while LIN was in dominant (low) state, recessive level at LIN for  $t > t_{\text{LINBUS}}$ , will switch the devices to Active mode.

### 4.9.4 Receive-only mode

The LIN transmitter can be disabled in Active mode by setting the bit LIN\_REC\_ONLY (CR2). In this mode it is possible to listen to the bus but not sending to it.

## 4.10 Serial Peripheral Interface (ST SPI Standard)

A 32-bit SPI is used for bi-directional communication with the microcontroller.

The SPI is driven by a microcontroller with its SPI peripheral running in following mode: CPOL = 0 and CPHA = 0. For this mode input data is sampled by the low to high transition of the clock CLK, and output data is changed from the high to low transition of CLK.

This device is not limited to microcontroller with a built-in SPI. Only three CMOS-compatible output pins and one input pin is needed to communicate with the device. A fault condition can be detected by setting CSN to low. If CSN = 0, the DO-Pin reflects the global error flag (fault condition) of the device.

- Chip Select Not (CSN)

The input Pin is used to select the serial interface of this device. When CSN is high, the output Pin (DO) is in high impedance state. A low signal activates the output driver and a serial communication can be started.

The state during CSN = 0 is called a communication frame.

If CSN = low for  $t > t_{\text{CSNfail}}$  the DO output is switched to high impedance in order not to block the signal line for other SPI nodes.

- Serial Data In (DI)

The input Pin is used to transfer data serial into the device. The data applied to the DI is sampled at the rising edge of the CLK signal and shifted into an internal 32-bit shift register. At the rising edge of the CSN signal the content of the shift register is transferred to Data Input Register. The writing to the selected Data Input Register is only enabled if exactly 32-bit are transmitted within one communication frame (i.e. CSN low). If more or less clock pulses are counted within one frame the complete frame is ignored. This safety function is implemented to avoid an activation of the output stages by a wrong communication frame.

*Note: Due to this safety functionality a daisy chaining of SPI is not possible. Instead, a parallel operation of the SPI bus by controlling the CSN signal of the connected IC's is recommended.*

- Serial Data Out (DO)

The data output driver is activated by a logical low level at the CSN input and will go from high impedance to a low or high level depending on the global error flag (fault condition). The first rising edge of the CLK input after a high to low transition of the CSN Pin will transfer the content of the selected status register into the data out shift register. Each subsequent falling edge of the CLK will shift the next bit out.

- Serial Clock (CLK)

The CLK input is used to synchronize the input and output serial bit streams. The data input (DI) is sampled at the rising edge of the CLK and the data output (DO) will change with the falling edge of the CLK signal. The SPI can be driven with a CLK Frequency up to 4 MHz.

## 4.11 Power supply failure

### 4.11.1 $V_S$ supply failure

#### $V_S$ overvoltage

If the supply voltages  $V_S$  reaches the overvoltage threshold  $V_{SOV}$ :

- LIN remains enabled
- OUT1 to OUT\_14 are turned off (default).  
The shutdown of outputs may be disabled by SPI ( $VS\_OV\_SD\_EN$  (CR 3) = 0)
- Charge pump is disabled (and is switched on automatically in case the supply voltage recovers to normal operating voltage)
- H-bridge gate driver is switched into sink condition
- Recovery of outputs after overvoltage condition is configurable by SPI:
  - $VS\_LOCK\_EN$  (CR 3) = 1: outputs are off until Read&Clear  $VS\_OV$  (SR 2).
  - $VS\_LOCK\_EN$  (CR 3) = 0: outputs turned on automatically after  $V_S$  overvoltage condition has recovered.
- The overvoltage bit  $VS\_OV$  (SR 2) is set and can be cleared with a 'Read&Clear' command. The overvoltage bit is reset automatically if  $VS\_LOCK\_EN$  (CR 3) = 0 and the overvoltage condition has recovered.

#### $V_S$ undervoltage

If the supply voltage  $V_S$  drops below the under voltage threshold voltage ( $V_{SUV}$ ):

- LIN remains enabled
- OUT1 to OUT14 are turned off (default).
- The shutdown of outputs may be disabled by SPI ( $VS\_UV\_SD\_EN$  (CR 3) = 0)
- Recovery of outputs after undervoltage condition is configurable by SPI:
  - $VS\_LOCK\_EN$  (CR 3) = 1: outputs are off until Read&Clear  $VS\_UV$  (SR 2).
  - $VS\_LOCK\_EN$  (CR 3) = 0: outputs turned on automatically after  $V_S$  undervoltage condition has recovered.
- The undervoltage bit  $VS\_UV$  (SR 2) is set and can be cleared with a 'Read&Clear' command. The undervoltage bit is removed automatically if  $VS\_LOCK\_EN$  (CR 3) = 0 and the undervoltage condition has recovered.

### 4.11.2 V<sub>SREG</sub> supply failure

#### V<sub>SREG</sub> overvoltage

If the supply voltages V<sub>SREG</sub> reaches the overvoltage threshold V<sub>SREG\_OV</sub>:

- LIN is switched to high impedance
- OUT15 and OUT\_HS are turned off (default).  
The shutdown of outputs may be disabled by SPI (V<sub>SREG\_OV\_SD\_EN</sub> (CR 3) = 0)
- Recovery of outputs after overvoltage condition is configurable by SPI:
  - VSREG\_LOCK\_EN (CR 3) = 1: outputs are off until Read&Clear VSREG\_OV (SR 2).
  - VSREG\_LOCK\_EN (CR 3) = 0: outputs turned on automatically after V<sub>SREG</sub> overvoltage condition has recovered.
- The overvoltage bit VSREG\_OV (SR 2) is set and can be cleared with a 'Read&Clear' command. The overvoltage bit is reset automatically if VSREG\_LOCK\_EN (CR 3) = 0 and the overvoltage condition has recovered.

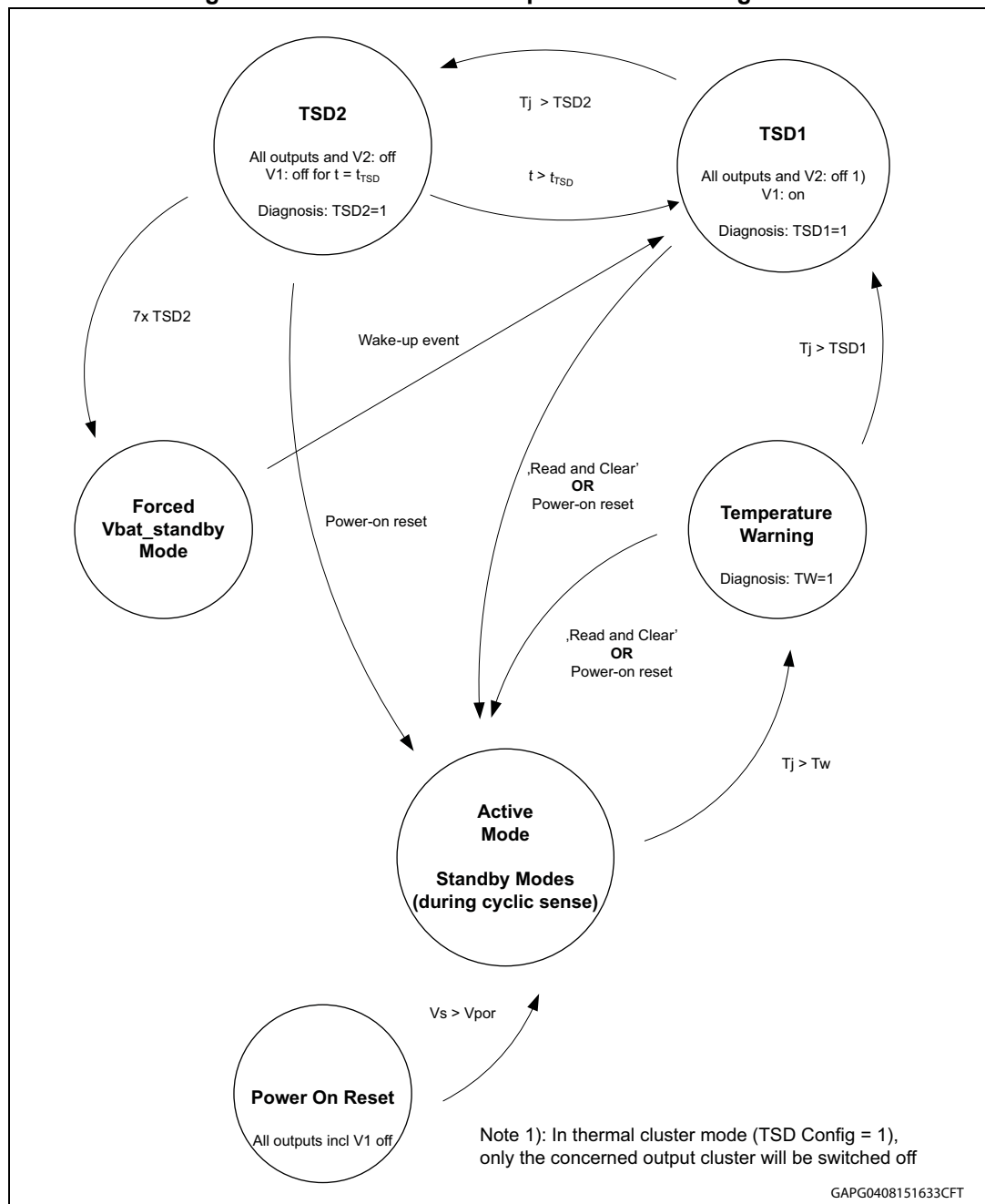
#### V<sub>SREG</sub> undervoltage

If the supply voltage V<sub>SREG</sub> drops below the under voltage threshold voltage (V<sub>SREG\_UV</sub>):

- LIN is switched to high impedance
- OUT15 and OUT\_HS are turned off (default).
- The shutdown of outputs may be disabled by SPI (VSREG\_UV\_SD\_EN (CR 3) = 0)
- Recovery of outputs after undervoltage condition is configurable by SPI:
  - VSREG\_LOCK\_EN (CR 3) = 1: outputs are off until Read&Clear VSREG\_UV (SR 2).
  - VSREG\_LOCK\_EN (CR 3) = 0: Outputs turned on automatically after V<sub>SREG</sub> undervoltage condition has recovered.
- The undervoltage bit VSREG\_UV (SR 2) is set and can be cleared with a 'Read&Clear' command. The undervoltage bit is removed automatically if VSREG\_LOCK\_EN (CR 3) = 0 and the undervoltage condition has recovered.

## 4.12 Temperature warning and thermal shutdown

Figure 31. Thermal shutdown protection and diagnosis



**Note:** The Thermal State machine will recover the same state as before entering Standby mode. In case of a TSD2 it will enter TSD1 state.

## 4.13 Power outputs OUT1..15 and OUT\_HS

The component provides a total of 4 half bridges outputs OUT1, OUT4-6 to drive motors and 10 stand alone high-side outputs OUT7..15 and OUT\_HS to drive e.g. LED's, bulbs or to supply contacts. All high-side outputs beside OUT\_HS and OUT15 are supplied by the pin VS and OUT\_HS and OUT15 are supplied by the buffered supply VSREG. OUT\_HS is intended to be used as contact supply. Beside OUT15 and OUT\_HS the high-side switches can be activated only in case of running charge pump. OUT15 and OUT\_HS can be activated also in standby modes.

All high-side and low-side outputs switch off in case of:

- $V_S$  ( $V_{SREG}$ ) overvoltage and undervoltage (depending on configuration, see [Section 4.11.2:  \$V\_{SREG}\$  supply failure](#))
- Overcurrent (depending on configuration, auto recovery mode (see below))
- Overtemperature (TSD1x/ cluster or single mode)
- Fail safe event
- Loss of GND at SGND pin

In case of overcurrent or overtemperature (TSD1\_CLx (SR 6)) condition, the drivers will switch off. The relevant status bit will be latched and can be read and optionally cleared by SPI. The drivers remain off until the status is cleared. In case overvoltage/ undervoltage condition, the drivers will be switched off. The relevant status bit will be latched and can be read and optionally cleared by SPI. If VSREG\_LOCK\_EN (CR 3) respectively VS\_LOCK\_EN (CR 3) are set, the drivers remain off until the status is cleared. If the VS\_LOCK\_EN or VSREG\_LOCK\_EN bit is set to 0, the drivers will switch on automatically if the error condition disappears. Undervoltage and overvoltage shutdown can be disabled by SPI. In case of open-load condition, the relevant status register will be latched. The status can be read and optionally cleared by SPI. The high and low-side outputs are not switched off in case of open-load condition.

For OUT1, OUT4-8 and OUT\_HS the auto recovery feature (OUTx\_OCR (CR 7)) can be enabled; half-bridges and high-side drivers have different Auto recovery frequencies (frecx\_hs and frecx\_hb). If these bits are set to 1 the driver will automatically restart from an overload condition. This overload recovery feature is intended for loads which have an initial current higher than the overcurrent limit of the output (e.g. Inrush current of cold light bulbs). The SPI bits OUTx\_OCR\_ALERT (SR4) indicate that the output reached auto-recovery condition.

**Note:** *The maximum voltage and current applied to the high-side Outputs is specified in the 'Absolute Maximum Ratings'. Appropriate external protection may be required in order to respect these limits under application conditions. In case of outputs switch off due to loss of ground at SGND pin, the device has to be re-started through a power off on both  $V_S$  and  $V_{SREG}$*

Each of the stand alone high-side driver outputs OUT7 ... OUT15 and OUT\_HS can be driven with an internally generated PWM signal, an internal Timer or with DIR1 respectively DIR2. See [Table 49](#).

Table 49. Power output settings

| OUTx_3 | OUTx_2 | OUTx_1 | OUTx_0 | Description                                                                       |
|--------|--------|--------|--------|-----------------------------------------------------------------------------------|
| 0      | 0      | 0      | 0      | OFF                                                                               |
| 0      | 0      | 0      | 1      | ON                                                                                |
| 0      | 0      | 1      | 0      | Timer1 output is controlled by timer1; starting with ON phase after timer restart |
| 0      | 0      | 1      | 1      | Timer2 output is controlled by timer2; starting with ON phase after timer restart |
| 0      | 1      | 0      | 0      | PWM1                                                                              |
| 0      | 1      | 0      | 1      | PWM2                                                                              |
| 0      | 1      | 1      | 0      | PWM3                                                                              |
| 0      | 1      | 1      | 1      | PWM4                                                                              |
| 1      | 0      | 0      | 0      | PWM5                                                                              |
| 1      | 0      | 0      | 1      | PWM6                                                                              |
| 1      | 0      | 1      | 0      | PWM7                                                                              |
| 1      | 0      | 1      | 1      | PWM8                                                                              |
| 1      | 1      | 0      | 0      | PWM9                                                                              |
| 1      | 1      | 0      | 1      | PWM10                                                                             |
| 1      | 1      | 1      | 0      | DIR1                                                                              |
| 1      | 1      | 1      | 1      | DIR2                                                                              |

#### 4.14 Auto-recovery alert and thermal expiration

The thermal expiration feature provides a robust protection against possible microcontroller malfunction, switching off a given channel if continuously driven in auto-recovery. If the temperature of the related cluster increases by more than 30 °C after reaching the auto-recovery time  $t_{AR}$ , the channel is switched off. The thermal expiration status bit OUTx\_TH\_EX (SR 3) is set.

During auto-recovery condition, OUTx\_OCR\_ALERT (SR 4) is set. The Alert bit indicates that an overload condition (load in-rush, short-circuit, etc) is present.

The thermal expiration feature is controlled by SPI (OUTx\_OCR\_THX\_EN (CR 8).

**Figure 32. Example of long auto-recovery on OUT7. Temperature acquisition starts after  $t_{AR}$ , thermal expiration occurs after a  $\Delta T = 30^\circ$**

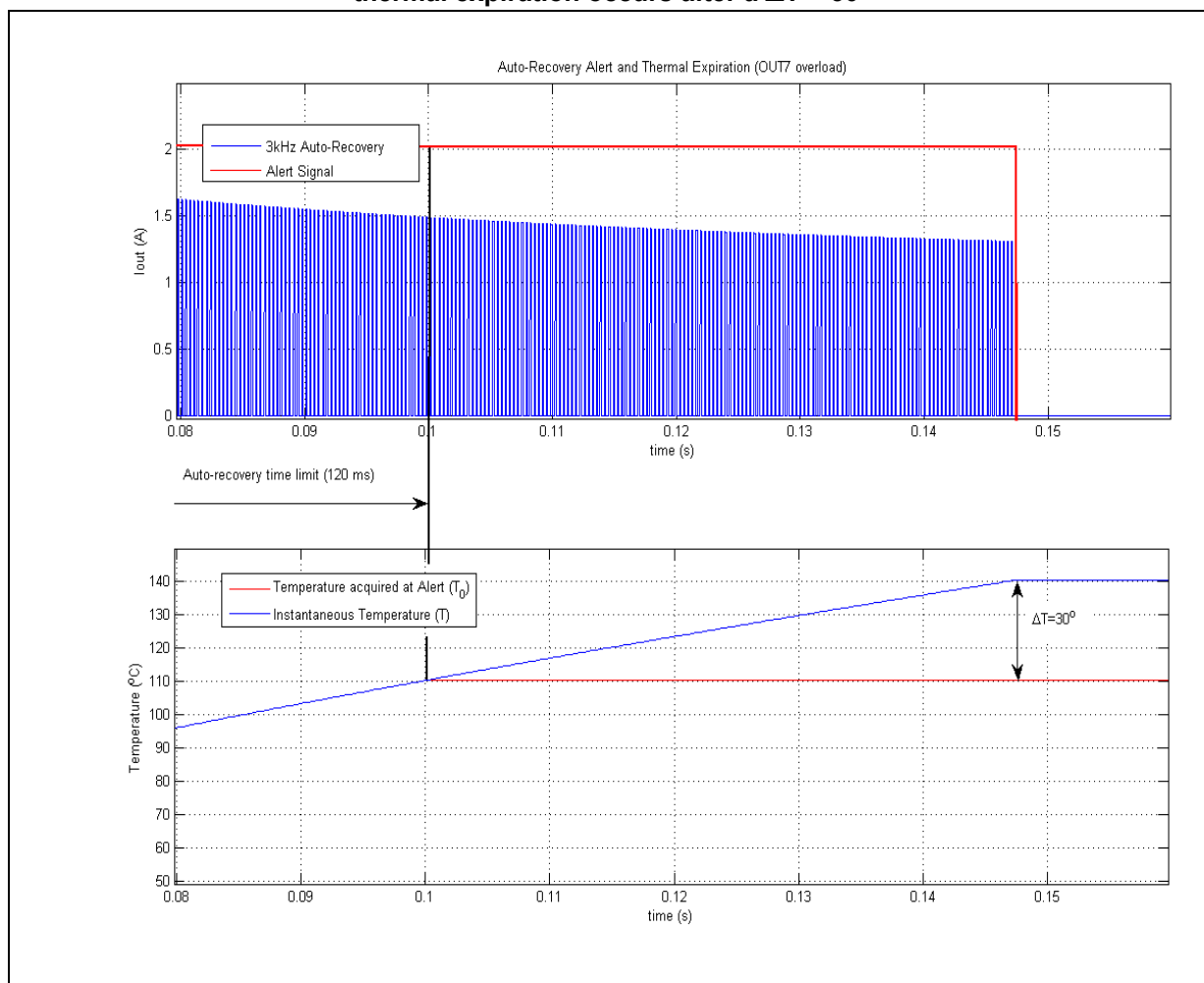
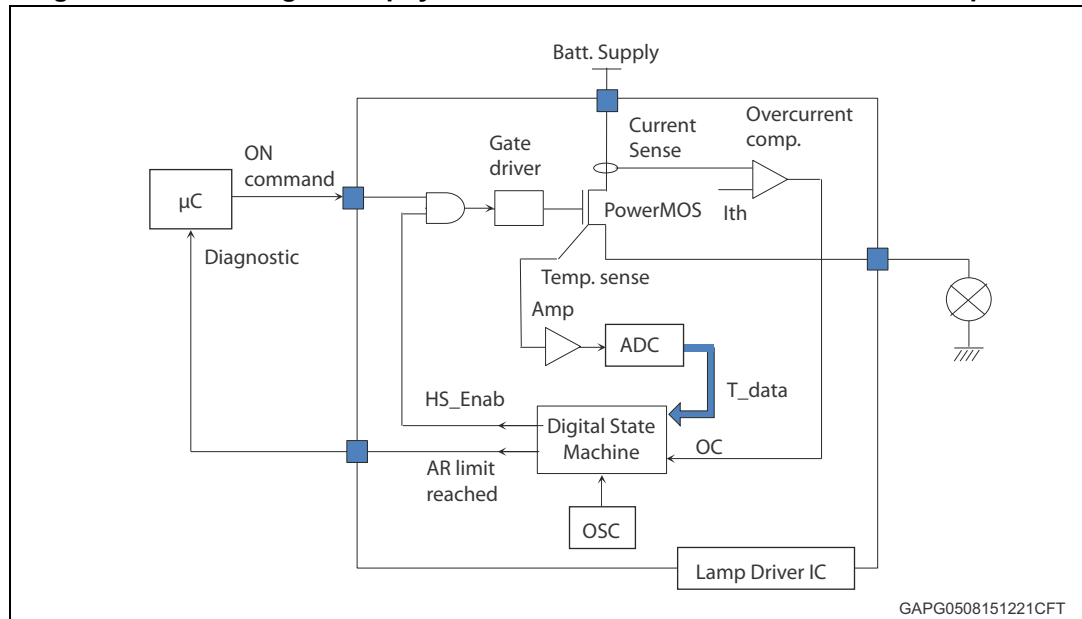


Figure 33. Block diagram of physical realization of AR alert and thermal expiration

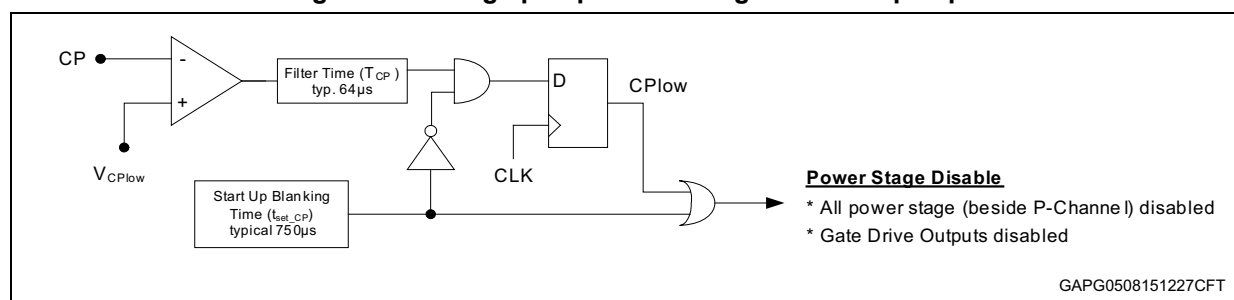


## 4.15 Charge pump

The charge pump uses two external capacitors, which are switched with  $f_{CP}$ . The output of the charge pump has a current limitation. In standby mode and after a thermal shutdown has been triggered the charge pump is disabled. If the charge pump output voltage remains too low for longer than  $T_{CP}$ , the power-MOS outputs and the EC-control are switched off. The H-bridge MOSFET gate drivers are switched to resistive low and CP\_LOW (SR 2) is set. This bit has to be cleared to reactivate the drivers. If the bit CP\_LOW\_CONFIG (Configuration Register 0x3F) is set to '1', CP\_LOW (SR2) behaves as a 'live' bit and the outputs are re-activated automatically upon recovery of the charge pump output voltage.

In case of reaching the overvoltage shutdown threshold  $V_{SOV}$  the charge pump is disabled and automatically restarted after  $V_S$  recovered to normal operating voltage.

Figure 34. Charge pump low filtering and start up implementation



## 4.16 Inductive loads

Each of the half bridges is built by internally connected high-side and low-side power DMOS transistors. Due to the built-in reverse diodes of the output transistors, inductive loads can

be driven at the outputs OUT1 and OUT4-6 without external freewheeling diodes. The high-side drivers OUT7 to OUT15 and OUT\_HS are intended to drive resistive loads only. Therefore only a limited energy ( $E < 1 \text{ mJ}$ ) can be dissipated by the internal ESD-diodes in freewheeling condition. For inductive loads ( $L > 100 \text{ }\mu\text{H}$ ) an external freewheeling diode connected between GND and the corresponding output is required.

#### 4.17 Open-load detection

The open-load detection monitors the load current in each activated output stage. If the load current is below the open-load detection threshold for  $t > t_{OL\_OUT}$  the corresponding open-load bit OUTx\_OL (SR 5) is set in the status register.

#### 4.18 Overcurrent detection

An overcurrent condition is detected after a filter time (see [Figure 11](#) and [Figure 12](#)) and is indicated by the status bit OUTx\_OC (SR 3). In case of overcurrent, the corresponding driver switches off to reduce the power dissipation and to protect the integrated circuit. If the outputs are not configured in recovery mode, the microcontroller has to clear the relevant status bits to reactivate the corresponding drivers.

#### 4.19 Current monitor

The current monitor sources a current image of the power stage output current at the current monitor pin CM, which has a fixed ratio ( $I_{CMr}$ ) of the instantaneous current of the selected high-side driver. The signal at output CM is blanked for  $t_{cmb}$  after switching on the driver until the correct settlement of the circuitry. The bits CM\_SELx (CR 7) define which of the outputs is multiplexed to the current monitor output CM. The current monitor output allows a more precise analysis of the actual state of the load rather than the detection of an open-load or overload condition. For example, it can be used to detect the motor state (starting, free running, stalled). The current monitor output is enabled after the current-monitor blanking time, when the selected output is switched on. If this output is off, the current monitor output is in high impedance mode. The current monitor can be deactivated by CM\_EN (CR 7).

#### 4.20 PWM mode of the power outputs

Description see [Section 7.3: Status register overview](#).

#### 4.21 Cross-current protection

The four half-bridges of the device are cross-current protected by an internal delay time. If one driver (LS or HS) is turned off, the activation of the other driver of the same half-bridge will be automatically delayed by the crosscurrent protection time. After the crosscurrent protection time is expired the slew-rate limited switch-off phase of the driver is changed to a fast turn-off phase and the opposite driver is turned-on with slew-rate limitation. Due to this behavior, it is always guaranteed that the previously activated driver is completely turned off before the opposite driver starts to conduct.

## 4.22 Programmable soft-start function to drive loads with higher inrush current

Loads with start-up currents higher than the overcurrent limits (e.g. inrush current of lamps, start current of motors) can be driven by using the programmable soft-start function (i.e. overcurrent recovery mode). Each driver has a corresponding overcurrent recovery bit `OUTx_OCR` (CR 7). If this bit is set, the device automatically switches the outputs on again after a programmable recovery time. The PWM modulated current will provide sufficient average current to power up the load (e.g. heat up the bulb) until the load reaches operating condition.

The PWM frequency is defined by setting `OCR_FREQ` (CR7).

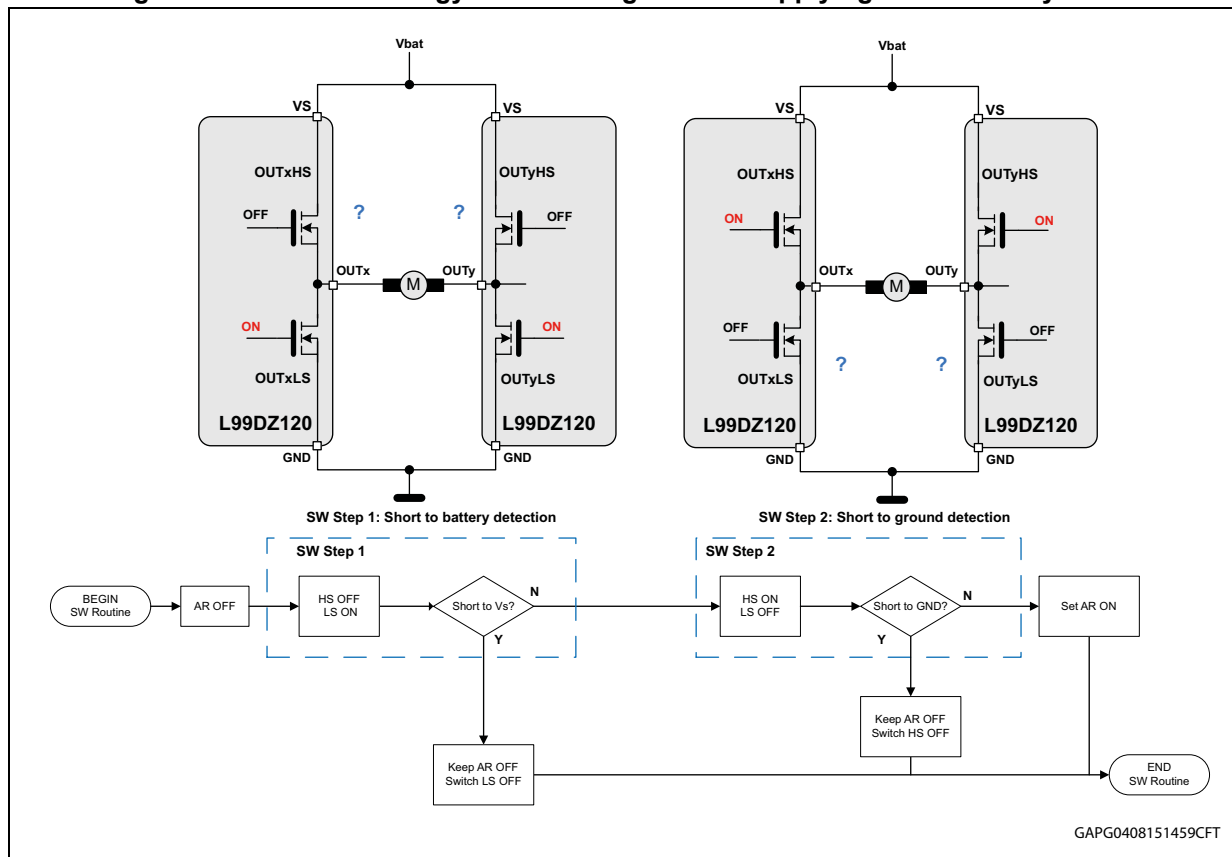
The device itself cannot distinguish between a real overload (e.g. short-circuit condition) and a load characterized by operation currents exceeding the short-circuit threshold.

Examples are non-linear loads like a light bulb used on the HS outputs or a motor used on the half bridge output with inrush and stall currents that shall be limited by the auto recovery feature.

For the bulb, a real overload condition can only be qualified by time. For overload detection the microcontroller can switch on the light bulbs by setting the overcurrent recovery bit for the first e.g. 50 ms. After clearing the recovery bit, the output will be switched off automatically if the overload condition remains.

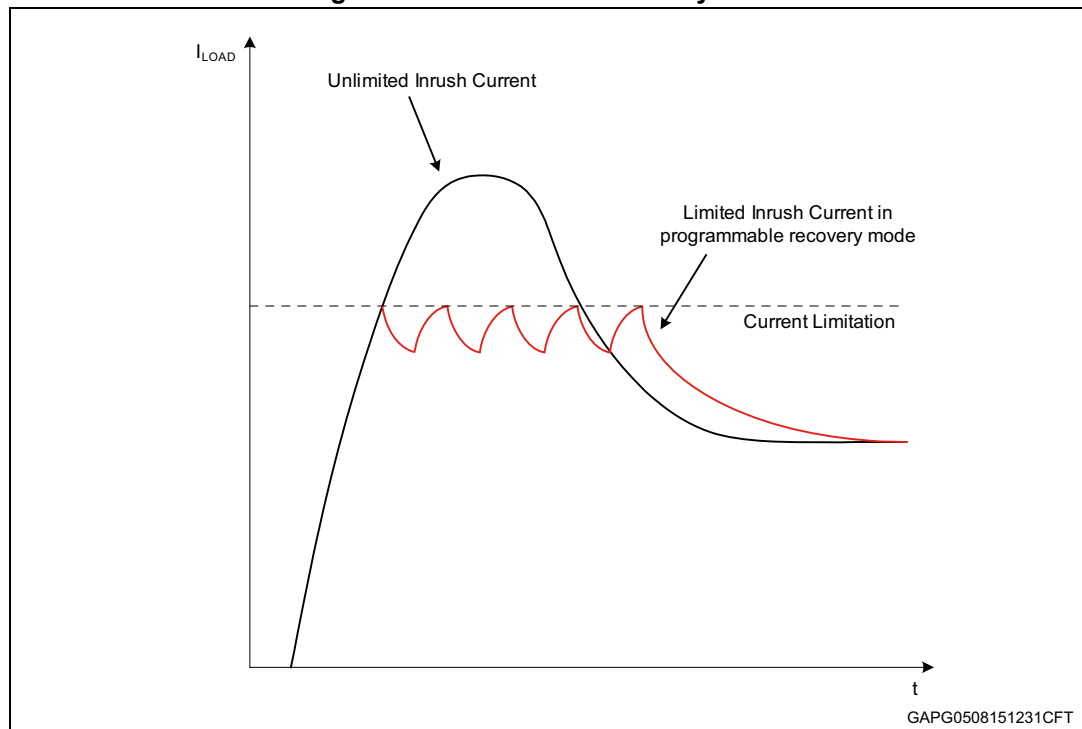
For the half bridges the high current can be present during all motor activation and another SW strategy must be applied to identify a SC to GND or Supply. Before running the motor e.g. with a first SPI command all bridges LS are switched on (without auto recovery functionality / cleared overcurrent recovery bit), all HS are switched off and a SC to Battery can be diagnosed. With a next SPI command, all HS are switched on (without auto recovery functionality/ cleared overcurrent recovery bit) and all LS are switched off. In this sequence, a short to GND can be diagnosed. If in both sequences no overload condition is identified, the motor can be run by switching on the relevant HS and LS each configured in auto recovery mode (see [Figure 35](#)). Such sequence can be applied before any motor activation to identify SC just before operating the motor (in case the delay due to the 2 additional SPI commands is not limiting the application) or in case of power up of the system resp. applied on a certain time base.

Figure 35. Software strategy for half bridges before applying auto-recovery mode



As soon as an output reaches auto-recovery condition, OUTx\_OCR\_ALERT (SR 4)) is set. The Alert bit indicates that an overload condition (load in-rush, short-circuit, etc) is present.

Figure 36. Overcurrent recovery mode



## 4.23 H-bridge control

The PWMH and DIRH inputs control the drivers of the external H-bridge transistors. In single Motor mode the motor direction can be chosen with the direction input (DIRH), the duty cycle<sup>(a)</sup> and frequency with the PWMH input (single mode). With the SPI bits SD (CR 10) and SDS (CR 10) four different slow-decay modes (via drivers and via diode) can be selected using the high-side or the low-side transistors. Unconnected inputs are defined by internal pull-down current.

a. If tcpc is programmed to 4  $\mu$ s and frequency to 50 kHz, max duty cycle achievable is 92%.

Table 50. H-bridge control truth table

| Nb | Control pins |      | Control bits |    |     | Failure bits |       |       |    |      | Output pins      |                  |                  |                  | Motor config | Comment                        |
|----|--------------|------|--------------|----|-----|--------------|-------|-------|----|------|------------------|------------------|------------------|------------------|--------------|--------------------------------|
|    | DIRH         | PWMH | HEN          | SD | SDS | CP_LOW       | VS_OV | VS_UV | DS | TSD1 | GH1              | GL1              | GH2              | GL2              |              |                                |
| 1  | x            | x    | 0            | x  | x   | x            | x     | x     | x  | x    | RL               | RL               | RL               | RL               |              | H-bridge disabled              |
| 2  | x            | x    | 1            | x  | x   | 1            | 0     | 0     | 0  | 0    | RL               | RL               | RL               | RL               | Single       | Charge pump voltage too low    |
| 3  | x            | x    | 1            | x  | x   | 0            | x     | x     | x  | 1    | RL               | RL               | RL               | RL               |              | Thermal shutdown               |
| 4  | x            | x    | 1            | x  | x   | 0            | 1     | 0     | 0  | 0    | L                | L                | L                | L                |              | Overvoltage                    |
| 5  | x            | x    | 1            | x  | x   | 0            | 0     | 0     | 1  | 0    | L <sup>(1)</sup> | L <sup>(1)</sup> | L <sup>(1)</sup> | L <sup>(1)</sup> |              | Short-circuit <sup>(1)</sup>   |
| 6  | 0            | 1    | 1            | x  | x   | 0            | 0     | 0     | 0  | 0    | L                | H                | H                | L                |              | Bridge H2/L1 on                |
| 7  | x            | 0    | 1            | 0  | 0   | 0            | 0     | 0     | 0  | 0    | L                | H                | L                | H                |              | Slow-decay mode LS1 and LS2 on |
| 8  | 0            | 0    | 1            | 0  | 1   | 0            | 0     | 0     | 0  | 0    | L                | H                | L                | L                |              | Slow-decay mode LS1 on         |
| 9  | 1            | 0    | 1            | 0  | 1   | 0            | 0     | 0     | 0  | 0    | L                | L                | L                | H                |              | Slow-decay mode LS2 on         |
| 10 | 1            | 1    | 1            | x  | x   | 0            | 0     | 0     | 0  | 0    | H                | L                | L                | H                |              | Bridge H1/L2 on                |
| 11 | x            | 0    | 1            | 1  | 0   | 0            | 0     | 0     | 0  | 0    | H                | L                | H                | L                |              | Slow-decay mode HS1 and HS2 on |
| 12 | 0            | 0    | 1            | 1  | 1   | 0            | 0     | 0     | 0  | 0    | L                | L                | H                | L                |              | Slow-decay mode HS1 on         |
| 13 | 1            | 0    | 1            | 1  | 1   | 0            | 0     | 0     | 0  | 0    | H                | L                | L                | L                |              | Slow-decay mode HS2 on         |

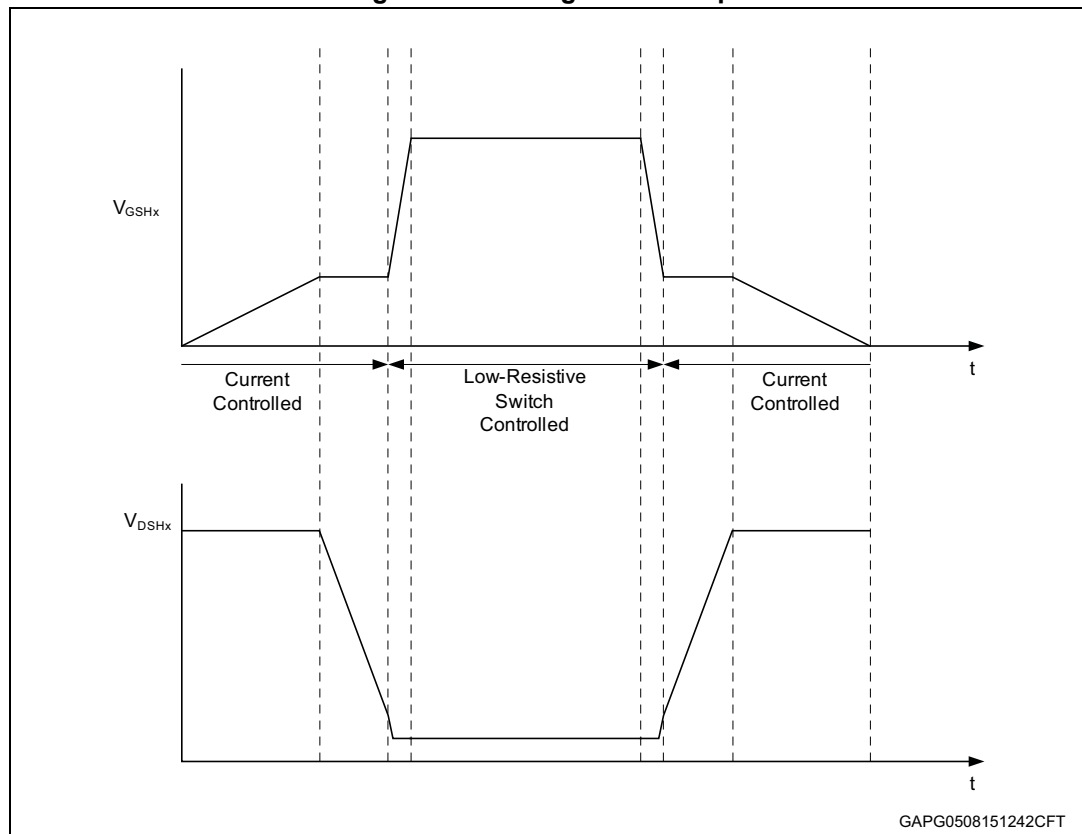
1. Only the H-bridge leg (low-side and high-side), in which one MOSFET is in short-circuit condition is switched off. Both MOSFETs of the other H-bridge leg remain active and driven by DIRH and PWMH.

During watchdog long-open window, the H-bridge drivers are forced off until the first valid watchdog trigger in window mode (setting TRIG = 0 during safe window). The Control Registers remain accessible during long open window.

## 4.24 H-bridge driver slew-rate control

The rising and falling slope of the drivers for the external high-side Power-MOS can be slew rate controlled. If this mode is enabled the gate of the external high-side Power-MOS is driven by a current source instead of a low-impedance output driver switch as long as the drain-source voltage over this Power-MOS is below the switch threshold. The current is programmed using the bits SLEW\_x<4:0> (CR 10), which represent a binary number. This number is multiplied by the minimum current step. This minimum current step is the maximum source-/sink-current ( $I_{GHx\max}$  /  $I_{GHx\max}$ ) divided by 31. Programming SLEW\_x <4:0> to 0 disables the slew rate control and the output is driven by the low-impedance output driver switch.

Figure 37. H-bridge GSHx slope



## 4.25 Resistive low

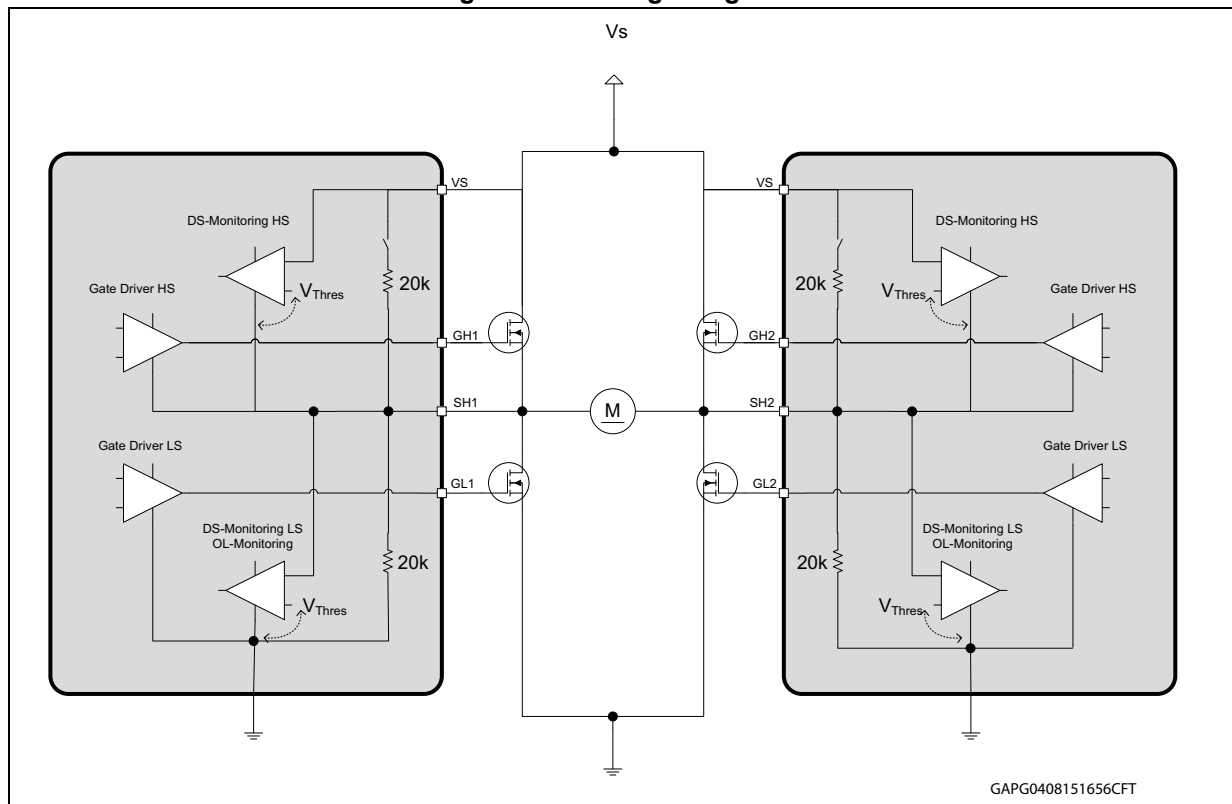
The resistive output mode protects the devices and the H-bridge in the standby mode and in some failure modes (thermal shutdown TSD1 (SR 1), charge pump low CP\_LOW (SR 2) and DI pin stuck at '1' SPI\_INV\_CMD (SR 2)). When a gate driver changes into the resistive output mode due to a failure a sequence is started. In this sequence the concerning driver is switched into sink condition for 32  $\mu$ s to 64  $\mu$ s to ensure a fast switch-off of the H-bridge transistor. If slew rate control is enabled, the sink condition is slew-rate controlled. Afterwards the driver is switched into the resistive output mode (resistive path to source).

## 4.26 Short circuit detection / drain source monitoring

The Drain - Source voltage of each activated external MOSFET of the H-bridge is monitored by comparators to detect shorts to ground or battery. If the voltage-drop over the external MOSFET exceeds the configurable threshold voltage  $V_{SCd\_HB}$  (DIAG\_x (CR 10) for longer  $t > t_{SCd\_HB}$  the corresponding gate driver switches off the external MOSFET and the corresponding drain source monitoring flag DS\_MON\_x (SR 2) is set. The DSMON\_x bits have to be cleared through the SPI to reactivate the gate drivers. This monitoring is only active while the corresponding gate driver is activated. If a drain-source monitor event is detected, the corresponding gate-driver remains activated for at maximum the filter time. When the gate driver switches on, the drain-source comparator requires the specified settling time until the drain-source monitoring is valid. During this time, this drain-source

monitor event may start the filter time. The threshold voltage  $V_{SCd\_HB}$  can be programmed using the SPI bits DIAG\_x (CR 10).

**Figure 38. H-bridge diagnosis**



## 4.27 H-bridge monitoring in off-mode

The drain source voltages of the H-bridge driver external transistors can be monitored, while the transistors are switched off. If either bit OL\_H1L2 (CR 10) or OL\_H2L1 (CR 10) is set to 1, while bit HEN (CR 1) = 1, the H-drivers enter resistive low mode and the drain-source voltages can be monitored. Since the pull-up resistance is equal to the pull-down resistance on both sides of the bridge a voltage of  $2/3 V_S$  on the pull-up highside and  $1/3 V_S$  on the low-side is expected, if they drive a low-resistive inductive load (e.g. motor). If the drain source voltage on each of these Power-MOS is less than  $1/6 V_S$ , the drain-source monitor bit of the associated driver is set.

The open-load filter time is  $t_{OL\_HB}$ .

Figure 39. H-bridge open-load-detection (no open-load detected)

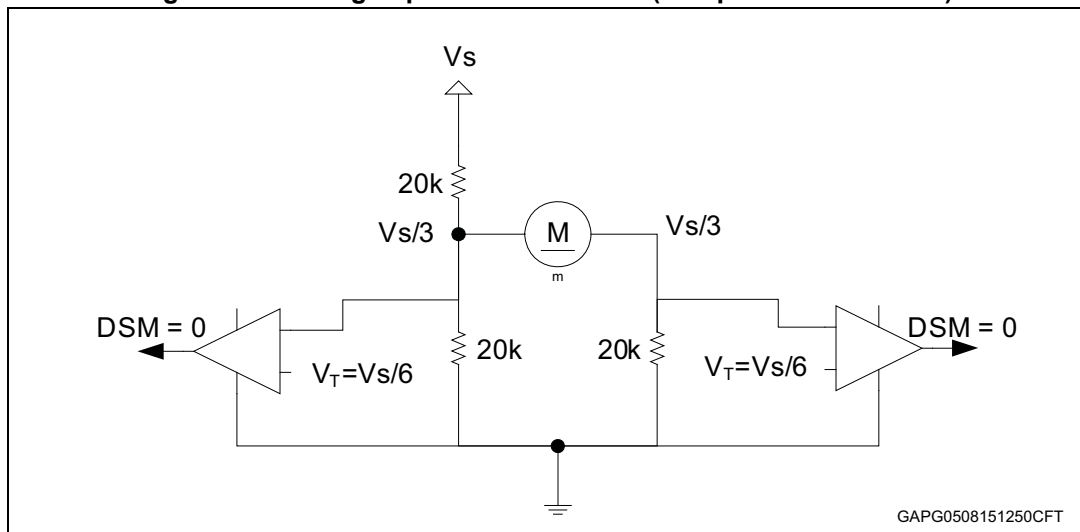


Figure 40. H-bridge open-load-detection (open-load detected)

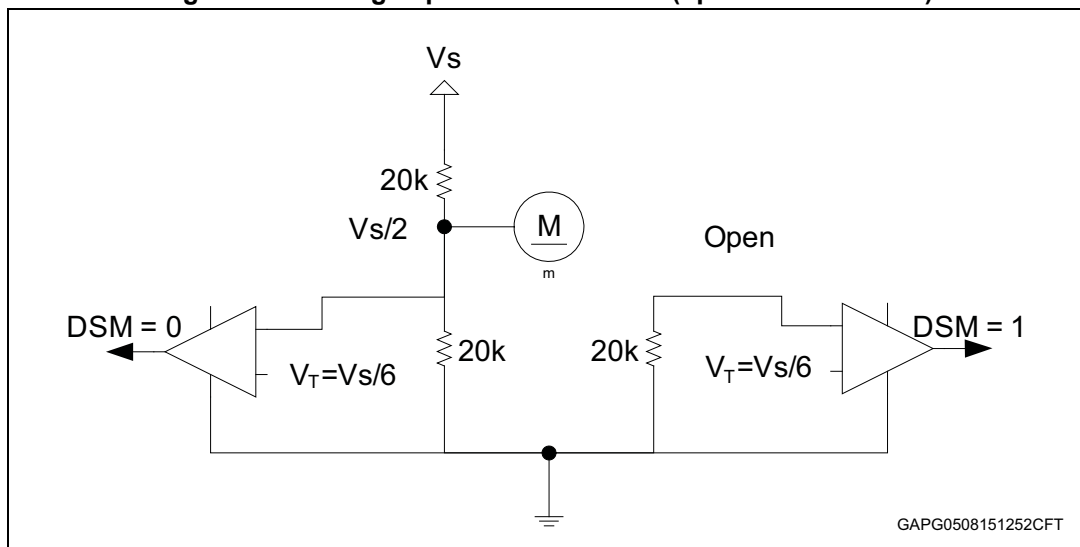


Figure 41. H-bridge open-load-detection (short to ground detected)

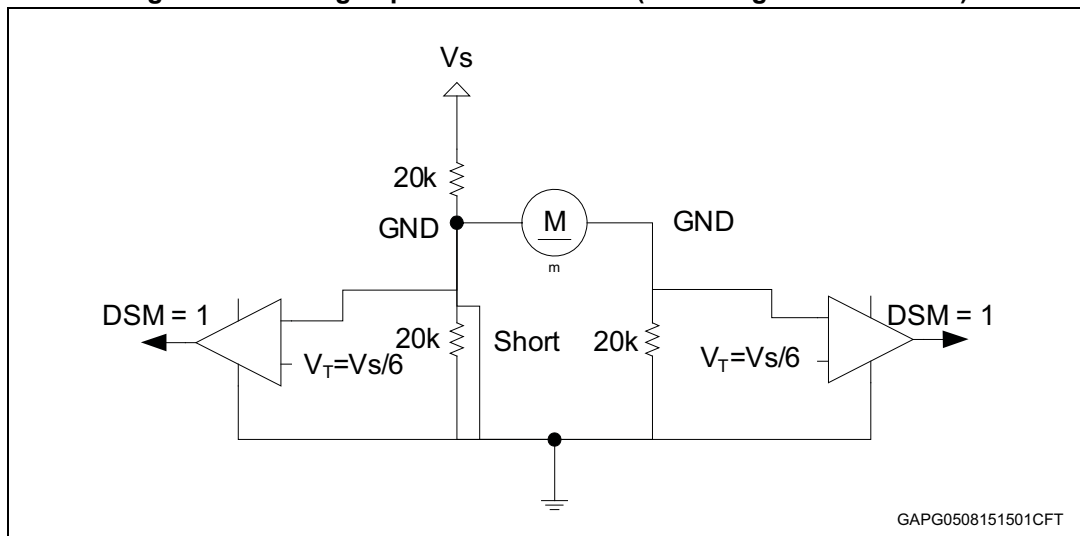
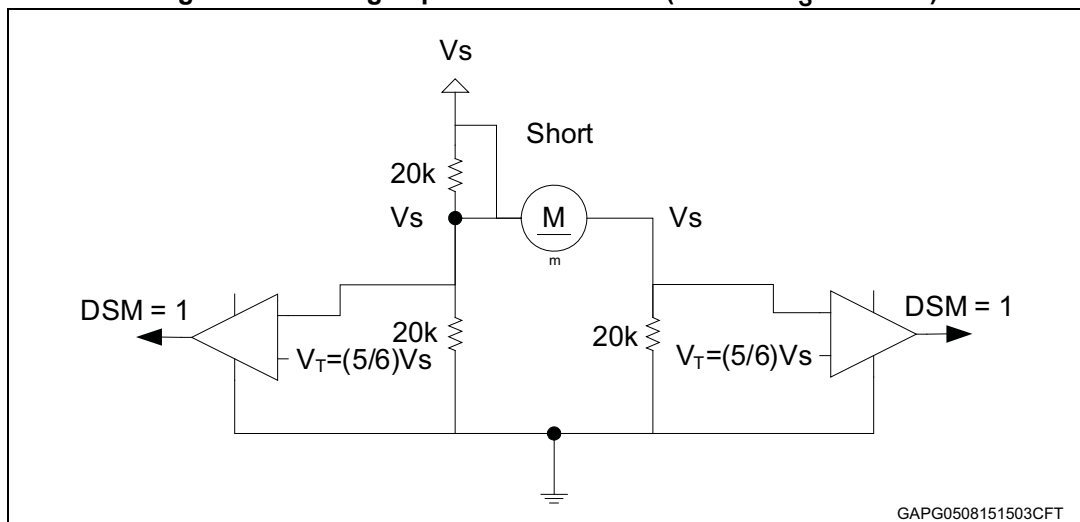
Figure 42. H-bridge open-load detection (short to  $V_S$  detected)

Table 51. H-bridge monitoring in off-mode

| Nb | Control bits |         |             | Failure bits |           | Comments                      |
|----|--------------|---------|-------------|--------------|-----------|-------------------------------|
|    | OL H1L2      | OL H2L1 | H OLTH High | DSMON LS1    | DSMON LS2 |                               |
| 1  | 0            | 0       | 0           | 0            | 0         | Drain-Source monitor disabled |
| 2  | 1            | 0       | x           | 0            | 0         | No open-load detected         |
| 3  | 1            | 0       | 0           | 0            | 1         | Open-load SH2                 |
| 4  | 1            | 0       | 0           | 1            | 1         | Short to GND                  |
| 5  | 1            | 0       | 1           | 1            | 1         | Short to VS                   |
| 6  | 0            | 1       | x           | 0            | 0         | No open-load detected         |
| 7  | 0            | 1       | 0           | 1            | 0         | Open-load SH1                 |

Table 51. H-bridge monitoring in off-mode (continued)

| Nb | Control bits |         |             | Failure bits |           | Comments     |
|----|--------------|---------|-------------|--------------|-----------|--------------|
|    | OL H1L2      | OL H2L1 | H OLTH High | DSMON LS1    | DSMON LS2 |              |
| 8  | 0            | 1       | 0           | 1            | 1         | Short to GND |
| 9  | 0            | 1       | 1           | 1            | 1         | Short to VS  |

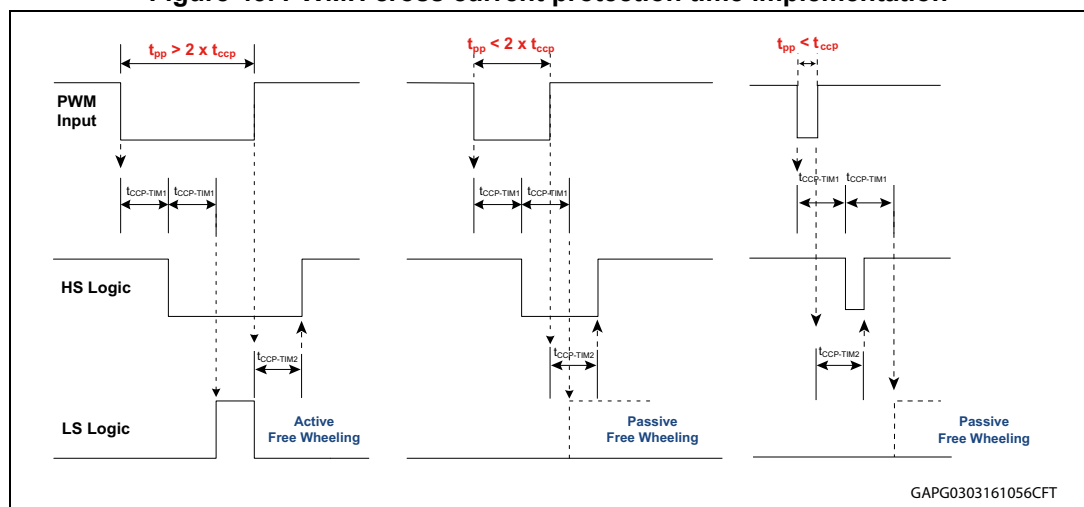
## 4.28 Programmable cross current protection

The external PowerMOSFETs transistors in H-bridge (two half-bridges) configuration are switched on with an additional delay time  $t_{CCP}$  to prevent cross current in the halfbridge. The cross current protection time  $t_{CCP}$  can be programmed with the SPI bits COPT\_x<3:0> (CR 10). The timer is started when the gate driver is switched on in the device.

The PWMH module has 2 timers to configure locking time for high-side and freewheeling low-side. The programmable time  $t_{CCP-TIM1}$  /  $t_{CCP-TIM2}$  is the same. Sequence for switching in PWM mode is the following:

- HS switch off after locking  $t_{CCP-TIM1}$
- LS switch on after 2nd locking  $t_{CCP-TIM1}$
- HS switch on after locking  $t_{CCP-TIM2}$  which starts with rising edge on PWM input

Figure 43. PWMH cross current protection time implementation



## 4.29 Power window H-bridge safety switch off block

The two LS Switches LS1\_FSO and LS2\_FSO are intended to be used to switch off the gates of the external high-side MOSFETs in the power window h-bridge if a fatal error happens. This block must work also in case the MOSFET driver and the according control blocks on the chip are destroyed. Therefore it is necessary to have a complete separated safety block on the device, which has its own supply and GND connection, separated from the other supplies and GNDs. In the block is implemented an own voltage regulator and oscillator.

The safety block is surrounded by a GND isolation ring realized by deep trench isolation. The LS driver must work down to a lower voltage than the other circuits. The block has its own internal supply and an own oscillator for monitoring the failure signals (WWD, V1 fail, SPI fail & Tj) which are Manchester encoded and decoupled by high ohmic resistances. In case of fail-safe event, both LS switches LS1\_FSO and LS2\_FSO are switched on.

In case of entering V1\_standby mode or Vbat\_standby mode both fail safe low-side switches are switched on to minimize the current drawn by the fail safe block (e.g. oscillator is switched off and Manchester Encoding is deactivated). Short circuit protection to  $V_S$  is active in both standby modes limiting the current to  $I_{OLimit}$  for a filter of  $t_{SCF}$ .

After this filter time the fail-safe switches are switched off and LSxFSO\_OC (SR 3) is set. To reactivate the low-side functionality this bit has to be set back by a read and clear command. In case of  $V_S$  loss the fail safe switches are biased by their own output voltage to turn on the low-side switches down to  $V_{OUT\_max}$ .

To allow verification of the Fail-Safe path, the low-side switches LS1\_FSO and LS2\_FSO can be turned on by SPI (Configuration Register 0x3F bit 4: FS\_FORCED)

**Figure 44. LSx\_FSO: low-side driver “passively” turned on, taking supply from output pin (if main supply fails), can guarantee  $V_{LSx\_FSO} < V_{OUT\_max}$**

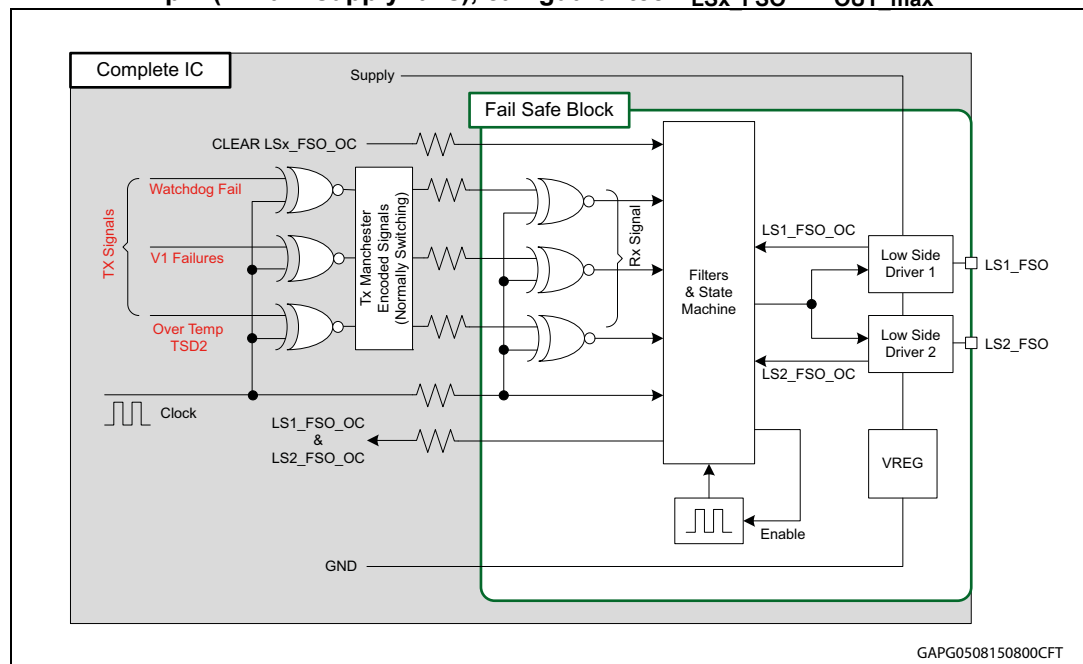
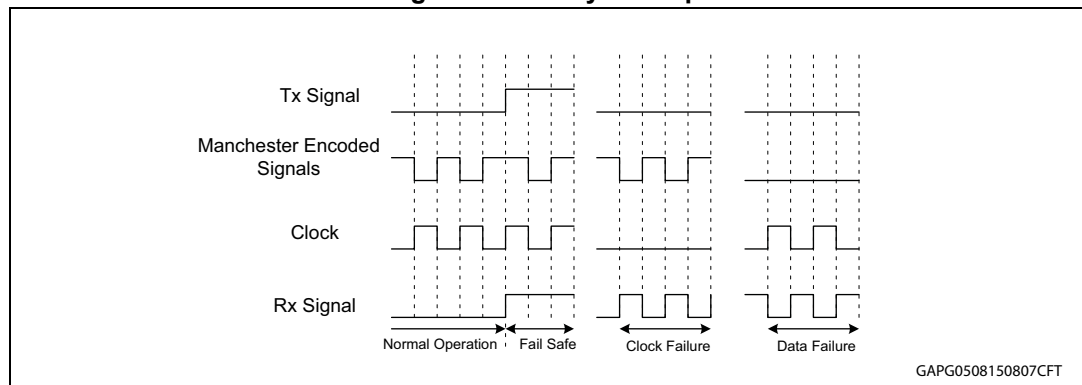


Figure 45. Safety concept



## 4.30 Temperature warning and shutdown

If any of the cluster (see [Section 4.31: Thermal clusters](#)) junction temperatures rises above the temperature warning threshold TW, the temperature warning flag TW (SR 2) is set after the temperature warning filter time  $t_{jft}$  and can be read via SPI. If the junction temperature increases above the temperature shutdown threshold (TSD1), the thermal shutdown bit TSD1 (SR 1) is set and the power transistors of all output stages are switched off to protect the device after the thermal shutdown filter time. The gates of the H-bridge is discharged by the 'Resistive Low' mode. After these bits have been cleared, the output stages are reactivated. If the temperature is still above the thermal warning threshold, the thermal warning bit is set after  $t_{jft}$ . Once this bit is set and the temperature is above the temperature shutdown threshold, temperature shutdown is detected after  $t_{jft}$  and the outputs are switched off. Therefore the minimum time after which the outputs are switched off after the bits have been cleared in case the temperature is still above the thermal shutdown threshold is twice the thermal warning/ thermal shutdown filter time  $t_{jft}$ .

## 4.31 Thermal clusters

In order to provide an advanced on-chip temperature control, the power outputs are grouped in six clusters with dedicated thermal sensors. The sensors are suitably located on the device (see [Figure 46: Thermal clusters identification](#)). In case the temperature of an output cluster reaches the thermal shutdown threshold, the outputs assigned to this cluster are shut down (all other outputs remain active). Each output cluster has a dedicated temperature warning and shutdown flag (SR 6) and the cluster temperature can be read out by SPI.

Hence, the thermal cluster concept allows to identify a group of outputs in which one or more channels are in overload condition.

If thermal shutdown has occurred within an output cluster, or if temperature is rising within a cluster, it may be desired to identify which of the output (s) is (are) determining the temperature increase. An additional evaluation, based on current monitoring and cluster temperature read-out, supports identification of the outputs mainly contributing to the temperature increase. The cluster temperatures are available in SR 7, SR 8 and SR 9 and can be calculated from the binary coded register value using the following formula:

$$\text{Decimal code} = (350 - \text{Temp}) / 0.488$$

T = 25 °C => decimal code is 666 (0x29A)

- Standard mode (default): as soon as any cluster reaches thermal threshold the device is switched off. V1 regulator remains on and is switched off reaching TSD2.
- Cluster mode: only the cluster which reached shutdown temperature is switched off.

*Note: Clusters related to power outputs (clusters 1 to 4, see [Figure 46: Thermal clusters identification](#)) will be managed digitally only, by mean of the ADC conversion of related thermal sensors, while clusters 5 and 6 will be managed in an analog way (comparators) since ADC can be off, e.g. in V1\_standby mode. Temperature reading provided by ADC may differ from real junction temperature of a specific output due to spatial placement of thermal sensor. Such an effect is more visible during fast thermal increases of junction temperature.*

The diagram shows a square chip with 64 pins. The pins are numbered 1 to 64. The functions and thermal cluster assignments are as follows:

| Pin Number | Function   | Thermal Cluster   |
|------------|------------|-------------------|
| 1          | WU1        |                   |
| 2          | CP2M       |                   |
| 3          | CP2P       |                   |
| 4          | CP         |                   |
| 5          | CP1P       |                   |
| 6          | CP1M       |                   |
| 7          | NC         |                   |
| 8          | NC         |                   |
| 9          | OUT14      | Thermal Cluster 4 |
| 10         | OUT13      | Thermal Cluster 4 |
| 11         | OUT12      | Thermal Cluster 4 |
| 12         | OUT9       | Thermal Cluster 4 |
| 13         | OUT10      | Thermal Cluster 4 |
| 14         | OUT11      | Thermal Cluster 4 |
| 15         | LS1_FSO    |                   |
| 16         | LS2_FSO    |                   |
| 17         | VS         |                   |
| 18         | VS         |                   |
| 19         | OUT7       | Thermal Cluster 3 |
| 20         | OUT6       | Thermal Cluster 3 |
| 21         | OUT1       | Thermal Cluster 3 |
| 22         | NC         |                   |
| 23         | OUT5       | Thermal Cluster 2 |
| 24         | OUT5       | Thermal Cluster 2 |
| 25         | VSREG      |                   |
| 26         | OUT_HS     | Thermal Cluster 2 |
| 27         | OUT4       | Thermal Cluster 2 |
| 28         | OUT4       | Thermal Cluster 2 |
| 29         | NC         |                   |
| 30         | VS         |                   |
| 31         | OUT15      | Thermal Cluster 5 |
| 32         | PGND       |                   |
| 33         | GL2        |                   |
| 34         | SH2        |                   |
| 35         | GH2        |                   |
| 36         | GH1        |                   |
| 37         | SH1        |                   |
| 38         | GL1        |                   |
| 39         | 5V_2       | Thermal Cluster 2 |
| 40         | LIN        |                   |
| 41         | Debug      |                   |
| 42         | NC         |                   |
| 43         | NC         |                   |
| 44         | NINT       |                   |
| 45         | NC         |                   |
| 46         | 5V_1       | Thermal Cluster 2 |
| 47         | NRESET     |                   |
| 48         | DIR2       |                   |
| 49         | DIRH       |                   |
| 50         | PWMH       |                   |
| 51         | DIR1       |                   |
| 52         | NC         |                   |
| 53         | LIN FLASH  |                   |
| 54         | RxD_L/NINT |                   |
| 55         | TxD_L      |                   |
| 56         | CSN        |                   |
| 57         | DI         |                   |
| 58         | DO         |                   |
| 59         | CLK        |                   |
| 60         | NC         |                   |
| 61         | CM         |                   |
| 62         | SGND       |                   |
| 63         | NC         |                   |
| 64         | OUT8       | Thermal Cluster 5 |

Legend for Thermal Clusters:

- Thermal Cluster 1: Blue
- Thermal Cluster 2: Red
- Thermal Cluster 3: Green
- Thermal Cluster 4: Purple
- Thermal Cluster 5: Orange
- Thermal Cluster 6: Grey

Table 52. Thermal cluster definition

| Th_CL1                           | Th_CL2                           | Th_CL3                           | Th_CL4                           | Th_CL5                                                  | Th_CL6                                      |
|----------------------------------|----------------------------------|----------------------------------|----------------------------------|---------------------------------------------------------|---------------------------------------------|
| 5 W Driver + OUT15               | Door lock + OUT_HS               | OUT1 + OUT6                      | 10W driver high ohmic channels   | VREG 1<br>VREG 2                                        | Global                                      |
| TW & TSD1 Both digitally managed | TW & TSD1 Both digitally managed | TW & TSD1 Both digitally managed | TW & TSD1 Both digitally managed | TW digitally managed<br>TSD1 & TSD2 Both analog managed | TW digitally managed<br>TSD1 Analog managed |

## 4.32 $V_S$ compensation (duty cycle adjustment) module

All stand-alone HS outputs can be programmed to calculate some internal duty cycle adjustment to adapt the duty cycle to a changing supply voltage at  $V_S$ . This feature is aimed to avoid LED brightness flickering in case of alternating supply voltage. The correction of the duty cycle is based on the following formula:

### Equation 1: Duty cycle correction

$$\text{DutyCycle} = \frac{V_{th} - V_{LED}}{V_{Bat} - V_{LED}} \times DC_{nom}$$

$V_{th}$  = Duty cycle reference voltage: defined as 10 V

$V_{Bat}$  = Reference voltage: defined as voltage at pin VS

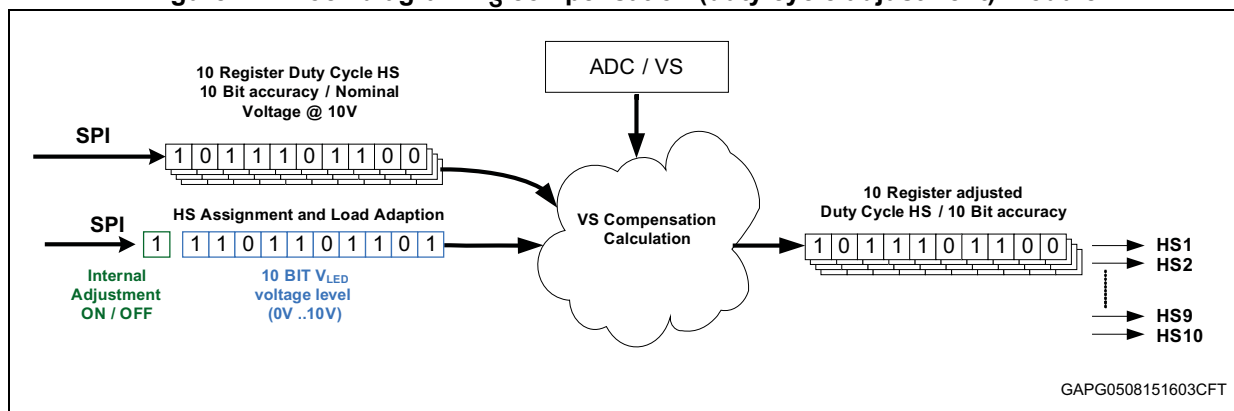
$V_{LED}$  = Voltage drop on the external LED

$DC_{nom}$  = Nominal Duty Cycle programmed by SPI< PWMx DCx>

To be compatible to different LED load characteristics the value for  $V_{LED}$  can be programmed for each output by a dedicated control register OUT7\_VLED ...

OUT\_HS\_VLED (CR 18 to CR 22). Auto compensation features can be activated for all HS outputs each by setting OUTx\_AUTOCOMP\_EN (CR 18 to CR 22).

The programmed LED voltage (OUTx\_V\_LED (CR18 to CR22)) must be lower than  $V_{th}$  (10 V).

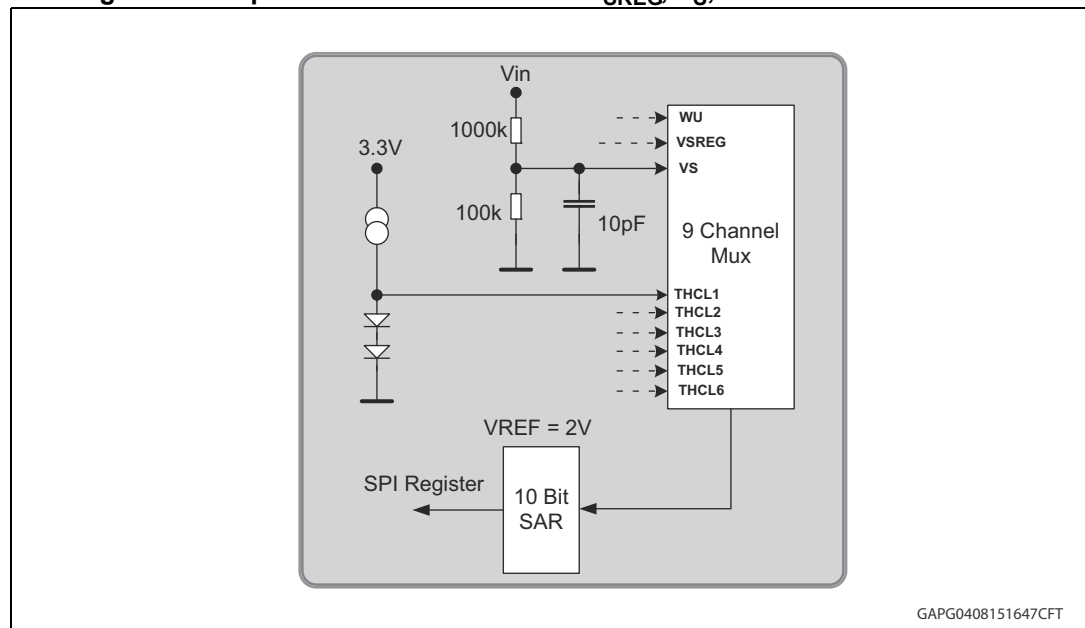
Figure 47. Block diagram  $V_S$  compensation (duty cycle adjustment) module

## Analog digital converter

Voltage signals  $V_S$ ,  $V_{SREG}$ ,  $V_{WU}$  and  $TH\_CL1..6$  are read out sequentially. The voltage signals are multiplexed to an ADC. The ADC is realized as a 10 Bit SAR, that is sampled with the main clock  $f_{clk2} / f_{ADC}$ .

Each channel will be converted with a conversion time  $t_{con}$ , therefore an update of the ADC value is available every  $t_{con} * 9$ . In case of WU is directly connected to Clamp 30, the input must be protected by a series resistance of typical 1k $\Omega$  to sustain reverse battery condition.

**Figure 48. Sequential ADC Read Out for V<sub>SREG</sub>, V<sub>S</sub>, WU and THCL1 ..THCL6**



## 5 Serial Peripheral Interface (SPI)

A 32-bit SPI is used for bi-directional communication with the microcontroller.

The SPI is driven by a microcontroller with its SPI peripheral running in the following mode: CPOL = 0 and CPHA = 0.

For this mode input data is sampled by the low to high transition of the clock CLK, and output data is changed from the high to low transition of CLK. This device is not limited to microcontroller with a built-in SPI. Only three CMOS-compatible output Pins and one input Pin will be needed to communicate with the device. A fault condition can be detected by setting CSN to low. If CSN = 0, the DO-Pin will reflect the global error flag (fault condition) of the device.

- Chip Select Not (CSN)

The input Pin is used to select the serial interface of this device. When CSN is high, the output Pin (DO) is in high impedance state. A low signal activates the output driver and a serial communication can be started. The state during CSN = 0 is called a communication frame. If CSN = low for  $t > t_{CSNfail}$  the DO output will be switched to high impedance in order to not block the signal line for other SPI nodes.

- Serial Data In (DI)

The input Pin is used to transfer data serial into the device. The data applied to the DI will be sampled at the rising edge of the CLK signal and shifted into an internal 32-bit shift register. At the rising edge of the CSN signal the content of the shift register will be transferred to Data Input Register. The writing to the selected Data Input Register is only enabled if exactly 32-bit are transmitted within one communication frame (i.e. CSN low). If more or less clock pulses are counted within one frame the complete frame will be ignored. This safety function is implemented to avoid an activation of the output stages by a wrong communication frame.

*Note: Due to this safety functionality a daisy chaining of SPI is not possible. Instead, a parallel operation of the SPI bus by controlling the CSN signal of the connected IC's is recommended.*

- Serial Data Out (DO)

The data output driver is activated by a logical low level at the CSN input and will go from high impedance to a low or high level depending on the global error flag (fault condition). The first rising edge of the CLK input after a high to low transition of the CSN Pin will transfer the content of the selected status register into the data out shift register. Each subsequent falling edge of the CLK will shift the next bit out.

- Serial Clock (CLK)

The CLK input is used to synchronize the input and output serial bit streams. The data input (DI) is sampled at the rising edge of the CLK and the data output (DO) will change with the falling edge of the CLK signal. The SPI can be driven with a CLK Frequency up to 4 MHz.

### 5.1 ST SPI 4.0

The ST-SPI is a standard used in ST Automotive ASSP devices.

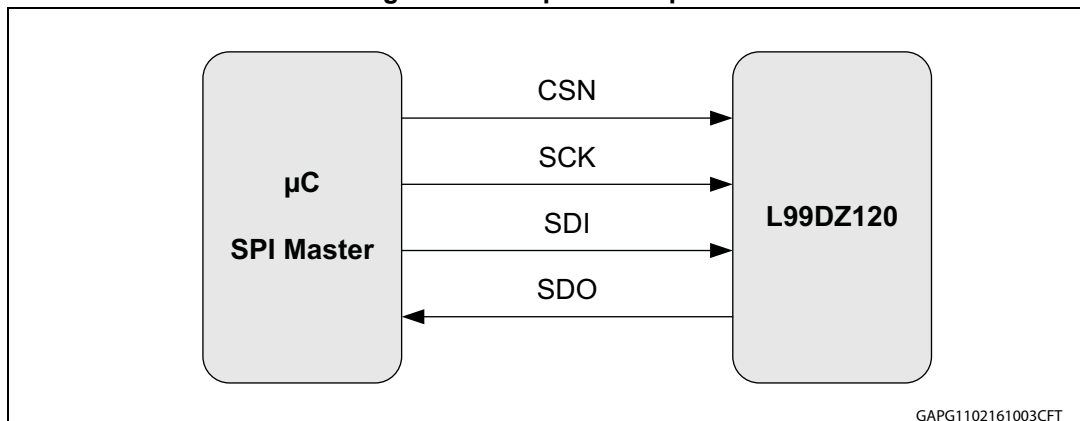
This chapter describes the SPI protocol standardization. It defines a common structure of the communication frames and defines specific addresses for product and status information.

The ST-SPI allows usage of generic software to operate the devices while maintaining the required flexibility to adapt it to the individual functionality of a particular product. In addition, failsafe mechanisms are implemented to protect the communication from external influences and wrong or unwanted usage.

The devices Serial Peripheral Interface are compliant to the ST SPI Standard Rev. 4.0.

### 5.1.1 Physical layer

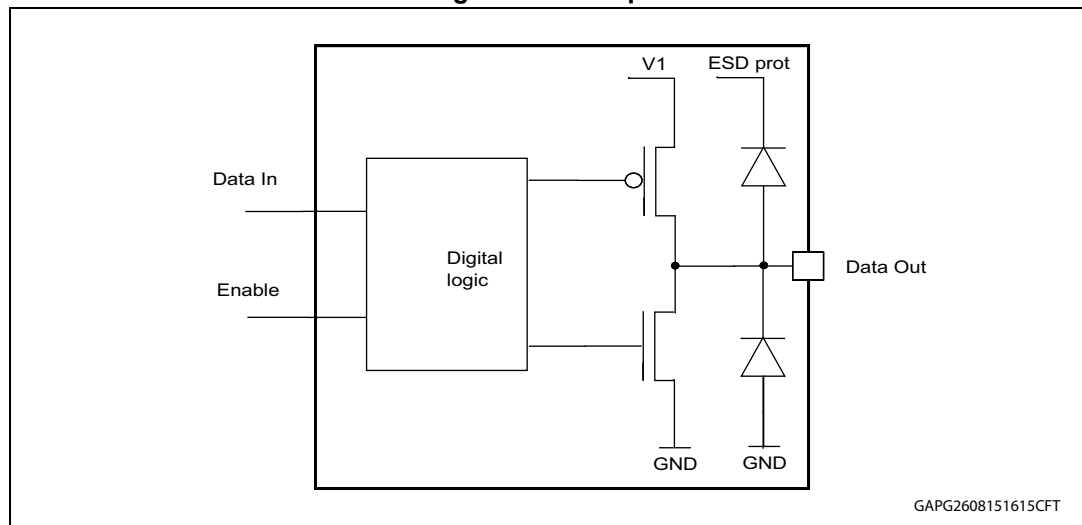
Figure 49. SPI pin description



## 5.2 Signal description

- **Chip Select Not (CSN)**  
The communication interface is de-selected, when this input signal is logically high. A falling edge on CSN enables and starts the communication while a rising edge finishes the communication and the sent command is executed when a valid frame was sent. During communication start and stop the Serial Clock (SCK) has to be logically low. The Serial Data Out (SDO) is in high impedance when CSN is high or a communication timeout was detected.
- **Serial Clock (SCK)**  
This SCK provides the clock of the SPI. Data present at Serial Data Input (SDI) is latched on the rising edge of Serial Clock (SCK) into the internal shift registers while on the falling edge data from the internal shift registers are shifted out to Serial Data Out (SDO).
- **Serial Data Input (SDI)**  
This input is used to transfer data serially into the device. Data is latched on the rising edge of Serial Clock (SCK).
- **Serial Data Output (SDO)**  
This output signal is used to transfer data serially out of the device. Data is shifted out on the falling edge of Serial Clock (SCK).

Figure 50. SDO pin



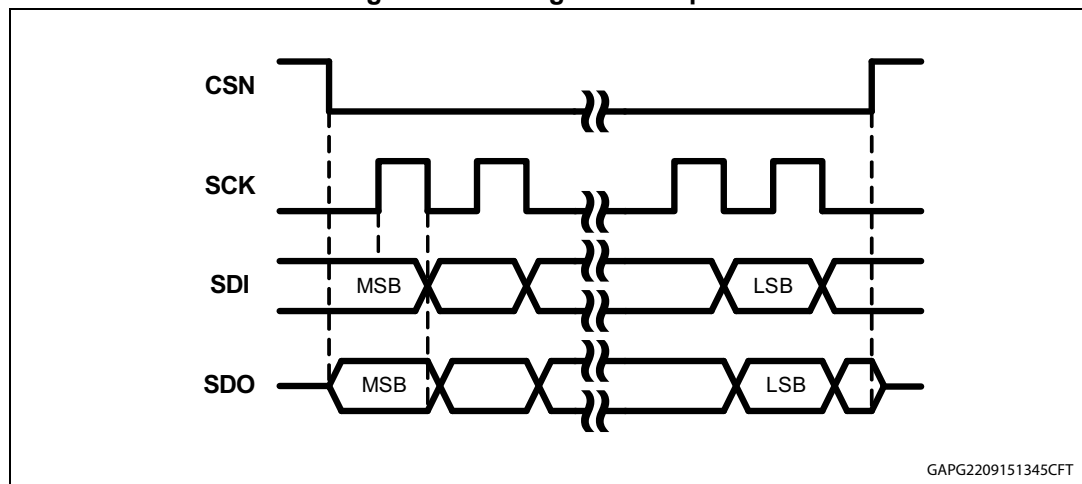
### 5.2.1 Clock and Data Characteristics

The ST-SPI can be driven by a microcontroller with its SPI peripheral running in the following mode:

CPOL = 0

CPHA = 0

Figure 51. SPI signal description



The communication frame starts with the falling edge of the CSN (Communication Start). SCK has to be low.

The SDI data is then latched at all following rising SCK edges into the internal shift registers. After Communication Start the SDO will leave 3-state mode and present the MSB of the data shifted out to SDO. At all following falling SCK edges data is shifted out through the internal shift registers to SDO.

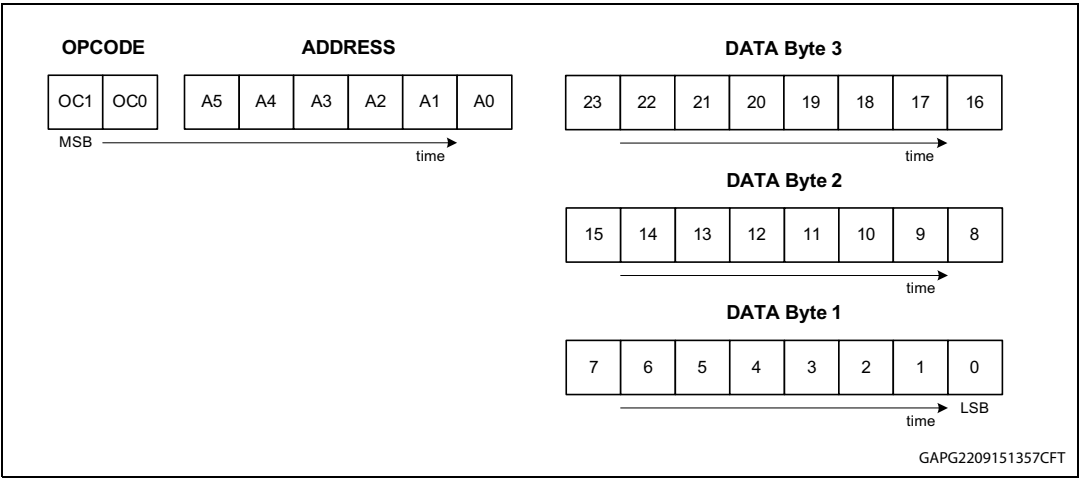
The communication frame is finished with the rising edge of CSN. If a valid communication took place (e.g. correct number of SCK cycles, access to a valid address), the requested operation according to the Operating Code will be performed (Write or Clear operation).

### 5.2.2 Communication protocol

#### SDI Frame

The devices Data-In Frame consist of 32-bit (OpCode (2 bits) + Address (6 bits) + Data Byte 3 + Data Byte 2 + Data Byte 1). The first two transmitted bits (MSB, MSB-1) contain the Operation Code which represents the instruction which will be performed. The following 6 bits (MSB-2 to MSB-7) represent the address on which the operation will be performed. The subsequent bytes contain the payload.

Figure 52. SDI Frame



#### Operating code

The operating code is used to distinguish between different access modes to the registers of the slave device.

Table 53. Operation codes

| OC1 | OC0 | Description             |
|-----|-----|-------------------------|
| 0   | 0   | Write Operation         |
| 0   | 1   | Read Operation          |
| 1   | 0   | Read & Clear Operation  |
| 1   | 1   | Read Device Information |

A Write Operation will lead to a modification of the addressed data by the payload if a write access is allowed (e.g. Control Register, valid data). Beside this a shift out of the content (data present at Communication Start) of the registers is performed.

A Read Operation shifts out the data present in the addressed register at Communication Start. The payload data will be ignored and internal data will not be modified. In addition a Burst Read can be performed.

A Read & Clear Operation will lead to a clear of addressed status bits. The bits to be cleared are defined first by address, second by payload bits set to '1'. Beside this a shift out of the content (data present at Communication Start) of the registers is performed.

*Note: Status registers which change status during communication could be cleared by the actual Read & Clear Operation and are neither reported in actual communication nor in the following communications. To avoid a loss of any reported status it is recommended just clear status registers which are already reported in the previous communication (Selective Bitwise Clear).*

### Advanced operation codes

To provide the separate write of all control registers and the bitwise clear of all status registers, two Advanced Operation Codes can be used to set all control registers to the default value and to clear all status registers. A 'set all control registers to default' command is performed when an OpCode '11' at address b'111111 is performed.

*Note: Please consider that potential device specific write protected registers cannot be cleared with this command in therefore a device Power-on-Reset is needed.*

A 'clear all status registers' command is performed when an OpCode '10' at address b'111111 is performed.

### Data-in payload

The Payload (Data Byte 1 to Data Byte 3) is the data transferred to the devices with every SPI communication. The Payload always follows the OpCode and the Address bits. For Write access the Payload represents the new data written to the addressed register. For Read & Clear operations the Payload defines which bits of the addressed Status Register will be cleared. In case of a '1' at the corresponding bit position the bit will be cleared.

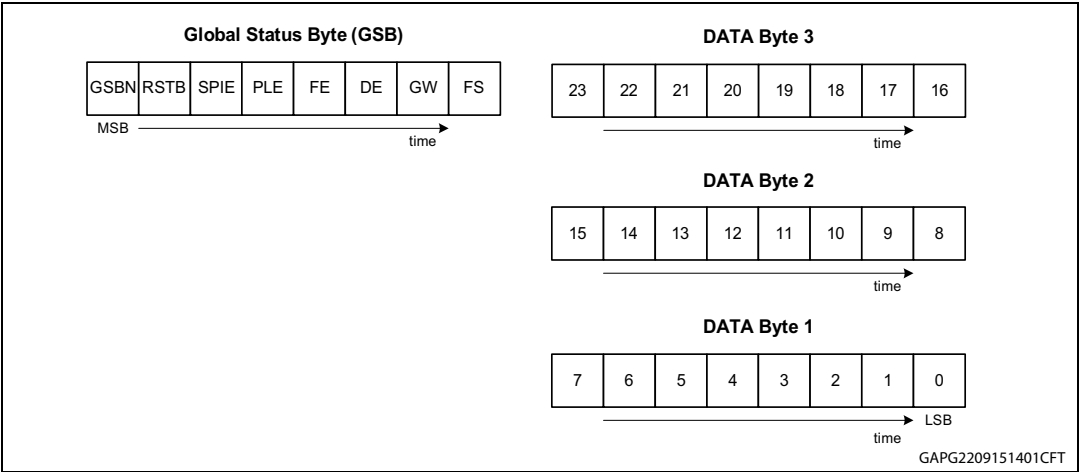
For a Read Operation the Payload is not used. For functional safety reasons it is recommended to set unused Payload to '0'.

### SDO frame

The data-out frame consists of 32-bit (GSB + Data Byte 1 to 3).

The first eight transmitted bits contain device related status information and are latched into the shift register at the time of the Communication Start. These 8-bit are transmitted at every SPI transaction. The subsequent bytes contain the payload data and are latched into the shift register with the eighth positive SCK edge. This could lead to an inconsistency in data between the GSB and Payload due to different shift register load times. Anyhow, no unwanted Status Register clear should appear, as status information should just be cleared with a dedicated bit clear after.

Figure 53. SDO frame



### Global Status Byte (GSB)

The bits (Bit0 to Bit4) represent a logical OR combination of bits located in the Status Registers. Therefore no direct Read & Clear can be performed on these bits inside the GSB.

Table 54. Global Status Byte

| Bit 31 | Bit 30 | Bit 29 | Bit 28 | Bit 27 | Bit 26 | Bit 25 | Bit 24 |
|--------|--------|--------|--------|--------|--------|--------|--------|
| GSBN   | RSTB   | SPIE   | PLE    | FE     | DE     | GW     | FS     |

### Global Status Bit Not (GSBN)

The GSBN is a logical NOR combination of Bit 24 to Bit 30. This bit can also be used as Global Status Flag without starting a complete communication frame as it is present directly after pulling CSN low.

### Reset Bit (RSTB)

The RSTB indicates a device reset. In case this bit is set, specific internal Control Registers are set to default and kept in that state until the bit is cleared. The RSTB bit is cleared after a Read & Clear of all the specific bits in the Status Registers which caused the reset event.

### SPI Error (SPIE)

The SPIE is a logical OR combination of errors related to a wrong SPI communication.

### Physical Layer Error (PLE)

The PLE is a logical OR combination of errors related to the LIN transceiver.

### Functional Error (FE)

The FE is a logical OR combination of errors coming from functional blocks (e.g. high-side overcurrent).

### Device Error (DE)

The DE is a logical OR combination of errors related to device specific blocks (e.g. VS overvoltage, overtemperature).

**Global Warning (GW)**

The GW is a logical OR combination of warning flags (e.g. thermal warning).

**Fail Safe (FS)**

The FS bit indicates that the device was forced into a safe state due to mistreatment or fundamental internal errors (e.g. Watchdog failure, Voltage regulator failure).

**Data-Out Payload**

The Payload (Data Bytes 1 to 3) is the data transferred from the slave device with every SPI communication to the master device. The Payload always follows the OpCode and the address bits of the actual shifted in data (In-frame-Response).

**5.2.3 Address definition****Table 55. Device application access**

| Operating Code |     |
|----------------|-----|
| OC1            | OC0 |
| 0              | 0   |
| 0              | 1   |
| 1              | 0   |

**Table 56. Device information read access**

| Operating Code |     |
|----------------|-----|
| OC1            | OC0 |
| 1              | 1   |

**Table 57. RAM address range**

| RAM Address | Description            | Access |
|-------------|------------------------|--------|
| 3FH         | Configuration Register | R/W    |
|             |                        |        |
| 3CH         | Status Register 12     | R/C    |
| ...         | ...                    |        |
| 32H         | Status Register 2      | R/C    |
| 31H         | Status Register 1      | R/C    |
| ...         | ...                    |        |
| 22H         | Control Register 34    | R/W    |
| 1DH         | Control Register 29    | R/W    |
| ...         | ...                    |        |
| 02H         | Control Register 2     | R/W    |

Table 57. RAM address range (continued)

| RAM Address | Description        | Access |
|-------------|--------------------|--------|
| 01H         | Control Register 1 | R/W    |
| 00H         | reserved           |        |

Table 58. ROM address range

| ROM Address | Description     | Access |
|-------------|-----------------|--------|
| 3FH         | <Advanced Op.>  | W      |
| 3EH         | <GSB Options>   | R      |
| ...         |                 |        |
| 20H         | <SPI CPHA test> | R      |
| 16H         | <WD bit pos. 4> | R      |
| 15H         | <WD bit pos. 3> | R      |
| 14H         | <WD bit pos. 2> | R      |
| 13H         | <WD bit pos. 1> | R      |
| 12H         | <WD Type 2>     | R      |
| 11H         | <WD Type 1>     | R      |
| 10H         | <SPI mode>      | R      |
| ...         |                 |        |
| 0AH         | <Silicon Ver.>  | R      |
| ...         |                 |        |
| 06H         | <Device No.5>   | R      |
| 05H         | <Device No.4>   | R      |
| 04H         | <Device No.3>   | R      |
| 03H         | <Device No.2>   | R      |
| 02H         | <Device No.1>   | R      |
| 01H         | <Device Family> | R      |
| 00H         | <Company Code>  | R      |

### Information registers

The *Device Information Registers* can be read by using OpCode '11'. After shifting out the GSB the 8-bit wide payload will be transmitted. By reading *Device Information Registers* a communication width which is minimum 16-bit plus a multiple by 8 can be used. After shifting out the GSB followed by the 8-bit wide payload a series of '0' is shifted out at the SDO.

Table 59. Information Registers Map

| ROM Address | Description     | Access |   | Bit 7          | Bit 6 | Bit 5 | Bit 4 | Bit 3          | Bit 2 | Bit 1 | Bit 0 |
|-------------|-----------------|--------|---|----------------|-------|-------|-------|----------------|-------|-------|-------|
| 3FH         | <Advanced Op.>  |        |   |                |       |       |       |                |       |       |       |
| 3EH         | <GSB Options>   | R      | → | 0              | 0     | 0     | 0     | 0              | 0     | 0     | 0     |
| ...         |                 |        |   |                |       |       |       |                |       |       |       |
| 20H         | <SPI CPHA test> | R      | → | 0              | 1     | 0     | 1     | 0              | 1     | 0     | 1     |
| 16H         | <WD bit pos. 4> | R      | → | C0H            |       |       |       |                |       |       |       |
| 15H         | <WD bit pos. 3> | R      | → | 7FH            |       |       |       |                |       |       |       |
| 14H         | <WD bit pos. 2> | R      | → | C0H            |       |       |       |                |       |       |       |
| 13H         | <WD bit pos. 1> | R      | → | 41H            |       |       |       |                |       |       |       |
| 12H         | <WD Type 2>     | R      | → | 91H            |       |       |       |                |       |       |       |
| 11H         | <WD Type 1>     | R      | → | 28H            |       |       |       |                |       |       |       |
| 10H         | <SPI mode>      | R      | → | B0H            |       |       |       |                |       |       |       |
| ...         |                 |        | → |                |       |       |       |                |       |       |       |
| 0AH         | <Silicon Ver.>  | R      | → | major revision |       |       |       | minor revision |       |       |       |
| ...         |                 |        | → |                |       |       |       |                |       |       |       |
| 06H         | <Device No.5>   | R      |   | L99DZ120: 01H  |       |       |       |                |       |       |       |
| 05H         | <Device No.4>   | R      | → | 06H            |       |       |       |                |       |       |       |
| 04H         | <Device No.3>   | R      | → | 4DH            |       |       |       |                |       |       |       |
| 03H         | <Device No.2>   | R      | → | 41H            |       |       |       |                |       |       |       |
| 02H         | <Device No.1>   | R      | → | 55H            |       |       |       |                |       |       |       |
| 01H         | <Device Family> | R      | → | 01H            |       |       |       |                |       |       |       |
| 00H         | <Company Code>  | R      | → | 00H            |       |       |       |                |       |       |       |

### Device Identification Registers

These registers represent a unique signature to identify the device and silicon version.

<Company Code>: 00H (STMicroelectronics)

<Device Family>: 01H (BCD Power Management)

<Device No. 1>: 55H

<Device No. 2>: 41H

<Device No. 3>: 4DH

<Device No. 4>: 06H

<Device No. 5>: for L99DZ120: 01H

### SPI modes

By reading out the <SPI mode> register general information of SPI usage of the *Device Application Registers* can be read.

Table 60. SPI Mode Register

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-------|-------|-------|-------|-------|-------|-------|-------|
| BR    | DL2   | DL1   | DL0   | 0     | 0     | S1    | S0    |
| 1     | 0     | 1     | 1     | 0     | 0     | 0     | 0     |

<SPI mode>: B0H (Burst mode read available, 32-bit, no data consistency check)

#### SPI Burst Read

Table 61. Burst Read Bit

| Bit 7 | Description      |
|-------|------------------|
| 0     | BR not available |
| 1     | BR available     |

The SPI Burst Read bit indicates if a burst read operation is implemented. The intention of a Burst Read is e.g. used to perform a device internal memory dump to the SPI Master.

The start of the Burst Read is like a normal Read Operation. The difference is, that after the SPI Data Length the CSN is not pulled high and the SCK will be continuously clocked. When the normal SCK max count is reached (SPI Data Length) the consecutive addressed data will be latched into the shift register. This procedure is performed every time when the SCK payload length is reached.

In case the automatic incremented address is not used by the device, undefined data is shifted out. An automatic address overflow is implemented when address 3FH is reached. The SPI Burst Read is limited by the CSN low timeout.

#### SPI Data Length

The SPI Data Length value indicates the length of the SCK count monitor which is running for all accesses to the Device Application Registers. In case a communication frame with an SCK count is not equal to the reported one it will lead to a SPI Error and the data will be rejected.

Table 62. SPI Data Length

| Bit 6 | Bit 5 | Bit 4 | Description |
|-------|-------|-------|-------------|
| DL2   | DL1   | DL0   |             |
| 0     | 0     | 0     | invalid     |
| 0     | 0     | 1     | 16-bit SPI  |
| 0     | 1     | 0     | 24-bit SPI  |
| 0     | 1     | 1     | 32-bit SPI  |
|       |       |       | ...         |
| 1     | 1     | 1     | 64-bit SPI  |

#### Data Consistency Check (Parity/CRC)

N/A

Table 63. Data Consistency Check

| Bit 1 | Bit 0 | Description |
|-------|-------|-------------|
| S1    | S0    |             |
| 0     | 0     | not used    |
| 0     | 1     | Parity used |
| 1     | 0     | CRC used    |
| 1     | 1     | Invalid     |

### Watchdog Definition

In case a watchdog is implemented the default settings can be read out via the *Device Information Registers*.

Table 64. WD Type/Timing

|               | Bit 7 | Bit 6 | Bit 5                                             | Bit 4 | Bit 3 | Bit 2                       | Bit 1 | Bit 0 |
|---------------|-------|-------|---------------------------------------------------|-------|-------|-----------------------------|-------|-------|
|               | WD1   | WD0   |                                                   |       |       |                             |       |       |
| <WD Type 1/2> | 0     | 0     | Register is not used                              |       |       |                             |       |       |
|               |       |       |                                                   |       |       |                             |       |       |
| <WD Type 1>   | 0     | 1     | WT5                                               | WT4   | WT3   | WT2                         | WT1   | WT0   |
|               |       | 1     | 1                                                 | 0     | 1     | 0                           | 0     | 0     |
|               |       |       | Watchdog Timeout / Long Open Window WT[5:0] * 5ms |       |       |                             |       |       |
|               |       |       |                                                   |       |       |                             |       |       |
| <WD Type 2>   | 1     | 0     | OW2                                               | OW1   | OW0   | CW2                         | CW1   | CW0   |
|               | 1     | 0     | 0                                                 | 1     | 0     | 0                           | 0     | 1     |
|               |       |       | Open Window OW[2:0] * 5ms                         |       |       | Closed Window CW[2:0] * 5ms |       |       |
|               |       |       |                                                   |       |       |                             |       |       |
| <WD Type 1/2> | 1     | 1     | Invalid                                           |       |       |                             |       |       |

<WD Type 1>: 28H (Long Open Window: 200ms)

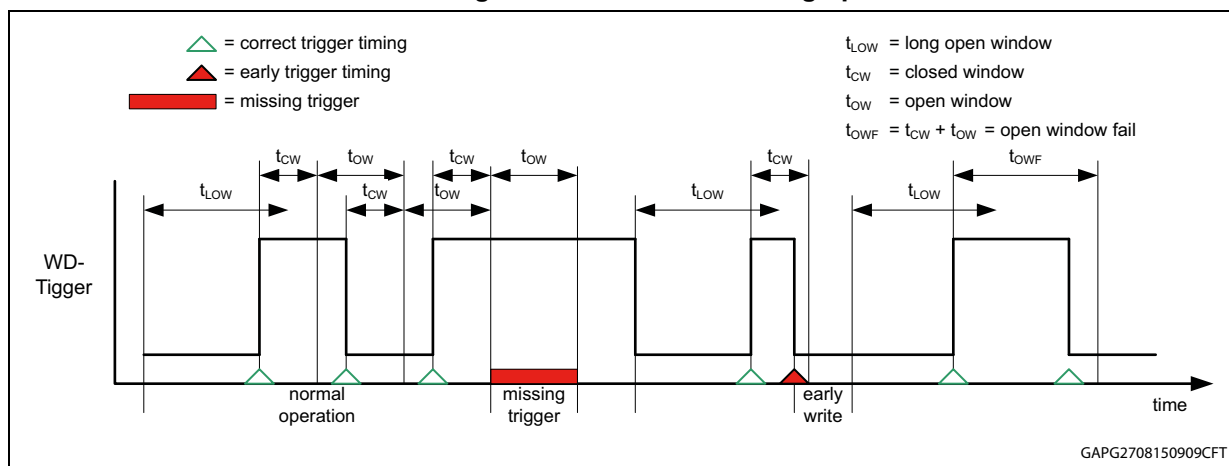
<WD Type 2>: 91H (Open Window: 10ms, Closed Window: 5ms)

<WD Type 1> indicates the Long Open Window (timeout) which is opened at the start of the watchdog. The binary value of WT[5:0] times 5ms indicates the typical value of the Timeout Time.

<WD Type 2> describes the default timing of the window watchdog.

The binary value of CW[2:0] times 5ms defines the typical Closed Window time and OW[2:0] times 5ms defines the typical Open Window time.

Figure 54. Window watchdog operation



The watchdog trigger bit location is defined by the <WD bit pos. X> registers.

Table 65. WD bit position

|                                                                                                                                                | Bit 7 | Bit 6 | Bit 5                | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|------------------------------------------------------------------------------------------------------------------------------------------------|-------|-------|----------------------|-------|-------|-------|-------|-------|
|                                                                                                                                                | WB1   | WB0   |                      |       |       |       |       |       |
| <WD bit pos. X>                                                                                                                                | 0     | 0     | Register is not used |       |       |       |       |       |
| <WD bit pos. X>                                                                                                                                | 0     | 1     | WBA5                 | WBA4  | WBA3  | WBA2  | WBA1  | WBA0  |
| <WD bit pos. 1>                                                                                                                                | 0     | 1     | 0                    | 0     | 0     | 0     | 0     | 1     |
| <WD bit pos. 3>                                                                                                                                | 0     | 1     | 1                    | 1     | 1     | 1     | 1     | 1     |
| Defines the register addresses of the WD trigger bits                                                                                          |       |       |                      |       |       |       |       |       |
| <WD bit pos. X>                                                                                                                                | 1     | 0     | WBA5                 | WBA4  | WBA3  | WBA2  | WBA1  | WBA0  |
| Defines the stop address of the address range (previous <WD bit pos. X> is a WB = '01'). The consecutive <WD bit pos. X> has to be a WB = '11' |       |       |                      |       |       |       |       |       |
| <WD bit pos. X>                                                                                                                                | 1     | 1     | 0                    | WBP 4 | WBP3  | WBP2  | WBP1  | WBP0  |
| <WD bit pos. 2>                                                                                                                                | 1     | 1     | 0                    | 0     | 0     | 0     | 0     | 0     |
| <WD bit pos. 4>                                                                                                                                | 1     | 1     | 0                    | 0     | 0     | 0     | 0     | 0     |
| Defines the binary bit position of the WD trigger bit within the register                                                                      |       |       |                      |       |       |       |       |       |

<WD bit pos 1>: 41H; watchdog trigger bit located at address 01H (CR1)

<WD bit pos 2>: C0H; watchdog trigger bit location is bit0

<WD bit pos 3>: 7FH; watchdog trigger bit located at address 3FH (Config Register)

<WD bit pos 4>: C0H; watchdog trigger bit location is bit0

### Device Application Registers (RAM)

The *Device Application Registers* are all registers accessible using OpCode '00', '01' and '10'. The functions of these registers are defined in the device specification.

## 5.2.4 Protocol failure detection

To realize a protocol which covers certain failsafe requirements a basic set of failure detection mechanisms is implemented.

### Clock monitor

During communication (CSN low to high phase) a clock monitor counts the valid SCK clock edges. If the SCK edges do not correlate with the SPI Data Length an SPIE is reported with the next command and the actual communication is rejected.

By accessing the Device Information Registers (OpCode = '11') the Clock Monitor is set to a minimum of 16 SCK edges plus a multiple by 8 (e.g. 16, 25, 32, ...). Providing no SCK edge during a CSN low to high phase is not recognized as an SPIE. For a SPI Burst Read also the SPI Data Length plus multiple numbers of Payloads SCK edges are assumed as a valid communication.

### SCK Polarity (CPOL) check

To detect the wrong polarity access via SCK the internal Clock monitor is used. Providing first a negative edge on SCK during communication (CSN low to high phase) or a positive edge at last will lead to an SPI Error reported in the next communication and the actual data is rejected.

### SCK Phase (CPHA) check

To verify, that the SCK Phase of the SPI master is set correctly a special Device Information Register is implemented. By reading this register the data must be 55H. In case AAH is read the CPHA setting of the SPI master is wrong and a proper communication cannot be guaranteed.

### CSN timeout

By pulling CSN low the SDO is set active and leaves its 3-state condition. To ensure communication between other SPI devices within the same bus even in case of CSN stuck at low a CSN timeout is implemented. By pulling CSN low an internal timer is started. After timer end is reached the actual communication is rejected and the SDO is set to 3-state condition.

### SDI stuck at GND

As a communication with data all-'0' and OpCode '00' on address b'000000 cannot be distinguished between a valid command and a SDI stuck at GND this communication is not allowed. Nevertheless, in case a stuck at GND is detected the communication will be rejected and the SPIE will be set with the next communication.

### SDI stuck at HIGH

As a communication with data all-'1' and OpCode '11' on address b'111111 cannot be distinguished between a valid command and a SDI stuck at HIGH this communication is not

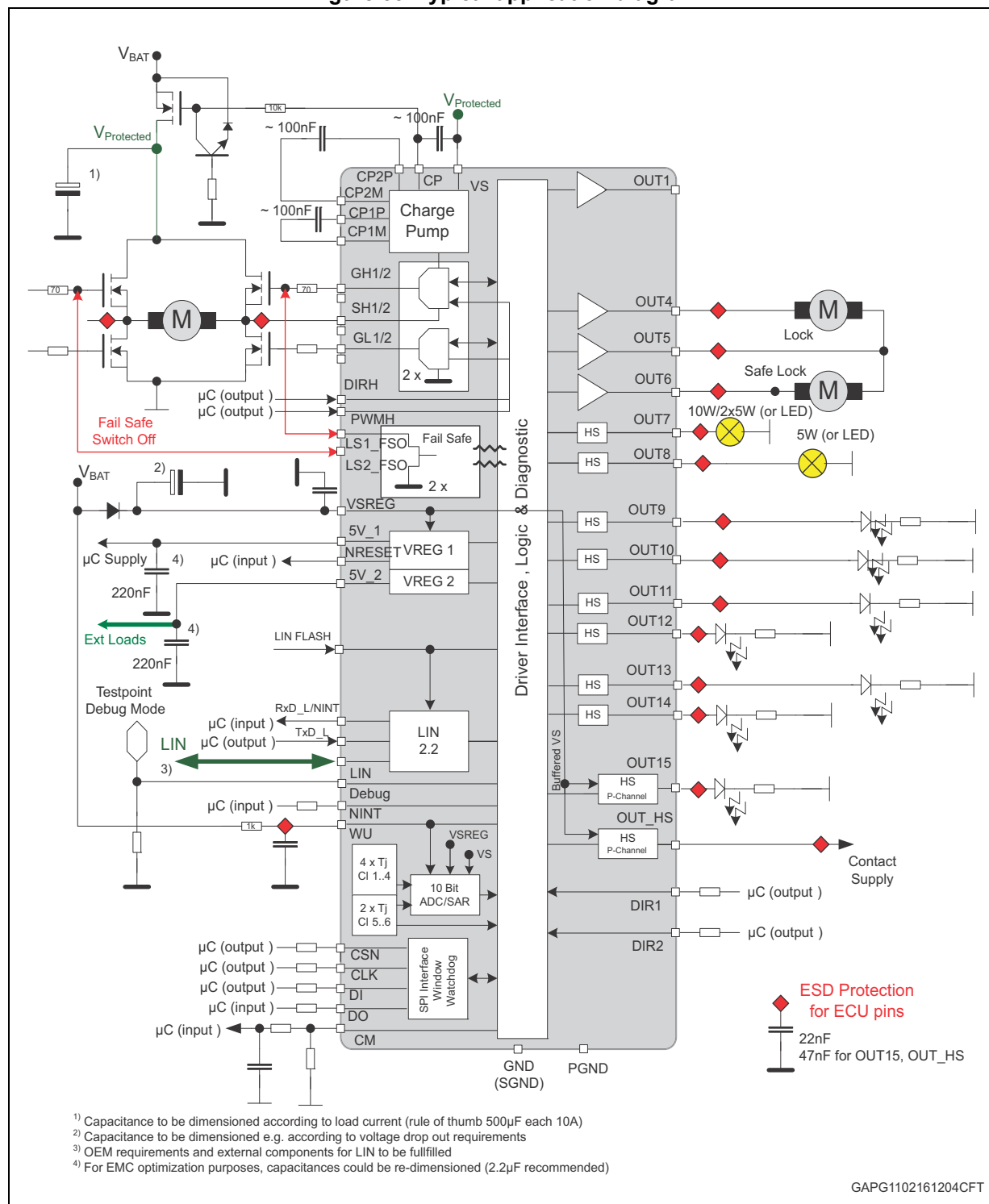
allowed. In case a stuck at HIGH is detected the communication will be rejected and the SPIE will be set with the next communication.

**SDO stuck @**

The SDO stuck at GND and stuck at HIGH have to be detected by the SPI master. As the definition of the GSB guarantees at least one toggle, a GSB with all-'0' or all -'1' reports a stuck at error.

## 6 Application

**Figure 55. Typical application diagram**



## 7 SPI Registers

### 7.1 Global Status Byte GSB

**Table 66. Global Status Byte (GSB)**

|          | 31   | 30   | 29   | 28  | 27 | 26 | 25 | 24 |
|----------|------|------|------|-----|----|----|----|----|
| Bit name | GSBN | RSTB | SPIE | PLE | FE | DE | GW | FS |
| Reset    | 1    | 0    | 0    | 0   | 0  | 0  | 0  | 0  |
| Access   | R    |      |      |     |    |    |    |    |

**Table 67. GSB signals description**

| Bit | Name                | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |
|-----|---------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31  | GSBN                | <p>Global Status Bit Inverted</p> <p>The GSBN is a logically NOR combination of GSB Bits 24 to Bit 30<sup>(1)</sup>.</p> <p>This bit can also be used as Global Status Flag without starting a complete communication frame as it is present at SDO directly after pulling CSN low.</p> <p>0: error detected (1 or several GSB bits from 24 to 30 are set)</p> <p>1: no error detected (default after Power-on)</p> <p>Specific failures may be masked in the Configuration Register 0x3F. A masked failure will still be reported in the GSB by the related failure flag, however it is not reflected in the GSBN (bit 31).</p> |
| 30  | RSTB                | <p>Reset</p> <p>The RSTB indicates a device reset and it is set in case of the following events:</p> <ul style="list-style-type: none"> <li>– VPOR (SR1 - 0x31)</li> <li>– WDFAIL (SR1 - 0x31)</li> <li>– V1UV (SR1 - 0x31)</li> <li>– FORCED_SLEEP_TSD2/V1SC (SR1 - 0x31)</li> </ul> <p>0: no reset signal has been generated (default)</p> <p>1: Reset signal has been generated</p> <p>RSTB is cleared by a <i>Read &amp; Clear</i> command to all bits in <i>Status Register 1</i> causing the Reset event.</p>                                                                                                              |
| 29  | SPIE <sup>(2)</sup> | <p>SPI Error Bit</p> <p>The SPIE indicates errors related to a wrong SPI communication.</p> <ul style="list-style-type: none"> <li>– SPI_INV_CMD (SR2 - 0x32)</li> <li>– SPI_SCK_CNT (SR2 - 0x32)</li> </ul> <p>The bit is also set in case of an SPI CSN Time-out detection</p> <p>0: no error (default)</p> <p>1: error detected</p> <p>SPIE is cleared by a valid SPI command.</p>                                                                                                                                                                                                                                            |

Table 67. GSB signals description (continued)

| Bit | Name               | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |
|-----|--------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 28  | PLE <sup>(2)</sup> | <p>Physical Layer Error</p> <p>The PLE is a logical OR combination of errors related to the LIN transceiver.</p> <ul style="list-style-type: none"> <li>– LIN_PERM_DOM (SR2 - 0x32)</li> <li>– LIN_TXD_DOM (SR2 - 0x32)</li> <li>– LIN_PERM_REC (SR2 - 0x32)</li> </ul> <p>0: no error (default)<br/>1: error detected</p> <p>PLE is cleared by a <i>Read &amp; Clear</i> command to all related bits in <i>Status Registers 2 and 12</i>.</p>                                                                                                                                                                                                                                                                                                                             |
| 27  | FE                 | <p>Functional Error Bit</p> <p>The FE is a logical OR combination of errors coming from functional blocks.</p> <ul style="list-style-type: none"> <li>– V2SC (SR2 - 0x32)</li> <li>– DSMON_HSx (SR2 - 0x32)</li> <li>– DSMON_LSx (SR2 - 0x32)</li> <li>– OUTxHS_OC TH EX (SR3 - 0x33)</li> <li>– OUTxLS_OC TH EX (SR3 - 0x33)</li> <li>– OUTHS_OC TH EX (SR3 - 0x33)</li> <li>– OUTx_OC (SR3 - 0x33)</li> <li>– LSxFS_OC (SR3 - 0x33)</li> <li>– OUTxHS_OL (SR5 - 0x35)<sup>(3)</sup></li> <li>– OUTxLS_OL (SR5 - 0x35)</li> <li>– OUTx_OL (SR5 - 0x35)</li> <li>– OUTHS_OL (SR5 - 0x35)</li> </ul> <p>0: no error (default)<br/>1: error detected</p> <p>FE is cleared by a <i>Read &amp; Clear</i> command to all related bits in <i>Status Registers 2, 3, 4, 5</i></p> |
| 26  | DE                 | <p>Device Error Bit</p> <p>DE is a logical OR combination of global errors related to the device.</p> <ul style="list-style-type: none"> <li>– VS_OV (SR2 - 0x32)</li> <li>– VS_UV (SR2 - 0x32)</li> <li>– VSREG_OV (SR2 - 0x32)</li> <li>– VSREG_UV (SR2 - 0x32)</li> <li>– CP_LOW (SR2 - 0x32)</li> <li>– TSD1_CLx (SR6 - 0x36)</li> </ul> <p>0: no error (default)<br/>1: error detected</p> <p>DE is cleared by a <i>Read &amp; Clear</i> command to all related bits in <i>Status Registers 2 and 6</i></p>                                                                                                                                                                                                                                                           |

Table 67. GSB signals description (continued)

| Bit | Name              | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |
|-----|-------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 25  | GW <sup>(2)</sup> | <p>Global Warning Bit</p> <p>GW is a logical OR combination of warning flags. Warning bits do not lead to any device state change or switch off of functions.</p> <ul style="list-style-type: none"> <li>– VSREG_EW (SR2 - 0x32)</li> <li>– V1_FAIL (SR2 - 0x32)</li> <li>– V2_FAIL (SR2 - 0x32)</li> <li>– TW <sup>(3)</sup> (SR2 - 0x32)</li> <li>– SPI_INV_CMD (SR2 - 0x32)</li> <li>– SPI_SCK_CNT (SR2 - 0x32)</li> </ul> <p>0: no error (default)</p> <p>1: error detected</p> <p>GW is cleared by a <i>Read &amp; Clear</i> command to all related bits in <i>Status Register 2</i>.</p>                                                                                                                                                                                                                                                                                                                                                              |
| 24  | FS                | <p>Fail Safe</p> <p>The FS bit indicates the device was forced into a safe state due to the following failure conditions:</p> <ul style="list-style-type: none"> <li>– WDFAIL (SR1 - 0x31)</li> <li>– V1UV (SR1 - 0x31)</li> <li>– TSD2 (SR1 - 0x31)</li> <li>– FORCED_SLEEP_TSD/V1SC (SR1 - 0x31)</li> </ul> <p>All Control Registers are set to default</p> <p>Control Registers are blocked for WRITE access except the following bits:</p> <ul style="list-style-type: none"> <li>– TRIG (CR1 - 0x01)</li> <li>– V2_0 (CR1 - 0x01)</li> <li>– V2_1 (CR1 - 0x01)</li> <li>– Timer settings (bits 8...23) (CR2 - 0x02)</li> <li>– OUTHS_x (bits 0...3) (CR5 - 0x05)</li> <li>– OUT15_x (bits 0...3) (CR6 - 0x06)</li> <li>– CR12 (0x0C) to CR17 (0x11); PWM frequency and duty cycles</li> </ul> <p>0: Fail Safe inactive (default)</p> <p>1: Fail Safe active</p> <p>FS is cleared upon exit from Fail-Safe mode (refer to chapter 'Fail-Safe mode')</p> |

1. Individual failure flags may be masked in the Configuration Register (0x3F).
2. Bit may be masked in the Configuration Register (0x3F), i.e. the bit will not be included in the Global Status Bit (GSBN).
3. Open-load status flags may be masked in the Configuration register (0x3F), i.e. the open-load flag will be included in the FE flag, but will not set the GSBN. TW failure status flags may be masked in the Configuration register (0x3F), i.e. the TW flag will be included in the GW flag, but will not set the GSBN.

## 7.2 Control register overview

Table 68. Control register overview

|       |      | Bit           |            |                |                |             |             |           |           |                     |               |          |         |         |          |              |              |              |                 |              |              |              |              |              |              |        |        |          |         |      |     |
|-------|------|---------------|------------|----------------|----------------|-------------|-------------|-----------|-----------|---------------------|---------------|----------|---------|---------|----------|--------------|--------------|--------------|-----------------|--------------|--------------|--------------|--------------|--------------|--------------|--------|--------|----------|---------|------|-----|
| Addr. | Reg. | 23            | 22         | 21             | 20             | 19          | 18          | 17        | 16        | 15                  | 14            | 13       | 12      | 11      | 10       | 9            | 8            | 7            | 6               | 5            | 4            | 3            | 2            | 1            | 0            | Access |        |          |         |      |     |
| 0x00  |      | Reserved      |            |                |                |             |             |           |           |                     |               |          |         |         |          |              |              |              |                 |              |              |              |              |              |              |        |        |          |         |      |     |
| 0x01  | CR1  | Reserved      | WU_EN      | Reserved       | WU_PU          | Reserved    | Reserved    | WU_FILT_1 | WU_FILT_0 | TIMER_NINT_WAKE_SEL | TIMER_NINT_EN | Reserved |         |         |          |              |              |              |                 |              |              |              |              | HEN          | V2_1         | V2_0   | PARITY | STBY_SEL | GO_STBY | TRIG | R/W |
| 0x02  | CR2  | T1_RESTART    | T1_DIR     | T1_ON_2        | T1_ON_1        | T1_ON_0     | T1_PER_2    | T1_PER_1  | T1_PER_0  | T2_RESTART          | T2_DIR        | T2_ON_2  | T2_ON_1 | T2_ON_0 | T2_PER_2 | T2_PER_1     | T2_PER_0     | LIN_REC_ONLY | LIN_TXD_TOUT_EN | Reserved     | Reserved     | V1_RESET_1   | V1_RESET_0   | WD_TIME_1    | WD_TIME_0    | R/W    |        |          |         |      |     |
| 0x03  | CR3  | VSREG_LOCK_EN | VS_LOCK_EN | VSREG_OV_SD_EN | VSREG_UV_SD_EN | VS_OV_SD_EN | VS_UV_SD_EN | Reserved  |           |                     |               |          |         |         |          | VSREG_EWTH_9 | VSREG_EWTH_8 | VSREG_EWTH_7 | VSREG_EWTH_6    | VSREG_EWTH_5 | VSREG_EWTH_4 | VSREG_EWTH_3 | VSREG_EWTH_2 | VSREG_EWTH_1 | VSREG_EWTH_0 | R/W    |        |          |         |      |     |
| 0x04  | CR4  | Reserved      | OUT1_HS    | OUT1_LS        | Reserved       |             |             |           |           |                     |               |          |         |         | OUT4_HS  | OUT4_LS      | Reserved     | OUT5_HS      | OUT5_LS         | Reserved     | OUT6_HS      | OUT6_LS      | R/W          |              |              |        |        |          |         |      |     |
| 0x05  | CR5  | OUT7_3        | OUT7_2     | OUT7_1         | OUT7_0         | OUT8_3      | OUT8_2      | OUT8_1    | OUT8_0    | Reserved            |               |          |         | OUT10_3 | OUT10_2  | OUT10_1      | OUT10_0      | Reserved     |                 |              |              | OUTHS_3      | OUTHS_2      | OUTHS_1      | OUTHS_0      | R/W    |        |          |         |      |     |
| 0x06  | CR6  | OUT9_3        | OUT9_2     | OUT9_1         | OUT9_0         | OUT11_3     | OUT11_2     | OUT11_1   | OUT11_0   | OUT12_3             | OUT12_2       | OUT12_1  | OUT12_0 | OUT13_3 | OUT13_2  | OUT13_1      | OUT13_0      | OUT14_3      | OUT14_2         | OUT14_1      | OUT14_0      | OUT15_3      | OUT15_2      | OUT15_1      | OUT15_0      | R/W    |        |          |         |      |     |
| 0x07  | CR7  | OUT1_OCR      | Reserved   | OUT4_OCR       | OUT5_OCR       | OUT6_OCR    | OUT7_OCR    | OUT8_OCR  | OUTHS_OCR | Reserved            |               |          |         |         |          |              | OCR_FREQ     | OUT5_OC1     | OUT5_OC0        | CM_EN        | Reserved     | CM_SEL_3     | CM_SEL_2     | CM_SEL_1     | CM_SEL_0     | R/W    |        |          |         |      |     |

Table 68. Control register overview (continued)

|       |      | Bit             |             |             |             |                 |                 |                 |                 |                 |                  |             |             |             |             |             |             |             |             |              |              |           |           |           |         |        |
|-------|------|-----------------|-------------|-------------|-------------|-----------------|-----------------|-----------------|-----------------|-----------------|------------------|-------------|-------------|-------------|-------------|-------------|-------------|-------------|-------------|--------------|--------------|-----------|-----------|-----------|---------|--------|
| Addr. | Reg. | 23              | 22          | 21          | 20          | 19              | 18              | 17              | 16              | 15              | 14               | 13          | 12          | 11          | 10          | 9           | 8           | 7           | 6           | 5            | 4            | 3         | 2         | 1         | 0       | Access |
| 0x08  | CR8  | OUT1_OCR_THX_EN | Reserved    |             |             | OUT4_OCR_THX_EN | OUT5_OCR_THX_EN | OUT6_OCR_THX_EN | OUT7_OCR_THX_EN | OUT8_OCR_THX_EN | OUTHS_OCR_THX_EN | Reserved    |             |             |             |             |             |             |             |              |              |           |           |           | R/W     |        |
| 0x09  | CR9  | OUT7_RDSON      | OUT8_RDSON  | Reserved    |             |                 |                 |                 |                 | OUTHS_OL        | OUT15_OL         | OUT14_OL    | OUT13_OL    | OUT12_OL    | OUT11_OL    | OUT10_OL    | OUT9_OL     | OUTHS_OC    | OUT15_OC    | OUT14_OC     | OUT13_OC     | OUT12_OC  | OUT11_OC  | OUT10_OC  | OUT9_OC | R/W    |
| 0x0A  | CR10 | DIAG_2          | DIAG_1      | DIAG_0      | Reserved    |                 |                 |                 |                 |                 | SD               |             | SDS         | COPT_3      | COPT_2      | COPT_1      | COPT_0      | H_OLTH_HIGH | OL_H1L2     | OL_H2L1      | SLEW_4       | SLEW_3    | SLEW_2    | SLEW_1    | SLEW_0  | R/W    |
| 0x0B  | CR11 | Reserved        |             |             |             |                 |                 |                 |                 |                 |                  |             |             |             |             |             |             |             |             |              |              |           |           | R/W       |         |        |
| 0x0C  | CR12 | PMW1_FREQ_1     | PMW1_FREQ_0 | PMW2_FREQ_1 | PMW2_FREQ_0 | PMW3_FREQ_1     | PMW3_FREQ_0     | PMW4_FREQ_1     | PMW4_FREQ_0     | PMW5_FREQ_1     | PMW5_FREQ_0      | PMW6_FREQ_1 | PMW6_FREQ_0 | PMW7_FREQ_1 | PMW7_FREQ_0 | PMW8_FREQ_1 | PMW8_FREQ_0 | PMW9_FREQ_1 | PMW9_FREQ_0 | PMW10_FREQ_1 | PMW10_FREQ_0 | Reserved  |           |           |         | R/W    |
| 0x0D  | CR13 | Reserved        | PWM1_DC_9   | PWM1_DC_8   | PWM1_DC_7   | PWM1_DC_6       | PWM1_DC_5       | PWM1_DC_4       | PWM1_DC_3       | PWM1_DC_2       | PWM1_DC_1        | PWM1_DC_0   | Reserved    |             | PWM2_DC_9   | PWM2_DC_8   | PWM2_DC_7   | PWM2_DC_6   | PWM2_DC_5   | PWM2_DC_4    | PWM2_DC_3    | PWM2_DC_2 | PWM2_DC_1 | PWM2_DC_0 | R/W     |        |
| 0x0E  | CR14 | Reserved        | PWM3_DC_9   | PWM3_DC_8   | PWM3_DC_7   | PWM3_DC_6       | PWM3_DC_5       | PWM3_DC_4       | PWM3_DC_3       | PWM3_DC_2       | PWM3_DC_1        | PWM3_DC_0   | Reserved    |             | PWM4_DC_9   | PWM4_DC_8   | PWM4_DC_7   | PWM4_DC_6   | PWM4_DC_5   | PWM4_DC_4    | PWM4_DC_3    | PWM4_DC_2 | PWM4_DC_1 | PWM4_DC_0 | R/W     |        |
| 0x0F  | CR15 | Reserved        | PWM5_DC_9   | PWM5_DC_8   | PWM5_DC_7   | PWM5_DC_6       | PWM5_DC_5       | PWM5_DC_4       | PWM5_DC_3       | PWM5_DC_2       | PWM5_DC_1        | PWM5_DC_0   | Reserved    |             | PWM6_DC_9   | PWM6_DC_8   | PWM6_DC_7   | PWM6_DC_6   | PWM6_DC_5   | PWM6_DC_4    | PWM6_DC_3    | PWM6_DC_2 | PWM6_DC_1 | PWM6_DC_0 | R/W     |        |

Table 68. Control register overview (continued)

| Addr. | Reg. | Bit      |    |                   |              |              |              |              |              |              |              |              |              |              |          |            |              |              |              |              |              |              |              |              |              | Access       |     |
|-------|------|----------|----|-------------------|--------------|--------------|--------------|--------------|--------------|--------------|--------------|--------------|--------------|--------------|----------|------------|--------------|--------------|--------------|--------------|--------------|--------------|--------------|--------------|--------------|--------------|-----|
|       |      | 23       | 22 | 21                | 20           | 19           | 18           | 17           | 16           | 15           | 14           | 13           | 12           | 11           | 10       | 9          | 8            | 7            | 6            | 5            | 4            | 3            | 2            | 1            | 0            |              |     |
| 0x10  | CR16 | Reserved |    | PWM7_DC_9         | PWM7_DC_8    | PWM7_DC_7    | PWM7_DC_6    | PWM7_DC_5    | PWM7_DC_4    | PWM7_DC_3    | PWM7_DC_2    | PWM7_DC_1    | PWM7_DC_0    | Reserved     |          | PWM8_DC_9  | PWM8_DC_8    | PWM8_DC_7    | PWM8_DC_6    | PWM8_DC_5    | PWM8_DC_4    | PWM8_DC_3    | PWM8_DC_2    | PWM8_DC_1    | PWM8_DC_0    | R/W          |     |
| 0x11  | CR17 | Reserved |    | PWM9_DC_9         | PWM9_DC_8    | PWM9_DC_7    | PWM9_DC_6    | PWM9_DC_5    | PWM9_DC_4    | PWM9_DC_3    | PWM9_DC_2    | PWM9_DC_1    | PWM9_DC_0    | Reserved     |          | PWM10_DC_9 | PWM10_DC_8   | PWM10_DC_7   | PWM10_DC_6   | PWM10_DC_5   | PWM10_DC_4   | PWM10_DC_3   | PWM10_DC_2   | PWM10_DC_1   | PWM10_DC_0   | R/W          |     |
| 0x12  | CR18 | Reserved |    | OUT7_AUTOCOMP_EN  | OUT7_VLED_9  | OUT7_VLED_8  | OUT7_VLED_7  | OUT7_VLED_6  | OUT7_VLED_5  | OUT7_VLED_4  | OUT7_VLED_3  | OUT7_VLED_2  | OUT7_VLED_1  | OUT7_VLED_0  | Reserved |            | OUT8_VLED_9  | OUT8_VLED_8  | OUT8_VLED_7  | OUT8_VLED_6  | OUT8_VLED_5  | OUT8_VLED_4  | OUT8_VLED_3  | OUT8_VLED_2  | OUT8_VLED_1  | OUT8_VLED_0  | R/W |
| 0x13  | CR19 | Reserved |    | OUT9_AUTOCOMP_EN  | OUT9_VLED_9  | OUT9_VLED_8  | OUT9_VLED_7  | OUT9_VLED_6  | OUT9_VLED_5  | OUT9_VLED_4  | OUT9_VLED_3  | OUT9_VLED_2  | OUT9_VLED_1  | OUT9_VLED_0  | Reserved |            | OUT10_VLED_9 | OUT10_VLED_8 | OUT10_VLED_7 | OUT10_VLED_6 | OUT10_VLED_5 | OUT10_VLED_4 | OUT10_VLED_3 | OUT10_VLED_2 | OUT10_VLED_1 | OUT10_VLED_0 | R/W |
| 0x14  | CR20 | Reserved |    | OUT11_AUTOCOMP_EN | OUT11_VLED_9 | OUT11_VLED_8 | OUT11_VLED_7 | OUT11_VLED_6 | OUT11_VLED_5 | OUT11_VLED_4 | OUT11_VLED_3 | OUT11_VLED_2 | OUT11_VLED_1 | OUT11_VLED_0 | Reserved |            | OUT12_VLED_9 | OUT12_VLED_8 | OUT12_VLED_7 | OUT12_VLED_6 | OUT12_VLED_5 | OUT12_VLED_4 | OUT12_VLED_3 | OUT12_VLED_2 | OUT12_VLED_1 | OUT12_VLED_0 | R/W |

Table 68. Control register overview (continued)

|       |          | Bit       |                   |              |              |              |              |                |              |              |              |              |              |          |                   |              |              |              |               |              |              |              |              |              |              | Access |     |      |     |  |
|-------|----------|-----------|-------------------|--------------|--------------|--------------|--------------|----------------|--------------|--------------|--------------|--------------|--------------|----------|-------------------|--------------|--------------|--------------|---------------|--------------|--------------|--------------|--------------|--------------|--------------|--------|-----|------|-----|--|
| Addr. | Reg.     | 23        | 22                | 21           | 20           | 19           | 18           | 17             | 16           | 15           | 14           | 13           | 12           | 11       | 10                | 9            | 8            | 7            | 6             | 5            | 4            | 3            | 2            | 1            | 0            |        |     |      |     |  |
| 0x15  | CR21     | Reserved  | OUT13_AUTOCOMP_EN | OUT13_VLED_9 | OUT13_VLED_8 | OUT13_VLED_7 | OUT13_VLED_6 | OUT13_VLED_5   | OUT13_VLED_4 | OUT13_VLED_3 | OUT13_VLED_2 | OUT13_VLED_1 | OUT13_VLED_0 | Reserved | OUT14_AUTOCOMP_EN | OUT14_VLED_9 | OUT14_VLED_8 | OUT14_VLED_7 | OUT14_VLED_6  | OUT14_VLED_5 | OUT14_VLED_4 | OUT14_VLED_3 | OUT14_VLED_2 | OUT14_VLED_1 | OUT14_VLED_0 | R/W    |     |      |     |  |
|       |          |           | OUT15_AUTOCOMP_EN | OUT15_VLED_9 | OUT15_VLED_8 | OUT15_VLED_7 | OUT15_VLED_6 | OUT15_VLED_5   | OUT15_VLED_4 | OUT15_VLED_3 | OUT15_VLED_2 | OUT15_VLED_1 | OUT15_VLED_0 |          | OUTHS_VLED_9      | OUTHS_VLED_8 | OUTHS_VLED_7 | OUTHS_VLED_6 | OUTHS_VLED_5  | OUTHS_VLED_4 | OUTHS_VLED_3 | OUTHS_VLED_2 | OUTHS_VLED_1 | OUTHS_VLED_0 | R/W          |        |     |      |     |  |
|       |          |           | Reserved          |              |              |              |              |                |              |              |              |              |              |          |                   |              |              |              |               |              |              |              |              | CP_OFF       | ICMP         | WD_EN  | R/W |      |     |  |
|       |          |           | Reserved          |              |              |              |              |                |              |              |              |              |              |          |                   |              |              |              |               |              |              |              |              | Reserved     |              |        |     | TRIG | R/W |  |
|       |          |           | Reserved          |              |              |              |              |                |              |              |              |              |              |          |                   |              |              |              |               |              |              |              |              | Reserved     |              |        |     | TRIG | R/W |  |
|       |          |           | Reserved          |              |              |              |              |                |              |              |              |              |              |          |                   |              |              |              |               |              |              |              |              | Reserved     |              |        |     | TRIG | R/W |  |
|       |          |           | Reserved          |              |              |              |              |                |              |              |              |              |              |          |                   |              |              |              |               |              |              |              |              | Reserved     |              |        |     | TRIG | R/W |  |
|       |          |           | Reserved          |              |              |              |              |                |              |              |              |              |              |          |                   |              |              |              |               |              |              |              |              | Reserved     |              |        |     | TRIG | R/W |  |
|       |          |           | Reserved          |              |              |              |              |                |              |              |              |              |              |          |                   |              |              |              |               |              |              |              |              | Reserved     |              |        |     | TRIG | R/W |  |
|       |          |           | Reserved          |              |              |              |              |                |              |              |              |              |              |          |                   |              |              |              |               |              |              |              |              | Reserved     |              |        |     | TRIG | R/W |  |
|       |          |           | Reserved          |              |              |              |              |                |              |              |              |              |              |          |                   |              |              |              |               |              |              |              |              | Reserved     |              |        |     | TRIG | R/W |  |
|       |          |           | Reserved          |              |              |              |              |                |              |              |              |              |              |          |                   |              |              |              |               |              |              |              |              | Reserved     |              |        |     | TRIG | R/W |  |
|       |          |           | Reserved          |              |              |              |              |                |              |              |              |              |              |          |                   |              |              |              |               |              |              |              |              | Reserved     |              |        |     | TRIG | R/W |  |
|       |          |           | Reserved          |              |              |              |              |                |              |              |              |              |              |          |                   |              |              |              |               |              |              |              |              | Reserved     |              |        |     | TRIG | R/W |  |
|       |          |           | Reserved          |              |              |              |              |                |              |              |              |              |              |          |                   |              |              |              |               |              |              |              |              | Reserved     |              |        |     | TRIG | R/W |  |
|       |          |           | Reserved          |              |              |              |              |                |              |              |              |              |              |          |                   |              |              |              |               |              |              |              |              | Reserved     |              |        |     | TRIG | R/W |  |
| 0x3F  | Conf Reg | WU_CONFIG | LIN_WU_CONFIG     | LIN_HS_EN    | TSD_CONFIG   | Reserved     | DM           | ICMP_CONFIG_EN | WD_CONFIG_EN | MASK_OL_HS1  | MASK_OL_LS1  | MASK_TW      | Reserved     | MASK_OL  | MASK_SPIE         | MASK_PLE     | MASK_GW      | CP_OFF_EN    | CP_LOW_CONFIG | CP_DITH_DIS  | FS_FORCED    | Reserved     |              |              |              | TRIG   | R/W |      |     |  |

**Note:** All reserved bits (RES) are read-only (R) and will be read as '0'. Writing '1' to a reserved bit is ignored and does not cause an SPI error.

## 7.3 Status register overview

Table 69. Status register overview

|       |      | Bit               |                   |              |          |          |          |            |                   |                   |                   |                   |                   |                   |                |                |              |                |                |          |          |                       |                 |                |           | Access    |   |
|-------|------|-------------------|-------------------|--------------|----------|----------|----------|------------|-------------------|-------------------|-------------------|-------------------|-------------------|-------------------|----------------|----------------|--------------|----------------|----------------|----------|----------|-----------------------|-----------------|----------------|-----------|-----------|---|
| Addr. | Reg. | 23                | 22                | 21           | 20       | 19       | 18       | 17         | 16                | 15                | 14                | 13                | 12                | 11                | 10             | 9              | 8            | 7              | 6              | 5        | 4        | 3                     | 2               | 1              | 0         |           |   |
| 0x31  | SR1  | Reserved          | WU_STATE          | Reserved     | WU_WAKE  | Reserved | WAKE_LIN | WAKE_TIMER | DEBUG_ACTIVE      | V1UV              | V1_RESTART_2      | V1_RESTART_1      | V1_RESTART_0      | WDFAIL_CNT_3      | WDFAIL_CNT_2   | WDFAIL_CNT_1   | WDFAIL_CNT_0 | DEVICE_STATE_1 | DEVICE_STATE_0 | TSD2     | TSD1     | FORCED_SLEEP_TSD2N1SC | FORCED_SLEEP_WD | WDFAIL         | VPOR      | ⌘         |   |
| 0x32  | SR2  | LIN_PERM_DOM      | LIN_TXD_DOM       | LIN_PERM_REC | Reserved |          |          |            |                   | DSMON_HS2         | DSMON_HS1         | DSMON_LS2         | DSMON_LS1         | SPI_INV_CMD       | SPI_SCK_CNT    | CP_LOW         | TW           | V2SC           | V2FAIL         | V1FAIL   | VSREG_EW | VSREG_OV              | VSREG_UV        | VS_OV          | VS_UV     | ⌘         |   |
| 0x33  | SR3  | OUT1_HS_OC_TH_EX  | OUT1_LS_OC_TH_EX  | Reserved     |          |          |          |            | OUT4_HS_OC_TH_EX  | OUT4_LS_OC_TH_EX  | OUT5_HS_OC_TH_EX  | OUT5_LS_OC_TH_EX  | OUT6_HS_OC_TH_EX  | OUT6_LS_OC_TH_EX  | OUT7_OC_TH_EX  | OUT8_OC_TH_EX  | OUT9_OC      | OUT10_OC       | OUT11_OC       | OUT12_OC | OUT13_OC | OUT14_OC              | OUT15_OC        | OUTHS_OC_TH_EX | LS2FSO_OC | LS1FSO_OC | ⌘ |
| 0x34  | SR4  | OUT1_HS_OCR_ALERT | OUT1_LS_OCR_ALERT | Reserved     |          |          |          |            | OUT4_HS_OCR_ALERT | OUT4_LS_OCR_ALERT | OUT5_HS_OCR_ALERT | OUT5_LS_OCR_ALERT | OUT6_HS_OCR_ALERT | OUT6_LS_OCR_ALERT | OUT7_OCR_ALERT | OUT8_OCR_ALERT | Reserved     |                |                |          |          |                       | OUTHS_OCR_ALERT | Reserved       |           | ⌘         |   |
| 0x35  | SR5  | OUT1_HS_OL        | OUT1_LS_OL        | Reserved     |          |          |          |            | OUT4_HS_OL        | OUT4_LS_OL        | OUT5_HS_OL        | OUT5_LS_OL        | OUT6_HS_OL        | OUT6_LS_OL        | OUT7_OL        | OUT8_OL        | OUT9_OL      | OUT10_OL       | OUT11_OL       | OUT12_OL | OUT13_OL | OUT14_OL              | OUT15_OL        | OUTHS_OL       | Reserved  | ⌘         |   |

**Table 69. Status register overview (continued)**

|       |      | Bit              |                  |            |            |            |            |            |            |            |            |            |            |          |        |            |            |            |            |            |            |            |            |            |            | Access   |          |   |
|-------|------|------------------|------------------|------------|------------|------------|------------|------------|------------|------------|------------|------------|------------|----------|--------|------------|------------|------------|------------|------------|------------|------------|------------|------------|------------|----------|----------|---|
| Addr. | Reg. | 23               | 22               | 21         | 20         | 19         | 18         | 17         | 16         | 15         | 14         | 13         | 12         | 11       | 10     | 9          | 8          | 7          | 6          | 5          | 4          | 3          | 2          | 1          | 0          |          |          |   |
| 0x36  | SR6  | WD_TIMER_STATE_1 | WD_TIMER_STATE_0 | Reserved   |            |            |            |            |            |            |            |            |            | TW_CL6   | TW_CL5 | TW_CL4     | TW_CL3     | TW_CL2     | TW_CL1     | Reserved   |            | TSD1_CL6   | TSD1_CL5   | TSD1_CL4   | TSD1_CL3   | TSD1_CL2 | TSD1_CL1 | R |
|       |      |                  |                  |            |            |            |            |            |            |            |            |            |            |          |        |            |            |            |            |            |            |            |            |            |            |          |          |   |
| 0x37  | SR7  | Reserved         |                  | TEMP_CL2_9 | TEMP_CL2_8 | TEMP_CL2_7 | TEMP_CL2_6 | TEMP_CL2_5 | TEMP_CL2_4 | TEMP_CL2_3 | TEMP_CL2_2 | TEMP_CL2_1 | TEMP_CL2_0 | Reserved |        | TEMP_CL1_9 | TEMP_CL1_8 | TEMP_CL1_7 | TEMP_CL1_6 | TEMP_CL1_5 | TEMP_CL1_4 | TEMP_CL1_3 | TEMP_CL1_2 | TEMP_CL1_1 | TEMP_CL1_0 | R        |          |   |
| 0x38  | SR8  | Reserved         |                  | TEMP_CL4_9 | TEMP_CL4_8 | TEMP_CL4_7 | TEMP_CL4_6 | TEMP_CL4_5 | TEMP_CL4_4 | TEMP_CL4_3 | TEMP_CL4_2 | TEMP_CL4_1 | TEMP_CL4_0 | Reserved |        | TEMP_CL3_9 | TEMP_CL3_8 | TEMP_CL3_7 | TEMP_CL3_6 | TEMP_CL3_5 | TEMP_CL3_4 | TEMP_CL3_3 | TEMP_CL3_2 | TEMP_CL3_1 | TEMP_CL3_0 | R        |          |   |
| 0x39  | SR9  | Reserved         |                  | TEMP_CL6_9 | TEMP_CL6_8 | TEMP_CL6_7 | TEMP_CL6_6 | TEMP_CL6_5 | TEMP_CL6_4 | TEMP_CL6_3 | TEMP_CL6_2 | TEMP_CL6_1 | TEMP_CL6_0 | Reserved |        | TEMP_CL5_9 | TEMP_CL5_8 | TEMP_CL5_7 | TEMP_CL5_6 | TEMP_CL5_5 | TEMP_CL5_4 | TEMP_CL5_3 | TEMP_CL5_2 | TEMP_CL5_1 | TEMP_CL5_0 | R        |          |   |
| 0x3A  | SR10 | Reserved         |                  | VSREG_9    | VSREG_8    | VSREG_7    | VSREG_6    | VSREG_5    | VSREG_4    | VSREG_3    | VSREG_2    | VSREG_1    | VSREG_0    | Reserved |        |            |            |            |            |            |            |            |            |            |            | R        |          |   |
| 0x3B  | SR11 | Reserved         |                  | VS_9       | VS_8       | VS_7       | VS_6       | VS_5       | VS_4       | VS_3       | VS_2       | VS_1       | VS_0       | Reserved |        | VWU_9      | VWU_8      | VWU_7      | VWU_6      | VWU_5      | VWU_4      | VWU_3      | VWU_2      | VWU_1      | VWU_0      | R        |          |   |

## 7.4 Control registers

### 7.4.1 Control Register CR1 (0x01)

Table 70. Control Register CR1

|          | 23       | 22    | 21       | 20    | 19       | 18 | 17        | 16        | 15                  | 14            | 13       | 12 | 11 | 10 | 9 | 8 | 7 | 6   | 5    | 4    | 3      | 2        | 1       | 0    |
|----------|----------|-------|----------|-------|----------|----|-----------|-----------|---------------------|---------------|----------|----|----|----|---|---|---|-----|------|------|--------|----------|---------|------|
| Bit name | Reserved | WU_EN | Reserved | WU_PU | Reserved |    | WU_FILT_1 | WU_FILT_0 | TIMER_NINT_WAKE_SEL | TIMER_NINT_EN | Reserved |    |    |    |   |   |   | HEN | V2_1 | V2_0 | PARITY | STBY_SEL | GO_STBY | TRIG |
| Reset    | 0        | 1     | 0        | 0     | 0        | 0  | 0         | 0         | 0                   | 0             | 1        | 0  | 0  | 0  | 0 | 0 | 0 | 0   | 0    | 0    | 0      | 0        | 0       | 0    |
| Access   | R        | R/W   | R        | R/W   | R        |    | R/W       |           |                     |               |          |    |    |    |   |   |   |     |      |      |        |          |         |      |

Table 71. CR1 signals description

| Bit | Name                | Description                                                                                                                                                 |
|-----|---------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 23  | Reserved            | —                                                                                                                                                           |
| 22  | WU_EN               | Wake-up Input 1 (WU) enable <sup>(1)</sup><br>0: WU disabled<br>1: WU enabled (default)                                                                     |
| 21  | Reserved            | —                                                                                                                                                           |
| 20  | WU_PU               | Wake-up Input1 Pull-up/down configuration: configuration of internal current source <sup>(1)</sup><br>0: pull-down (default)<br>1: pull-up                  |
| 19  | Reserved            | —                                                                                                                                                           |
| 18  |                     |                                                                                                                                                             |
| 17  | WU_FILT_1           | Wake-up Input1 Filter configuration Bits: configuration of input filter <sup>(1)</sup><br>See <a href="#">Table 72: Wake-up input1 filter configuration</a> |
| 16  | WU_FILT_0           |                                                                                                                                                             |
| 15  | TIMER_NINT_WAKE_SEL | Select Timer for NINT / Wake: select timer for periodic interrupt in standby modes<br>0: Timer 2 (default)<br>1: Timer 1                                    |

Table 71. CR1 signals description (continued)

| Bit  | Name          | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                |
|------|---------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 14   | TIMER_NINT_EN | Timer NINT enable: enable timer interrupt in standby modes<br>0: timer interrupt disabled (default)<br>1: timer interrupt enabled<br>V1_standby mode: periodic NINT pulse generated by timer (NINT pulse at start of timer on-phase)<br>Vbat_standby mode: device wakes up after timer expiration and generates NReset                                                                                                                                     |
| 13:7 | Reserved      | —                                                                                                                                                                                                                                                                                                                                                                                                                                                          |
| 6    | HEN           | Enable H-bridge<br>0: H-bridge disabled (default)<br>1: H-bridge enabled<br>Refer to chapter <i>H-bridge Control</i> for details                                                                                                                                                                                                                                                                                                                           |
| 5    | V2_1          | Voltage Regulator V2 Configuration<br>See <a href="#">Table 73: Voltage regulator V2 configuration</a>                                                                                                                                                                                                                                                                                                                                                     |
| 4    | V2_0          |                                                                                                                                                                                                                                                                                                                                                                                                                                                            |
| 3    | PARITY        | PARITY: Standby Command Parity Bit                                                                                                                                                                                                                                                                                                                                                                                                                         |
| 2    | STBY_SEL      | STBY SEL: Select Standby mode<br>GO_STBY: Execute transition into Standby mode                                                                                                                                                                                                                                                                                                                                                                             |
| 1    | GO_STBY       | The STBY_SEL and GO_STBY bits are protected by a parity check.<br>The bits STBY_SEL, GO_STBY and PARITY must represent an even number of '1', otherwise the command is ignored and the SPI_INV_CMD bit is set.<br><a href="#">Table 74: Standby transition configuration</a> shows the valid settings.<br>All other settings are invalid; command will be ignored and SPI_INV_CMD will be set. The GO_STBY bit is not cleared automatically after wake-up. |
| 0    | TRIG          | Watchdog Trigger Bit                                                                                                                                                                                                                                                                                                                                                                                                                                       |

1. Setting is only valid if input is configured as wake-up input in Configuration Register (0x3F).

Table 72. Wake-up input1 filter configuration

| WU_FILT_1 | WU_FILT_0 |                                                                                                                        |
|-----------|-----------|------------------------------------------------------------------------------------------------------------------------|
| 0         | 0         | Wake-up inputs monitored in static mode (filter time $t_{wu\_stat}$ ) (default)                                        |
| 0         | 1         | Wake- up inputs monitored in cyclic mode with Timer2 (filter time: $t_{wu\_cyc}$ ; blanking time 80% of timer ON time) |
| 1         | 0         | Wake- up inputs monitored in cyclic mode with Timer1 (filter time: $t_{wu\_cyc}$ ; blanking time 80% of timer ON time) |
| 1         | 1         | Invalid setting; command will be ignored and SPI INV CMD will be set                                                   |

Table 73. Voltage regulator V2 configuration

| V2_1 | V2_0 |                                            |
|------|------|--------------------------------------------|
| 0    | 0    | V2 OFF in all modes (default)              |
| 0    | 1    | V2 ON in Active mode; OFF in Standby modes |

Table 73. Voltage regulator V2 configuration (continued)

| V2_1 | V2_0 |                                                               |
|------|------|---------------------------------------------------------------|
| 1    | 0    | V2 ON in Active and V1_standby mode; OFF in Vbat_standby mode |
| 1    | 1    | V2 ON in all modes                                            |

Table 74. Standby transition configuration

| PARITY | STBY_SEL | GO_STBY |                          |
|--------|----------|---------|--------------------------|
| 0      | 1        | 1       | Go to V1 standby         |
| 1      | 0        | 1       | Go to Vbat_standby       |
| 0      | 0        | 0       | No transition to standby |
| 1      | 1        | 0       |                          |

## 7.4.2 Control Register CR2 (0x02)

Table 75. Control Register CR2

|          | 23         | 22     | 21      | 20      | 19      | 18       | 17       | 16       | 15         | 14     | 13      | 12      | 11      | 10       | 9        | 8        | 7            | 6               | 5        | 4 | 3          | 2          | 1         | 0         |
|----------|------------|--------|---------|---------|---------|----------|----------|----------|------------|--------|---------|---------|---------|----------|----------|----------|--------------|-----------------|----------|---|------------|------------|-----------|-----------|
| Bit name | T1_RESTART | T1_DIR | T1_ON_2 | T1_ON_1 | T1_ON_0 | T1_PER_2 | T1_PER_1 | T1_PER_0 | T2_RESTART | T2_DIR | T2_ON_2 | T2_ON_1 | T2_ON_0 | T2_PER_2 | T2_PER_1 | T2_PER_0 | LIN_REC_ONLY | LIN_TXD_TOUT_EN | Reserved |   | V1_RESET_1 | V1_RESET_0 | WD_TIME_1 | WD_TIME_0 |
| Reset    | 0          | 0      | 0       | 0       | 0       | 0        | 0        | 0        | 0          | 0      | 0       | 0       | 0       | 0        | 0        | 0        | 0            | 1               | 0        | 0 | 0          | 0          | 0         | 0         |
| Access   | R/W        |        |         |         |         |          |          |          |            |        |         |         |         |          |          |          |              |                 |          |   |            |            |           |           |

Table 76. CR2 signals description

| Bit | Name       | Description                                                                                                                                                                                                                                                            |
|-----|------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 23  | T1_RESTART | Timer 1 Restart: Restart of Timer 1<br>0: timer is running with period and on-time according to configuration (default)<br>1: restart of timer at CSN low to high transition; starting with ON phase <sup>(1)</sup><br>Bit is automatically reset with next SPI frame. |
| 22  | T1_DIR1    | T1_DIR1: Timer 1 Direct Drive by DIR1<br>T1_ON_x: Timer 1 On-Time Bits<br>Configuration of Timer 1 on-time, for details see <a href="#">Table 77</a> and <a href="#">Figure 56</a>                                                                                     |
| 21  | T1_ON_2    |                                                                                                                                                                                                                                                                        |
| 20  | T1_ON_1    |                                                                                                                                                                                                                                                                        |
| 19  | T1_ON_0    |                                                                                                                                                                                                                                                                        |

Table 76. CR2 signals description (continued)

| Bit | Name            | Description                                                                                                                                                                                                                                                            |  |
|-----|-----------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--|
| 18  | T1_PER_2        | Configuration of Timer 1 Period<br>000: T1 (default)<br>001: T2<br>010: T3<br>011: T4<br>100: T5<br>101: T6<br>110: T7<br>111: T8                                                                                                                                      |  |
| 17  | T1_PER_1        |                                                                                                                                                                                                                                                                        |  |
| 16  | T1_PER_0        |                                                                                                                                                                                                                                                                        |  |
|     |                 |                                                                                                                                                                                                                                                                        |  |
| 15  | T2_RESTART      | Timer 2 Restart: restart of timer 2<br>0: timer is running with period and on-time according to configuration (default)<br>1: restart of timer at CSN low to high transition; starting with ON phase <sup>(1)</sup><br>Bit is automatically reset with next SPI frame. |  |
| 14  | T2_DIR1         | T2_DIR1: Timer 2 Direct Drive by DIR1<br>T2_ON_x: Timer 2 On-Time Bits<br>Configuration of Timer 2 on-time, for details see <a href="#">Table 77</a> and <a href="#">Figure 56</a>                                                                                     |  |
| 13  | T2_ON_2         |                                                                                                                                                                                                                                                                        |  |
| 12  | T2_ON_1         |                                                                                                                                                                                                                                                                        |  |
| 11  | T2_ON_0         |                                                                                                                                                                                                                                                                        |  |
| 10  | T2_PER_2        | Configuration of Timer 2 Period<br>000: T1 (default)<br>001: T2<br>010: T3<br>011: T4<br>100: T5<br>101: T6<br>110: T7<br>111: T8                                                                                                                                      |  |
| 9   | T2_PER_1        |                                                                                                                                                                                                                                                                        |  |
| 8   | T2_PER_0        |                                                                                                                                                                                                                                                                        |  |
|     |                 |                                                                                                                                                                                                                                                                        |  |
| 7   | LIN_REC_ONLY    | LIN Transceiver Receive Only mode<br>0: LIN receive only mode disabled (default)<br>1: LIN receive only mode enabled                                                                                                                                                   |  |
| 6   | LIN_TXD_TOUT_EN | LIN TxD Timeout Enable<br>0: LIN TxD timeout detection disabled<br>1: LIN TxD timeout detection enabled (default)                                                                                                                                                      |  |
| 5:4 | Reserved        | —                                                                                                                                                                                                                                                                      |  |

**Table 76. CR2 signals description (continued)**

| Bit | Name       | Description                                                                                                                                                                                                                                                                                                                       |
|-----|------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 3   | V1_RESET_1 | Voltage Regulator V1 Reset Threshold                                                                                                                                                                                                                                                                                              |
| 2   | V1_RESET_0 | 00: Vrt4 (default)<br>01: Vrt3<br>10: Vrt2<br>11: Vrt1<br>thresholds are monitored in Active mode and V1_standby mode                                                                                                                                                                                                             |
| 1   | WD_TIME_1  | Watchdog Trigger Time                                                                                                                                                                                                                                                                                                             |
| 0   | WD_TIME_0  | 00: TSW1 (default)<br>01: TSW2<br>10: TSW3<br>11: TSW4<br>Writing to WD_TIME_x is blocked unless WD CONFIG EN = 1.<br>The modified WD Trigger Time is valid immediately after the Write command (CSN transition low-high).<br>The watchdog timer is reset when the trigger time is modified (restart at CSN transition low-high). |

## 1. Timer restart behavior:

Write to CR2 when Tx\_ON\_x and Tx\_PERx remain unchanged:

Tx\_RESTART = 1: timers restart at end of SPI frame, starting with ON time

Tx\_RESTART = 0: write operation to CR2 has no effect on timers

Write to CR2 when Tx\_ON\_x and Tx\_PERx are modified

Tx\_RESTART = 1: timers restart at end of SPI frame, starting with ON time and according to new setting (ON time and period)

Tx\_RESTART = 0: behavior is not defined; if a predictable behavior is needed, it is recommended to set Tx\_RESTART = 1

**Table 77. Configuration of Timer x on-time**

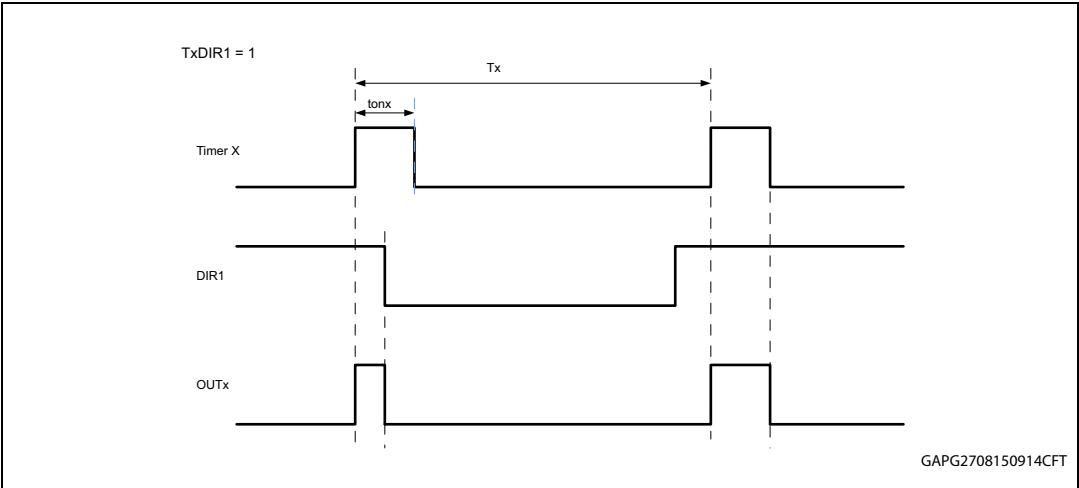
| Tx_DIR1          | Tx_ON_2 | Tx_ON_1 | Tx_ON_0 |                                                                      |
|------------------|---------|---------|---------|----------------------------------------------------------------------|
| 0                | 0       | 0       | 0       | ton1 (default)                                                       |
| 0                | 0       | 0       | 1       | ton2                                                                 |
| 0                | 0       | 1       | 0       | ton3                                                                 |
| 0                | 0       | 1       | 1       | ton4                                                                 |
| 0                | 1       | 0       | 0       | ton5                                                                 |
| 0                | 1       | 0       | 1       | Invalid setting; command will be ignored and SPI INV CMD will be set |
| 0                | 1       | 1       | 0       |                                                                      |
| 0                | 1       | 1       | 1       |                                                                      |
| 1 <sup>(1)</sup> | 0       | 0       | 0       | ton1 controlled by DIR1 input signal (logical AND)                   |
| 1 <sup>(1)</sup> | 0       | 0       | 1       | ton2 controlled by DIR1 input signal (logical AND)                   |
| 1 <sup>(1)</sup> | 0       | 1       | 0       | ton3 controlled by DIR1 input signal (logical AND)                   |
| 1 <sup>(1)</sup> | 0       | 1       | 1       | ton4 controlled by DIR1 input signal (logical AND)                   |
| 1 <sup>(1)</sup> | 1       | 0       | 0       | ton5 controlled by DIR1 input signal (logical AND)                   |

Table 77. Configuration of Timer x on-time (continued)

| Tx_DIR1          | Tx_ON_2 | Tx_ON_1 | Tx_ON_0 |                                                                             |
|------------------|---------|---------|---------|-----------------------------------------------------------------------------|
| 1 <sup>(1)</sup> | 1       | 0       | 1       | Invalid setting; command will be ignored and <i>SPI/INV_CMD</i> will be set |
| 1 <sup>(1)</sup> | 1       | 1       | 0       |                                                                             |
| 1 <sup>(1)</sup> | 1       | 1       | 1       |                                                                             |

1. Tx\_DIR1 = 1 is only valid for OUT7-OUT15 and OUT\_HS control; the DIR1 signal has no influence for WU monitoring if WU is monitored by timer.

Figure 56. Timer\_x controlled by DIR1



7.4.3 Control Register CR3 (0x03)

Table 78. Control Register CR3

|          | 23            | 22         | 21             | 20             | 19          | 18          | 17       | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9            | 8            | 7            | 6            | 5            | 4            | 3            | 2            | 1            | 0            |
|----------|---------------|------------|----------------|----------------|-------------|-------------|----------|----|----|----|----|----|----|----|--------------|--------------|--------------|--------------|--------------|--------------|--------------|--------------|--------------|--------------|
| Bit name | VSREG_LOCK_EN | VS_LOCK_EN | VSREG_OV_SD_EN | VSREG_UV_SD_EN | VS_OV_SD_EN | VS_UV_SD_EN | Reserved |    |    |    |    |    |    |    | VSREG_EWTH_9 | VSREG_EWTH_8 | VSREG_EWTH_7 | VSREG_EWTH_6 | VSREG_EWTH_5 | VSREG_EWTH_4 | VSREG_EWTH_3 | VSREG_EWTH_2 | VSREG_EWTH_1 | VSREG_EWTH_0 |
| Reset    | 1             | 1          | 1              | 1              | 1           | 1           | 0        | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0            | 0            | 0            | 0            | 0            | 0            | 0            | 0            | 0            | 0            |
| Access   | R/W           |            |                |                |             |             |          |    |    |    |    |    |    |    |              |              |              |              |              |              |              |              |              |              |

Table 79. CR3 signals description

| Bit   | Name           | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |
|-------|----------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 23    | VSREG_LOCK_EN  | <p>VSREG lockout enable: Lockout of V<sub>SREG</sub> related outputs after V<sub>SREG</sub> overvoltage/undervoltage shutdown</p> <p>0: V<sub>SREG</sub> related Outputs are turned on automatically and status bits (VSREG_UV, VSREG_OV) are cleared</p> <p>1: V<sub>SREG</sub> related Outputs remain turned off until status bits (VSREG_UV, VSREG_OV) are cleared (default)</p> <p>Lockout is always disabled in standby modes in order to ensure supply of external contacts and detect wake-up conditions</p> |
| 22    | VS_LOCK_EN     | <p>V<sub>S</sub> lockout enable: Lockout of V<sub>S</sub> related outputs after V<sub>S</sub> over/undervoltage shutdown</p> <p>0: V<sub>S</sub> related Outputs are turned on automatically and status bits (VS_UV, VS_OV) are cleared</p> <p>1: V<sub>S</sub> related Outputs remain turned off until status bits (VS_UV, VS_OV) are cleared (default)</p> <p>Lockout is always disabled in standby modes in order to ensure supply of external contacts and detect wake-up conditions</p>                        |
| 21    | VSREG_OV_SD_EN | <p>VSREG overvoltage shutdown enable: shutdown of V<sub>SREG</sub> related outputs in case of V<sub>SREG</sub> overvoltage</p> <p>0: no shutdown of V<sub>SREG</sub> related outputs in case of V<sub>SREG</sub> overvoltage</p> <p>1: shutdown of V<sub>SREG</sub> related outputs in case of V<sub>SREG</sub> overvoltage (default)</p>                                                                                                                                                                           |
| 20    | VSREG_UV_SD_EN | <p>VSREG undervoltage shutdown enable: shutdown of V<sub>SREG</sub> related outputs in case of V<sub>SREG</sub> undervoltage</p> <p>0: no shutdown of V<sub>SREG</sub> related outputs in case of V<sub>SREG</sub> undervoltage</p> <p>1: shutdown of V<sub>SREG</sub> related outputs in case of V<sub>SREG</sub> undervoltage (default)</p> <p>In case of V1 undervoltage due to VSREG_UV, the device enters Fail-Safe mode and the outputs are turned off</p>                                                    |
| 19    | VS_OV_SD_EN    | <p>V<sub>S</sub> overvoltage shutdown enable: shutdown of V<sub>S</sub> related outputs in case of V<sub>S</sub> overvoltage</p> <p>0: no shutdown of V<sub>S</sub> related outputs in case of V<sub>S</sub> overvoltage if charge pump output voltage is still sufficient (until CPLOW threshold is reached)</p> <p>1: shutdown of V<sub>S</sub> related outputs in case of V<sub>S</sub> overvoltage (default)</p>                                                                                                |
| 18    | VS_UV_SD_EN    | <p>V<sub>S</sub> undervoltage shutdown enable: shutdown of V<sub>S</sub> related outputs in case of V<sub>S</sub> undervoltage</p> <p>0: no shutdown V<sub>S</sub> related of outputs in case of V<sub>S</sub> undervoltage</p> <p>1: shutdown of V<sub>S</sub> related outputs in case of V<sub>S</sub> undervoltage (default)</p> <p>In case of V1 undervoltage due to VS_UV, the device enters Fail-Safe mode and the outputs are turned off</p>                                                                 |
| 17:10 | Reserved       | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |

Table 79. CR3 signals description (continued)

| Bit | Name          | Description                                                                                                                                                                                                                                                                                  |
|-----|---------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 9   | VSREG_EW_TH_9 | <p>VSREG early warning threshold.</p> <p>At <math>V_{SREG} &lt; VSREG\_EW\_TH</math>, an interrupt is generated at NINT and status bit VSREG_EW in SR2 is set (in Active mode)</p> <p>0000000000: 0 V (default) feature deactivated</p> <p>...</p> <p>1111111111: <math>V_{AINVS}</math></p> |
| 8   | VSREG_EW_TH_8 |                                                                                                                                                                                                                                                                                              |
| 7   | VSREG_EW_TH_7 |                                                                                                                                                                                                                                                                                              |
| 6   | VSREG_EW_TH_6 |                                                                                                                                                                                                                                                                                              |
| 5   | VSREG_EW_TH_5 |                                                                                                                                                                                                                                                                                              |
| 4   | VSREG_EW_TH_4 |                                                                                                                                                                                                                                                                                              |
| 3   | VSREG_EW_TH_3 |                                                                                                                                                                                                                                                                                              |
| 2   | VSREG_EW_TH_2 |                                                                                                                                                                                                                                                                                              |
| 1   | VSREG_EW_TH_1 |                                                                                                                                                                                                                                                                                              |
| 0   | VSREG_EW_TH_0 |                                                                                                                                                                                                                                                                                              |

#### 7.4.4 Control Register CR4 (0x04)

Table 80. Control Register CR4

|          | 23       | 22 | 21      | 20      | 19       | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9       | 8       | 7        | 6 | 5       | 4       | 3        | 2 | 1       | 0       |
|----------|----------|----|---------|---------|----------|----|----|----|----|----|----|----|----|----|---------|---------|----------|---|---------|---------|----------|---|---------|---------|
| Bit name | Reserved |    | OUT1_HS | OUT1_LS | Reserved |    |    |    |    |    |    |    |    |    | OUT4_HS | OUT4_LS | Reserved |   | OUT5_HS | OUT5_LS | Reserved |   | OUT6_HS | OUT6_LS |
| Reset    | 0        | 0  | 0       | 0       | 0        | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0       | 0       | 0        | 0 | 0       | 0       | 0        | 0 | 0       | 0       |
| Access   | R/W      |    |         |         |          |    |    |    |    |    |    |    |    |    |         |         |          |   |         |         |          |   |         |         |

Table 81. CR4 signals description

| Bit   | Name     | Description                                                                                                                                                                                                                                                          |
|-------|----------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 23:22 | Reserved | Reserved                                                                                                                                                                                                                                                             |
| 21    | OUT1_HS  | <p>OUT1 high-side Driver control</p> <p>0: OUT1_HS is turned off (default)</p> <p>1: OUT1_HS is turned on</p> <p>An internal cross-current protection prevents, that both the low- and high-side drivers of the half-bridge OUT1 are switched on simultaneously.</p> |
| 20    | OUT1_LS  | <p>OUT1 low-side Driver control</p> <p>0: OUT1_LS is turned off (default)</p> <p>1: OUT1_LS is turned on</p> <p>An internal cross-current protection prevents, that both the low- and high-side drivers of the half-bridge OUT1 are switched on simultaneously.</p>  |
| 19:10 | Reserved | Reserved                                                                                                                                                                                                                                                             |

Table 81. CR4 signals description (continued)

| Bit | Name     | Description                                                                                                                                                                                                                                           |
|-----|----------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 9   | OUT4_HS  | OUT4 high-side Driver control<br>0: OUT4_HS is turned off (default)<br>1: OUT4_HS is turned on<br>An internal cross-current protection prevents, that both the low- and high-side drivers of the half-bridge OUT4 are switched on simultaneously.     |
| 8   | OUT4_LS  | OUT4 low-side Driver control<br>0: OUT4_LS is turned off (default)<br>1: OUT4_LS is turned on<br>An internal cross-current protection prevents, that both the low- and high-side drivers of the half-bridge OUT4 are switched on simultaneously.      |
| 7:6 | Reserved | Reserved                                                                                                                                                                                                                                              |
| 5   | OUT5_HS  | OUT5 high-side Driver control<br>0: OUT5_HS is turned off (default)<br>1: OUT5_HS is turned on<br>An internal cross-current protection prevents, that both the low- and high-side drivers of the half-bridge OUT5 are switched on simultaneously.     |
| 4   | OUT5_LS  | OUT5 low-side Driver control<br>0: OUT5_LS is turned off (default)<br>1: OUT5_LS is turned on<br>An internal cross-current protection prevents, that both the low- and high-side drivers of the half-bridge OUT5 are switched on simultaneously.      |
| 3:2 | Reserved | Reserved                                                                                                                                                                                                                                              |
| 1   | OUT6_HS  | OUT6 high-side Driver control<br>0: OUT6_HS is turned off (default)<br>1: OUT6_HS is turned on<br>An internal cross-current protection prevents, that both the low-side and high-side drivers of the half-bridge OUT6 are switched on simultaneously. |
| 0   | OUT6_LS  | OUT6 low-side Driver control<br>0: OUT6_LS is turned off (default)<br>1: OUT6_LS is turned on<br>An internal cross-current protection prevents, that both the low-side and high-side drivers of the half-bridge OUT6 are switched on simultaneously.  |

#### 7.4.5 Control Register CR5 (0x05)

Table 82. Control Register CR5

|          | 23     | 22     | 21     | 20     | 19     | 18     | 17     | 16     | 15       | 14 | 13 | 12 | 11      | 10      | 9       | 8       | 7        | 6 | 5 | 4 | 3       | 2       | 1       | 0       |
|----------|--------|--------|--------|--------|--------|--------|--------|--------|----------|----|----|----|---------|---------|---------|---------|----------|---|---|---|---------|---------|---------|---------|
| Bit name | OUT7_3 | OUT7_2 | OUT7_1 | OUT7_0 | OUT8_3 | OUT8_2 | OUT8_1 | OUT8_0 | Reserved |    |    |    | OUT10_3 | OUT10_2 | OUT10_1 | OUT10_0 | Reserved |   |   |   | OUTHS_3 | OUTHS_2 | OUTHS_1 | OUTHS_0 |
| Reset    | 0      | 0      | 0      | 0      | 0      | 0      | 0      | 0      | 0        | 0  | 0  | 0  | 0       | 0       | 0       | 0       | 0        | 0 | 0 | 0 | 0       | 0       | 0       | 0       |
| Access   | R/W    |        |        |        |        |        |        |        |          |    |    |    |         |         |         |         |          |   |   |   |         |         |         |         |

Table 83. CR5 signals description

| Bit   | Name     | Description                                                                                                                                          |
|-------|----------|------------------------------------------------------------------------------------------------------------------------------------------------------|
| 23    | OUT7_3   | OUT7 Configuration Bits: high-side Driver OUT7 Configuration<br>For OUT7 bits configuration see <a href="#">Table 84: OUTx Configuration bits</a>    |
| 22    | OUT7_2   |                                                                                                                                                      |
| 21    | OUT7_1   |                                                                                                                                                      |
| 20    | OUT7_0   |                                                                                                                                                      |
| 19    | OUT8_3   | OUT8 Configuration Bits: high-side Driver OUT8 Configuration<br>For OUT8 bits configuration see <a href="#">Table 84: OUTx Configuration bits</a>    |
| 18    | OUT8_2   |                                                                                                                                                      |
| 17    | OUT8_1   |                                                                                                                                                      |
| 16    | OUT8_0   |                                                                                                                                                      |
| 15:12 | Reserved | —                                                                                                                                                    |
| 11    | OUT10_3  | OUT10 Configuration Bits: high-side Driver OUT10 Configuration<br>For OUT10 bits configuration see <a href="#">Table 84: OUTx Configuration bits</a> |
| 10    | OUT10_2  |                                                                                                                                                      |
| 9     | OUT10_1  |                                                                                                                                                      |
| 8     | OUT10_0  |                                                                                                                                                      |
| 7:4   | Reserved | —                                                                                                                                                    |
| 3     | OUTHS_3  | OUTHS Configuration Bits: high-side Driver OUTHS Configuration<br>For OUTHS bits configuration see <a href="#">Table 84: OUTx Configuration bits</a> |
| 2     | OUTHS_2  |                                                                                                                                                      |
| 1     | OUTHS_1  |                                                                                                                                                      |
| 0     | OUTHS_0  |                                                                                                                                                      |

Table 84. OUTx Configuration bits

| OUTx_3 | OUTx_2 | OUTx_1 | OUTx_0 | Description   |
|--------|--------|--------|--------|---------------|
| 0      | 0      | 0      | 0      | Off (default) |
| 0      | 0      | 0      | 1      | On            |
| 0      | 0      | 1      | 0      | Timer1        |
| 0      | 0      | 1      | 1      | Timer2        |
| 0      | 1      | 0      | 0      | PWM1          |
| 0      | 1      | 0      | 1      | PWM2          |
| 0      | 1      | 1      | 0      | PWM3          |
| 0      | 1      | 1      | 1      | PWM4          |
| 1      | 0      | 0      | 0      | PWM5          |
| 1      | 0      | 0      | 1      | PWM6          |
| 1      | 0      | 1      | 0      | PWM7          |
| 1      | 0      | 1      | 1      | PWM8          |
| 1      | 1      | 0      | 0      | PWM9          |

Table 84. OUTx Configuration bits (continued)

| OUTx_3 | OUTx_2 | OUTx_1 | OUTx_0 | Description |
|--------|--------|--------|--------|-------------|
| 1      | 1      | 0      | 1      | PWM10       |
| 1      | 1      | 1      | 0      | DIR1        |
| 1      | 1      | 1      | 1      | DIR2        |

#### 7.4.6 Control Register CR6 (0x06)

Table 85. Control Register CR6

|          | 23     | 22     | 21     | 20     | 19      | 18      | 17      | 16      | 15      | 14      | 13      | 12      | 11      | 10      | 9       | 8       | 7       | 6       | 5       | 4       | 3       | 2       | 1       | 0       |
|----------|--------|--------|--------|--------|---------|---------|---------|---------|---------|---------|---------|---------|---------|---------|---------|---------|---------|---------|---------|---------|---------|---------|---------|---------|
| Bit name | OUT9_3 | OUT9_2 | OUT9_1 | OUT9_0 | OUT11_3 | OUT11_2 | OUT11_1 | OUT11_0 | OUT12_3 | OUT12_2 | OUT12_1 | OUT12_0 | OUT13_3 | OUT13_2 | OUT13_1 | OUT13_0 | OUT14_3 | OUT14_2 | OUT14_1 | OUT14_0 | OUT15_3 | OUT15_2 | OUT15_1 | OUT15_0 |
| Reset    | 0      | 0      | 0      | 0      | 0       | 0       | 0       | 0       | 0       | 0       | 0       | 0       | 0       | 0       | 0       | 0       | 0       | 0       | 0       | 0       | 0       | 0       | 0       | 0       |
| Access   | R/W    |        |        |        |         |         |         |         |         |         |         |         |         |         |         |         |         |         |         |         |         |         |         |         |

Table 86. CR6 signals description

| Bit | Name    | Description                                                                                                                                          |
|-----|---------|------------------------------------------------------------------------------------------------------------------------------------------------------|
| 23  | OUT9_3  | OUT9 Configuration Bits: high-side Driver OUT9 Configuration<br>For OUT9 bits configuration see <a href="#">Table 84: OUTx Configuration bits</a>    |
| 22  | OUT9_2  |                                                                                                                                                      |
| 21  | OUT9_1  |                                                                                                                                                      |
| 20  | OUT9_0  |                                                                                                                                                      |
| 19  | OUT11_3 | OUT11 Configuration Bits: high-side Driver OUT11 Configuration<br>For OUT11 bits configuration see <a href="#">Table 84: OUTx Configuration bits</a> |
| 18  | OUT11_2 |                                                                                                                                                      |
| 17  | OUT11_1 |                                                                                                                                                      |
| 16  | OUT11_0 |                                                                                                                                                      |
| 15  | OUT12_3 | OUT12 Configuration Bits: high-side Driver OUT12 Configuration<br>For OUT12 bits configuration see <a href="#">Table 84: OUTx Configuration bits</a> |
| 14  | OUT12_2 |                                                                                                                                                      |
| 13  | OUT12_1 |                                                                                                                                                      |
| 12  | OUT12_0 |                                                                                                                                                      |
| 11  | OUT13_3 | OUT13 Configuration Bits: high-side Driver OUT13 Configuration<br>For OUT13 bits configuration see <a href="#">Table 84: OUTx Configuration bits</a> |
| 10  | OUT13_2 |                                                                                                                                                      |
| 9   | OUT13_1 |                                                                                                                                                      |
| 8   | OUT13_0 |                                                                                                                                                      |

Table 86. CR6 signals description (continued)

| Bit | Name    | Description                                                                                                                                          |
|-----|---------|------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7   | OUT14_3 | OUT14 Configuration Bits: high-side Driver OUT14 Configuration<br>For OUT14 bits configuration see <a href="#">Table 84: OUTx Configuration bits</a> |
| 6   | OUT14_2 |                                                                                                                                                      |
| 5   | OUT14_1 |                                                                                                                                                      |
| 4   | OUT14_0 |                                                                                                                                                      |
| 3   | OUT15_3 | OUT15 Configuration Bits: high-side Driver OUT15 Configuration<br>For OUT15 bits configuration see <a href="#">Table 84: OUTx Configuration bits</a> |
| 2   | OUT15_2 |                                                                                                                                                      |
| 1   | OUT15_1 |                                                                                                                                                      |
| 0   | OUT15_0 |                                                                                                                                                      |

#### 7.4.7 Control Register CR7 (0x07)

Table 87. Control Register CR7

|          | 23       | 22       | 21 | 20       | 19       | 18       | 17       | 16       | 15        | 14       | 13 | 12 | 11 | 10 | 9 | 8        | 7        | 6        | 5     | 4        | 3        | 2        | 1        | 0        |
|----------|----------|----------|----|----------|----------|----------|----------|----------|-----------|----------|----|----|----|----|---|----------|----------|----------|-------|----------|----------|----------|----------|----------|
| Bit name | OUT1_OCR | Reserved |    | OUT4_OCR | OUT5_OCR | OUT6_OCR | OUT7_OCR | OUT8_OCR | OUTHS_OCR | Reserved |    |    |    |    |   | OCR_FREQ | OUT5_OC1 | OUT5_OC0 | CM_EN | Reserved | CM_SEL_3 | CM_SEL_2 | CM_SEL_1 | CM_SEL_0 |
| Reset    | 0        | 0        | 0  | 0        | 0        | 0        | 0        | 0        | 0         | 0        | 0  | 0  | 0  | 0  | 0 | 0        | 0        | 0        | 1     | 0        | 0        | 0        | 0        | 0        |
| Access   | R/W      |          |    |          |          |          |          |          |           |          |    |    |    |    |   |          |          |          |       |          |          |          |          |          |

Table 88. CR7 signals description

| Bit   | Name      | Description                                                                                                               |
|-------|-----------|---------------------------------------------------------------------------------------------------------------------------|
| 23    | OUT1_OCR  | Overcurrent recovery for OUT1<br>0: overcurrent recovery is turned off (default)<br>1: overcurrent recovery is turned on  |
| 22:21 | Reserved  | —                                                                                                                         |
| 20    | OUT4_OCR  | Overcurrent recovery for OUTx<br>0: overcurrent recovery is turned off (default)<br>1: overcurrent recovery is turned on  |
| 19    | OUT5_OCR  |                                                                                                                           |
| 18    | OUT6_OCR  |                                                                                                                           |
| 17    | OUT7_OCR  |                                                                                                                           |
| 16    | OUT8_OCR  | Overcurrent recovery for OUTHS<br>0: overcurrent recovery is turned off (default)<br>1: overcurrent recovery is turned on |
| 15    | OUTHS_OCR |                                                                                                                           |
| 14:9  | Reserved  | —                                                                                                                         |

Table 88. CR7 signals description (continued)

| Bit | Name     | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |  |
|-----|----------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--|
| 8   | OCR_FREQ | Overcurrent recovery frequency<br>0: freq0 (default)<br>1: freq1                                                                                                                                                                                                                                                                                                                                                                                                             |  |
| 7   | OUT5_OC1 | Overcurrent Threshold for OUT5<br>00: IOC5_3 overcurrent threshold 3 (default)                                                                                                                                                                                                                                                                                                                                                                                               |  |
| 6   | OUT5_OC0 | 01: IOC5_1 overcurrent threshold 1<br>10: IOC5_2 overcurrent threshold 2<br>11: IOC5_3 overcurrent threshold 3                                                                                                                                                                                                                                                                                                                                                               |  |
| 5   | CM_EN    | Current monitor:<br>0: off (3-state)<br>1: on (default)                                                                                                                                                                                                                                                                                                                                                                                                                      |  |
| 4   | Reserved | —                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |  |
| 3   | CM_SEL_3 | Current Monitor Select Bits.<br>A current image of the selected binary coded output is multiplexed to the CM output. If a corresponding output does not exist, the current monitor is deactivated.<br>0000: OUT1<br>0001: invalid configuration<br>0010: invalid configuration<br>0011: OUT4<br>0100: OUT5<br>0101: OUT6<br>0110: OUT7<br>0111: OUT8<br>1000: OUT9<br>1001: OUT10<br>1010: OUT11<br>1011: OUT12<br>1100: OUT13<br>1101: OUT14<br>1110: OUT15<br>1111: OUT_HS |  |
| 2   | CM_SEL_2 |                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |  |
| 1   | CM_SEL_1 |                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |  |
| 0   | CM_SEL_0 |                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |  |
|     |          |                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |  |

## 7.4.8 Control Register CR8 (0x08)

Table 89. Control Register CR8

|          | 23              | 22       | 21 | 20 | 19              | 18              | 17              | 16              | 15              | 14               | 13      | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----------|-----------------|----------|----|----|-----------------|-----------------|-----------------|-----------------|-----------------|------------------|---------|----|----|----|---|---|---|---|---|---|---|---|---|---|
| Bit name | OUT1_OCR_THX_EN | Reserved |    |    | OUT4_OCR_THX_EN | OUT5_OCR_THX_EN | OUT6_OCR_THX_EN | OUT7_OCR_THX_EN | OUT8_OCR_THX_EN | OUTHS_OCR_THX_EN | Resrved |    |    |    |   |   |   |   |   |   |   |   |   |   |
| Reset    | 1               | 1        | 1  | 1  | 1               | 1               | 1               | 1               | 1               | 0                | 0       | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Access   | R/W             |          |    |    |                 |                 |                 |                 |                 |                  |         |    |    |    |   |   |   |   |   |   |   |   |   |   |

Table 90. CR8 signals description

| Bit   | Name             | Description                                                                                                                                                                                                                                       |
|-------|------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 23    | OUT1_OCR_THX_EN  | Enable Overcurrent Recovery with Thermal Expiration for OUTx.<br>0: Overcurrent Recovery with Thermal Expiration is off<br>1: Overcurrent Recovery with Thermal Expiration is on (default)<br>The output is turned off after Thermal Expiration.  |
| 22:21 | Reserved         | —                                                                                                                                                                                                                                                 |
| 20    | OUT4_OCR_THX_EN  | Enable Overcurrent Recovery with Thermal Expiration for OUTx.<br>0: Overcurrent Recovery with Thermal Expiration is off<br>1: Overcurrent Recovery with Thermal Expiration is on (default)<br>The output is turned off after Thermal Expiration.  |
| 19    | OUT5_OCR_THX_EN  |                                                                                                                                                                                                                                                   |
| 18    | OUT6_OCR_THX_EN  |                                                                                                                                                                                                                                                   |
| 17    | OUT7_OCR_THX_EN  |                                                                                                                                                                                                                                                   |
| 16    | OUT8_OCR_THX_EN  |                                                                                                                                                                                                                                                   |
| 15    | OUTHS_OCR_THX_EN | Enable Overcurrent Recovery with Thermal Expiration for OUTHS.<br>0: Overcurrent Recovery with Thermal Expiration is off<br>1: Overcurrent Recovery with Thermal Expiration is on (default)<br>The output is turned off after Thermal Expiration. |
| 14:0  | Reserved         | —                                                                                                                                                                                                                                                 |

### 7.4.9 Control Register CR9 (0x09)

**Table 91. Control Register CR9**

|          | 23         | 22         | 21       | 20 | 19 | 18 | 17 | 16 | 15 | 14       | 13       | 12       | 11       | 10       | 9        | 8        | 7       | 6        | 5        | 4        | 3        | 2        | 1        | 0        |         |
|----------|------------|------------|----------|----|----|----|----|----|----|----------|----------|----------|----------|----------|----------|----------|---------|----------|----------|----------|----------|----------|----------|----------|---------|
| Bit name | OUT7_RDSON | OUT8_RDSON | Reserved |    |    |    |    |    |    | OUTHS_OL | OUT15_OL | OUT14_OL | OUT13_OL | OUT12_OL | OUT11_OL | OUT10_OL | OUT9_OL | OUTHS_OC | OUT15_OC | OUT14_OC | OUT13_OC | OUT12_OC | OUT11_OC | OUT10_OC | OUT9_OC |
| Reset    | 0          | 0          | 0        | 0  | 0  | 0  | 0  | 0  | 0  | 0        | 0        | 0        | 0        | 0        | 0        | 0        | 0       | 0        | 0        | 0        | 0        | 0        | 0        | 0        |         |
| Access   | R/W        |            |          |    |    |    |    |    |    |          |          |          |          |          |          |          |         |          |          |          |          |          |          |          |         |

**Table 92. CR9 signals description**

| Bit   | Name       | Description                                                                                                     |
|-------|------------|-----------------------------------------------------------------------------------------------------------------|
| 23    | OUT7_RDSON | Select Rdson for OUT7<br>0: $r_{on\_low}$ (default)<br>1: $r_{on\_high}$                                        |
| 22    | OUT8_RDSON | Select Rdson for OUT8<br>0: $r_{on\_low}$ (default)<br>1: $r_{on\_high}$                                        |
| 21:16 | Reserved   | —                                                                                                               |
| 15    | OUTHS_OL   | Open-load Threshold for OUTx<br>0: $I_{OLD1}$ ; high-current mode (default)<br>1: $I_{OLD1}$ ; low-current mode |
| 14    | OUT15_OL   |                                                                                                                 |
| 13    | OUT14_OL   |                                                                                                                 |
| 12    | OUT13_OL   |                                                                                                                 |
| 11    | OUT12_OL   |                                                                                                                 |
| 10    | OUT11_OL   |                                                                                                                 |
| 9     | OUT10_OL   |                                                                                                                 |
| 8     | OUT9_OL    |                                                                                                                 |
| 7     | OUTHS_OC   | Overcurrent Threshold for OUTx<br>0: $I_{OC}$ ; high-current mode (default)<br>1: $I_{OC}$ ; low-current mode   |
| 6     | OUT15_OC   |                                                                                                                 |
| 5     | OUT14_OC   |                                                                                                                 |
| 4     | OUT13_OC   |                                                                                                                 |
| 3     | OUT12_OC   |                                                                                                                 |
| 2     | OUT11_OC   |                                                                                                                 |
| 1     | OUT10_OC   |                                                                                                                 |
| 0     | OUT9_OC    |                                                                                                                 |

## 7.4.10 Control Register CR10 (0x0A)

Table 93. Control Register CR10

|          | 23     | 22     | 21     | 20       | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12  | 11     | 10     | 9      | 8      | 7           | 6       | 5       | 4      | 3      | 2      | 1      | 0      |
|----------|--------|--------|--------|----------|----|----|----|----|----|----|----|-----|--------|--------|--------|--------|-------------|---------|---------|--------|--------|--------|--------|--------|
| Bit name | DIAG_2 | DIAG_1 | DIAG_0 | Reserved |    |    |    |    |    |    | SD | SDS | COPT_3 | COPT_2 | COPT_1 | COPT_0 | H_OLTH_HIGH | OL_H1L2 | OL_H2L1 | SLEW_4 | SLEW_3 | SLEW_2 | SLEW_1 | SLEW_0 |
| Reset    | 1      | 1      | 1      | 0        | 0  | 1  | 1  | 1  | 0  | 0  | 0  | 0   | 1      | 1      | 1      | 1      | 0           | 0       | 0       | 0      | 0      | 0      | 0      | 0      |
| Access   | R/W    |        |        |          |    |    |    |    |    |    |    |     |        |        |        |        |             |         |         |        |        |        |        |        |

Table 94. CR10 signals description

| Bit   | Name        | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |
|-------|-------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 23    | DIAG_2      | Drain-source monitoring threshold for external H-bridge<br>000: V <sub>SCd1_HB</sub><br>001: V <sub>SCd2_HB</sub><br>010: V <sub>SCd3_HB</sub><br>011: V <sub>SCd4_HB</sub><br>100: V <sub>SCd5_HB</sub><br>101: V <sub>SCd6_HB</sub><br>110: V <sub>SCd7_HB</sub><br>111: V <sub>SCd7_HB</sub> (default)                                                                                                                                                                                                                      |
| 22    | DIAG_1      |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |
| 21    | DIAG_0      |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |
| 20:14 | Reserved    |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |
| 13    | SD          | Slow decay                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |
| 12    | SDS         | Slow decay single                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |
| 11    | COPT_3      | Cross current protection time<br>0000: not allowed<br>0001: tccp <sub>0001</sub><br>0010: tccp <sub>0010</sub><br>0011: tccp <sub>0011</sub><br>0100: tccp <sub>0100</sub><br>0101: tccp <sub>0101</sub><br>0110: tccp <sub>0110</sub><br>0111: tccp <sub>0111</sub><br>1000: tccp <sub>1000</sub><br>1001: tccp <sub>1001</sub><br>1010: tccp <sub>1010</sub><br>1011: tccp <sub>1011</sub><br>1100: tccp <sub>1100</sub><br>1101: tccp <sub>1101</sub><br>1110: tccp <sub>1110</sub><br>1111: tccp <sub>1111</sub> (default) |
| 10    | COPT_2      |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |
| 9     | COPT_1      |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |
| 8     | COPT_0      |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |
| 7     | H_OLTH_HIGH | H-bridge OL high threshold (5/6 * V <sub>S</sub> ) select                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |

Table 94. CR10 signals description (continued)

| Bit | Name    | Description                                                                                                             |
|-----|---------|-------------------------------------------------------------------------------------------------------------------------|
| 6   | OL_H1L2 | Test open-load condition between H1 and L2                                                                              |
| 5   | OL_H2L1 | Test open-load condition between H2 and L1                                                                              |
| 4   | SLEW_4  | Binary coded slew rate of H-bridge (bit0 = LSB; bit4 = MSB)<br>00000: Control disabled (default)<br>11111: $I_{GHxmax}$ |
| 3   | SLEW_3  |                                                                                                                         |
| 2   | SLEW_2  |                                                                                                                         |
| 1   | SLEW_1  |                                                                                                                         |
| 0   | SLEW_0  |                                                                                                                         |

#### 7.4.11 Control Register CR11 (0x0B)

Table 95. Control Register CR11

|          | 23       | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----------|----------|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| Bit name | Reserved |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| Reset    | 0        | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 |
| Access   | R/W      |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |

Table 96. CR11 signals description

| Bit  | Name     | Description |
|------|----------|-------------|
| 23:0 | Reserved | —           |

#### 7.4.12 Control Register CR12 (0x0C)

Table 97. Control Register CR12

|          | 23          | 22          | 21          | 20          | 19          | 18          | 17          | 16          | 15          | 14          | 13          | 12          | 11          | 10          | 9           | 8           | 7           | 6           | 5            | 4            | 3        | 2 | 1 | 0 |
|----------|-------------|-------------|-------------|-------------|-------------|-------------|-------------|-------------|-------------|-------------|-------------|-------------|-------------|-------------|-------------|-------------|-------------|-------------|--------------|--------------|----------|---|---|---|
| Bit name | PMW1_FREQ_1 | PMW1_FREQ_0 | PMW2_FREQ_1 | PMW2_FREQ_0 | PMW3_FREQ_1 | PMW3_FREQ_0 | PMW4_FREQ_1 | PMW4_FREQ_0 | PMW5_FREQ_1 | PMW5_FREQ_0 | PMW6_FREQ_1 | PMW6_FREQ_0 | PMW7_FREQ_1 | PMW7_FREQ_0 | PMW8_FREQ_1 | PMW8_FREQ_0 | PMW9_FREQ_1 | PMW9_FREQ_0 | PMW10_FREQ_1 | PMW10_FREQ_0 | Reserved |   |   |   |
| Reset    | 0           | 0           | 0           | 0           | 0           | 0           | 0           | 0           | 0           | 0           | 0           | 0           | 0           | 0           | 0           | 0           | 0           | 0           | 0            | 0            | 0        | 0 | 0 | 0 |
| Access   | R/W         |             |             |             |             |             |             |             |             |             |             |             |             |             |             |             |             |             |              |              |          |   |   |   |

Table 98. CR12 signals description

| Bit | Name        | Description                                                                                                                     |
|-----|-------------|---------------------------------------------------------------------------------------------------------------------------------|
| 23  | PMW1_FREQ_1 | Frequency of PWM channel PWM1<br>00: $f_{PWMx}(00)$ (default)<br>01: $f_{PWMx}(01)$<br>10: $f_{PWMx}(10)$<br>11: $f_{PWMx}(11)$ |
| 22  | PMW1_FREQ_0 |                                                                                                                                 |
| 21  | PMW2_FREQ_1 | Frequency of PWM channel PWM2<br>00: $f_{PWMx}(00)$ (default)<br>01: $f_{PWMx}(01)$<br>10: $f_{PWMx}(10)$<br>11: $f_{PWMx}(11)$ |
| 20  | PMW2_FREQ_0 |                                                                                                                                 |
| 19  | PMW3_FREQ_1 | Frequency of PWM channel PWM3<br>00: $f_{PWMx}(00)$ (default)<br>01: $f_{PWMx}(01)$<br>10: $f_{PWMx}(10)$<br>11: $f_{PWMx}(11)$ |
| 18  | PMW3_FREQ_0 |                                                                                                                                 |
| 17  | PMW4_FREQ_1 | Frequency of PWM channel PWM4<br>00: $f_{PWMx}(00)$ (default)<br>01: $f_{PWMx}(01)$<br>10: $f_{PWMx}(10)$<br>11: $f_{PWMx}(11)$ |
| 16  | PMW4_FREQ_0 |                                                                                                                                 |
| 15  | PMW5_FREQ_1 | Frequency of PWM channel PWM5<br>00: $f_{PWMx}(00)$ (default)<br>01: $f_{PWMx}(01)$<br>10: $f_{PWMx}(10)$<br>11: $f_{PWMx}(11)$ |
| 14  | PMW5_FREQ_0 |                                                                                                                                 |
| 13  | PMW6_FREQ_1 | Frequency of PWM channel PWM6<br>00: $f_{PWMx}(00)$ (default)<br>01: $f_{PWMx}(01)$<br>10: $f_{PWMx}(10)$<br>11: $f_{PWMx}(11)$ |
| 12  | PMW6_FREQ_0 |                                                                                                                                 |
| 11  | PMW7_FREQ_1 | Frequency of PWM channel PWM7<br>00: $f_{PWMx}(00)$ (default)<br>01: $f_{PWMx}(01)$<br>10: $f_{PWMx}(10)$<br>11: $f_{PWMx}(11)$ |
| 10  | PMW7_FREQ_0 |                                                                                                                                 |
| 9   | PMW8_FREQ_1 | Frequency of PWM channel PWM8<br>00: $f_{PWMx}(00)$ (default)<br>01: $f_{PWMx}(01)$<br>10: $f_{PWMx}(10)$<br>11: $f_{PWMx}(11)$ |
| 8   | PMW8_FREQ_0 |                                                                                                                                 |

Table 98. CR12 signals description (continued)

| Bit | Name         | Description                                                                                                                     |
|-----|--------------|---------------------------------------------------------------------------------------------------------------------------------|
| 7   | PMW9_FREQ_1  | Frequency of PWM channel PWM9<br>00: $f_{PWMx}(00)$ (default)<br>01: $f_{PWMx}(01)$<br>10: $f_{PWMx}(10)$<br>11: $f_{PWMx}(11)$ |
| 6   | PMW9_FREQ_0  |                                                                                                                                 |
| 5   | PMW10_FREQ_1 |                                                                                                                                 |
| 4   | PMW10_FREQ_0 |                                                                                                                                 |
| 3:0 | Reserved     | —                                                                                                                               |

### 7.4.13 Control Register CR13 (0x0D) to CR17 (0x11)

Table 99. Control Register CR13 to CR17

|          | 23       | 22 | 21        | 20        | 19        | 18        | 17        | 16        | 15        | 14        | 13        | 12        | 11       | 10 | 9         | 8         | 7         | 6         | 5         | 4         | 3         | 2         | 1         | 0         |
|----------|----------|----|-----------|-----------|-----------|-----------|-----------|-----------|-----------|-----------|-----------|-----------|----------|----|-----------|-----------|-----------|-----------|-----------|-----------|-----------|-----------|-----------|-----------|
| Bit name | Reserved |    | PWMx_DC_9 | PWMx_DC_8 | PWMx_DC_7 | PWMx_DC_6 | PWMx_DC_5 | PWMx_DC_4 | PWMx_DC_3 | PWMx_DC_2 | PWMx_DC_1 | PWMx_DC_0 | Reserved |    | PWMy_DC_9 | PWMy_DC_8 | PWMy_DC_7 | PWMy_DC_6 | PWMy_DC_5 | PWMy_DC_4 | PWMy_DC_3 | PWMy_DC_2 | PWMy_DC_1 | PWMy_DC_0 |
| Reset    | 0        | 0  | 0         | 0         | 0         | 0         | 0         | 0         | 0         | 0         | 0         | 0         | 0        | 0  | 0         | 0         | 0         | 0         | 0         | 0         | 0         | 0         | 0         | 0         |
| Access   | R/W      |    |           |           |           |           |           |           |           |           |           |           |          |    |           |           |           |           |           |           |           |           |           |           |

Where:

$$x = 1 + (z * 2), z = 0 \text{ to } 4$$

$$y = 2 + (z * 2), z = 0 \text{ to } 4$$

Table 100. CR13 to CR17 signals description

| Bit   | Name     | Description |
|-------|----------|-------------|
| 23:22 | Reserved | —           |

Table 100. CR13 to CR17 signals description (continued)

| Bit   | Name      | Description                                                                                                                                                                                               |
|-------|-----------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 21    | PWMx_DC_9 | Binary coded on-dutycycle of PWM channel PWMx (bit12 = LSB; bit21 = MSB)<br>00 0000 0000: duty cycle 0% (default)<br>xx xxxx xxxx: duty cycle 100%/1023 x register value<br>11 1111 1111: duty cycle 100% |
| 20    | PWMx_DC_8 |                                                                                                                                                                                                           |
| 19    | PWMx_DC_7 |                                                                                                                                                                                                           |
| 18    | PWMx_DC_6 |                                                                                                                                                                                                           |
| 17    | PWMx_DC_5 |                                                                                                                                                                                                           |
| 16    | PWMx_DC_4 |                                                                                                                                                                                                           |
| 15    | PWMx_DC_3 |                                                                                                                                                                                                           |
| 14    | PWMx_DC_2 |                                                                                                                                                                                                           |
| 13    | PWMx_DC_1 |                                                                                                                                                                                                           |
| 12    | PWMx_DC_0 |                                                                                                                                                                                                           |
| 11:10 | Reserved  | —                                                                                                                                                                                                         |
| 9     | PWMy_DC_9 | Binary coded on-dutycycle of PWM channel PWMy (bit0 = LSB; bit9 = MSB)<br>00 0000 0000: duty cycle 0% (default)<br>xx xxxx xxxx: duty cycle 100%/1023 x register value<br>11 1111 1111: Duty cycle 100%   |
| 8     | PWMy_DC_8 |                                                                                                                                                                                                           |
| 7     | PWMy_DC_7 |                                                                                                                                                                                                           |
| 6     | PWMy_DC_6 |                                                                                                                                                                                                           |
| 5     | PWMy_DC_5 |                                                                                                                                                                                                           |
| 4     | PWMy_DC_4 |                                                                                                                                                                                                           |
| 3     | PWMy_DC_3 |                                                                                                                                                                                                           |
| 2     | PWMy_DC_2 |                                                                                                                                                                                                           |
| 1     | PWMy_DC_1 |                                                                                                                                                                                                           |
| 0     | PWMy_DC_0 |                                                                                                                                                                                                           |

#### 7.4.14 Control Register CR18 (0x12) to CR22 (0x16)

Table 101. Control Register CR18

|          | 23       | 22               | 21          | 20          | 19          | 18          | 17          | 16          | 15          | 14          | 13          | 12          | 11       | 10               | 9           | 8           | 7           | 6           | 5           | 4           | 3           | 2           | 1           | 0           |
|----------|----------|------------------|-------------|-------------|-------------|-------------|-------------|-------------|-------------|-------------|-------------|-------------|----------|------------------|-------------|-------------|-------------|-------------|-------------|-------------|-------------|-------------|-------------|-------------|
| Bit name | Reserved | OUTx_AUTOCOMP_EN | OUTx_VLED_9 | OUTx_VLED_8 | OUTx_VLED_7 | OUTx_VLED_6 | OUTx_VLED_5 | OUTx_VLED_4 | OUTx_VLED_3 | OUTx_VLED_2 | OUTx_VLED_1 | OUTx_VLED_0 | Reserved | OUTy_AUTOCOMP_EN | OUTy_VLED_9 | OUTy_VLED_8 | OUTy_VLED_7 | OUTy_VLED_6 | OUTy_VLED_5 | OUTy_VLED_4 | OUTy_VLED_3 | OUTy_VLED_2 | OUTy_VLED_1 | OUTy_VLED_0 |
| Reset    | 0        | 0                | 0           | 0           | 0           | 0           | 0           | 0           | 0           | 0           | 0           | 0           | 0        | 0                | 0           | 0           | 0           | 0           | 0           | 0           | 0           | 0           | 0           | 0           |
| Access   | R/W      |                  |             |             |             |             |             |             |             |             |             |             |          |                  |             |             |             |             |             |             |             |             |             |             |

Where:

$$x = 7 + (z * 2), z = 0 \text{ to } 4$$

$$y = 8 + (z * 2), z = 0 \text{ to } 4$$

**Table 102. CR18 to CR22 signals description**

| Bit | Name             | Description                                                                                                                                                                                                                                                                       |
|-----|------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 23  | Reserved         | —                                                                                                                                                                                                                                                                                 |
| 22  | OUTx_AUTOCOMP_EN | Setting this bit to '1' enables the automatic $V_S$ compensation for OUTx                                                                                                                                                                                                         |
| 21  | OUTx_VLED_9      | Binary coded nominal LED voltage of OUTx (bit12 = LSB; bit21 = MSB)<br>00 0000 0000: $V_{LED} = 0 \text{ V}$ (default)<br>xx xxxx xxxx: $V_{LED} = V_{AINVS} / 1023 \times \text{register value}$<br>01 1101 0000: $V_{LED} = V_{AINVS}$<br>$V_{LED}$ is clamped at 10 V (0x1D0h) |
| 20  | OUTx_VLED_8      |                                                                                                                                                                                                                                                                                   |
| 19  | OUTx_VLED_7      |                                                                                                                                                                                                                                                                                   |
| 18  | OUTx_VLED_6      |                                                                                                                                                                                                                                                                                   |
| 17  | OUTx_VLED_5      |                                                                                                                                                                                                                                                                                   |
| 16  | OUTx_VLED_4      |                                                                                                                                                                                                                                                                                   |
| 15  | OUTx_VLED_3      |                                                                                                                                                                                                                                                                                   |
| 14  | OUTx_VLED_2      |                                                                                                                                                                                                                                                                                   |
| 13  | OUTx_VLED_1      |                                                                                                                                                                                                                                                                                   |
| 12  | OUTx_VLED_0      |                                                                                                                                                                                                                                                                                   |
| 11  | Reserved         | —                                                                                                                                                                                                                                                                                 |
| 10  | OUTy_AUTOCOMP_EN | Setting this bit to '1' enables the automatic $V_S$ compensation for OUTy                                                                                                                                                                                                         |
| 9   | OUTy_VLED_9      | Binary coded nominal LED voltage of OUTy (bit0 = LSB; bit9 = MSB)<br>00 0000 0000: $V_{LED} = 0 \text{ V}$ (default)<br>xx xxxx xxxx: $V_{LED} = V_{AINVS} / 1023 \times \text{register value}$<br>01 1101 0000: $V_{LED} = V_{AINVS}$<br>$V_{LED}$ is clamped at 10 V (0x1D0h)   |
| 8   | OUTy_VLED_8      |                                                                                                                                                                                                                                                                                   |
| 7   | OUTy_VLED_7      |                                                                                                                                                                                                                                                                                   |
| 6   | OUTy_VLED_6      |                                                                                                                                                                                                                                                                                   |
| 5   | OUTy_VLED_5      |                                                                                                                                                                                                                                                                                   |
| 4   | OUTy_VLED_4      |                                                                                                                                                                                                                                                                                   |
| 3   | OUTy_VLED_3      |                                                                                                                                                                                                                                                                                   |
| 2   | OUTy_VLED_2      |                                                                                                                                                                                                                                                                                   |
| 1   | OUTy_VLED_1      |                                                                                                                                                                                                                                                                                   |
| 0   | OUTy_VLED_0      |                                                                                                                                                                                                                                                                                   |

### 7.4.15 Control Register CR34 (0x22)

Table 103. Control Register CR34

|          | 23       | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2      | 1    | 0     |
|----------|----------|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|--------|------|-------|
| Bit name | Reserved |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   | CP_OFF | ICMP | WD_EN |
| Reset    | 0        | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0      | 0    | 1     |
| Access   | R/W      |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |        |      |       |

Table 104. CR34 signals description

| Bit  | Name     | Description                                                                                                                                                                                                                                            |
|------|----------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 23:3 | Reserved | —                                                                                                                                                                                                                                                      |
| 2    | CP_OFF   | Charge pump control<br>0: Enabled; charge pump on in active mode (default)<br>1: Disabled; charge pump off in active mode<br>setting CP_OFF = 1 is only possible when CP_OFF_EN = 1                                                                    |
| 1    | ICMP     | V1 load current supervision<br>0: Enabled; Watchdog is disabled in V1 Standby when $I_{V1} < I_{CMP}$ (default)<br>1: Disabled; watchdog is disabled upon transition into V1_standby mode<br>setting ICMP = 1 is only possible when ICMP_config_en = 1 |
| 0    | WD_EN    | Watchdog Enable<br>0: Watchdog disabled<br>1: Watchdog enabled (default)                                                                                                                                                                               |

### 7.4.16 Configuration Register (0x3F)

Table 105. Configuration Register

|          | 23        | 22            | 21        | 20         | 19       | 18 | 17             | 16           | 15          | 14          | 13      | 12       | 11      | 10        | 9        | 8       | 7         | 6             | 5           | 4         | 3        | 2 | 1 | 0    |
|----------|-----------|---------------|-----------|------------|----------|----|----------------|--------------|-------------|-------------|---------|----------|---------|-----------|----------|---------|-----------|---------------|-------------|-----------|----------|---|---|------|
| Bit name | WU_CONFIG | LIN_WU_CONFIG | LIN_HS_EN | TSD_CONFIG | Reserved | DM | ICMP_CONFIG_EN | WD_CONFIG_EN | MASK_OL_HS1 | MASK_OL_LS1 | MASK_TW | Reserved | MASK_OL | MASK_SPIE | MASK_PLE | MASK_GW | CP_OFF_EN | CP_LOW_CONFIG | CP_DITH_DIS | FS_FORCED | Reserved |   |   | TRIG |
| Reset    | 1         | 0             | 0         | 0          | 0        | 0  | 0              | 0            | 0           | 0           | 0       | 0        | 0       | 0         | 0        | 0       | 0         | 0             | 0           | 0         | 0        | 0 | 0 | 1    |
| Access   | R/W       |               |           |            |          |    |                |              |             |             |         |          |         |           |          |         |           |               |             |           |          |   |   |      |

Table 106. CR signals description

| Bit | Name           | Description                                                                                                                                                                                                                                                         |
|-----|----------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 23  | WU_CONFIG      | Configuration of input pin WU<br>Input configured as wake-up input<br>0: WU configured as wake-up input<br>1: WU configured for input voltage measurement (default)                                                                                                 |
| 22  | LIN_WU_CONFIG  | Configuration of LIN wake-up behaviour<br>0: wake up at recessive - dominant - recessive with $t_{dom} > t_{dom\_LIN}$ (default)<br>(according to LIN 2.2a and Hardware Requirements for Transceivers version 1.3)<br>1: wake up at recessive - dominant transition |
| 21  | LIN_HS_EN      | Configuration of LIN transceiver bit rate<br>0: LIN transceiver in normal communication mode (20kbit/s) (default)<br>1: LIN transceiver in high speed mode for fast Flashing (115kbit/s)                                                                            |
| 20  | TSD_CONFIG     | Configuration of thermal shutdown behaviour<br>0: in case of TSD1 all power stages are switched off (default)<br>1: selective shut down of power stage cluster                                                                                                      |
| 19  | Reserved       | —                                                                                                                                                                                                                                                                   |
| 18  | DM             | H-bridge configuration<br>0: single motor mode (default)<br>1: reserved                                                                                                                                                                                             |
| 17  | ICMP_CONFIG_EN | ICMP configuration Enable<br>0: writing ICMP = 1 is blocked (writing ICMP=0 is possible); (default)<br>1: writing ICMP = 1 is possible with next SPI command<br>bit is automatically reset to 0 after next SPI command                                              |
| 16  | WD_CONFIG_EN   | Watchdog configuration Enable<br>0: writing to WD Configuration (CR2 [0:1] is blocked (default)<br>1: writing to WD Configuration Bits is possible with next SPI command<br>bit is automatically reset to 0 after next SPI command                                  |
| 15  | MASK_OL_HS1    | Mask Open-load HS1<br>0: Open-load condition at HS1 is not masked (default)<br>1: Open-load condition at HS1 is masked<br>i.e. it is reported as a Functional Error (GSB bit 3) but not as a Global Error (GSB bit 7)                                               |
| 14  | MASK_OL_LS1    | Mask Open-load LS1<br>0: Open-load condition at LS1 is not masked (default)<br>1: Open-load condition at LS1 is masked<br>i.e. it is reported as a Functional Error (GSB bit 3) but not as a Global Error (GSB bit 7)                                               |
| 13  | MASK_TW        | Mask Thermal Warning<br>0: Thermal warning is not masked (default)<br>1: Thermal warning is masked<br>i.e. it is reported as a Global Warning (GSB bit 1) but not as a Global Error (GSB bit 7)                                                                     |

Table 106. CR signals description (continued)

| Bit | Name          | Description                                                                                                                                                                                                                                                                  |
|-----|---------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 12  | Reserved      | —                                                                                                                                                                                                                                                                            |
| 11  | MASK_OL       | Mask open-load<br>0: Open-load condition at all outputs are not masked (default)<br>1: Open-load condition at all outputs are masked<br>i.e. it is reported as a Functional Error (GSB bit 3) but not as a Global Error (GSB bit 7)                                          |
| 10  | MASK_SPIE     | Mask SPI error<br>0: SPI errors are not masked (default)<br>1: SPI errors are masked<br>i.e. reported as an SPI Error (GSB bit 5) but not as a Global Error (GSB bit 7)                                                                                                      |
| 9   | MASK_PLE      | Mask physical layer error<br>0: Physical Layer Errors are not masked (default)<br>1: Physical Layer Errors are masked<br>i.e. reported as a Physical Layer Error (GSB bit 4) but not as a Global Error (GSB bit 7)                                                           |
| 8   | MASK_GW       | Mask global warning<br>0: Global Warning conditions are not masked (default)<br>1: Global Warning conditions are masked<br>i.e. reported as a Global Warning (GSB bit 1) but not as a Global Error (GSB bit 7)                                                               |
| 7   | CP_OFF_EN     | Charge pump control enable<br>0: writing CP_OFF = 1 is blocked (writing CP_OFF = 0 is possible); (default)<br>1: writing CP_OFF = 1 is possible with next SPI command<br>Bit is automatically reset to 0 after next SPI command                                              |
| 6   | CP_LOW_CONFIG | Charge pump low configuration<br>0: CP_low (SR 2, bit 9) is latched and outputs are off until R&C; (default)<br>1: CP_low (SR 2, bit 9) is a 'live' bit; outputs are re-activated automatically upon recovery of the charge pump output voltage                              |
| 5   | CP_DITH_DIS   | Charge pump clock dithering<br>0: CP clock dithering is enabled; (default)<br>1: CP clock dithering is disabled                                                                                                                                                              |
| 4   | FS_FORCED     | Force LSx_FSO ON<br>LSx_FSO low-side outputs are forced ON (to allow diagnosis of the fail-safe path)<br>0: LSx_FSO outputs are controlled by the Fail-safe logic (default)<br>1: LSx_FSO outputs are forced ON and the device enters Fail-Safe mode; no NReset is generated |
| 3:1 | Reserved      | —                                                                                                                                                                                                                                                                            |
| 0   | TRIG          | Watchdog Trigger bit                                                                                                                                                                                                                                                         |

## 7.5 Status Registers

### 7.5.1 Status Register SR1 (0x31)

**Table 107. Status Register SR1 (0x31)**

|          | 23       | 22       | 21       | 20      | 19       | 18       | 17         | 16           | 15   | 14           | 13           | 12           | 11           | 10           | 9            | 8            | 7              | 6              | 5    | 4    | 3                      | 2               | 1      | 0    |
|----------|----------|----------|----------|---------|----------|----------|------------|--------------|------|--------------|--------------|--------------|--------------|--------------|--------------|--------------|----------------|----------------|------|------|------------------------|-----------------|--------|------|
| Bit name | Reserved | WU_STATE | Reserved | WU_WAKE | Reserved | WAKE_LIN | WAKE_TIMER | DEBUG_ACTIVE | V1UV | V1_RESTART_2 | V1_RESTART_1 | V1_RESTART_0 | WDFAIL_CNT_3 | WDFAIL_CNT_2 | WDFAIL_CNT_1 | WDFAIL_CNT_0 | DEVICE_STATE_1 | DEVICE_STATE_0 | TSD2 | TSD1 | FORCED_SLEEP_TSD2/V1SC | FORCED_SLEEP_WD | WDFAIL | VPOR |
| Access   | R/C      | R        |          |         | R/C      |          |            |              |      |              |              |              | R            |              |              |              |                |                |      | R/C  |                        |                 |        |      |

**Table 108. SR1 signals description**

| Bit | Name         | Description                                                                                                                                                                                                                                                                                                          |
|-----|--------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 23  | Reserved     | —                                                                                                                                                                                                                                                                                                                    |
| 22  | WU_STATE     | State of WU input<br>0: input level is low<br>1: input level is high<br>The bit shows the momentary status of WU and cannot be cleared (“Live bit”)<br>Note: The status is only valid if WU is configured as wake-up input in Configuration Register (0x3F). Otherwise this bit remains at his previous logic state. |
| 21  | Reserved     | —                                                                                                                                                                                                                                                                                                                    |
| 20  | WU_WAKE      | Wake-up by WU: shows wake up source<br>1: wake-up<br>Bits are latched until a “Read and clear” command                                                                                                                                                                                                               |
| 19  | Reserved     | —                                                                                                                                                                                                                                                                                                                    |
| 18  | WAKE_LIN     | Wake-up by LIN: shows wake up source<br>1: wake-up<br>Bits are latched until a “Read and clear” command                                                                                                                                                                                                              |
| 17  | WAKE_TIMER   | Wake-up by Timer: shows wake up source<br>1: wake-up<br>Bits are latched until a “Read and clear” command                                                                                                                                                                                                            |
| 16  | DEBUG_ACTIVE | Debug Mode Active: indicates Device is in Debug mode<br>1: Debug mode<br>The bit shows the momentary status and cannot be cleared (“Live bit”)                                                                                                                                                                       |

Table 108. SR1 signals description (continued)

| Bit | Name                   | Description                                                                                                                                                                                                                                                                                                                                                                                                           |
|-----|------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15  | V1UV                   | Indicates undervoltage condition at voltage regulator V1 ( $V1 < V_{RTX}$ )<br>1: undervoltage<br>Bit is latched until a "Read and clear" command                                                                                                                                                                                                                                                                     |
| 14  | V1_RESTART_2           | Indicates the number of TSD2 events which caused a restart of voltage regulator V1<br>Bits cannot be cleared; counter will be cleared automatically if no additional TSD2 event occurs within 1 minute.                                                                                                                                                                                                               |
| 13  | V1_RESTART_1           |                                                                                                                                                                                                                                                                                                                                                                                                                       |
| 12  | V1_RESTART_0           |                                                                                                                                                                                                                                                                                                                                                                                                                       |
| 11  | WDFAIL_CNT_3           | Indicates number of subsequent watchdog failures.<br>Bits cannot be cleared; will be cleared with a valid watchdog trigger                                                                                                                                                                                                                                                                                            |
| 10  | WDFAIL_CNT_2           |                                                                                                                                                                                                                                                                                                                                                                                                                       |
| 9   | WDFAIL_CNT_1           |                                                                                                                                                                                                                                                                                                                                                                                                                       |
| 8   | WDFAIL_CNT_0           |                                                                                                                                                                                                                                                                                                                                                                                                                       |
| 7   | DEVICE_STATE_1         | State from which the device woke up                                                                                                                                                                                                                                                                                                                                                                                   |
| 6   | DEVICE_STATE_0         | 00: Active Mode after Read&Clear command or after Flash Mode state<br>01: Active mode after wake-up from V1_standby mode (before Read&Clear command)<br>10: Active Mode after Power-on or after wake-up from Vbat_standby Mode (before Read&Clear command)<br>11: Flash mode (LIN Flash mode)<br>Bit is latched until a "Read and clear" command<br>After a "read and clear access", the device state will be updated |
| 5   | TSD2                   | Thermal Shutdown 2 was reached<br>Bit is latched until a "Read and clear" command                                                                                                                                                                                                                                                                                                                                     |
| 4   | TSD1                   | Thermal Shutdown 1 was reached (Logical Or combination of all TSD1_CLx; see status register SR6).<br>This bit cannot be cleared directly. It is reset if the corresponding TSD1_CLx bits in SR6 are cleared.                                                                                                                                                                                                          |
| 3   | FORCED_SLEEP_TSD2/V1SC | Device entered Forced Vbat_standby mode due to:<br>– Thermal shutdown or<br>– Short circuit on V1 during startup<br>Bit is latched until a "Read and clear" command                                                                                                                                                                                                                                                   |
| 2   | FORCED_SLEEP_WD        | Device entered Forced Vbat_standby mode due to multiple watchdog failures<br>Bit is latched until a "Read and clear" command                                                                                                                                                                                                                                                                                          |
| 1   | WDFAIL                 | Watchdog failure<br>Bit is latched until a "Read and clear" command                                                                                                                                                                                                                                                                                                                                                   |
| 0   | VPOR                   | $V_S$ Power-on Reset threshold (VPOR) reached<br>Bit is latched until a "Read and clear" command                                                                                                                                                                                                                                                                                                                      |

## 7.5.2 Status Register SR2 (0x32)

**Table 109. Status Register SR2 (0x32)**

|          | 23           | 22          | 21           | 20       | 19 | 18 | 17 | 16 | 15 | 14        | 13        | 12        | 11        | 10          | 9           | 8      | 7  | 6    | 5      | 4      | 3        | 2        | 1        | 0     |       |
|----------|--------------|-------------|--------------|----------|----|----|----|----|----|-----------|-----------|-----------|-----------|-------------|-------------|--------|----|------|--------|--------|----------|----------|----------|-------|-------|
| Bit name | LIN_PERM_DOM | LIN_TXD_DOM | LIN_PERM_REC | Reserved |    |    |    |    |    | DSMON_HS2 | DSMON_HS1 | DSMON_LS2 | DSMON_LS1 | SPI_INV_CMD | SPI_SCK_CNT | CP_LOW | TW | V2SC | V2FAIL | V1FAIL | VSREG_EW | VSREG_OV | VSREG_UV | VS_OV | VS_UV |
| Access   | R/C          |             |              |          |    |    |    |    |    |           |           |           |           |             | R           | R/C    |    |      |        |        |          |          |          |       |       |

**Table 110. SR2 signals description**

| Bit   | Name         | Description                                                                                                                                                                                                                                                                                                                                   |
|-------|--------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 23    | LIN_PERM_DOM | LIN bus signal is dominant for $t > t_{dom(bus)}$<br>Bit is latched until a “Read and clear” command                                                                                                                                                                                                                                          |
| 22    | LIN_TXD_DOM  | TxDL pin is dominant for $t > t_{dom(TXDL)}$<br>The LIN transmitter is disabled until the bit is cleared<br>Bit is latched until a “Read and clear” command                                                                                                                                                                                   |
| 21    | LIN_PERM_REC | LIN bus signal does not follow TxDL within $t_{LIN}$<br>The LIN transmitter is disabled until the bit is cleared<br>Bit is latched until a “Read and clear” command                                                                                                                                                                           |
| 20:16 | Reserved     | —                                                                                                                                                                                                                                                                                                                                             |
| 15    | DSMON_HS2    | Drain-Source Monitoring<br>‘1’ indicates a short-circuit or open-load condition was detected<br>Bit is latched until a “Read and clear” command                                                                                                                                                                                               |
| 14    | DSMON_HS1    |                                                                                                                                                                                                                                                                                                                                               |
| 13    | DSMON_LS2    |                                                                                                                                                                                                                                                                                                                                               |
| 12    | DSMON_LS1    |                                                                                                                                                                                                                                                                                                                                               |
| 11    | SPI_INV_CMD  | Invalid SPI command<br>‘1’ indicates one of the following conditions was detected:<br>– access to undefined address<br>– Write operation to Status Register<br>– DI stuck at ‘0’ or ‘1’<br>– CSN timeout<br>– Parity failure<br>– invalid or undefined setting<br>The SPI frame is ignored<br>Bit is latched until a “Read and clear” command |
| 10    | SPI_SCK_CNT  | SPI clock counter<br>‘1’ indicates an SPI frame with wrong number of CLK cycles was detected<br>Bit is latched until a valid SPI frame                                                                                                                                                                                                        |
| 9     | CP_LOW       | Charge pump voltage low<br>‘1’ indicates that the charge pump voltage is too low<br>Bit is latched until a “Read and clear” command                                                                                                                                                                                                           |

Table 110. SR2 signals description (continued)

| Bit | Name     | Description                                                                                                                                                                                                                                                                                                   |
|-----|----------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 8   | TW       | Thermal warning<br>'1' indicates the temperature has reached the thermal warning threshold (logical OR combination of bits TW_CLx in SR6)<br>Bit is latched until a "Read and clear" command                                                                                                                  |
| 7   | V2SC     | V2 short circuit detection<br>'1' indicates a short circuit to GND condition of V2 at turn-on of the regulator ( $V2 < V2\_fail$ for $t > t_{V2\_short}$ )<br>Bit is latched until a "Read and clear" command                                                                                                 |
| 6   | V2FAIL   | V2 failure detection<br>'1' indicates a V2 fail event occurred since last readout ( $V2 < V2\_fail$ for $t > t_{V2\_fail}$ )<br>Bit is latched until a "Read and clear" command                                                                                                                               |
| 5   | V1FAIL   | V1 failure detection<br>'1' indicates a V1 fail event occurred since last readout ( $V1 < V1\_fail$ for $t > t_{V1\_fail}$ )<br>Bit is latched until a "Read and clear" command                                                                                                                               |
| 4   | VSREG_EW | VSREG early warning<br>'1' indicates the voltage at VSREG has reached the early warning threshold (configured in CR3)<br>In Active mode, an interrupt pulse is generated at NINT<br>Bit is latched until a "Read and clear" command.<br>Bit needs a "Read and clear" command after wake-up from standby modes |
| 3   | VSREG_OV | VSREG overvoltage<br>'1' indicates the voltage at VSREG has reached the overvoltage threshold<br>Bit is latched until a "Read and clear" command                                                                                                                                                              |
| 2   | VSREG_UV | VSREG undervoltage<br>'1' indicates the voltage at VSREG has reached the undervoltage threshold<br>Bit is latched until a "Read and clear" command                                                                                                                                                            |
| 1   | VS_OV    | VS overvoltage<br>'1' indicates the voltage at VS has reached the overvoltage threshold<br>Bit is latched until a "Read and clear" command                                                                                                                                                                    |
| 0   | VS_UV    | VS undervoltage<br>'1' indicates the voltage at VS has reached the undervoltage threshold<br>Bit is latched until a "Read and clear" command                                                                                                                                                                  |

### 7.5.3 Status Register SR3 (0x33)

**Table 111. Status Register SR3 (0x33)**

|          | 23               | 22               | 21       | 20 | 19 | 18 | 17               | 16               | 15               | 14               | 13               | 12               | 11            | 10            | 9       | 8        | 7        | 6        | 5        | 4        | 3        | 2              | 1         | 0         |
|----------|------------------|------------------|----------|----|----|----|------------------|------------------|------------------|------------------|------------------|------------------|---------------|---------------|---------|----------|----------|----------|----------|----------|----------|----------------|-----------|-----------|
| Bit name | OUT1_HS_OC_TH_EX | OUT1_LS_OC_TH_EX | Reserved |    |    |    | OUT4_HS_OC_TH_EX | OUT4_LS_OC_TH_EX | OUT5_HS_OC_TH_EX | OUT5_LS_OC_TH_EX | OUT6_HS_OC_TH_EX | OUT6_LS_OC_TH_EX | OUT7_OC_TH_EX | OUT8_OC_TH_EX | OUT9_OC | OUT10_OC | OUT11_OC | OUT12_OC | OUT13_OC | OUT14_OC | OUT15_OC | OUTHS_OC_TH_EX | LS2FSO_OC | LS1FSO_OC |
| Access   | R/C              |                  |          |    |    |    |                  |                  |                  |                  |                  |                  |               |               |         |          |          |          |          |          |          |                |           |           |

**Table 112. SR3 signals description**

| Bit   | Name             | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |
|-------|------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 23    | OUT1_HS_OC_TH_EX | Overcurrent shutdown                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |
| 22    | OUT1_LS_OC_TH_EX | <p>'1' indicates the output was shut down due to overcurrent condition.</p> <p>If Overcurrent Recovery is disabled (CR7: OUTx_OCR = 0):<br/>Bit is set upon overcurrent condition and output is turned off.</p> <p>If Overcurrent Recovery is enabled (CR7: OUTx_OCR = 1):<br/>In case of overcurrent condition this bit is not set. The output goes into Overcurrent Recovery mode and OUTx_OCR_alert in SR4 is set to '1'</p> <p>In case of Thermal Expiration enabled (CR8: OUTx_OCR_THx_en = 1):<br/>Bit is set after thermal expiration and output is turned off</p> <p>Bit is latched until a "Read and clear" command</p> |
| 21:18 | Reserved         | —                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |
| 17    | OUT4_HS_OC_TH_EX | Overcurrent shutdown                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |
| 16    | OUT4_LS_OC_TH_EX | <p>'1' indicates the output was shut down due to overcurrent condition.</p> <p>If Overcurrent Recovery is disabled (CR7: OUTx_OCR = 0):<br/>Bit is set upon overcurrent condition and output is turned off.</p> <p>If Overcurrent Recovery is enabled (CR7: OUTx_OCR = 1):<br/>In case of overcurrent condition this bit is not set. The output goes into Overcurrent Recovery mode and OUTx_OCR_alert in SR4 is set to '1'</p> <p>In case of Thermal Expiration enabled (CR8: OUTx_OCR_THx_en = 1):<br/>Bit is set after thermal expiration and output is turned off</p> <p>Bit is latched until a "Read and clear" command</p> |
| 15    | OUT5_HS_OC_TH_EX |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |
| 14    | OUT5_LS_OC_TH_EX |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |
| 13    | OUT6_HS_OC_TH_EX |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |
| 12    | OUT6_LS_OC_TH_EX |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |
| 11    | OUT7_OC_TH_EX    |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |
| 10    | OUT8_OC_TH_EX    |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |

Table 112. SR3 signals description (continued)

| Bit | Name           | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |
|-----|----------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 9   | OUT9_OC        | Overcurrent shutdown<br>'1' indicates the output was shut down due to overcurrent condition.<br>Bit is latched until a "Read and clear" command                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |
| 8   | OUT10_OC       |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |
| 7   | OUT11_OC       |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |
| 6   | OUT12_OC       |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |
| 5   | OUT13_OC       |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |
| 4   | OUT14_OC       |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |
| 3   | OUT15_OC       |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |
| 2   | OUTHS_OC_TH_EX | Overcurrent shutdown<br>'1' indicates the output was shut down due to overcurrent condition.<br>If Overcurrent Recovery is disabled (CR7: OUTx_OCR = 0):<br>Bit is set upon overcurrent condition and output is turned off.<br>If Overcurrent Recovery is enabled (CR7: OUTx_OCR = 1):<br>In case of overcurrent condition this bit is not set. The output goes into Overcurrent Recovery mode and OUTx_OCR_alert in SR4 is set to '1'<br>In case of Thermal Expiration enabled (CR8: OUTx_OCR_THx_en = 1):<br>Bit is set after thermal expiration and output is turned off<br>Bit is latched until a "Read and clear" command |
| 1   | LS2FSO_OC      | Overcurrent shutdown                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |
| 0   | LS1FSO_OC      | '1' indicates the output was shut down due to overcurrent condition.<br>Bit is latched until a "Read and clear" command                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |

#### 7.5.4 Status Register SR4 (0x34)

Table 113. Status Register SR4 (0x34)

|          | 23                | 22                | 21       | 20 | 19 | 18 | 17                | 16                | 15                | 14                | 13                | 12                | 11             | 10             | 9        | 8 | 7 | 6 | 5 | 4 | 3 | 2               | 1        | 0 |
|----------|-------------------|-------------------|----------|----|----|----|-------------------|-------------------|-------------------|-------------------|-------------------|-------------------|----------------|----------------|----------|---|---|---|---|---|---|-----------------|----------|---|
| Bit name | OUT1_HS_OCR_ALERT | OUT1_LS_OCR_ALERT | Reserved |    |    |    | OUT4_HS_OCR_ALERT | OUT4_LS_OCR_ALERT | OUT5_HS_OCR_ALERT | OUT5_LS_OCR_ALERT | OUT6_HS_OCR_ALERT | OUT6_LS_OCR_ALERT | OUT7_OCR_ALERT | OUT8_OCR_ALERT | Reserved |   |   |   |   |   |   | OUTHS_OCR_ALERT | Reserved |   |
| Access   | R                 |                   |          |    |    |    |                   |                   |                   |                   |                   |                   |                |                | R/C      |   |   |   |   |   |   | R               | R/C      |   |

Table 114. SR4 signals description

| Bit   | Name              | Description                                                                                                                                                    |
|-------|-------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 23    | OUT1_HS_OCR_ALERT | Autorecovery Alert<br>'1' indicates that the output reached the overcurrent threshold and is in autorecovery mode<br>Bit is not latched and cannot be cleared. |
| 22    | OUT1_LS_OCR_ALERT |                                                                                                                                                                |
| 21:18 | Reserved          | —                                                                                                                                                              |
| 17    | OUT4_HS_OCR_ALERT | Autorecovery Alert<br>'1' indicates that the output reached the overcurrent threshold and is in autorecovery mode<br>Bit is not latched and cannot be cleared. |
| 16    | OUT4_LS_OCR_ALERT |                                                                                                                                                                |
| 15    | OUT5_HS_OCR_ALERT |                                                                                                                                                                |
| 14    | OUT5_LS_OCR_ALERT |                                                                                                                                                                |
| 13    | OUT6_HS_OCR_ALERT |                                                                                                                                                                |
| 12    | OUT6_LS_OCR_ALERT |                                                                                                                                                                |
| 11    | OUT7_OCR_ALERT    |                                                                                                                                                                |
| 10    | OUT8_OCR_ALERT    |                                                                                                                                                                |
| 9:3   | Reserved          | —                                                                                                                                                              |
| 2     | OUTHS_OCR_ALERT   | Autorecovery Alert<br>'1' indicates that the output reached the overcurrent threshold and is in autorecovery mode<br>Bit is not latched and cannot be cleared. |
| 1:0   | Reserved          | —                                                                                                                                                              |

### 7.5.5 Status Register SR5 (0x35)

Table 115. Status Register SR5 (0x35)

|          | 23         | 22         | 21       | 20 | 19 | 18 | 17         | 16         | 15         | 14         | 13         | 12         | 11      | 10      | 9       | 8        | 7        | 6        | 5        | 4        | 3        | 2        | 1        | 0 |
|----------|------------|------------|----------|----|----|----|------------|------------|------------|------------|------------|------------|---------|---------|---------|----------|----------|----------|----------|----------|----------|----------|----------|---|
| Bit name | OUT1_HS_OL | OUT1_LS_OL | Reserved |    |    |    | OUT4_HS_OL | OUT4_LS_OL | OUT5_HS_OL | OUT5_LS_OL | OUT6_HS_OL | OUT6_LS_OL | OUT7_OL | OUT8_OL | OUT9_OL | OUT10_OL | OUT11_OL | OUT12_OL | OUT13_OL | OUT14_OL | OUT15_OL | OUTHS_OL | Reserved |   |
| Access   | R/C        |            |          |    |    |    |            |            |            |            |            |            |         |         |         |          |          |          |          |          |          |          |          |   |

Table 116. SR5 signals description

| Bit   | Name       | Description                                                                                                                     |
|-------|------------|---------------------------------------------------------------------------------------------------------------------------------|
| 23    | OUT1_HS_OL | Open-load<br>'1' indicates an open-load condition was detected at the output<br>Bit is latched until a "Read and clear" command |
| 22    | OUT1_LS_OL |                                                                                                                                 |
| 21:18 | Reserved   | —                                                                                                                               |

Table 116. SR5 signals description (continued)

| Bit | Name       | Description                                                                                                                     |
|-----|------------|---------------------------------------------------------------------------------------------------------------------------------|
| 17  | OUT4_HS_OL | Open-load<br>'1' indicates an open-load condition was detected at the output<br>Bit is latched until a "Read and clear" command |
| 16  | OUT4_LS_OL |                                                                                                                                 |
| 15  | OUT5_HS_OL |                                                                                                                                 |
| 14  | OUT5_LS_OL |                                                                                                                                 |
| 13  | OUT6_HS_OL |                                                                                                                                 |
| 12  | OUT6_LS_OL |                                                                                                                                 |
| 11  | OUT7_OL    |                                                                                                                                 |
| 10  | OUT8_OL    |                                                                                                                                 |
| 9   | OUT9_OL    |                                                                                                                                 |
| 8   | OUT10_OL   |                                                                                                                                 |
| 7   | OUT11_OL   |                                                                                                                                 |
| 6   | OUT12_OL   |                                                                                                                                 |
| 5   | OUT13_OL   |                                                                                                                                 |
| 4   | OUT14_OL   |                                                                                                                                 |
| 3   | OUT15_OL   |                                                                                                                                 |
| 2   | OUTHS_OL   |                                                                                                                                 |
| 1:0 | Reserved   | —                                                                                                                               |

### 7.5.6 Status Register SR6 (0x36)

Table 117. Status Register SR6 (0x36)

|          | 23               | 22               | 21       | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12     | 11     | 10     | 9      | 8      | 7      | 6        | 5        | 4        | 3        | 2        | 1        | 0        |
|----------|------------------|------------------|----------|----|----|----|----|----|----|----|----|--------|--------|--------|--------|--------|--------|----------|----------|----------|----------|----------|----------|----------|
| Bit name | WD_TIMER_STATE_1 | WD_TIMER_STATE_0 | Reserved |    |    |    |    |    |    |    |    | TW_CL6 | TW_CL5 | TW_CL4 | TW_CL3 | TW_CL2 | TW_CL1 | Reserved | TSD1_CL6 | TSD1_CL5 | TSD1_CL4 | TSD1_CL3 | TSD1_CL2 | TSD1_CL1 |
| Access   | R                |                  | R/C      |    |    |    |    |    |    |    |    |        |        |        |        |        |        |          |          |          |          |          |          |          |

Table 118. SR6 signals description

| Bit | Name             | Description                                                           |
|-----|------------------|-----------------------------------------------------------------------|
| 23  | WD_TIMER_STATE_1 | Watchdog timer status<br>00: 0 - 33%<br>01: 33 - 66%<br>11: 66 - 100% |
| 22  | WD_TIMER_STATE_0 |                                                                       |

Table 118. SR6 signals description (continued)

| Bit   | Name     | Description                                                                                                                                                                                        |
|-------|----------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 21:14 | Reserved | —                                                                                                                                                                                                  |
| 13    | TW_CL6   | Thermal warning for Cluster x<br>'1' indicates Cluster x has reached the thermal warning threshold<br>Bit is latched until a "Read and clear" command                                              |
| 12    | TW_CL5   |                                                                                                                                                                                                    |
| 11    | TW_CL4   |                                                                                                                                                                                                    |
| 10    | TW_CL3   |                                                                                                                                                                                                    |
| 9     | TW_CL2   |                                                                                                                                                                                                    |
| 8     | TW_CL1   |                                                                                                                                                                                                    |
| 7:6   | Reserved | —                                                                                                                                                                                                  |
| 5     | TSD1_CL6 | Thermal shutdown of Cluster x<br>'1' indicates Cluster x has reached the thermal shutdown threshold (TSD1) and the output cluster was shut down<br>Bit is latched until a "Read and clear" command |
| 4     | TSD1_CL5 |                                                                                                                                                                                                    |
| 3     | TSD1_CL4 |                                                                                                                                                                                                    |
| 2     | TSD1_CL3 |                                                                                                                                                                                                    |
| 1     | TSD1_CL2 |                                                                                                                                                                                                    |
| 0     | TSD1_CL1 |                                                                                                                                                                                                    |

### 7.5.7 Status Register SR7 (0x37) to SR9 (0x39)

Table 119. Status Register SR7 (0x37) to SR9 (0x39)

|          | 23       | 22 | 21         | 20         | 19         | 18         | 17         | 16         | 15         | 14         | 13         | 12         | 11       | 10 | 9          | 8          | 7          | 6          | 5          | 4          | 3          | 2          | 1          | 0          |
|----------|----------|----|------------|------------|------------|------------|------------|------------|------------|------------|------------|------------|----------|----|------------|------------|------------|------------|------------|------------|------------|------------|------------|------------|
| Bit name | Reserved |    | TEMP_CLx_9 | TEMP_CLx_8 | TEMP_CLx_7 | TEMP_CLx_6 | TEMP_CLx_5 | TEMP_CLx_4 | TEMP_CLx_3 | TEMP_CLx_2 | TEMP_CLx_1 | TEMP_CLx_0 | Reserved |    | TEMP_Cly_9 | TEMP_Cly_8 | TEMP_Cly_7 | TEMP_Cly_6 | TEMP_Cly_5 | TEMP_Cly_4 | TEMP_Cly_3 | TEMP_Cly_2 | TEMP_Cly_1 | TEMP_Cly_0 |
| Access   | R/C      |    | R          |            |            |            |            |            |            |            |            |            | R/C      |    | R          |            |            |            |            |            |            |            |            |            |

Where:

$$x = 2 + (z * 2), z = 0 \text{ to } 2$$

$$y = 1 + (z * 2), z = 0 \text{ to } 2$$

Table 120. SR7 to SR9 signals description

| Bit   | Name     | Description |
|-------|----------|-------------|
| 23:22 | Reserved | —           |

Table 120. SR7 to SR9 signals description (continued)

| Bit   | Name       | Description                                                                                                                                                                                |
|-------|------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 21    | TEMP_CLx_9 | Temperature Cluster x: Binary coded voltage of temperature diode for cluster x (bit12 = LSB; bit21 = MSB) (see <a href="#">Section 4.31: Thermal clusters</a> )<br>Bits cannot be cleared. |
| 20    | TEMP_CLx_8 |                                                                                                                                                                                            |
| 19    | TEMP_CLx_7 |                                                                                                                                                                                            |
| 18    | TEMP_CLx_6 |                                                                                                                                                                                            |
| 17    | TEMP_CLx_5 |                                                                                                                                                                                            |
| 16    | TEMP_CLx_4 |                                                                                                                                                                                            |
| 15    | TEMP_CLx_3 |                                                                                                                                                                                            |
| 14    | TEMP_CLx_2 |                                                                                                                                                                                            |
| 13    | TEMP_CLx_1 |                                                                                                                                                                                            |
| 12    | TEMP_CLx_0 |                                                                                                                                                                                            |
| 11:10 | Reserved   | —                                                                                                                                                                                          |
| 9     | TEMP_CLy_9 | Temperature Cluster y: binary coded voltage of temperature diode for cluster y (bit0 = LSB; bit9 = MSB) (see <a href="#">Section 4.31: Thermal clusters</a> )<br>Bits cannot be cleared.   |
| 8     | TEMP_CLy_8 |                                                                                                                                                                                            |
| 7     | TEMP_CLy_7 |                                                                                                                                                                                            |
| 6     | TEMP_CLy_6 |                                                                                                                                                                                            |
| 5     | TEMP_CLy_5 |                                                                                                                                                                                            |
| 4     | TEMP_CLy_4 |                                                                                                                                                                                            |
| 3     | TEMP_CLy_3 |                                                                                                                                                                                            |
| 2     | TEMP_CLy_2 |                                                                                                                                                                                            |
| 1     | TEMP_CLy_1 |                                                                                                                                                                                            |
| 0     | TEMP_CLy_0 |                                                                                                                                                                                            |

### 7.5.8 Status Register SR10 (0x3A)

Table 121. Status Register SR10 (0x3A)

|          | 23       | 22 | 21      | 20      | 19      | 18      | 17      | 16      | 15      | 14      | 13      | 12      | 11       | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----------|----------|----|---------|---------|---------|---------|---------|---------|---------|---------|---------|---------|----------|----|---|---|---|---|---|---|---|---|---|---|
| Bit name | Reserved |    | VSREG_9 | VSREG_8 | VSREG_7 | VSREG_6 | VSREG_5 | VSREG_4 | VSREG_3 | VSREG_2 | VSREG_1 | VSREG_0 | Reserved |    |   |   |   |   |   |   |   |   |   |   |
| Access   | R/C      |    | R       |         |         |         |         |         |         |         |         |         | R/C      |    |   |   |   |   |   |   |   |   |   |   |

Table 122. SR10 signals description

| Bit   | Name     | Description |
|-------|----------|-------------|
| 23:22 | Reserved | —           |

Table 122. SR10 signals description (continued)

| Bit  | Name     | Description                                                                                                                                                                                                            |
|------|----------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 21   | VSREG_9  | Binary coded voltage at V <sub>SREG</sub> pin (bit12 = LSB; bit21 = MSB)<br>00 0000 0000: 0V<br>xx xxxx xxxx: V <sub>AINVS</sub> /1023 x register value<br>11 1111 1111: V <sub>AINVS</sub><br>Bits cannot be cleared. |
| 20   | VSREG_8  |                                                                                                                                                                                                                        |
| 19   | VSREG_7  |                                                                                                                                                                                                                        |
| 18   | VSREG_6  |                                                                                                                                                                                                                        |
| 17   | VSREG_5  |                                                                                                                                                                                                                        |
| 16   | VSREG_4  |                                                                                                                                                                                                                        |
| 15   | VSREG_3  |                                                                                                                                                                                                                        |
| 14   | VSREG_2  |                                                                                                                                                                                                                        |
| 13   | VSREG_1  |                                                                                                                                                                                                                        |
| 12   | VSREG_0  |                                                                                                                                                                                                                        |
| 11:0 | Reserved | —                                                                                                                                                                                                                      |

### 7.5.9 Status Register SR11 (0x3B)

Table 123. Status Register SR11 (0x3B)

|          | 23       | 22 | 21   | 20   | 19   | 18   | 17   | 16   | 15   | 14   | 13   | 12   | 11       | 10 | 9     | 8     | 7     | 6     | 5     | 4     | 3     | 2     | 1     | 0     |
|----------|----------|----|------|------|------|------|------|------|------|------|------|------|----------|----|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|
| Bit name | Reserved |    | VS_9 | VS_8 | VS_7 | VS_6 | VS_5 | VS_4 | VS_3 | VS_2 | VS_1 | VS_0 | Reserved |    | VWU_9 | VWU_8 | VWU_7 | VWU_6 | VWU_5 | VWU_4 | VWU_3 | VWU_2 | VWU_1 | VWU_0 |
| Access   | R/C      |    | R    |      |      |      |      |      |      |      |      |      | R/C      |    | R     |       |       |       |       |       |       |       |       |       |

Table 124. SR11 signals description

| Bit   | Name     | Description                                                                                                                                                                                                         |
|-------|----------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 23:22 | Reserved | —                                                                                                                                                                                                                   |
| 21    | VS_9     | Binary coded voltage at V <sub>S</sub> pin (bit12 = LSB; bit21 = MSB)<br>00 0000 0000: 0V<br>xx xxxx xxxx: V <sub>AINVS</sub> /1023 x register value<br>11 1111 1111: V <sub>AINVS</sub><br>Bits cannot be cleared. |
| 20    | VS_8     |                                                                                                                                                                                                                     |
| 19    | VS_7     |                                                                                                                                                                                                                     |
| 18    | VS_6     |                                                                                                                                                                                                                     |
| 17    | VS_5     |                                                                                                                                                                                                                     |
| 16    | VS_4     |                                                                                                                                                                                                                     |
| 15    | VS_3     |                                                                                                                                                                                                                     |
| 14    | VS_2     |                                                                                                                                                                                                                     |
| 13    | VS_1     |                                                                                                                                                                                                                     |
| 12    | VS_0     |                                                                                                                                                                                                                     |
| 11:10 | Reserved | —                                                                                                                                                                                                                   |

Table 124. SR11 signals description (continued)

| Bit | Name  | Description                                                                                                                                                                                        |
|-----|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 9   | VWU_9 | Binary coded voltage at WU pin (bit0 = LSB; bit9 = MSB)<br>00 0000 0000: 0V<br>xx xxxx xxxx: $V_{AINVS}/1023 \times \text{register value}$<br>11 1111 1111: $V_{AINVS}$<br>Bits cannot be cleared. |
| 8   | VWU_8 |                                                                                                                                                                                                    |
| 7   | VWU_7 |                                                                                                                                                                                                    |
| 6   | VWU_6 |                                                                                                                                                                                                    |
| 5   | VWU_5 |                                                                                                                                                                                                    |
| 4   | VWU_4 |                                                                                                                                                                                                    |
| 3   | VWU_3 |                                                                                                                                                                                                    |
| 2   | VWU_2 |                                                                                                                                                                                                    |
| 1   | VWU_1 |                                                                                                                                                                                                    |
| 0   | VWU_0 |                                                                                                                                                                                                    |

## 8 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK® is an ST trademark.

### 8.1 LQFP-64 package information

Figure 57. LQFP-64 package dimension

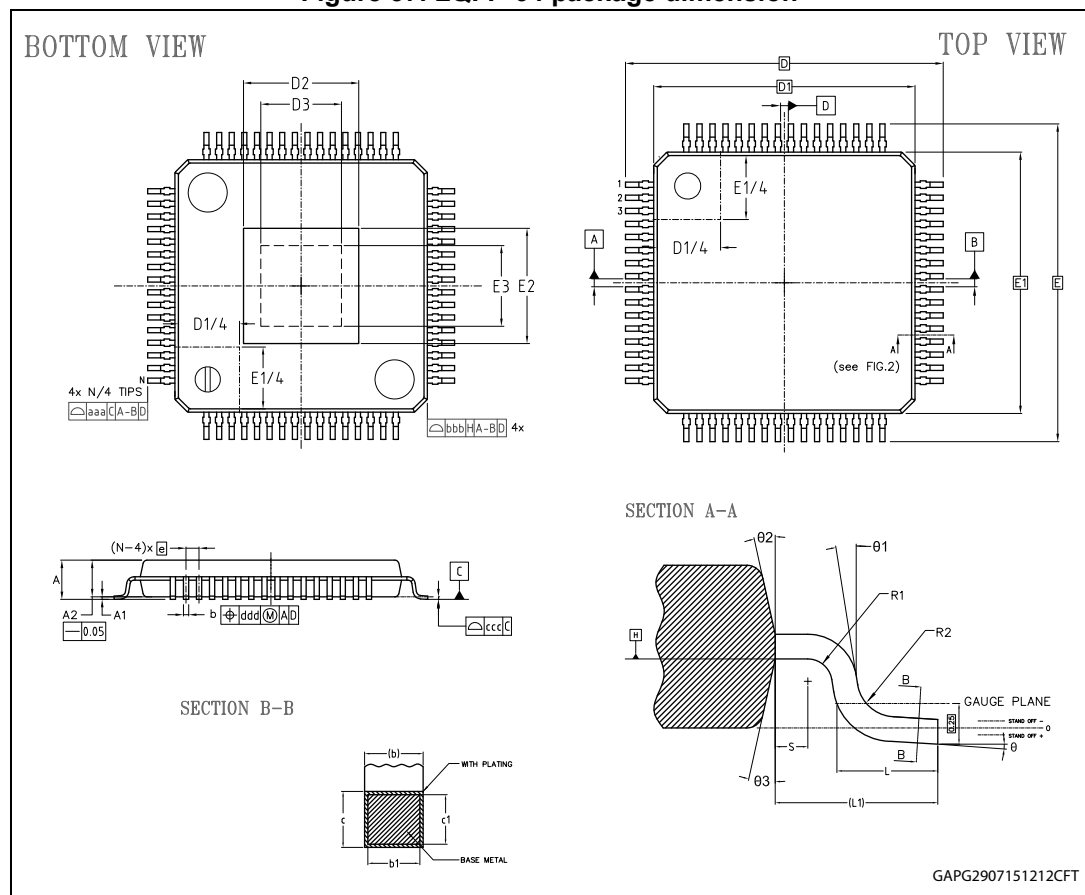


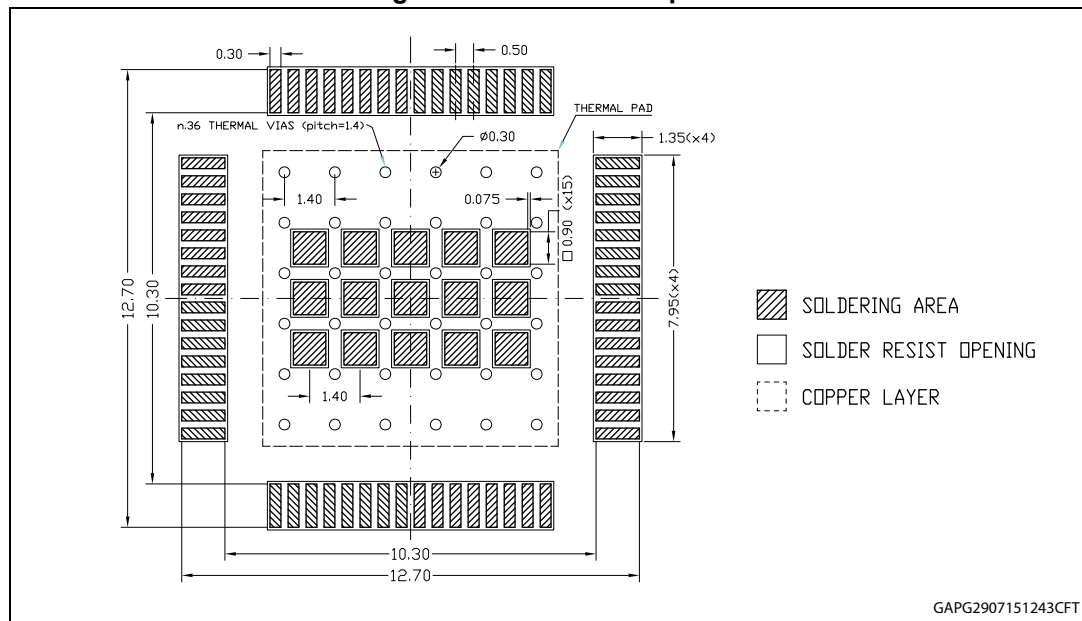
Table 125. LQFP-64 mechanical data

| Symbol     | Millimeters |      |      |
|------------|-------------|------|------|
|            | Min.        | Typ. | Max. |
| $\Theta$   | 0°          | 3.5° | 6°   |
| $\Theta 1$ | 0°          | 9°   | 12°  |
| $\Theta 2$ | 11°         | 12°  | 13°  |
| $\Theta 3$ | 11°         | 12°  | 13°  |

Table 125. LQFP-64 mechanical data (continued)

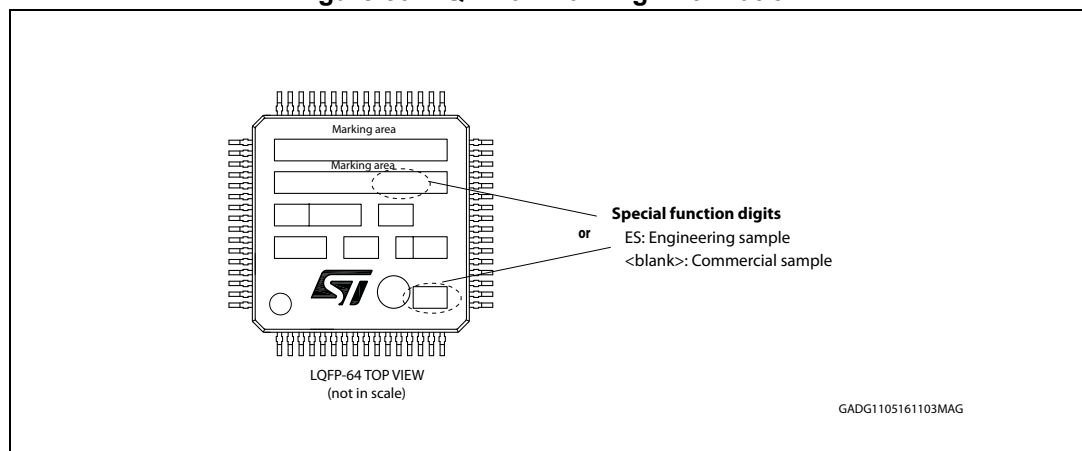
| Symbol                                | Millimeters |       |      |
|---------------------------------------|-------------|-------|------|
|                                       | Min.        | Typ.  | Max. |
| A                                     |             |       | 1.60 |
| A1                                    | 0.05        |       | 0.15 |
| A2                                    | 1.35        | 1.40  | 1.45 |
| b                                     |             |       | 0.27 |
| b1                                    | 0.17        | 0.20  | 0.23 |
| c                                     | 0.09        |       | 0.20 |
| c1                                    | 0.09        | 0.127 | 0.16 |
| D                                     | 12.00 BSC   |       |      |
| D1                                    | 10.00 BSC   |       |      |
| D2                                    |             |       | 6.85 |
| D3                                    | 5.7         |       |      |
| e                                     | 0.50 BSC    |       |      |
| E                                     | 12.00 BSC   |       |      |
| E1                                    | 10.00 BSC   |       |      |
| E2                                    |             |       | 4.79 |
| E3                                    | 3.3         |       |      |
| L                                     | 0.45        | 0.60  | 0.75 |
| L1                                    | 1.00        |       |      |
| N                                     | 64          |       |      |
| R1                                    | 0.08        |       |      |
| R2                                    | 0.08        |       | 0.20 |
| S                                     | 0.20        |       |      |
| <b>Tolerance of form and position</b> |             |       |      |
| aaa                                   | 0.20        |       |      |
| bbb                                   | 0.20        |       |      |
| ccc                                   | 0.08        |       |      |
| ddd                                   | 0.08        |       |      |

**Figure 58. LQFP-64 footprint**



## 8.2 LQFP-64 marking information

**Figure 59. LQFP-64 marking information**



Parts marked as ES are not yet qualified and therefore not approved for use in production. ST is not responsible for any consequences resulting from such use. In no event will ST be liable for the customer using any of these engineering samples in production. ST's Quality department must be contacted to run a qualification activity prior to any decision to use these engineering samples.

## 9 Revision history

**Table 126. Document revision history**

| Date        | Revision | Changes                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |
|-------------|----------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 27-Apr-2016 | 1        | Initial release.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |
| 11-May-2016 | 2        | Updated <a href="#">Section 3.3.1: LQFP64 thermal data</a><br>Updated <a href="#">Table 20</a><br>Updated <a href="#">Table 22</a><br>Updated <a href="#">Table 40</a><br>Updated <a href="#">Figure 59</a><br>Updated <a href="#">Section 4.14: Auto-recovery alert and thermal expiration</a><br>Updated <a href="#">Section 4.22: Programmable soft-start function to drive loads with higher inrush current</a><br>Updated <a href="#">Figure 43</a><br>Updated <a href="#">Table 114</a>                                                                                                                                                                                        |
| 12-Sep-2016 | 3        | Updated <a href="#">Table 29</a>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |
| 22-Nov-2016 | 4        | Added AEC-Q100 qualified in <a href="#">Features</a> .<br>Updated <a href="#">Table 4: ESD protection</a> ,<br>Added <a href="#">Section 3.4.12: Over Current Recovery settings</a><br>Updated <a href="#">Section 4.22: Programmable soft-start function to drive loads with higher inrush current</a><br>Added <a href="#">Table 18: Half bridges (OUT1, OUT4, OUT5 and OUT6) OCR timing parameters</a> and <a href="#">Table 19: High-side (OUT7, OUT8 and OUT_HS) OCR timing parameters</a><br>Updated <a href="#">Table 20: Current monitoring</a><br>Updated <a href="#">Table 110: SR2 signals description</a><br>Updated <a href="#">Table 124: SR11 signals description</a> |
| 11-Mar-2019 | 5        | Moved "Device summary" table in cover page.<br>Added the "Sustainable Technology" logo to the datasheet in cover page.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |

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